ANALOG DEVICES

16×16-Bit CMOS Single Port Multiplier/Accumulator

ADSP-1110A

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16×16-bit multiplier/accumulator integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	ADSP-1110AS(X)/883B
−2	ADSP-1110AT(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin DIP
E	E-28	28-Contact LCC

1.3 Absolute Maximum Ratings.

Supply Voltage	−0.3 V to 7 V
Input Voltage	−0.3 V to V_{DD}
Output Voltage	−0.3 V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC}: see MIL-M-38510, Appendix C.

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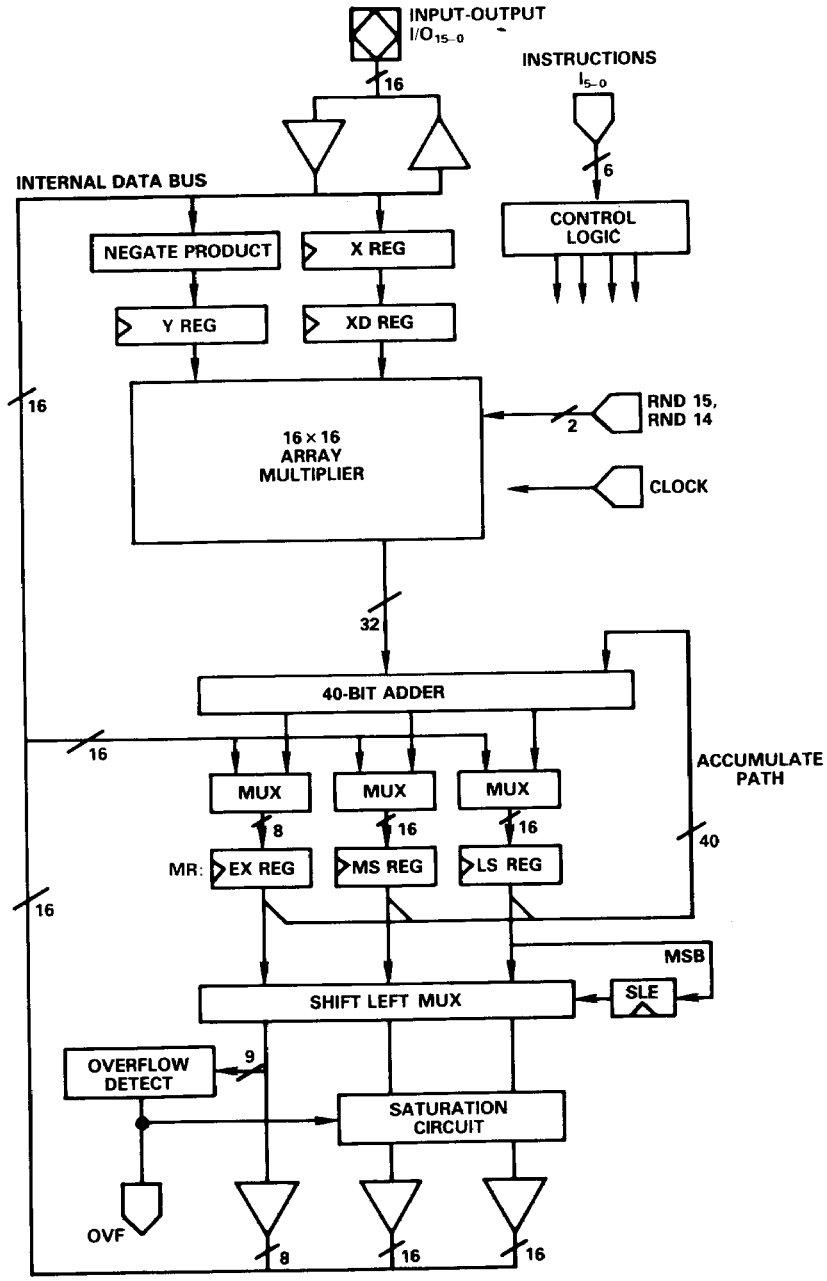
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9, 10, 11	Test Condition[1]	Units
Digital Input High Voltage*	V_{IH}	−1, 2	2.0	2.2	2.2		V_{DD} = max	V min
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8		V_{DD} = min	V max
Digital Output High Voltage	V_{OH}	−1, 2	2.4	2.4	2.4		V_{DD} = min I_{OH} = −1 mA	V min
Digital Output Low Voltage*	V_{OL}	−1, 2	0.4	0.6	0.6		V_{DD} = min I_{OH} = +4 mA	V max
Digital Input High Current	I_{IH}	−1, 2	10	10	10		V_{DD} = max V_{IN} = +5.0 V	μA max
Digital Input Low Current	I_{IL}	−1, 2	10	10	10		V_{DD} = max V_{IN} = 0.0 V	μA max
Three-State Leakage* Current Low	I_{OZL}	−1, 2	50	50	50		V_{DD} = max V_{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I_{OZH}	−1, 2	50	50	50		V_{DD} = max V_{IH} = max (High Z)	μA max
Supply Current*	I_{DD1}	−1, 2	70	80	80		V_{DD} = max; TTL Inputs; f = max	mA max
	I_{DD2}	−1, 2	35	40	40		V_{DD} = max All V_{IN} = 2.4 V	mA max
Clock Pulse Width	t_{PW}	−1, 2	15			15	Note 2	ns min
Input Control Hold Time	t_{CH}	−1, 2	5			6	Note 2	ns min
Input Data Setup Time	t_{DS}	−1, 2	15			15	Note 2	ns min
Clock Period*	t_{CLK}	−1	50			60	Note 2	ns min
		−2	42.5			50		
Input Control Setup Time	t_{CS}	−1	25			25	Note 2	ns min
		−2	20			20		
Input Data Hold Time*	t_{DH}	−1, 2	3			4	Note 2	ns min
Multiply/Accumulate Time*	t_{MAC}	−1	100			120	Note 2	ns max
		−2	85			100		
Control to Valid Output*	t_D	−1	30			30	Note 2	ns max
		−2	25			30		
Control to Valid Output* with Saturation	t_{DSAT}	−1	35			40	Note 2	ns max
		−2	32			35		
Output Driver Disable Time	t_{DIS}	−1, 2	25			25	Notes 2 and 3	ns max
Control to Overflow Flag*	t_O	−1	30			35	Note 2	ns max
		−2	25			30		
Control to Overflow Flag* W/SL	t_{LO}	−1	40			45	Note 2	ns max
		−2	35			45		

NOTES
*Indicates that a limit for this parameter has changed from REV. C.
[1]T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).
[2]TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).
[3]Transitions measured per Figure 2.

Table 1.

REV. D

3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

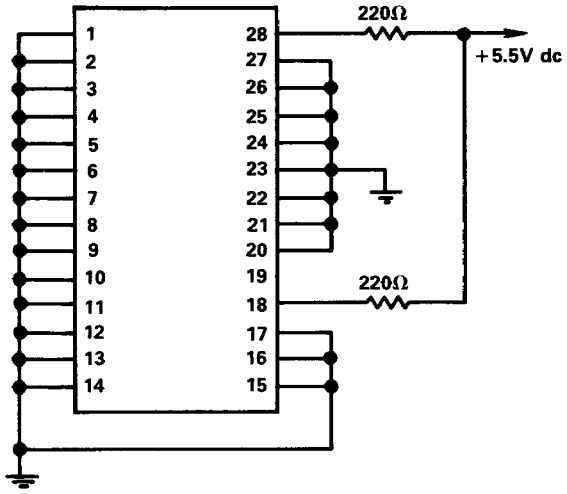
PIN	FUNCTION	PIN	FUNCTION
1	RND15	15	CLK
2	RND14	16	I_3
3	I/O_{14}	17	I_4
4	I/O_{12}	18	I_5
5	I/O_{10}	19	OVF
6	I/O_8	20	I/O_1
7	I/O_6	21	I/O_3
8	I/O_4	22	I/O_5
9	I/O_2	23	I/O_7
10	I/O_0	24	I/O_9
11	I_0	25	I/O_{11}
12	I_1	26	I/O_{13}
13	I_2	27	I/O_{15}
14	GND	28	V_{DD}

3.2.4 Microcircuit Technology Group.

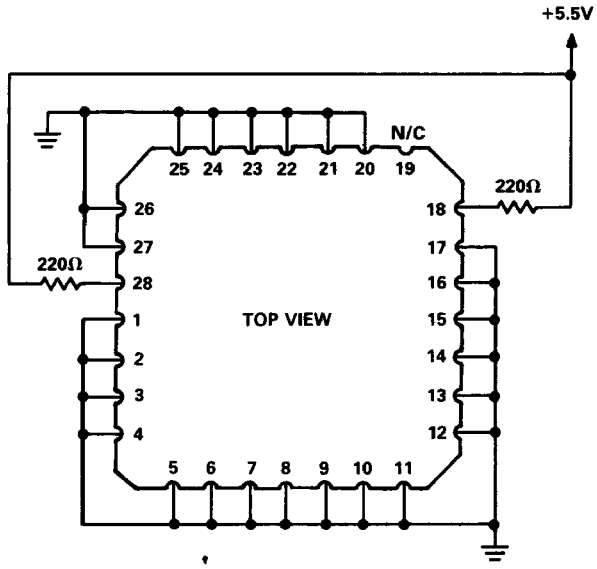
This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1110AD Life Test and Burn-In Circuit



ADSP-1110AE Life Test and Burn-In Circuit

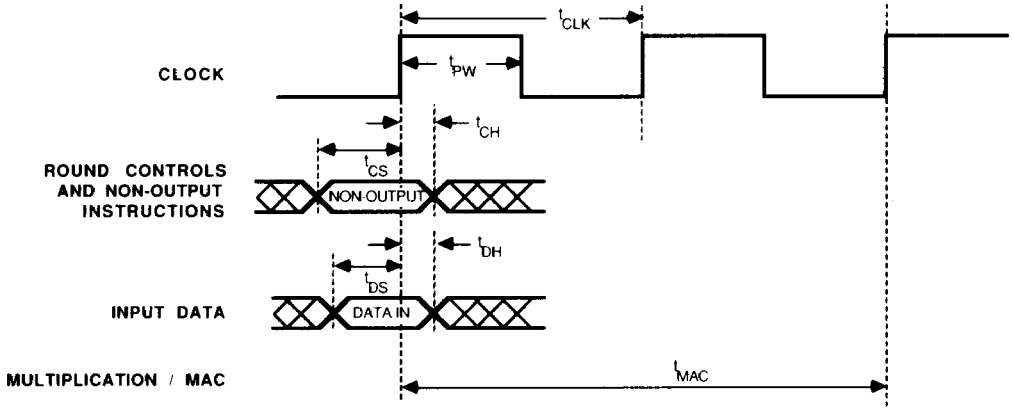


Figure 1. ADSP-1110A Timing: Clocked (Synchronous) Operations All Non-Output Instructions

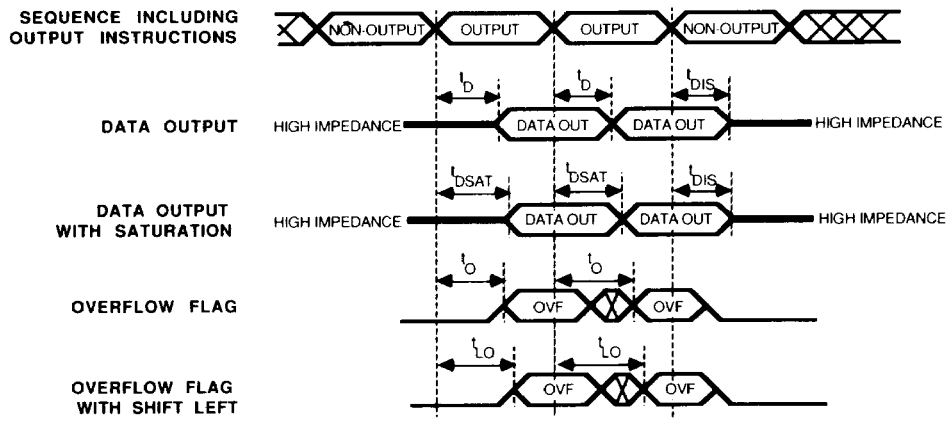


Figure 2. ADSP-1110A Timing: Unclocked (Asynchronous) Operations All Output Instructions

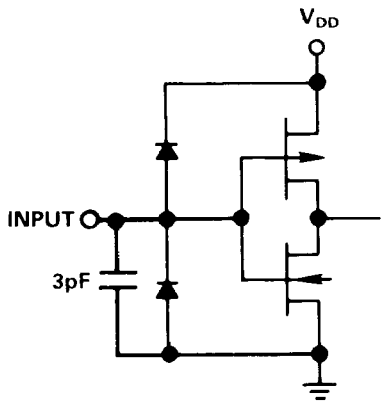


Figure 3. Equivalent Input Circuit

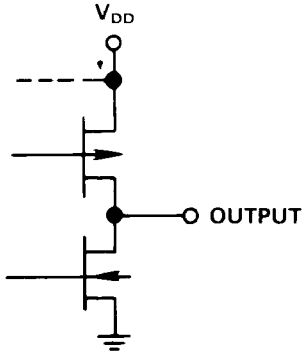


Figure 4. Equivalent Output Circuit

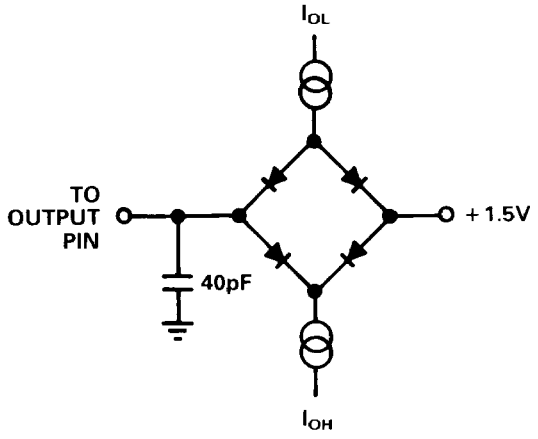


Figure 5. Normal Load Circuit for AC Measurements

Instruction Group	Instruction	Microcode Instruction 5	4	3	2	1	0	Comments
Miscellaneous	NOP	0	0	0	0	X	X	No Operation
	CKMR	0	0	0	1	X	X	Clock MR
Input	X = BUS	0	0	1	0	X	X	
Preload	LS = BUS	0	1	0	0	0	0	
	MS = BUS	0	1	0	1	X	0	
	EX = BUS	0	1	0	0	1	0	
Transfer	LS = MS	0	1	0	0	0	1	Set SLE register
	MS = EX	0	1	0	1	0	1	
Sign Extend	EX = SIGN EXT MS	0	1	0	0	1	1	
	MS = SIG EXT LS	0	1	0	1	1	1	
Output	BUS = EX	0	0	1	1	0	1	All output instructions are asynchronous
	BUS = EX (sl)	0	0	1	1	0	0	I5–I2:
	BUS = MS	0	1	1	0	0	1	0011 = EX
	BUS = MS (sl)	0	1	1	0	0	0	0110 = MS
	BUS = MS (sat)	0	1	1	0	1	1	0111 = LS
	BUS = MS (sl, sat)	0	1	1	0	1	0	I1–I0:
	BUS = LS	0	1	1	1	0	1	01 = to bus
	BUS = LS (sl)	0	1	1	1	0	0	00 = to bus shifted
	BUS = LS (sat)	0	1	1	1	1	1	10 = to bus shifted w/saturation
	BUS = LS (sl, sat)	0	1	1	1	1	0	11 = to bus w/saturation
Multi-Operation	Y = BUS; CKMR; $X_{US}*Y_{US}$	1	0	0	X	0	0	Require two cycles to complete.
	Y = BUS; CKMR; $-X_{US}*Y_{US}$	1	0	0	X	0	1	Other instructions can be executed
	Y = BUS; CKMR; $X_{US}*Y_{US}$ +MR	1	0	0	0	1	0	on the second cycle.
	Y = BUS; CKMR; $-X_{US}*Y_{US}$ +MR	1	0	0	0	1	1	
	Y = BUS; CKMR; $X_{US}*Y_{US}$ −MR	1	0	0	1	1	0	I5 = Multiply/MAC operation
	Y = BUS; CKMR; $-X_{US}*Y_{US}$ −MR	1	0	0	1	1	1	I4 = Y twos complement
	Y = BUS; CKMR; $X_{TC}*Y_{US}$	1	0	1	X	0	0	I3 = X twos complement
	Y = BUS; CKMR; $-X_{TC}*Y_{US}$	1	0	1	X	0	1	I2 = Subtract previous result
	Y = BUS; CKMR; $X_{TC}*Y_{US}$ +MR	1	0	1	0	1	0	I1 = Add/subtract previous result
	Y = BUS; CKMR; $-X_{TC}*Y_{US}$ +MR	1	0	1	0	1	1	from product
	Y = BUS; CKMR; $X_{TC}*Y_{US}$ −MR	1	0	1	1	1	0	I0 = Negate product
	Y = BUS; CKMR; $-X_{TC}*Y_{US}$ −MR	1	0	1	1	1	1	
	Y = BUS; CKMR; $X_{US}*Y_{TC}$	1	1	0	X	0	0	
	Y = BUS; CKMR; $-X_{US}*Y_{TC}$	1	1	0	X	0	1	
	Y = BUS; CKMR; $X_{US}*Y_{TC}$ +MR	1	1	0	0	1	0	
	Y = BUS; CKMR; $-X_{US}*Y_{TC}$ +MR	1	1	0	0	1	1	
	Y = BUS; CKMR; $X_{US}*Y_{TC}$ −MR	1	1	0	1	1	0	
	Y = BUS; CKMR; $-X_{US}*Y_{TC}$ −MR	1	1	0	1	1	1	
	Y = BUS; CKMR; $X_{TC}*Y_{TC}$	1	1	1	X	0	0	
	Y = BUS; CKMR; $-X_{TC}*Y_{TC}$	1	1	1	X	0	1	
	Y = BUS; CKMR; $X_{TC}*Y_{TC}$ +MR	1	1	1	0	1	0	
	Y = BUS; CKMR; $-X_{TC}*Y_{TC}$ +MR	1	1	1	0	1	1	
	Y = BUS; CKMR; $X_{TC}*Y_{TC}$ −MR	1	1	1	1	1	0	
	Y = BUS; CKMR; $-X_{TC}*Y_{TC}$ −MR	1	1	1	1	1	1	

Mnemonic Definitions

=	Assign right side to left.	sl	Shift left.
BUS	16-bit external data bus used for all I/O operations.	sat	Conditional on overflow, saturate the outputted value.
X	Input register for multiplier.	TC	Twos complement number.
Y	Input register for multiplier.	US	Unsigned magnitude number.
EX	8-bit extension register for accumulator.	SIGN	Sign bit (MSB) of specified register.
MS	16-bit most significant product register.	CKMR	Clock product into EX, MS and LS.
LS	16-bit least significant product register.	*	Multiply
MR	40-bit accumulator comprising EX, MS and LS.	X	Microcode instruction bit can be either a 0 or 1.

Table 2. ADSP-1110A Instruction Set