Quadruple Output Regulator with Two High-Side Switches, BU/ACC Voltage Detectors, and Mute Delay

FEATURES AND BENEFITS

- Four independent, high current switching regulators
- Adjustable 1.0 A/±1.5% always-on asynchronous buck regulator with an integrated 150 mΩ MOSFET (SW1)
  - Employs PFM to deliver 3.3 V/40 µA while drawing less than 50 µA from V_{IN} of 12 V
  - Operates down to at least 3.6 V_{IN}
- Adjustable 1.5 A/±1.5% asynchronous buck regulator with an integrated 120 mΩ high-side MOSFET (SW2)
- Adjustable 2.0 A/±1.5% asynchronous buck regulator with an integrated 110 mΩ MOSFET (SW3)
- Adjustable ±1.5% synchronous buck controller with integrated gate drivers and current sensing (SW4)
- Fixed 425 kHz, interleaved PWM switching frequency
- EN/SYNC input for PWM frequency scaling
- Adjustable soft-start time for each switching regulator
- All switching regulators provide pre-bias startup with zero reverse current
- All switching regulators have overvoltage protection
- External compensation for all switching regulators

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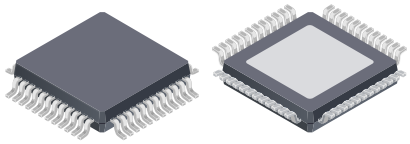
PACKAGE: 48-pin LQFP (suffix JP)



Not to scale

DESCRIPTION

Designed to provide the power supply requirements of next generation car audio and infotainment systems, the A8600 provides all the control and protection circuitry to produce four high current regulators, each with ±1.5% accuracy. The A8600 includes control circuitry to implement three adjustable, asynchronous buck regulators with integrated MOSFETs. Also, the A8600 provides the control circuitry, gate drivers, and current sensing to implement a synchronous buck controller with external MOSFETs. In standby mode, the A8600 draws less than 50 µA from V_{IN} of 12 V while employing pulse frequency modulation (PFM) to deliver 3.3 V/40 µA via the always-on regulator, SW1. The always-on regulator operates down to at least V_{IN} of 3.6 V (V_{IN} falling).

Features of the A8600 include: an EN/SYNC input to either turn the A8600 on/off or increase/decrease the base pulse width modulation (PWM) frequency, four adjustable soft-start times, and four external compensation pins. Output voltage monitoring of switchers SW2, SW3, and SW4 is provided by a single, open-drain POK output. In addition, the A8600 provides two high voltage, high-side switches with foldback overcurrent protection. These two high-side switches actively block reverse current. The A8600 also provides direct battery (BU) and switched (accessory) battery (ACC) detectors and a mute pulse output with an adjustable delay.

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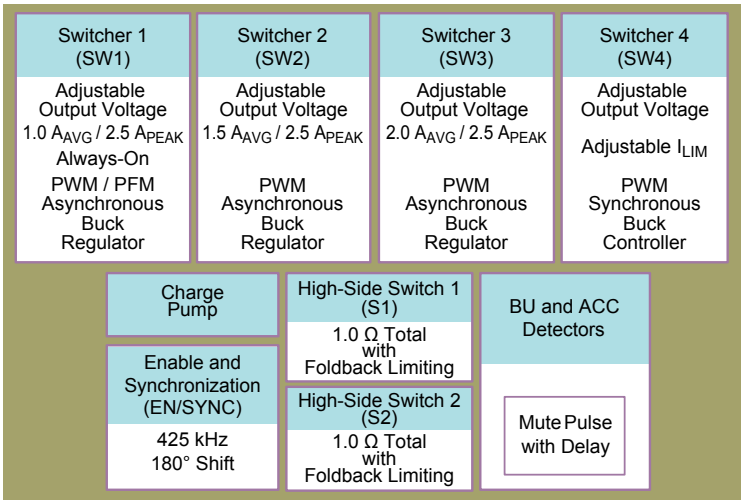

Figure 1. A8600 major features

FEATURES AND BENEFITS (continued)

- Power OK (POK) open-drain output with de-glitch
- BU and ACC voltage detectors and comparators
- Mute control with programmable delay
- Two internal high-voltage, high-side NMOS switches (S1 and S2) with foldback short circuit protection
- High-side switches simultaneously controlled on/off
- High-side switches block reverse current
- Internal charge pump for high-side switch biasing
- Withstands surge voltages up to 40 V
- −40°C to 85°C ambient operating temperature range
- 150°C maximum junction temperature
- Thermally enhanced, surface mount package

DESCRIPTION (continued)

Protection features of the A8600 include pulse-by-pulse current limit, hiccup mode short circuit protection, asynchronous diode protection, BOOT voltage protection, undervoltage lockout, over-voltage protection and thermal shutdown.

The A8600 is supplied in a low profile 48-pin LQFP package (suffix JP) with exposed power pad. It is lead (Pb) free, with 100% matte- tin leadframe plating.

SELECTION GUIDE

Part Number	Operating Ambient Temperature Range T_A, (°C)	Package	Packing*	Leadframe Plating
A8600EJPTR-T	–40 to 85	48-pin LQFP with exposed thermal pad	1500 pieces per 13-in. reel	100% Matte-Tin

*Contact Allegro™ for additional packing options.

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ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
OUTx Pins		Continuous	–0.3 to 40	V
BUI, VIN1/2/3, VINS, SSx, MUTE, POK Pins			–0.3 to 40	V
BIAS, CSP, CSN Pins			–0.3 to 7	V
HG4 Pin			–0.3 to V_{IN3} + 7	V
LG4 Pin			–0.3 to 8.5	V
BOOTx Pins		$V_{INx} = V_{IN1}, V_{IN2}, V_{IN3}$	–0.3 to V_{INx}+7	V
LX1/2/3 Pin to GND	$V_{LX1}, V_{LX2}, V_{LX3}$	Continuous, $V_{INx} = V_{IN1}, V_{IN2}, V_{IN3}$; minimum voltage is a function of temperature	–0.3 to V_{INx} +1	V
		t < 50 ns, $V_{INx} = V_{IN1}, V_{IN2}, V_{IN3}$	–1.0 to V_{INx} +3	V
LX4 Pin to GND	V_{LX4}	Continuous, lower limit is a function of temperature	–1.0 to 37	V
		t < 50 ns	–1.5 to 40	V
VREG Pin to GND	V_{VREG}		–0.3 to 5.5	V
ACCI Pin [2]	I_{ACCI}		1	mA
		t < 100 ms	–50	mA
All Other Pins			–0.3 to 5.5	V
Operating Ambient Temperature	T_A	E temperature range	–40 to 85	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.
[2] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	23	°C/W
		On 2-layer PCB with 3 in.^{2} of copper area on 2 sides	44	°C/W
Package Thermal Resistance, Junction to Pad	$R_{\theta JP}$		2	°C/W

*Additional thermal information available on the Allegro website.

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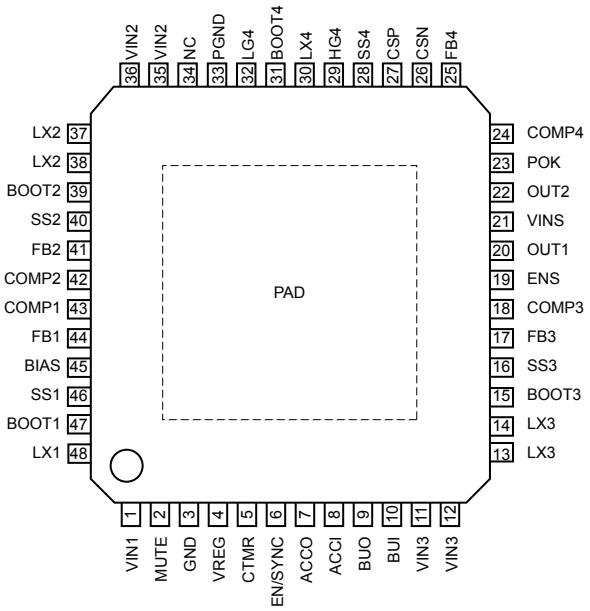
Pinout Diagram



Name	Number	Function
ACCI	8	Input to the ACC comparator
ACCO	7	Output of the ACC comparator
BIAS	45	Bias input, supplies internal circuitry when V_{SW1} is high enough
BOOT1	47	Floating gate drive for buck regulator SW1
BOOT2	39	Floating gate drive for buck regulator SW2
BOOT3	15	Floating gate drive for buck regulator SW3
BOOT4	31	Floating gate drive for buck regulator SW4
BUI	10	Input to the BU comparator
BUO	9	Output of the BU comparator
COMP1	43	Error amplifier compensation network for regulator SW1
COMP2	42	Error amplifier compensation network for regulator SW2
COMP3	18	Error amplifier compensation network for regulator SW3
COMP4	24	Error amplifier compensation network for regulator SW4
CSN	26	Current sense pin for buck regulator SW4
CSP	27	Current sense pin for buck regulator SW4
CTMR	5	Delay programming for the Mute pulse circuit
EN/SYNC	6	SWx enable and PFM control, and PWM synchronization
ENS	19	S1/S2 enable input
FB1	44	Feedback pin for buck regulator SW1
FB2	41	Feedback pin for buck regulator SW2
FB3	17	Feedback pin for buck regulator SW3

Name	Number	Function
FB4	25	Feedback pin for buck regulator SW4
GND	3	Ground
HG4	29	High side gate drive for buck regulator SW4
LG4	32	Low side gate drive for buck regulator SW4
LX1	48	Switching node for buck regulator SW1
LX2	37, 38	Switching node for buck regulator SW2
LX3	13, 14	Switching node for buck regulator SW3
LX4	30	Switching node for buck regulator SW4
MUTE	2	Open-drain, active low output of the Mute pulse circuit
NC	34	Unused
OUT1	20	High-side switch S1 output
OUT2	22	High-side switch S2 output
PAD	–	Exposed pad for enhanced thermal dissipation
PGND	33	Power ground
POK	23	Power OK open drain output
SS1	46	Soft start programming for regulator SW1
SS2	40	Soft start programming for regulator SW2
SS3	16	Soft start programming for regulator SW3
SS4	28	Soft start programming for regulator SW4
VIN1	1	Input supply for buck regulator SW1
VIN2	35, 36	Input supply for buck regulator SW2
VIN3	11, 12	Input supply for buck regulator SW3 (and SW4)
VINS	21	S1/S2 high-side switch input
VREG	4	Internal voltage regulator bypass capacitor pin

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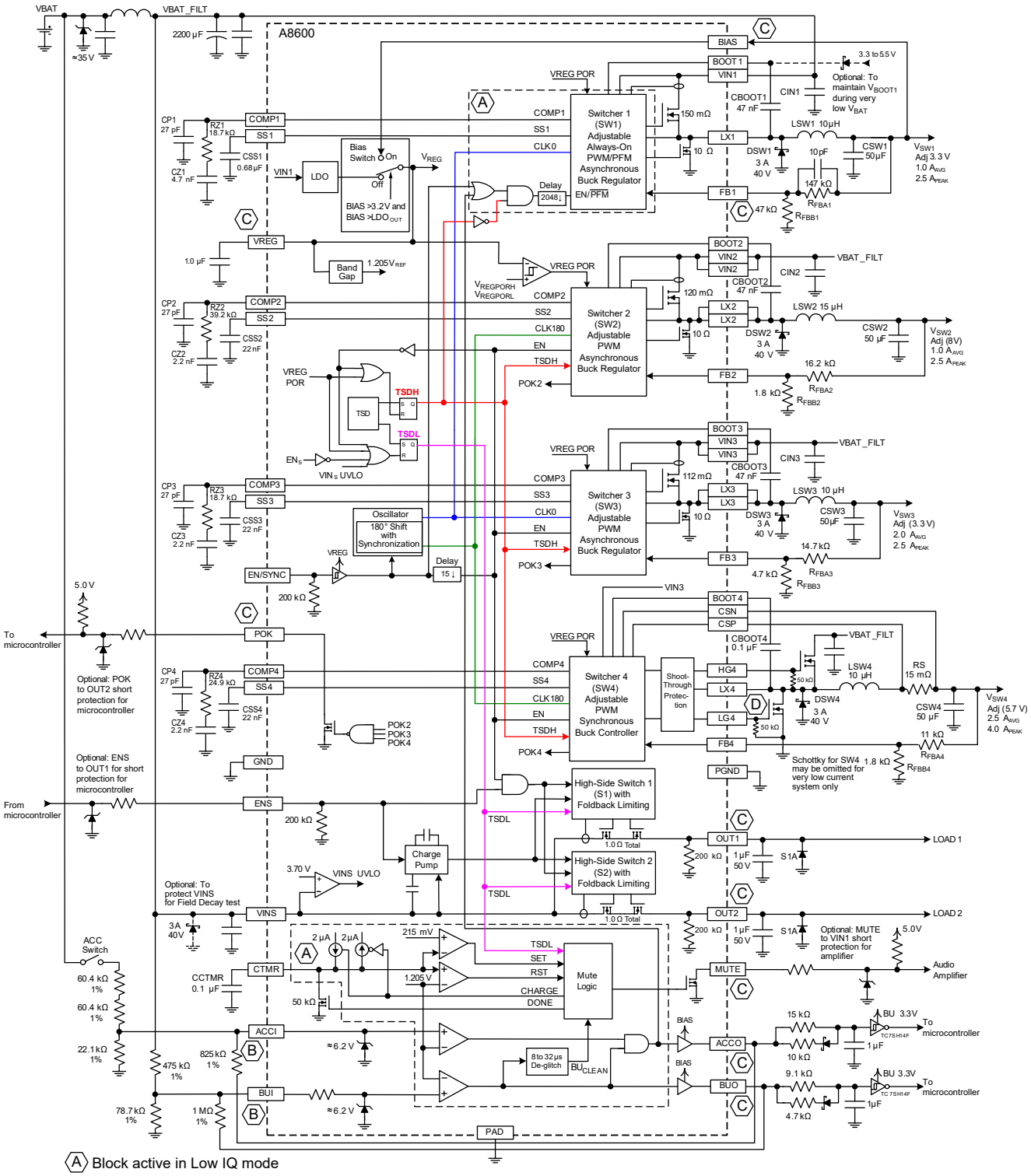
Top Level Functional Block Diagram and Typical Application Circuit



(A) Block active in Low IQ mode

(B) Current will not flow from ACCI to BUI or any VINx pin

(C) Current will not flow from ACCO, BUO, MUTE, BIAS, VREG, FB1, POK, or OUTx to any VINx pin

(D) SW4 lower FET must not cause V_{SW4} to decay during pre-bias startup

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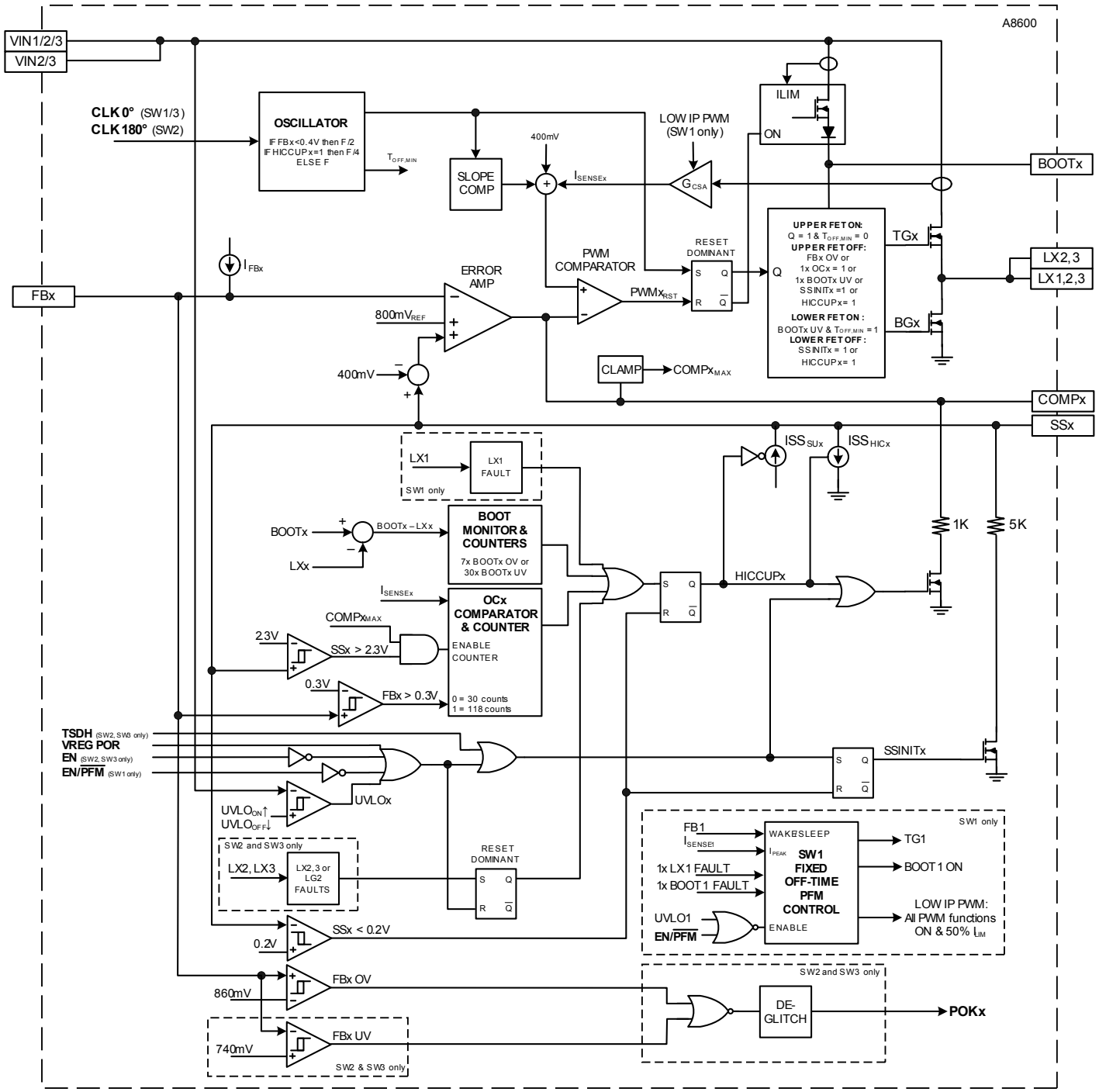

Figure 2. Detailed functional block diagram for SW1, SW2, and SW3

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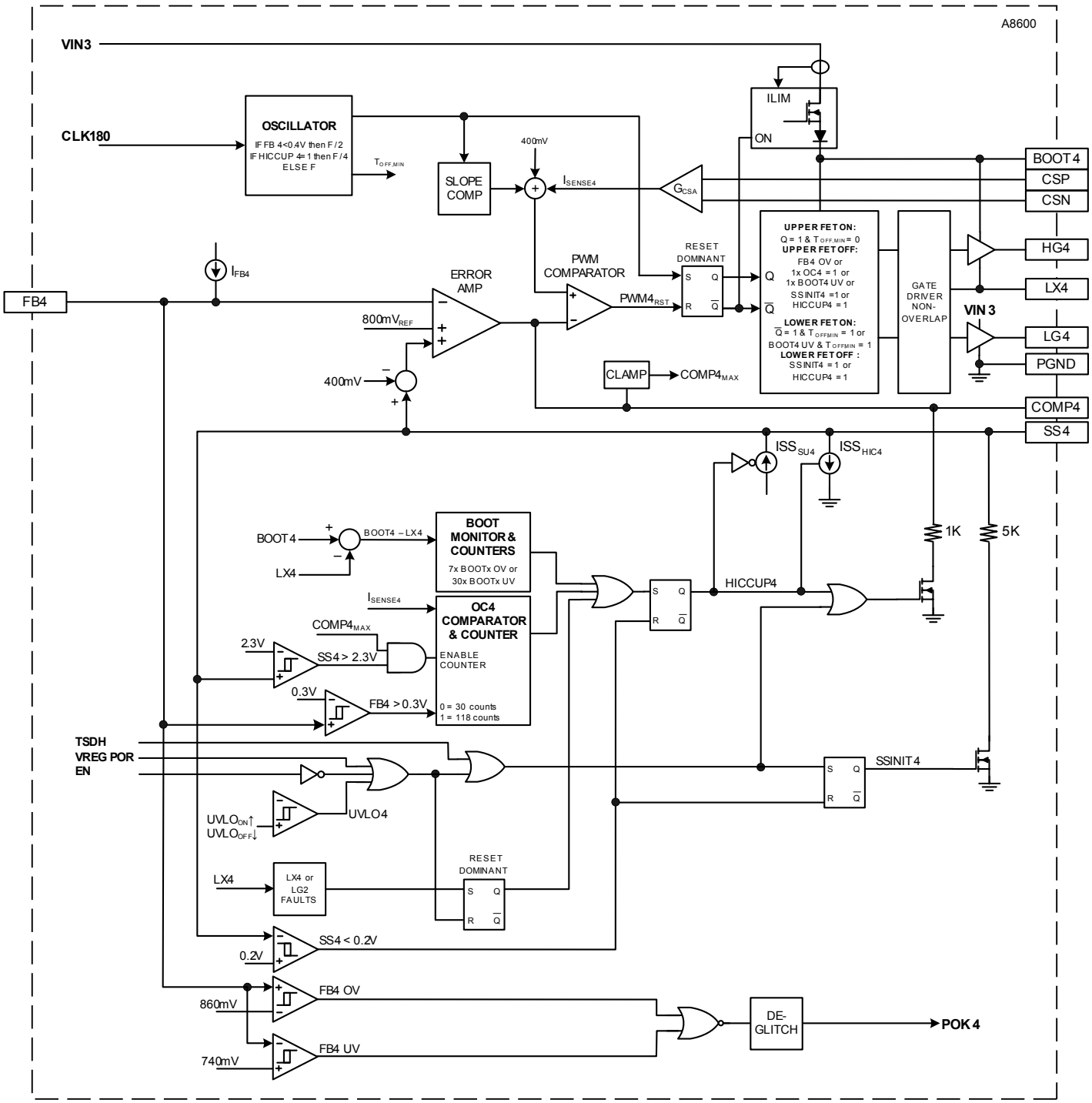

Figure 3. Detailed functional block diagram for SW4

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ELECTRICAL CHARACTERISTICS: Valid at 5.5 V ≤ V_{INx} ≤ 26 V, –40°C ≤ T_A ≤ 125°C, –40°C ≤ T_J ≤ 125°C; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Input Supply Current						
Input Supply Current [1]	I_{IN1}	V_{BIAS} > 3.2 V, I_{SW1} = 0 mA	–	7.5	10	mA
Input Supply Current, PFM [1][3] (Using components shown in Typical Application Circuit diagram and table 3.)	I_{LO_IQ0}	V_{IN1} = 12 V, V_{SW1} = 3.3 V, $V_{EN/SYNC}$ ≤ 0.4 V, BUO and ACCO open, I_{SW1} = 40 µA, T_A= 25°C	–	–	50	µA
	I_{LO_IQ1}	V_{IN1} = 12 V, V_{SW1} = 5.0 V, $V_{EN/SYNC}$ ≤ 0.4 V, BUO and ACCO open, I_{SW1} = 200 µA, T_A=25°C	–	–	250	µA
	I_{LO_IQ2}	V_{IN1} = 12 V, V_{SW1} = 6.5 V, $V_{EN/SYNC}$ ≤ 0.4 V, BUO and ACCO open, I_{SW1} = 1 mA, T_A = 25°C	–	–	750	µA
Internal Oscillator Frequency						
LX1/2/3/4 Switching Frequency	f_{OSC}		360	425	490	kHz
EN/SYNC Synchronization Timing						
Synchronization Input Frequency	f_{SYNC}		325	–	525	kHz
Synchronization Input Duty Cycle	D_{SYNC}		45	50	55	%
EN/SYNC Input						
EN/SYNC Pin High Threshold	V_{ENIH}	3.0 V < V_{BIAS} < 3.6 V, $V_{EN/SYNC}$ rising	–	–	2.0	V
		4.5 V < V_{BIAS} < 5.5 V, $V_{EN/SYNC}$ rising	–	–	2.6	V
EN/SYNC Pin Low Threshold	V_{ENIL}	3.0 V < V_{BIAS} < 3.6 V, $V_{EN/SYNC}$ falling	0.8	–	–	V
		4.5 V < V_{BIAS} < 5.5 V, $V_{EN/SYNC}$ falling	1.2	–	–	V
EN/SYNC Hysteresis	V_{ENHYS}	3.0 V < V_{BIAS} < 3.6 V, V_{ENIH} – V_{ENIL}	–	200	–	mV
		4.5 V < V_{BIAS} < 5.5 V, V_{ENIH} – V_{ENIL}	–	400	–	mV
EN/SYNC Input Resistance	R_{ENIN}		120	200	280	kΩ
EN/SYNC Turn-Off Delay	t_{dOFF}	Measured from EN/SYNC pulled low to SW2/3/4, S1/2, and TSD turned off	–	15	–	PWM cycles
	t_{dLo_IQ}	Measured from EN/SYNC pulled low or TSDH going high to SW1 entering Low IQ mode	–	2048	–	PWM cycles
VREG Output and BIAS Input						
VREG Output Voltage	V_{VREG}	V_{BIAS} = 0 V	2.95	3.05	3.175	V
VREG (REGOK rising)	$V_{REGPORHI}$	V_{VREG} rising	2.86	2.93	2.98	V
VREG (BIAS switch Off and POR)	$V_{REGPORLO}$	V_{VREG} falling	2.85	2.90	2.96	V
BIAS Switch Turn-On Threshold	$V_{BIAS(TH)}$	V_{BIAS} – V_{VREG}	−3	10	20	mV
Bias Switch Voltage Drop	V_{BIASSW}	V_{BIAS} – V_{VREG}	–	45	70	mV
BIAS Input Voltage Range	V_{BIAS}		3.2	–	5.5	V
Power OK (POK)						
POK Low Condition Output Voltage	$V_{POKO(L)}$	I_{POK} = 3 mA	–	–	300	mV
POK Leakage [1]	$I_{POK(LKG)}$	V_{POKO} = 5.0 V	−1	–	1	µA

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ELECTRICAL CHARACTERISTICS (continued): Valid at 5.5 V ≤ V_{INx} ≤ 26 V, –40°C ≤ T_A ≤ 125°C, –40°C ≤ T_J ≤ 125°C; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS (continued)						
Thermal Protection						
SW1/2/3/4 TSD Threshold [3]	T_{TSDH}	SW1 to Low IQ mode after 2048 cycles, reset by cycling EN/SYNC, or by a VREG POR	150	165	180	°C
S1/2 Latched TSD Threshold [3]	T_{TSDL}	Reset by cycling any of ENS, EN/SYNC, VINS, or by a VREG POR	140	155	170	°C
SW1 (ALWAYS-ON, LOW IQ, PWM/PFM REGULATOR)						
Input Voltage						
Input Voltage Range [2]	V_{IN1}		4.0	–	35	V
UVLO Start	$V_{UVLOON1}$	V_{IN1} rising	3.6	3.8	4.0	V
UVLO Stop	$V_{UVLOOFF1}$	V_{IN1} falling	3.2	3.4	3.6	V
UVLO Hysteresis	$V_{UVLOHYS1}$		–	400	–	mV
Voltage Regulation						
Feedback Voltage Accuracy	V_{FB1}	V_{IN1} ≥ 4.1 V, V_{FB1} = V_{COMP1}	788	800	812	mV
Output Voltage Setting Range	V_{SW1}	V_{SW1}(min) value is design target, see footnote 2 for typ and max voltages	3.3	5.0	6.5	V
Output Dropout Voltage	$V_{SW(PWM)1}$	V_{IN1} = 3.7 V, I_{SW1} = 50 mA	3.3	–	–	V
		V_{IN1} = 6.0 V, I_{SW1} = 1 A	5.0	–	–	V
Low IQ Peak Current Limit	$I_{PEAK(LO\_IQ)}$		600	800	1000	mA
Low IQ DC Current Capability	$I_{DC(LO\_IQ)}$		500	–	–	mA_{DC}
Low IQ Constant OFF Time	$t_{OFF(LO\_IQ)}$		220	300	380	ns
Low IQ Maximum ON Time	$t_{ON(LO\_IQ)}$		3.3	4	4.9	µs
Low IQ Mode Voltage Ripple [3]	$V_{PP1(LO\_IQ)}$	8 V < V_{IN1} < 12 V, configured as shown in the Typical Application Circuit	–	–	50	mV_{PP}
Internal MOSFET [2]						
High-Side MOSFET On-Resistance	$R_{DS(on)HS1}$	T_J = 25°C, I_{DS1} = 1.0 A	–	150	170	mΩ
High-Side MOSFET Leakage [1]	$I_{HS(LKG)1}$	T_J < 65°C,$V_{EN/SYNC}$ ≤ 0.8 V, V_{LX1} = 0 V, V_{IN1} = 12 V	–5	–	5	µA
Low-Side MOSFET On-Resistance	$R_{DS(on)LS1}$	T_J = 25°C	–	–	10	Ω
BOOT Regulator						
BOOT Voltage Enable Threshold	$V_{BOOT(TH)1}$	V_{BOOT1} rising	1.85	2.10	2.30	V
BOOT Voltage Enable Hysteresis	$V_{BOOT(HYS)1}$		–	375	–	mV
Error Amplifier						
Feedback Input Bias Current [1]	I_{FB1}		–30	–	–8	nA
Open Loop Voltage Gain	A_{VOL1}	V_{COMP1} = 1.2 V	52	58	65	dB
Transconductance	g_{m1}	400 mV < V_{FB1}	550	750	950	µA/V
		0 V < V_{FB1} < 400 mV	275	375	475	µA/V

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SW1 (ALWAYS-ON, LOW IQ, PWM/PFM REGULATOR) (continued)						
Error Amplifier (continued)						
Output Current	I_{EA1}	V_{COMP1} = 1.2 V	–	±75	–	µA
Maximum Output Voltage	$V_{EAO(max)1}$		1.3	1.7	2.1	V
Minimum Output Voltage	$V_{EAO(min)1}$		–	–	200	mV
COMP1 Pull Down Resistance	R_{COMP1}	Fault condition	–	1	–	kΩ
Pulse Width Modulation (PWM)						
PWM Ramp Offset	$V_{PWMOFFSET1}$	V_{COMP1} set for 0% duty cycle	–	400	–	mV
Minimum Controllable On-Time	$t_{ON(MIN)1}$		80	140	180	ns
Minimum Switch Off-Time	$t_{OFF(MIN)1}$		40	95	135	ns
COMP1 to SW1 Current Gain	$g_{mPOWER1}$		–	3.6	–	A/V
Slope Compensation	S_{E1}		300	450	600	mA/µs
Overcurrent Protection (OCP)						
Pulse-by-Pulse Current Limit	I_{LIM1}	$t_{ON1} = t_{ON(MIN)1}$, $f_{SW} = f_{OSC}$	3.9	4.4	4.9	A
		$t_{ON1} = (1 / f_{OSC}) – t_{OFF(MIN)1}$, $f_{SW} = f_{OSC}$	3.0	3.5	4.0	A
Overvoltage Protection (OVP)						
Output Overvoltage Threshold (SW1 Disable)	V_{OVO1}	V_{FB1} rising, PWM mode	840	860	880	mV
Overvoltage Hysteresis	$V_{OVOHYS1}$	V_{FB1} falling, relative to V_{OVO1}	–	−10	–	mV
Soft Start						
SS1 Hiccup Reset Voltage	V_{SSRST1}	V_{SS1} falling due to R_{SSFLT1}	140	200	275	mV
SS1 Switching Frequency	f_{SS1}	0 V < V_{FB1} < 300 mV, V_{COMP1} at maximum	–	$f_{SW1}/4$	–	kHz
		0 V < V_{FB1} < 300 mV	–	$f_{SW1}/2$	–	kHz
		300 mV < V_{FB1}	–	f_{SW1}	–	kHz
SS1 Startup (Source) Current [1]	I_{SSSU1}	Hiccup mode disabled (no fault condition)	−2.50	−2.00	−1.50	µA
SS1 Hiccup (Sink) Current [1]	I_{SSHIC1}	Hiccup mode enabled	0.75	1.00	1.25	µA
SS1 Delay Time	t_{dSS1}	CSS1 = 0.68 µF	–	136	–	ms
SS1 Ramp Time	$t_{SSRAMP1}$	CSS1 = 0.68 µF	–	272	–	ms
SS1 Pull Down Resistance	R_{SSFLT1}	Fault condition	–	5	–	kΩ
Hiccup Mode (PWM only, not in PFM)						
Hiccup OCP Enable Threshold	V_{HICEN1}	V_{SS1} rising	–	2.3	–	V
Hiccup Operation OCP Count	$t_{OCPLIM1}$	V_{SS1} > 2.3 V, V_{FB1} < 0.3 V	–	30	–	PWM cycles
		V_{SS1} > 2.3 V, V_{FB1} > 0.3 V	–	118	–	PWM cycles
Hiccup Operation BOOT Shorted Count	$t_{BOOTUV1}$		–	30	–	PWM cycles
Hiccup Operation BOOT Open Count	$t_{BOOTOPEN1}$		–	7	–	PWM cycles

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SW2 (ASYNCHRONOUS BUCK REGULATOR)						
Input Voltage						
Input Voltage Range [2]	V_{IN2}		4.4	–	35	V
UVLO Start	$V_{UVLOON2}$	V_{IN2} rising	4.1	4.25	4.4	V
UVLO Stop	$V_{UVLOOFF2}$	V_{IN2} falling	3.6	3.75	3.9	V
UVLO Hysteresis	$V_{UVLOHYS2}$		–	500	–	mV
Voltage Regulation						
Feedback Voltage Accuracy	V_{FB2}	V_{IN2} ≥ 4.4 V, V_{FB2} = V_{COMP2}	788	800	812	mV
Output Voltage Setting Range	V_{SW2}	V_{SW2}(typ) value is design target, see footnote 2 for min and max voltages	1.2	8.0	9.2	V
Output Dropout Voltage [3]	$V_{SW(PWM)2}$	V_{IN2} = 6.0 V, I_{SW2} = 1 A	5.0	–	–	V
Internal MOSFET [2]						
High-Side MOSFET On-Resistance	$R_{DS(on)HS2}$	T_J = 25°C, I_{DS2} = 1.5 A	–	120	140	mΩ
High-Side MOSFET Leakage [1]	$I_{HS(LKG)2}$	T_J < 65°C,$V_{EN/SYNC}$ ≤ 0.8 V, V_{LX2} = 0 V, V_{IN2} = 12 V	–5	–	5	µA
Low-Side MOSFET On-Resistance	$R_{DS(on)LS2}$	T_J = 25°C	–	–	10	Ω
BOOT Regulator						
BOOT Voltage Enable Threshold	$V_{BOOT(TH)2}$	V_{BOOT2} rising	1.85	2.10	2.30	V
BOOT Voltage Enable Hysteresis	$V_{BOOT(HYS)2}$		–	375	–	mV
Error Amplifier						
Feedback Input Bias Current [1]	I_{FB2}		–100	–	–8	nA
Open Loop Voltage Gain	A_{VOL2}	V_{COMP2} = 1.2 V	52	60	65	dB
Transconductance	g_{m2}	400 mV < V_{FB2}	550	750	950	µA/V
		0 V < V_{FB2} < 400 mV	275	375	475	µA/V
Output Current	I_{EA2}	V_{COMP2} = 1.2 V	–	±75	–	µA
Maximum Output Voltage	$V_{EAO(max)2}$		1.3	1.7	2.1	V
Minimum Output Voltage	$V_{EAO(min)2}$		–	–	200	mV
COMP2 Pull Down Resistance	R_{COMP2}	Fault condition	–	1	–	kΩ
Pulse Width Modulation (PWM)						
PWM Ramp Offset	$V_{PWMOFFSET2}$	V_{COMP2} set for 0% duty cycle	–	400	–	mV
Minimum Controllable On-Time	$t_{ON(MIN)2}$		80	140	180	ns
Minimum Switch Off-Time	$t_{OFF(MIN)2}$		40	95	135	ns
COMP2 to SW2 Current Gain	$g_{mPOWER2}$		–	3.6	–	A/V
Slope Compensation	S_{E2}		300	450	600	mA/µs

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SW2 (ASYNCHRONOUS BUCK REGULATOR) (continued)						
Overcurrent Protection (OCP)						
Pulse-by-Pulse Current Limit	I_{LIM2}	$t_{ON2} = t_{ON(MIN)2}$, $f_{SW} = f_{OSC}$	3.9	4.4	4.9	A
		$t_{ON2} = (1 / f_{OSC}) – t_{OFF(MIN)2}$, $f_{SW} = f_{OSC}$	3.0	3.5	4.0	A
Power OK (POK) Thresholds for Overvoltage (OV) and Undervoltage (UV)						
POK Threshold for Overvoltage	V_{POKOV2}	V_{FB2} rising	840	860	880	mV
POK Hysteresis for Overvoltage	$V_{POKOVHYS2}$	V_{FB2} falling, relative to V_{POKOV2}	–	−10	–	mV
POK Threshold for Undervoltage	V_{POKUV2}	V_{FB2} falling	720	740	760	mV
POK Hysteresis for Undervoltage	$V_{POKUVHYS2}$	V_{FB2} rising, relative to V_{POKUV2}	–	10	–	mV
Power OK (POK) Filtering						
POK Delay Time	$V_{POKDELAY2}$	Response to a step input	–	6	–	µs
Soft Start						
SS2 Hiccup Reset Voltage	V_{SSRST2}	V_{SS2} falling due to R_{SSFLT2}	140	200	275	mV
SS2 Switching Frequency	f_{SS2}	0 V < V_{FB2} < 300 mV, V_{COMP2} at maximum	–	$f_{SW2}/4$	–	kHz
		0 V < V_{FB2} < 300 mV	–	$f_{SW2}/2$	–	kHz
		300 mV < V_{FB2}	–	f_{SW2}	–	kHz
SS2 Startup (Source) Current [1]	I_{SSSU2}	Hiccup mode disabled (no fault condition)	−30	–20	−10	µA
SS2 Hiccup (Sink) Current [1]	I_{SSHIC2}	Hiccup mode enabled	5	10	20	µA
SS2 Delay Time	t_{dSS2}	CSS2 = 22 nF	–	440	–	µs
SS2 Ramp Time	$t_{SSRAMP2}$	CSS2 = 22 nF	–	880	–	µs
SS2 Pull Down Resistance	R_{SSFLT2}	Fault condition	–	5	–	kΩ
SS2 Startup Current Ratio	$I_{SSSUTRK2}$	Relative to I_{SSSU3} or I_{SSSU4}	−15	–	+15	%
Hiccup Mode						
Hiccup OCP Enable Threshold	V_{HICEN2}	V_{SS2} rising	–	2.3	–	V
Hiccup Operation OCP Count	$t_{OCPLIM2}$	V_{SS2} > 2.3 V, V_{FB2} < 0.3 V	–	30	–	PWM cycles
		V_{SS2} > 2.3 V, V_{FB2} > 0.3 V	–	118	–	PWM cycles
Hiccup Operation BOOT Shorted Count	$t_{BOOTUV2}$		–	30	–	PWM cycles
Hiccup Operation BOOT Open Count	$t_{BOOTOPEN2}$		–	7	–	PWM cycles

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SW3 (ASYNCHRONOUS BUCK REGULATOR)						
Input Voltage Specifications						
Input Voltage Range [2]	V_{IN3}		4.4	–	35	V
UVLO Start	$V_{UVLOON3}$	V_{IN3} rising	4.1	4.25	4.4	V
UVLO Stop	$V_{UVLOOFF3}$	V_{IN3} falling	3.6	3.75	3.9	V
UVLO Hysteresis	$V_{UVLOHYS3}$		–	500	–	mV
Voltage Regulation						
Feedback Voltage Accuracy	V_{FB3}	V_{IN3} ≥ 4.4 V, V_{FB3} = V_{COMP3}	788	800	812	mV
Output Voltage Setting Range	V_{SW3}	V_{SW3}(typ) value is design target, see footnote 2 for min and max voltages	1.2	3.3	9.2	V
Output Dropout Voltage [3]	$V_{SW(PWM)3}$	Configured as in Ty, V_{IN3} = 6.0 V, I_{SW3} = 1 A	5.0	–	–	V
Internal MOSFET Parameters [2]						
High-Side MOSFET On-Resistance	$R_{DS(on)HS3}$	T_J = 25°C, I_{DS3} = 2.0 A	–	112	130	mΩ
High-Side MOSFET Leakage [1]	$I_{HS(LKG)3}$	T_J < 65°C,$V_{EN/SYNC}$ ≤ 0.8 V, V_{LX3} = 0 V, V_{IN3} = 12 V	–5	–	5	µA
Low-Side MOSFET On-Resistance	$R_{DS(on)LS3}$	T_J = 25°C	–	–	10	Ω
BOOT Regulator						
BOOT Voltage Enable Threshold	$V_{BOOT(TH)3}$	V_{BOOT3} rising	1.85	2.10	2.30	V
BOOT Voltage Enable Hysteresis	$V_{BOOT(HYS)3}$		–	375	–	mV
Error Amplifier						
Feedback Input Bias Current [1]	I_{FB3}		–100	–	–8	nA
Open Loop Voltage Gain	A_{VOL3}	V_{COMP3} = 1.2 V	52	60	65	dB
Transconductance	g_{m3}	400 mV < V_{FB3}	550	750	950	µA/V
		0 V < V_{FB3} < 400 mV	275	375	475	µA/V
Output Current	I_{EA3}	V_{COMP3} = 1.2 V	–	±75	–	µA
Maximum Output Voltage	$V_{EAO(max)3}$		1.3	1.7	2.1	V
Minimum Output Voltage	$V_{EAO(min)3}$		–	–	200	mV
COMP3 Pull Down Resistance	R_{COMP3}	Fault condition	–	1	–	kΩ
Pulse Width Modulation (PWM)						
PWM Ramp Offset	$V_{PWMOFFSET3}$	V_{COMP3} set for 0% duty cycle	–	400	–	mV
Minimum Controllable On-Time	$t_{ON(MIN)3}$		80	140	180	ns
Minimum Switch Off-Time	$t_{OFF(MIN)3}$		40	95	135	ns
COMP3 to SW3 Current Gain	$g_{mPOWER3}$		–	3.6	–	A/V
Slope Compensation	S_{E3}		300	450	600	mA/µs

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SW3 (ASYNCHRONOUS BUCK REGULATOR) (continued)						
Overcurrent Protection (OCP)						
Pulse-by-Pulse Current Limit	I_{LIM3}	$t_{ON3} = t_{ON(MIN)3}$, $f_{SW} = f_{OSC}$	3.9	4.4	4.9	A
		$t_{ON3} = (1 / f_{OSC}) – t_{OFF(MIN)3}$, $f_{SW} = f_{OSC}$	3.0	3.5	4.0	A
Power OK (POK) Thresholds for Overvoltage (OV) and Undervoltage (UV)						
POK Threshold for Overvoltage	V_{POKOV3}	V_{FB3} rising	840	860	880	mV
POK Hysteresis for Overvoltage	$V_{POKOVHYS3}$	V_{FB3} falling, relative to V_{POKOV3}	–	−10	–	mV
POK Threshold for Undervoltage	V_{POKUV3}	V_{FB3} falling	720	740	760	mV
POK Hysteresis for Undervoltage	$V_{POKUVHYS3}$	V_{FB3} rising, relative to V_{POKUV3}	–	10	–	mV
Power OK (POK) Filtering						
POK Delay Time	$V_{POKDELAY3}$	Response to a step input	–	6	–	µs
Soft Start						
SS3 Hiccup Reset Voltage	V_{SSRST3}	V_{SS3} falling due to R_{SSFLT3}	140	200	275	mV
SS3 Switching Frequency	f_{SS3}	0 V < V_{FB3} < 300 mV, V_{COMP3} at maximum	–	$f_{SW3}/4$	–	kHz
		0 V < V_{FB3} < 300 mV	–	$f_{SW3}/2$	–	kHz
		300 mV < V_{FB3}	–	f_{SW3}	–	kHz
SS3 Startup (Source) Current [1]	I_{SSSU3}	Hiccup mode disabled (no fault condition)	−30	–20	−10	µA
SS3 Hiccup (Sink) Current [1]	I_{SSHIC3}	Hiccup mode enabled	5	10	20	µA
SS3 Delay Time	t_{dSS3}	CSS3 = 22 nF	–	440	–	µs
SS3 Ramp Time	$t_{SSRAMP3}$	CSS3 = 22 nF	–	880	–	µs
SS3 Pull Down Resistance	R_{SSFLT3}	Fault condition	–	5	–	kΩ
SS3 Startup Current Ratio	$I_{SSSUTRK3}$	Relative to I_{SSSU2} or I_{SSSU4}	−15	–	+15	%
Hiccup Mode						
Hiccup OCP Enable Threshold	V_{HICEN3}	V_{SS3} rising	–	2.3	–	V
Hiccup Operation OCP Count	$t_{OCPLIM3}$	V_{SS3} > 2.3 V, V_{FB3} < 0.3 V	–	30	–	PWM cycles
		V_{SS3} > 2.3 V, V_{FB3} > 0.3 V	–	118	–	PWM cycles
Hiccup Operation BOOT Shorted Count	$t_{BOOTUV3}$		–	30	–	PWM cycles
Hiccup Operation BOOT Open Count	$t_{BOOTOPEN3}$		–	7	–	PWM cycles

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SW4 (SYNCHRONOUS BUCK CONTROLLER WITH GATE DRIVERS)						
Input Voltage Specifications						
Input Voltage Range [2]	V_{IN3}		4.4	–	35	V
UVLO Start	$V_{UVLOON4}$	V_{IN3} rising	4.1	4.25	4.4	V
UVLO Stop	$V_{UVLOOFF4}$	V_{IN3} falling	3.6	3.75	3.9	V
UVLO Hysteresis	$V_{UVLOHYS4}$		–	500	–	mV
Voltage Regulation						
Feedback Voltage Accuracy	V_{FB4}	V_{IN3} ≥ 4.4 V, V_{FB4} = V_{COMP4}	788	800	812	mV
Output Voltage Setting Range	V_{SW4}	V_{SW4}(typ) value is design target, see footnote 2 for min and max voltages	1.2	5.7	6.5	V
Output Dropout Voltage [3]	$V_{SW(PWM)4}$	Configured as in Typical Application Circuit, V_{IN4} = 6.0 V, I_{SW4} = 1 A	5.0	–	–	V
External MOSFET Gate Drivers						
HG4 High Output Voltage	V_{HG4ON}	Measured as V_{HG4} – V_{IN3}	4.0	6.0	6.7	V
HG4 Low Output Voltage	V_{HG4OFF}	Measured as V_{HG4} – V_{LX4}, I_{HG4} = 100 mA	–	0.20	0.40	V
HG4 Sink Current [1]	I_{HG4ON}	V_{HG4} = V_{IN3} – 2 V	–	1000	–	mA
HG4 Source Current [1]	I_{HG4OFF}	V_{HG4} = V_{IN3} – 2 V	–	–150	–	mA
LG4 High Output Voltage	V_{LG4ON}	V_{IN3} ≥ 5.5 V	4.0	6.0	7.2	V
LG4 Low Output Voltage	V_{LG4OFF}	I_{LG4} = 100 mA	–	0.25	0.50	V
LG4 Source Current [1]	I_{LG4ON}		–	–500	–	mA
LG4 Sink Current [1]	I_{LG4OFF}		–	600	–	mA
BOOT Regulator						
BOOT Voltage Enable Threshold	$V_{BOOT(TH)4}$	V_{BOOT4} rising	2.25	2.60	2.90	V
BOOT Voltage Enable Hysteresis	$V_{BOOT(HYS)4}$		–	375	–	mV
Error Amplifier						
Feedback Input Bias Current [1]	I_{FB4}		–100	–	–8	nA
Open Loop Voltage Gain	A_{VOL4}	V_{COMP4} = 1.2 V	52	60	65	dB
Transconductance	g_{m4}	400 mV < V_{FB4}	550	750	950	µA/V
		0 V < V_{FB4} < 400 mV	275	375	475	µA/V
Output Current	I_{EA4}	V_{COMP4} = 1.2 V	–	±75	–	µA
Maximum Output Voltage	$V_{EAO(max)4}$		1.3	1.7	2.1	V
Minimum Output Voltage	$V_{EAO(min)4}$		–	–	200	mV
COMP4 Pull Down Resistance	R_{COMP4}	Fault condition	–	1	–	KΩ

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SW4 (SYNCHRONOUS BUCK CONTROLLER WITH GATE DRIVERS) (continued)						
Pulse Width Modulation (PWM)						
PWM Ramp Offset	$V_{PWMOFFSET4}$	V_{COMP4} set for 0% duty cycle	–	400	–	mV
COMP4 Cycle Skip Level	$V_{COMPSKIP4}$	V_{SS4} < 2.3 V	–	200	–	mV
Minimum Controllable On-Time	$t_{ON(MIN)4}$		40	100	150	ns
Minimum Switch Off-Time	$t_{OFF(MIN)4}$		80	120	160	ns
COMP4 to SW4 Current Gain	$g_{mPOWER4}$		–	63	–	(A•mΩ)/V
Slope Compensation	S_{E4}		4.5	6.8	9.0	mV/µs
Overcurrent Protection (OCP)						
Pulse-by-Pulse Current Limit	I_{LIM4}	$t_{ON4} = t_{ON(MIN)4}$	62	75	88	mV
		$t_{ON4} = (1/f_{OSC}) - t_{OFF(MIN)4}$, $f_{SW} = f_{OSC}$	48	60	72	mV
Power OK (POK) Thresholds for Overvoltage (OV) and Undervoltage (UV)						
POK Threshold for Overvoltage	V_{POKOV4}	V_{FB4} rising	840	860	880	mV
POK Hysteresis for Overvoltage	$V_{POKOVHYS4}$	V_{FB4} falling, relative to V_{POKOV4}	–	−10	–	mV
POK Threshold for Undervoltage	V_{POKUV4}	V_{FB4} falling	720	740	760	mV
POK Hysteresis for Undervoltage	$V_{POKUVHYS4}$	V_{FB4} rising, relative to V_{POKUV4}	–	10	–	mV
Power OK (POK) Filtering						
POK Delay / De-glitch	$V_{POKDELAY4}$	Response to a step input	–	6	–	µs
Soft Start						
SS4 Hiccup Reset Voltage	V_{SSRST4}	V_{SS4} falling due to R_{SSFLT4}	140	200	275	mV
SS4 Switching Frequency	f_{SS4}	0 V < V_{FB4} < 300 mV, V_{COMP4} at maximum	–	$f_{SW4}/4$	–	kHz
		0 V < V_{FB4} < 300 mV	–	$f_{SW4}/2$	–	kHz
		300 mV < V_{FB4}	–	f_{SW4}	–	kHz
SS4 Startup (Source) Current [1]	I_{SSSU4}	Hiccup mode disabled (no fault condition)	−30	–20	−10	µA
SS4 Hiccup (Sink) Current [1]	I_{SSHIC4}	Hiccup mode enabled	5	10	20	µA
SS4 Delay Time	t_{dSS4}	CSS4 = 22 nF	–	440	–	µs
SS4 Ramp Time	$t_{SSRAMP4}$	CSS4 = 22 nF	–	880	–	µs
SS4 Pull Down Resistance	R_{SSFLT4}	Fault condition	–	5	–	KΩ
SS4 Startup Current Ratio	$I_{SSSUTRK4}$	Relative to I_{SSSU2} or I_{SSSU3}	−15	–	+15	%

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Hiccup Mode						
Hiccup OCP Enable Threshold	V_{HICEN4}	V_{SS4} rising	–	2.3	–	V
Hiccup Operation OCP Count	$t_{OCPLIM4}$	V_{SS4} > 2.3 V, V_{FB4} < 0.3 V	–	30	–	PWM cycles
		V_{SS4} > 2.3 V, V_{FB4} > 0.3 V	–	118	–	PWM cycles
Hiccup Operation BOOT Shorted Count	$t_{BOOTUV4}$		–	30	–	PWM cycles
Hiccup Operation BOOT Open Count	$t_{BOOTOPEN4}$		–	7	–	PWM cycles
HIGH-SIDE SWITCHES (S1, S2)						
Input Voltage Range [2]	V_{INS}		4.5	–	35	V
UVLO Start	$V_{UVLOONS}$	V_{INS} rising	4.0	4.2	4.4	V
UVLO Stop	$V_{UVLOOFFS}$	V_{INS} falling	3.5	3.7	3.9	V
UVLO Hysteresis	$V_{UVLOHYSS}$		–	500	–	mV
Overvoltage Threshold (Rising)	$V_{OVRISES}$	V_{INS} rising	17.2	18.3	19.4	V
Overvoltage Threshold (Falling)	$V_{OVFALLS}$	V_{INS} falling	16.9	18.0	19.0	V
MOSFET On-Resistance	$R_{DS(on)S}$	I_S = 250 mA, T_J = 25°C	–	1.00	1.15	Ω
Voltage Drop	ΔV_S	V_{INS} ≥ 5.5 V, I_S = −250 mA, T_J = 25°C	–	250	290	mV
		V_{INS} ≥ 4.5 V, I_S = −100 mA, T_J = 25°C	–	100	115	mV
Current Limit [1][2]	I_{PEAKS}	Not continuous	−570	−450	−270	mA
Foldback Current [1]	I_{FLDBKS}	V_{OUTx} = 0 V, V_{INS} = 15 V	−150	−100	−55	mA
Leakage Current [1]	I_{LKGS}		−1	–	1	µA
Pull Down Resistance	R_{FLTS}		–	200	–	kΩ
Turn-On Delay	t_{dS}	V_{ENS} rise to 10% of ΔV_{OUTx}	10	60	200	µs
Output Rise Time	t_{rS}	237 Ω / 1 µF load, 10% to 90% of ΔV_{OUTx}	10	60	200	µs
ENS High Threshold	V_{ENSH}		–	–	2.0	V
ENS Low Threshold	V_{ENSL}		0.8	–	–	V
ENS Hysteresis	V_{ENSHYS}		–	100	–	mV
ENS Input Resistance	R_{INENS}		120	200	280	kΩ

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
BU AND ACC COMPARATORS						
BUI and ACCI Detect Threshold	V_{DET}		1.181	1.205	1.229	V
BUI and ACCI Input Bias [1]	I_{BUI}, I_{ACCI}	V_{BUI} or V_{ACCI} ≤ 5.0 V	30	65	100	nA
BUO Delay	t_{dBUO}	20 mV input overdrive	–	1.5	5	µs
ACCO Delay	t_{dACCO}	20 mV input overdrive	–	1.5	5	µs
BUO and ACCO Output Voltage	V_{BUOH}, V_{ACCOH}	I_{BUO} = I_{ACCO} = −3 mA	V_{BIAS} – 300 mV	–	V_{BIAS}	V
	V_{BUOL}, V_{ACCOL}	I_{BUO} = I_{ACCO} = 3 mA	–	–	300	mV
BUO and ACCO Forced Low	V_{BUOLF}, V_{ACCOLF}	I_{BUO} = I_{ACCO} = 3 mA , 2 V < V_{BIAS} < 3 V, V_{IN1} < 5.5 V	–	–	300	mV
CTMR and MUTE						
CTMR Charge Current [1]	$I_{CTMR(CHRG)}$	MUTE = low, V_{CTMR} rising	−2.50	−2.00	−1.50	µA
CTMR Discharge Current [1]	$I_{CTMR(DIS)}$	MUTE = low, V_{CTMR} falling	1.50	2.00	2.50	µA
CTMR Upper Threshold	V_{CTMRVH}	V_{CTMR} rising	1.181	1.205	1.229	V
CTMR Lower Threshold	V_{CTMRVL}	V_{CTMR} falling	185	215	245	mV
CTMR Pull Down Resistance	R_{CTMR}	MUTE = high	–	50	–	kΩ
MUTE Low Output Voltage	V_{MUTEOL}	I_{MUTE} = 3 mA	–	–	300	mV
MUTE Leakage Current [1]	$I_{MUTELKG}$	V_{MUTE} = 5.0 V	−1	–	1	µA
MUTE Rising Delay	t_{drMUTE}	C_{CTMR} = 0.10 µF	725	1000	1275	ms
MUTE Falling Delay (De-glitch)	t_{dfMUTE}	From BUO set low to MUTE low	8	16	32	µs
MUTE Self-Protect Shutoff	$V_{MUTE(OFF)}$		–	8.5	–	V

[1] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[2] Thermally limited depending on input voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3] Determined by design and characterization, not production tested.

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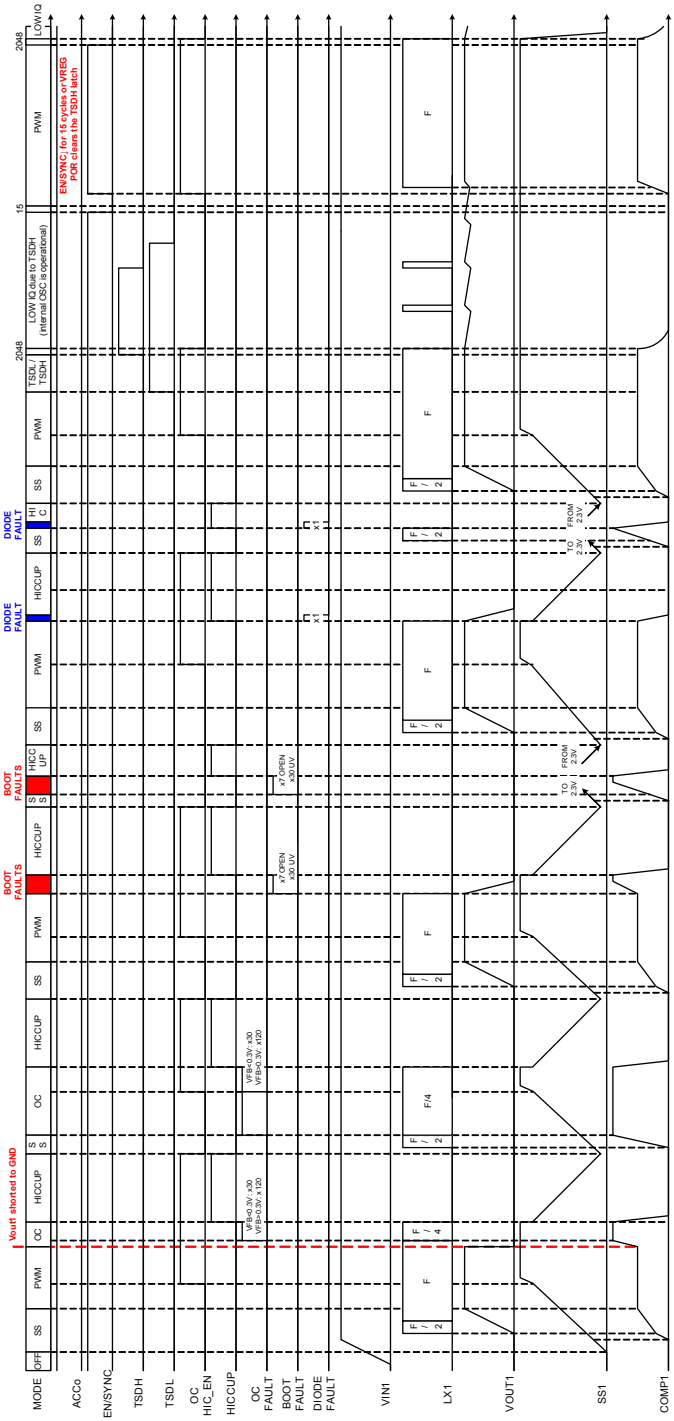

Figure 4. SW1 PWM Timing Diagram with EN/SYNC pin high

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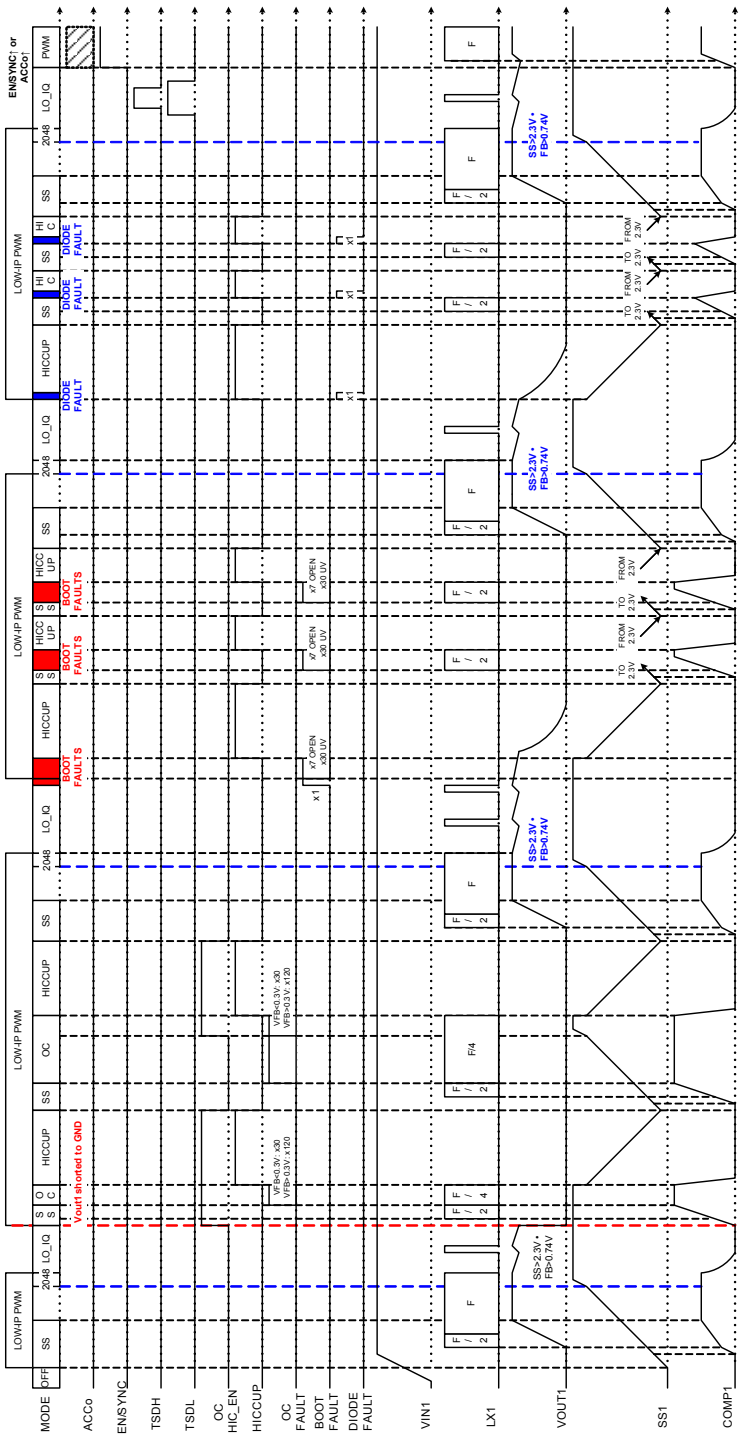

Figure 5. SW1 Low IQ PWM and Low IP PFM timing, with EN/SYNC low and ACCI low

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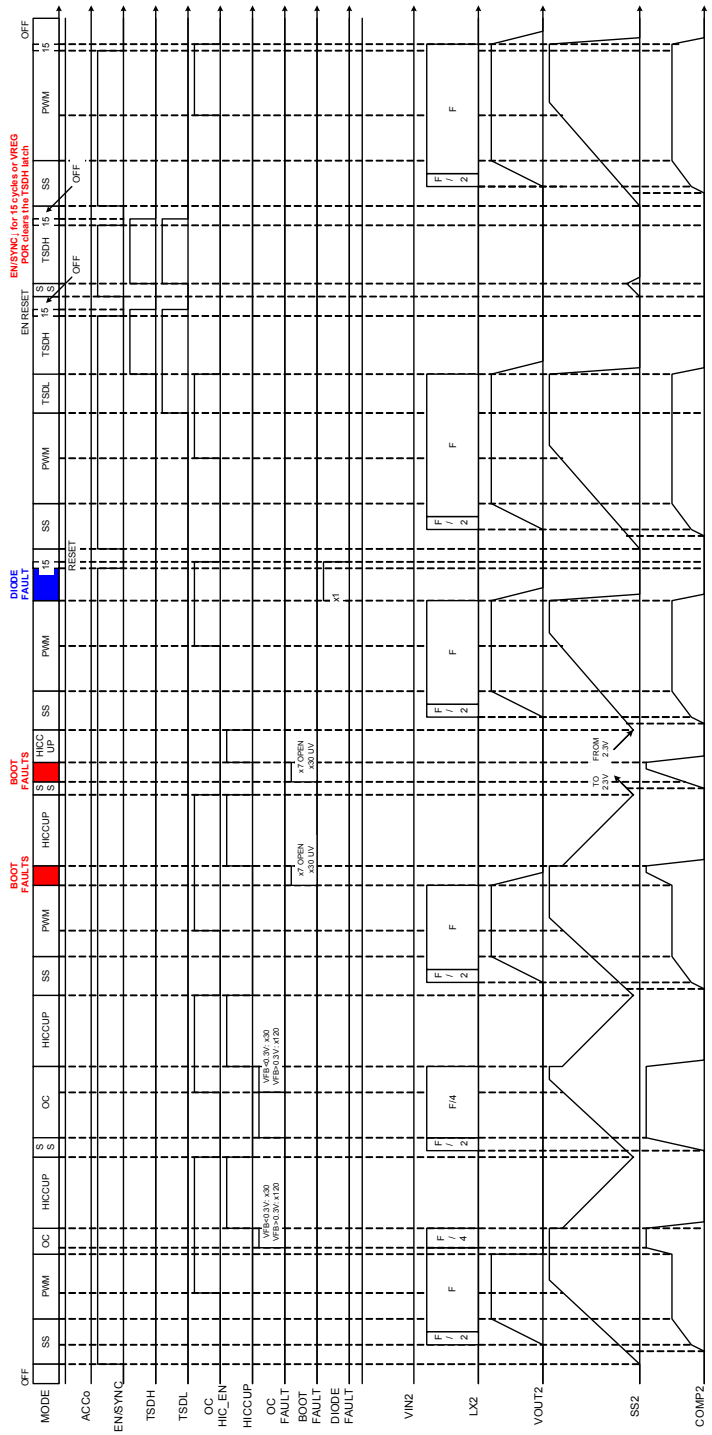

Figure 6. SW2, SW3, and SW4 PWM timing

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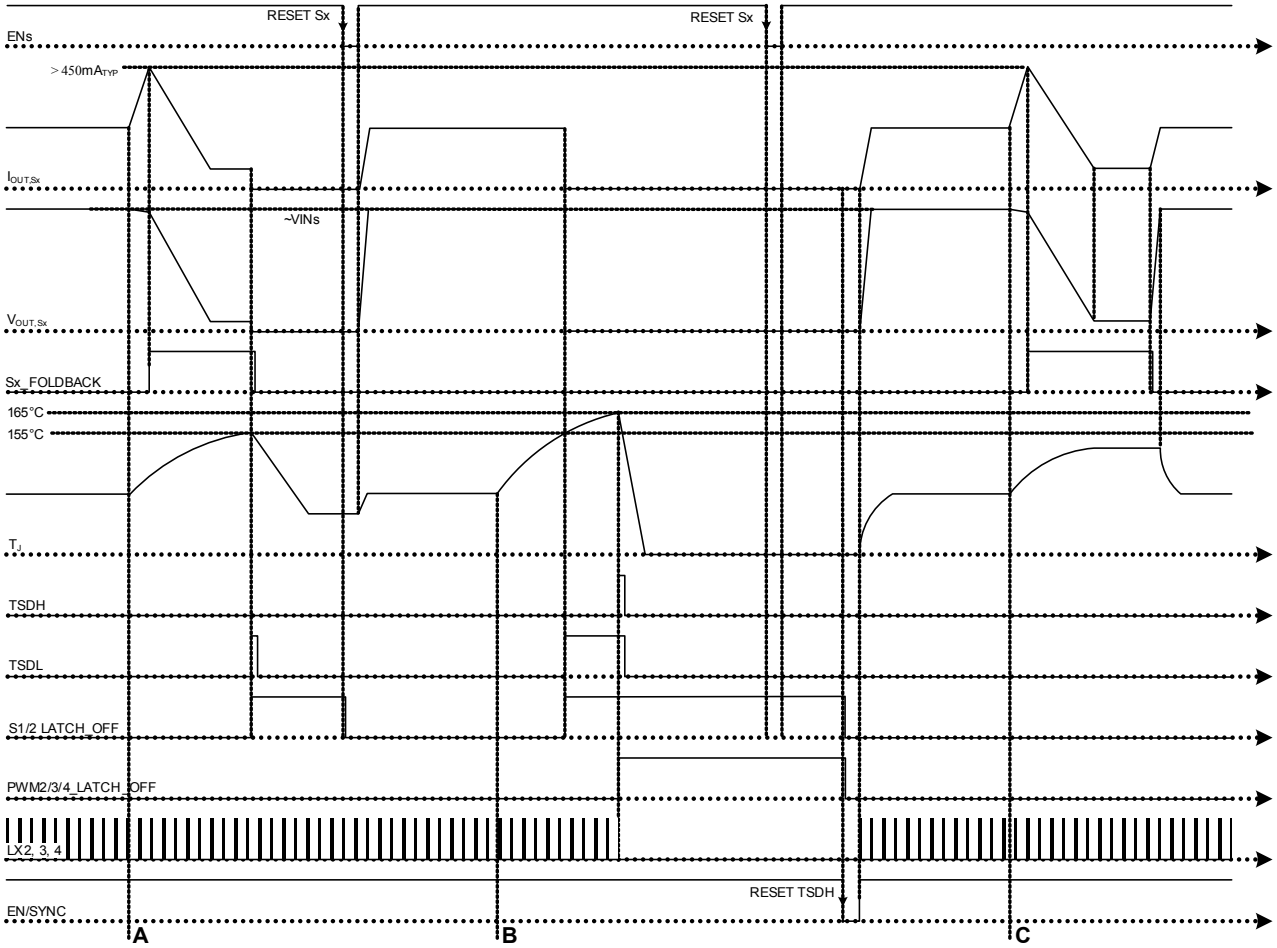

Figure 7. S1 and S2 Timing

A. The load on one of the high-side switches increases until it enters foldback. The A8600 junction temperature increases. When the junction temperature exceeds 155°C (TSDL) both high-side switches (S1, S2) are latched off. This state is maintained until the high-side switches are reset via the ENS.

B. The loads on the A8600 increase and the junction temperature begins to increase. When the junction temperature exceeds 155°C (TSDL) both high-side switches (S1, S2) are latched off. In this case, even though the switches are shut off, the junction temperature continues to increase. When the junction temperature exceeds 165°C (TSDH) switching regulators SW2, SW3, and SW4 are also latched off, and SW1 enters Low IQ PFM mode. After TSDH, both high side switches (S1, S2) and the switching regulators SW2, SW3, and SW4 remain latched off until they are reset via EN/SYNC.

C. The load on one of the high-side switches increases until it enters foldback. The junction temperature increases but does not exceed 155°C (TSDL). When the load on the high-side switch decreases, the switch exits foldback and the output voltage recovers.

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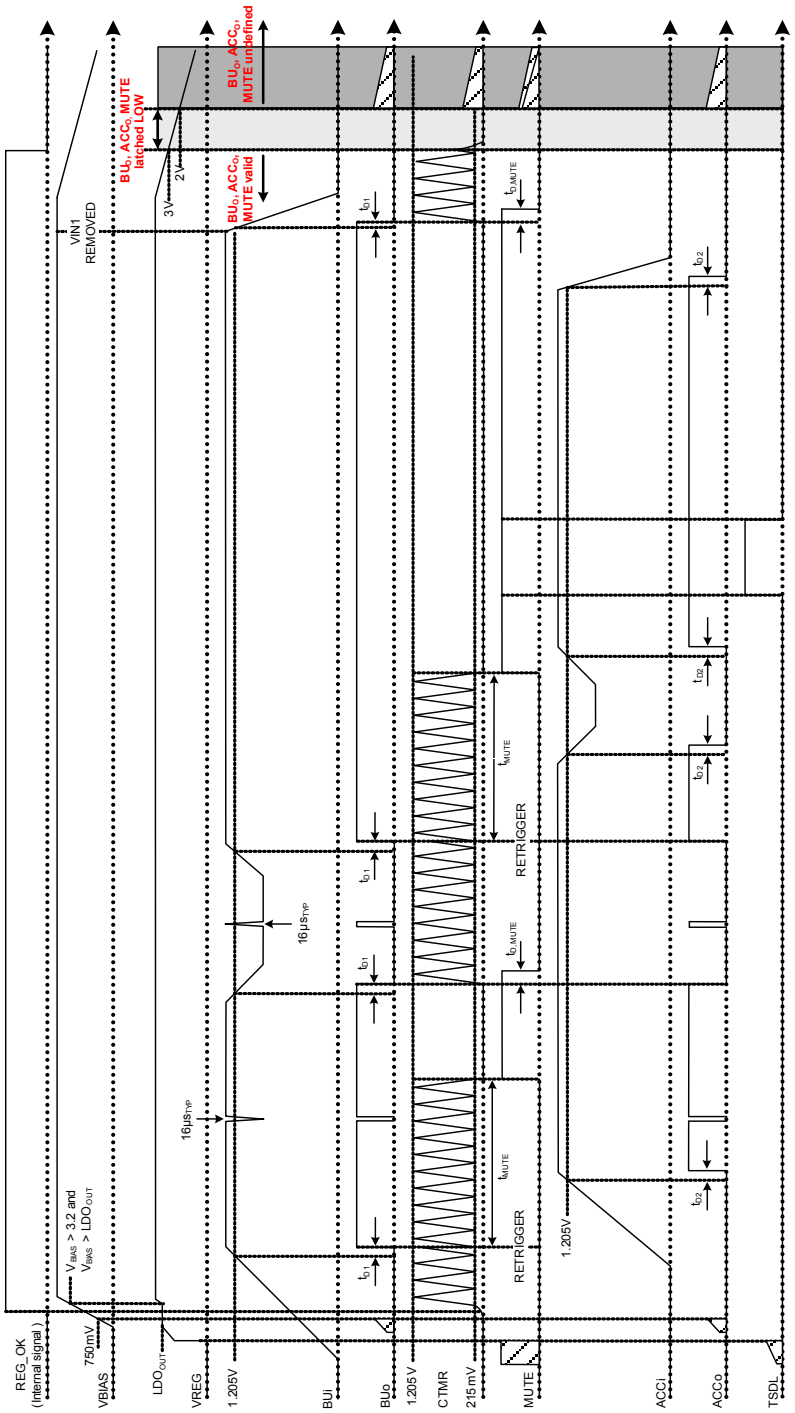

Figure 8. BUx, ACCx and MUTE/CTMR timing

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Functional Description

Overview

The A8600 is a highly sophisticated, multi-function IC that incorporates all the control and protection circuitry necessary to provide the power supply requirements of next generation car audio and infotainment systems.

The A8600 features three adjustable asynchronous peak current mode buck regulators with internal MOSFETS. These three regulators, SW1, SW2, and SW3, can continuously supply 1.0 A, 2.0 A and 2.5 A respectively. A synchronous controller, SW4, was designed to deliver up to 4 A but can be configured for as much as 8 A by setting the sense resistor accordingly.

SW1 is an always-on buck regulator that provides Low Quiescent Input Current (Low IQ) mode. When the EN/SYNC and ACCI pins are held low, SW1 employs pulse frequency modulation (PFM) to draw only 10s of microamperes from the input supply while delivering 3.3V, 5.0V, or 6.5V at no load.

SW4 is an adjustable, synchronous, peak current mode buck controller with internal MOSFET gate drivers and externally adjustable current limit.

In addition, the A8600 incorporates two 1 Ω high-side switches, S1 and S2) which typically provide 250 mA (DC) and 450 mA (peak), with foldback type overcurrent protection. For thermal reasons, S1 and S2 are allowed to be on only for input voltages up to approximately 18.3 V.

The A8600 also offers two detectors (that is, comparators) for sensing both battery voltage (BU circuit) and battery voltage remotely applied through a key type ignition switch (ACC circuit). There is also a Mute output with a programmable delay set by a capacitor at the CTMR pin.

Reference Voltage

The A8600 incorporates an internal reference that allows output voltages as low as 0.8 V. The accuracy of the internal reference is ±1.5% across the operating temperature range. The output voltage of each regulator is adjusted by connecting a resistor divider between the respective V_{SWx} nodes and FBx pins of the A8600, as shown in the Typical Application diagram.

PWM Switching Frequency

The PWM switching frequency of the A8600 is fixed at 425 kHz and has an accuracy of ±15% across the operating temperature range. The four buck switchers are interleaved at 180° intervals: SW1 and SW3 turn on at 0°, and SW2 and SW4 turn on at 180°.

During startup, the PWM switching frequency is reduced to 50% of the nominal frequency until FBx exceeds 300 mV. This is done to improve output regulation when V_{SWx} is starting to ramp upward and the PWM control loop is operating at the minimum controllable on-time and requires very low duty cycles.

If the voltage at the FBx pin is less than 300 mV, and the COMPx voltage reaches its maximum level, the PWM switching frequency is reduced to 25% of the nominal frequency. This is done because a very low FBx voltage combined with a maximum COMPx voltage indicates the regulator output is shorted to ground. The extra-low switching frequency allows additional off (decay) time between LXx pulses so the inductor current does not climb to a value that may damage the A8600 or the output inductor.

Enable/Synchronization Input (EN/SYNC)

The Enable/Synchronization input (EN/SYNC pin) provides two major functions. First, the EN/SYNC pin is a control input that sets the operating mode of the A8600. When EN/SYNC is a logic high, all 4 switchers operate in PWM mode and the high-side switches turn on or off via the ENS input. When EN/SYNC is a logic low, SW1 operates in low current keep-alive (Low IQ) mode, and SW2, SW3, SW4, S1, and S2 are turned off.

Second, when an external clock is applied to the EN/SYNC pin, the A8600 wakes-up, completes soft start at the nominal PWM frequency, and then synchronizes its PWM to the external clock. The external clock may be used to either increase or decrease the A8600 nominal PWM frequency. Synchronization operates when PWM is in the range from 325 to 550 kHz. When using synchronization, the external clock pulses must satisfy the pulse width, duty cycle, and rise/fall time requirements shown in the Electrical Characteristics table in this data sheet.

When EN/SYNC transitions to logic high, the A8600 turns on and then, provided there are no fault conditions, SW2, SW3, and SW4 initiate soft start and the output voltages will ramp to their final voltage in the time set by the soft start capacitors (CSSx). When EN/SYNC transitions to low, then the A8600 will wait 2048 PWM cycles before transitioning SW1 from PWM to PFM mode. However, after EN/SYNC transitions to low, the A8600 will wait only 15 PWM cycles before shutting off SW2, SW3, SW4, S1, and S2.

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BIAS Input Pin, Ratings, and Connections

When the A8600 is powering up, it operates an internal LDO regulator directly from VIN1. However, VIN1 is a relatively high voltage and an LDO regulator is very inefficient and generates heat. To improve efficiency, especially in PFM mode, a bias input is utilized. For most applications, the BIAS pin should be connected directly to the output of SW1. When V_{SW1} rises to an adequate level (approximately 2.93 V), the A8600 stops using the inefficient LDO and begins running its control circuitry directly from the output of SW1. This makes the A8600 more efficient and cooler.

The BIAS pin is designed to operate in the range from 3.2 to 5.5 V. If the output of SW1 is in this range, then the BIAS pin simply should be routed directly to the V_{SW1} node. However, if the output of SW1 is in the range from 5.6 to 6.5 V, then a very small LDO regulator, capable of at least 10 mA, must be used to reduce the output at V_{SW1} to either 3.3 V or 5.0 V before routing it to the BIAS pin.

Transconductance Error Amplifier

The transconductance error amplifier primary function is to control the output voltage of the switchers. The error amplifier circuit is shown in figure 9. Here, it is shown as a three-terminal input device with two positive and one negative input. The negative input is simply connected to the FBx pin and is used to sense the feedback voltage for regulation. The two positive inputs are used for soft start and steady-state regulation. The error amplifier performs an analog OR selection between its two positive inputs. The error amplifier regulates either to the soft start pin voltage (minus an offset of 400 mV) or to the A8600 internal reference, whichever is lower.

To stabilize the regulator, a series RC compensation network (RZx and CZx) must be connected from the error amplifier output (the COMPx pin) to GND as shown in the Typical Application diagram. In some instances, an additional, relatively low value capacitor (CPx) may be connected in parallel with the RZx/CZx components to roll-off the loop gain at higher frequencies. However, if the CPx capacitor is too large the phase margin of the converter may be reduced.

If the switcher is disabled or a fault occurs, the COMPx pin is immediately pulled to GND via approximately 1 kΩ and PWM switching is inhibited.

Slope Compensation

The A8600 incorporates internal slope compensation to allow PWM duty cycles above 50% for a wide range of input/output voltages and inductor values. As shown in the Functional Block Diagram the slope compensation signal is added to the sum of the current sense amplifier output and the PWM ramp offset. The slope compensation is based on the internal oscillator at 425 kHz and does not scale when the regulators are synchronized to an external clock.

Current Sense Amplifiers

The A8600 incorporates high-bandwidth current sense amplifiers to monitor the current in the upper MOSFETs of the three asynchronous regulators: SW1, SW2, and SW3. For the synchronous controller, SW4, a high-bandwidth differential amplifier is provided. The positive and negative inputs to this amplifier are CSP and CSN, respectively. As shown in the Typical Application diagram, the CSP and CSN pins must be routed to a discrete, current sense resistor, RS, in series with the SW4 output inductor.

Power MOSFETs

The A8600 includes high-side N-channel MOSFETs with low $R_{DS(on)}$, for SW1 (150 mΩ), SW2 (120 mΩ), and SW3 (112 mΩ) capable of continuously supplying 1.0 A, 1.5 A, and 2 A, respectively. The A8600 also includes a 10 Ω low-side MOSFET for each regulator to ensure the boot capacitor is always charged. The typical $R_{DS(on)}$ increase versus temperature is shown in figure 10.

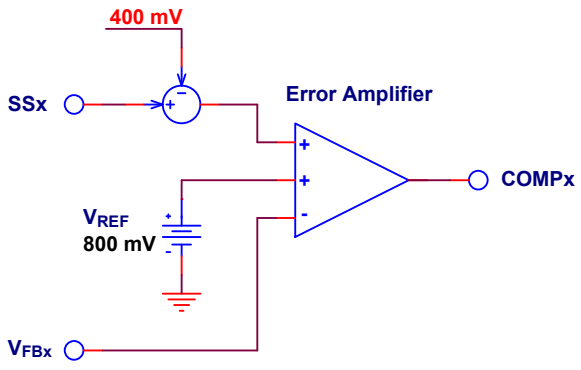

Figure 9. An A8600 error amplifier

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BOOT Regulators

Each of the four switchers has a regulator to charge its boot capacitor. The boot regulators detect undervoltage and overvoltage of the boot capacitor. Also, the boot regulators have a current limit circuit to protect the boot regulator during a short circuit condition. SW1, SW2, and SW3 derive their boot voltage from VIN1, VIN2, and VIN3, respectively. However, SW4 does not have a VIN pin because it drives external MOSFETs. Therefore, SW4 derives its boot voltage from the VIN3 pin. This sets a requirement that V_{IN3} should be approximately equal to the supply voltage at the drain of the external, high-side MOSFET (which could be considered to be V_{IN4}).

SW1/2/3/4 Pulse Width Modulation (PWM) Mode

The A8600s four buck switchers utilize fixed-frequency, peak current mode control to provide excellent load and line regulation, fast transient response, and ease of compensation.

A high-speed comparator and control logic, capable of pulse widths less than 180 ns, is included for each of the four buck switchers. The inverting input of the comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation, and a DC offset voltage ($V_{PWMOFFSETx}$, nominally 400 mV).

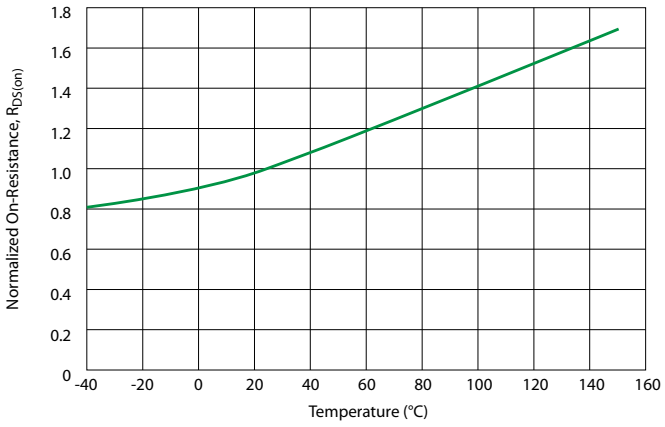

Figure 10. Typical MOSFET $R_{DS(on)}$ versus temperature

At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop and the upper MOSFET is turned on. When the summation of the DC offset, slope compensation, and current sense signal, rises above the error amplifier voltage the PWM flip-flop is reset and the upper MOSFET is turned off. The PWM flip-flop is reset dominant so the error amplifier may override the CLK signal in certain situations. For example, at very light loads or extremely high input voltage the error amplifier temporarily reduces its output voltage below the 400 mV DC offset and the PWM flip-flop ignores one or more of the incoming CLK pulses. The upper MOSFET does not turn on and the regulator skips pulses to maintain output voltage regulation.

In PWM mode all of the A8600 fault detection circuits are active. See the Timing Diagrams section for diagrams showing how faults are handled when in PWM mode. Also, the Protection Features section of this datasheet provides a detailed description of each fault and table 1 presents a summary.

SW1 Low IP PWM Mode

SW1 supports two different levels of PWM current limit: 100% current limit mode, which is normal PWM operation, and Low IP PWM mode, in which the current is limited to about 50% of the typical current limit. Low IP PWM mode is invoked when SW1 is commanded to be in Low IQ PFM mode (see next section) but is either soft starting (V_{FB1} < 700 mV) or a fault has occurred.

The purpose of Low IP PWM mode is to give priority to maintaining reliable regulation of V_{SW1} while enabling all the protection circuits inside the A8600 (high precision comparators, timers, and counters) that are normally off during Low IQ PFM mode. There are several faults that cause a transition from Low IQ PFM mode to Low IP PWM mode: a missing asynchronous diode, an open or shorted boot capacitor, V_{SW1} shorted to ground, or LX1 shorted to ground. See the Timing Diagrams section for operation of SW1 in normal PWM mode, and operation of SW1 when it transitions from Low IQ PFM mode to Low IP PWM mode.

SW1 Pulse Frequency Modulation (PFM) and Low IQ Mode

SW1 is an always-on buck regulator, with both PWM and PFM modes of operation (PWM mode is described in the previous section). SW1 operates in Low IQ PFM mode if both the EN/SYNC and ACCI pins are held low continuously for 2048 clock cycles.

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In PFM mode, SW1 operates with a switching frequency that depends on the load condition. The average current drawn from the input supply depends primarily on the load and how often the A8600 must wake up to maintain regulation.

In PFM mode, a comparator monitors the voltage at FB1. If the voltage at FB1 is above approximately 800 mV, the A8600 will remain in keep-alive mode and draw extremely low current from the input supply.

If the voltage at the FB1 pin drops below approximately 800 mV, the A8600 will wake up, and after a delay of approximately 2 µs for the IC to fully power-up, turn on the upper MOSFET. V_{SW1} rises at a rate dependent on the input voltage, inductor value, and output capacitance.

The upper MOSFET is turned off when either: (1) the upper MOSFET (that is, the output inductor) current reaches approximately 800 mA, or (2) the upper MOSFET has been on for approximately 4 µs. After the upper MOSFET is turned off, the A8600 will delay approximately 300 ns and either: (1) turn the MOSFET on again if the voltage at FB1 is still below 800 mV or (2) return to the extremely low current keep-alive mode. Figures 11 and 12 demonstrate PFM mode operation for a light load and an increased load, respectively.

In PFM mode the following faults are detected: a missing asynchronous diode, an open or shorted boot capacitor, V_{SW1} shorted to ground, or LX1 shorted to ground. As described in the previous section for PWM mode, if any of these faults occur the A8600 will transition from Low IQ PFM mode to Low IP PWM mode, and operate at 50% of the normal PWM current limit. See the Timing Diagrams section for operation of SW1 in Low IQ PFM mode.

In PFM mode the A8600 dissipates very little power, so the thermal monitoring circuit (TSD) is not required and is disabled to minimize the quiescent current.

Soft Start (Startup) and Inrush Current Control

Inrush currents to the 4 switchers are controlled by the soft start function. When the A8600 is enabled and all faults are cleared, the Soft Start pin, SSx, will source I_{SSSUx} and the voltage on the Soft Start capacitor, CSSx, will ramp upward from 0 V. When the voltage at the Soft Start pin exceeds approximately 400 mV, the error amplifier slews its output voltage above the PWM Ramp Offset ($V_{PWMOFFSETx}$). At that instant, the upper and lower MOSFETs will begin switching. As shown in figure 13, there is a delay (t_{dSSx}) between when the Enable pin transitions high and the combination of the soft start voltage exceeding 400 mV and the error amplifier slewing its output enough to initiate PWM switching.

Once the A8600 begins switching, the error amplifier will regulate the voltage at the FBx pin to the SSx pin voltage, minus approximately 400 mV. During the active portion of soft start, the

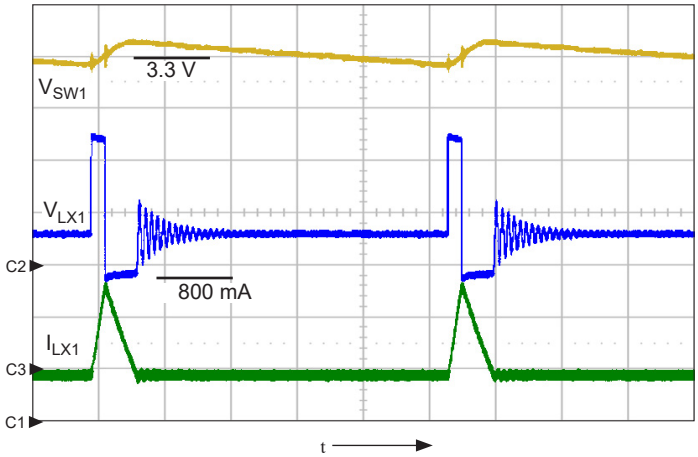

Figure 11. SW1 PFM operation at V_{IN1} = 12 V, V_{SW1} = 3.3 V, V_{SW1} = 50 mA load, LX1 turns on once every 26 µs to regulate V_{SW1}; shows V_{SW1} (ch1, 100 mV/div.), V_{LX1} (ch2, 5 V/div.), I_{LX1} (ch3, 500 mA/div.), t = 5 µs/div.

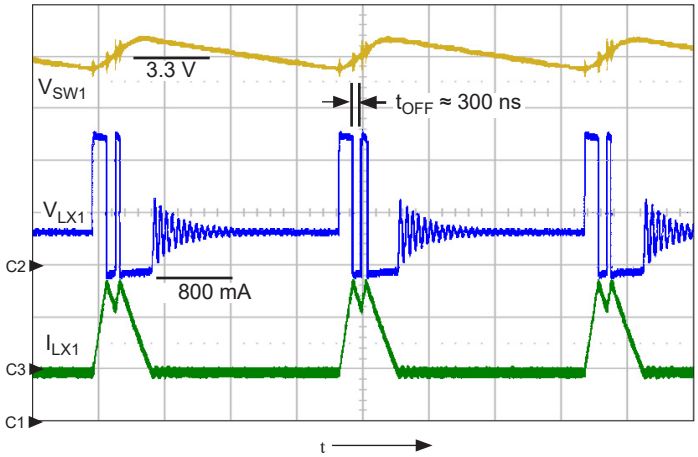

Figure 12. SW1 PFM operation at V_{IN1} = 12 V, V_{SW1} = 3.3 V, V_{SW1} = 120 mA load, LX1 turns on twice every 18 µs to regulate V_{SW1}; shows V_{SW1} (ch1, 100 mV/div.), V_{LX1} (ch2, 5 V/div.), I_{LX1} (ch3, 500 mA/div.), t = 5 µs/div.

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voltage at the SSx pin rises from 400 mV to 1.2 V (a difference of 800 mV), the voltage at the FBx pin rises from 0 V to 800 mV, and the switcher output voltage (V_{SWx}) will rise from 0 V to the setpoint determined by the feedback (FBx pin) resistor divider.

When the voltage at the Soft Start pin reaches approximately 1.2 V, the error amplifier will change mode and begin regulating the voltage at the FBx pin to the A8600 internal reference, 800 mV. The voltage at the Soft Start pin will continue to rise to about 3.3 V. Complete soft start operation from 0 V_{SWx} is shown in figure 13.

If the A8600 is disabled or a fault occurs, the internal fault latch is set and the Soft Start pin is discharged via approximately 5 kΩ. The A8600 will clear the internal fault latch when the voltage at the SSx pin decays to approximately 200 mV (V_{SSRSTx}).

If the A8600 enters hiccup mode, the capacitor on the Soft Start pin is discharged by a current sink, I_{SSHICx}. Therefore, the Soft Start capacitor (CSSx) not only controls the startup time but also the time between soft start attempts. Hiccup mode operation is discussed in more detail in the Hiccup Mode Protection section of this datasheet.

For initial startup, when the voltage at the FBx pin is between 0 and 300 mV, the PWM switching frequency, f_{SW}, is reduced to $f_{SW}/2$. This is done to achieve the extremely low duty cycles required for precise regulation when V_{INx} is relatively high and V_{SWx} is near 0 V. After V_{FBx} rises above 300 mV, the PWM switching frequency is increased to f_{SW}. If the output of the switcher is shorted to ground, the voltage at the FBx pin will remain less than 300 mV and the voltage at the COMPx pin will reach its maximum value. If these two conditions occur, the PWM switching frequency is reduced to $f_{SW}/4$ to allow additional off (decay) time between LXx pulses. This prevents the inductor current from rising to an unusually high value that may damage the A8600 or the output inductor.

Prebiased Startup

If the output of any of the regulators is pre-biased to some voltage, the A8600 will modify the normal startup routine to prevent discharging the output capacitors. As described previously, the error amplifier usually becomes active when the voltage at the Soft Start pin exceeds 400 mV. If the output is pre-biased the FBx pin will be at some non-zero voltage. The A8600 will not start switching until the voltage at the Soft Start pin increases to approximately V_{FBx} + 400 mV. When the soft start voltage exceeds this value, the error amplifier becomes active, the voltage at the COMPx pin rises, PWM switching starts, and V_{SWx} will ramp upward starting from the prebias level. Figure 14 shows startup when the output voltage is pre-biased to 2.0 V.

High-Side Switches (S1 and S2)

The A8600 contains two 1 Ω high-side switches, S1 and S2, capable of delivering at least 250 mA each. The VINS pin provides input voltage and current to both S1 and S2. The outputs of S1 and S2 are at OUT1 and OUT2, respectively. Both high-side switches are constructed from two back-to-back, series MOSFETs so current will not flow in the reverse direction (back

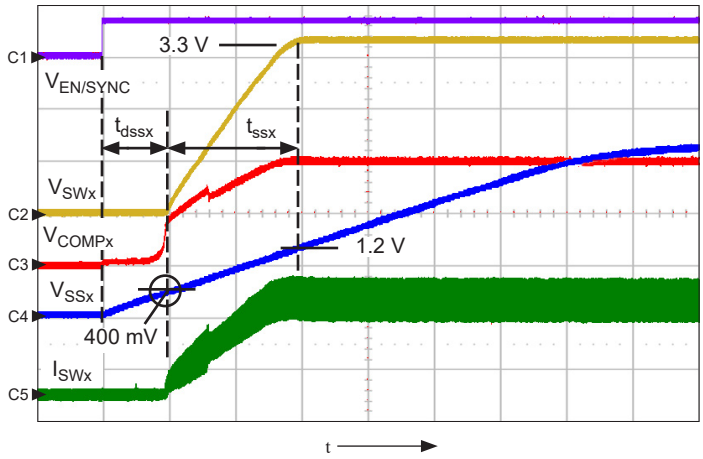

Figure 13. Normal startup to V_{SWx} = 3.3 V at I_{SWx} = 1.6 A load; shows $V_{EN/SYNC}$ (ch1, 10 V/div.), V_{SWx} (ch2, 1 V/div.), V_{COMP} (ch3, 500 mV/div.), V_{SSx} (ch4, 1 V/div.), V_{SWx} (ch5, 1 A/div.), t = 500 µs/div.

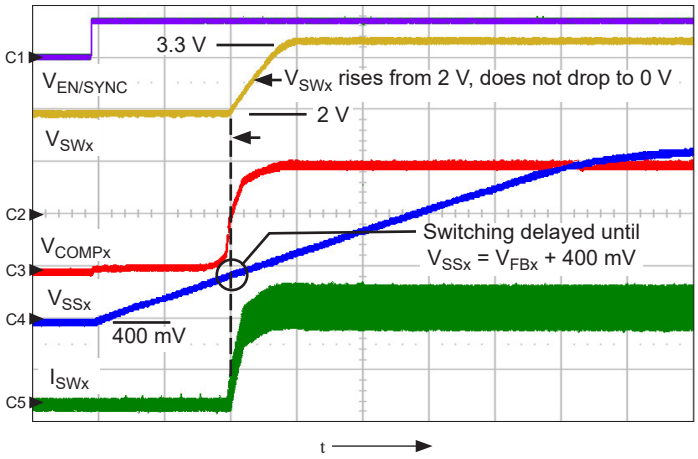

Figure 14. Pre-biased startup from V_{SWx} = 2 V rising to 3.3 V at I_{SWx} = 1.6 A load; shows $V_{EN/SYNC}$ (ch1, 10 V/div.), V_{SWx} (ch2, 1 V/div.), V_{COMP} (ch3, 500 mV/div.), V_{SSx} (ch4, 1 V/div.), V_{SWx} (ch5, 1 A/div.), t = 500 µs/div.

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to VINS) through the switches. S1 and S2 are simultaneously controlled on or off by the ENS pin. The A8600 contains an internal charge pump to provide gate drive to S1 and S2.

If OUT1 or OUT2 is pulled down relatively slowly by a heavy load, the switch will protect itself by limiting its current to about 350 mA_{DC}. If the output of S1 or S2 drops below 8 V, the switch will begin to foldback the current. At 0 V output, each switch typically delivers only 100 mA. However, if OUT1 or OUT2 is very quickly shorted to ground, the switch will allow a relatively high peak current, approximately 800 mA(peak) at V_{INS} = 18 V, for a short time. This scheme allows for minimal power dissipation while allowing OUT1/OUT2 startup with capacitive loads up to 1 µF. For thermal reasons, if VINS exceeds approximately 18.3 V, both S1 and S2 are turned off.

Figure 15 shows the typical DC fold back characteristics of the high-side switches. Figure 16 shows a high-side switch turning on with V_{INS} = 12 V and a 40 Ω/22 µF load. In figure 16, notice the switch is starting with foldback limiting, allowing only 100 mA when V_{OUTx} = 0 V, increasing the current to about 400 mA when V_{OUTx} exceeds 5 V, and providing full output voltage with a 300 mA load. Without foldback control, the switch would have allowed an extremely high peak current due to the capacitive load (> 20 A) and the A8600 may have been damaged or caused some other system level malfunction, such as UVLO of the entire IC.

In some applications, S1 and S2 are connected to a wiring harness to supply a remote load at a relatively long distance from the A8600. The wiring harness will introduce significant series inductance (4 to 6 µH) between the OUTx pin and the actual load. This forms an LC tank circuit with very low resistance. If the load is short circuited to ground, the OUTx pin will transition or ring below ground for a short time. To protect the A8600, Allegro strongly recommends the use of a 1 A, 30 V (min) diode, as shown in the Typical Application diagram, to help clamp the negative voltage at the OUT1/OUT2 pins. Preferably, this clamp diode would be a Schottky type.

For most applications, the VINS pin will share a common input node with the buck switcher VIN1/2/3/4 pins, as shown in figure 17. In this configuration, the VINs pin is protected from negative transients (such as during a Field Decay test) by two series diodes, the MOSFET body diodes and the external, asynchronous Schottky diodes, DSW1 through DSW4. Depending on the application, it may be necessary to isolate the VINS pin from the switching noise on the VIN1/2/3/4 pins.

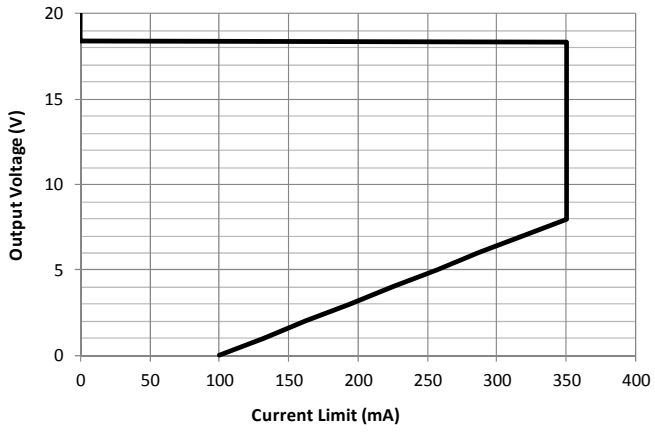

Figure 15. Typical DC current fold back versus V_{OUTx} of S1 and S2

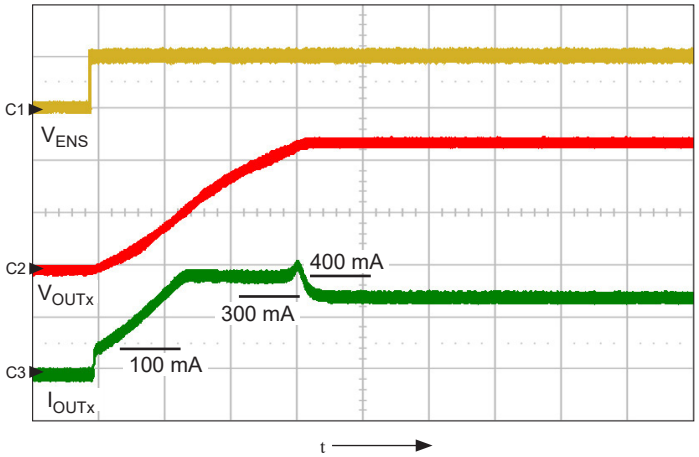

Figure 16. S1/S2 OUTx turning on with a load of 40 Ω and 22 µF; shows V_{ENS} (ch1, 5 V/div.), V_{OUTx} (ch2, 5 V/div.), I_{OUTx} (ch3, 200 mA/div.), t = 500 µs/div.

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One method to accomplish this is to add an additional LC filter, as shown in figure 18. In this configuration, the body diode and external Schottky diode from the buck switchers no longer protect the VINS pin from negative voltage transients. If the VINS pin is isolated in any way, Allegro recommends adding a Schottky diode, DVINS, at the VINS pin as shown in figure 18.

There are two levels of thermal protection in the A8600. A detailed description of these two levels, how they affect the operation of S1 and S2, and how they must be reset is provided in the Protections Features section of this data sheet.

See the Timing Diagrams section for operation of the high-side switches during current limit and high temperature.

BU and ACC Detectors and MUTE Output

The A8600 includes two relatively simple comparators to monitor both V_{BAT}/V_{IN} and V_{BAT}/V_{IN} applied through a key-type ignition switch. The BU comparator monitors V_{BAT}/V_{IN} at the BUI pin. The ACC comparator monitors the ignition switch at the ACCI pin. Both comparators have an internal reference of 1.205 V at their negative pins. Therefore, a resistor divider must be used to set the BU and ACC thresholds to something higher than 1.205 V, as shown in the Typical Application diagram. Also, if hysteresis is necessary, this must be done with an external resistor from BUO to BUI and ACCO to ACCI, as shown in the Typical Application diagram.

It should be noted that the ACC comparator also controls the mode of SW1. If the EN/SYNC and ACCI inputs are low, SW1 will enter Low IQ PFM mode after 2048 PWM cycles. If ACCI is high, it will immediately force SW1 into normal, high-current PWM mode.

See the Timing Diagrams section for operation of the BU and ACC detectors.

The A8600 has an open drain, active low MUTE output with a programmable on-time. The MUTE output is an open drain output, therefore an external pull-up resistor must be used as shown in the Typical Application Circuit diagram. The MUTE on-time is set by a counter and a capacitor from the CTMR pin to ground. Basically, any time the BU comparator changes state the MUTE output is pulled low while the CTMR pin transitions 10 times between V_{CTMRH} and V_{CTMRL}. If the BU comparator changes state before the counter reaches 10, the counter will be reset to 0 and the MUTE time extended. The BU comparator has a de-glitch filter, so any fast transient on BUI lasting less than 16 µs (typ) will be ignored and a false MUTE will not occur. T_{TSDL} and T_{TSDH} do not affect the MUTE output.

See Timing Diagrams section for operation of the MUTE and CTMR pins in conjunction with the BU detector.

Power OK (POK) Output

The A8600 has a Power OK (POK) output. The POK output is an open drain output, so an external pull-up resistor must be used as shown in the Typical Application Circuit diagram. The POK output is pulled low if either an under- or overvoltage condition occurs at FB2, FB3, or FB4. SW1 is an always-on regulator, so it does not help control POK. The typical POK thresholds are set at ±60 mV (±7.5% of 800 mV).

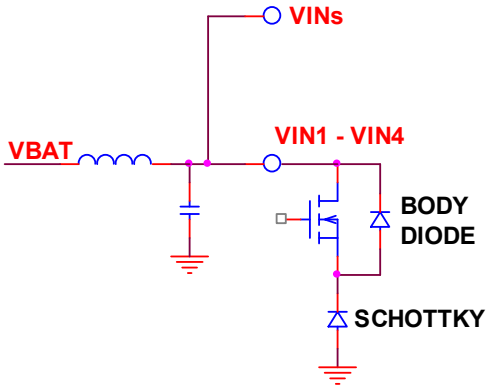

Figure 17. VINS pin connected directly to VIN1/2/3/4 pins

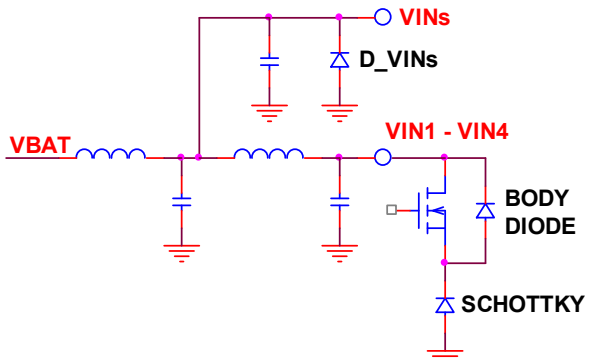

Figure 18. VINS isolated from VIN1/2/3/4, so the addition of D_{VINS} is required

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The POK comparators incorporate a small amount of hysteresis, 10 mV (typ), to help reduce chattering due to voltage ripple at any of the FBx pins.

Protection Features

The A8600 is designed to satisfy the most demanding automotive and non-automotive applications. In this section, a description of each protection feature is provided, and table 1 summarizes the protection features and their operation.

Undervoltage Lockout (UVLO)

For each of the three buck regulators, SW1/2/3, an Undervoltage Lock Out (UVLO) comparator monitors the voltage at the corresponding VINx pin and keeps the regulator disabled if the voltage is below the lockout threshold ($V_{UVLOONx}$). Each UVLO comparator incorporates some hysteresis ($V_{UVLOHYSx}$) to prevent on/off cycling of the regulator due to resistive or inductive drops in the V_{INx} path during heavy loading or during startup.

Thermal Shutdown (TSDL and TSDH)

The A8600 has two levels of thermal protection: low (TSDL) and high (TSDH). TSDL typically occurs at approximately 155°C and TSDH typically occurs at approximately 165°C.

If the junction temperature of the A8600 exceeds T_{TSDL}, but remains below T_{TSDH}, S1 and S2 are latched off, in order to reduce power and give priority to maintaining regulation of the buck outputs even though the regulator is getting hot. In this case, the TSDL latch may be reset by setting ENS to logic low after the A8600 cools. However, if the junction temperature of the A8600 exceeds T_{TSDH}, S1/2, and SW2/3/4 will all be latched off and SW1 will begin operating in Low IQ mode. For the extremely high temperature case, the TSDH latch may only be reset by setting EN/SYNC to a logic low for at least 15 PWM counts or by cycling VIN1.

Pulse-by-Pulse Overcurrent Protection (OCP)

The A8600 monitors the current in the upper MOSFET and if the current exceeds the pulse-by-pulse over current threshold (I_{LIMx}) then the upper MOSFET is turned off. Normal PWM operation resumes on the next clock pulse from the internal oscillator. The A8600 includes leading edge blanking to prevent falsely triggering the pulse-by-pulse current limit when the upper MOSFET is turned on. Pulse-by-pulse current limiting is always active.

Because of the addition of the slope compensation ramp to the inductor current, the A8600 delivers slightly less current at higher duty cycles than at lower duty cycles. If the synchronization input is used to reduce the switching frequency, the A8600 will, in effect, reduce the current limit with frequency too. Figure 19 shows the minimum, typical and maximum pulse-by-pulse current limit at the typical PWM frequency, 425 kHz. Also, figure 19 shows the minimum expected pulse-by-pulse current limit if the synchronization input is used to reduce the switching frequency to 325 kHz. The exact current each of the buck regulators can support is heavily dependent on duty cycle, ambient temperature, thermal resistance of the PCB, airflow, component selection, and nearby heat sources.

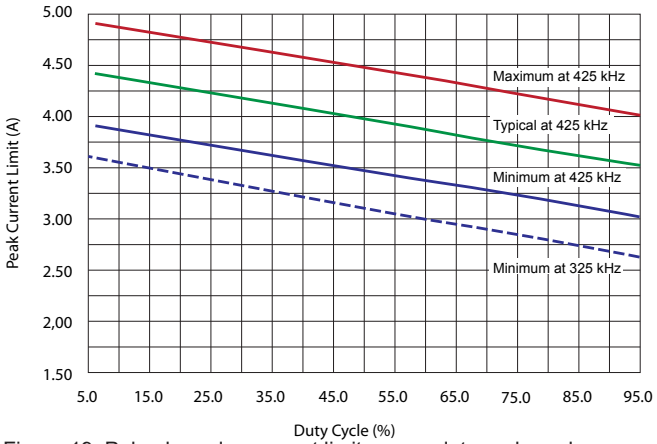

Figure 19. Pulse-by-pulse current limit versus duty cycle and PWM (SYNC) frequency

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Output Short Circuit (Hiccup Mode) Protection

Hiccup mode protects the buck switchers when their load is either too high or when the output of the switcher is shorted to ground. Hiccup mode operation is shown in figure 20.

When the voltage at the SSx pin is below the Hiccup OCP Enable Threshold (V_{HICENx}, 2.3 V (typ)) hiccup mode protection is disabled. After the voltage at the SSx pin exceeds the Hiccup OCP Enable Threshold, an OCP counter is enabled. The quantity of OCP pulses allowed then depends on the FBx voltage. If V_{FBx} is below 300 mV, only 30 OCP counts are allowed. If the FBx voltage is above 300 mV, the quantity of OCP pulses allowed increases to 118. This dual count technique provides maximum thermal protection for the A8600 and allowing robust attempts for starting with highly capacitive or heavy loads.

If the OCP counter reaches its limit, a latch is set and the COMPx pin is pulled low by a relatively low resistance (1 kΩ). The same latch enables a small current sink connected to the SSx pin (I_{SSHICx}). The result is the voltage at the Soft Start pin will begin to ramp downward. When the voltage at the Soft Start pin decays to a much lower level, V_{SSRSTx} (200 mV (typ)) the hiccup latch will be cleared and the small current sink turned off. At this instant, the SSx pin will begin to source current (I_{SSSUx}) and the voltage at the SSx pin will ramp upward. This marks the beginning of a new, normal soft start cycle as described earlier.

When the voltage at the Soft Start pin exceeds the PWM Ramp Offset ($V_{PWMOFFSET}$, 400 mV (typ)) the error amplifier will force the voltage at the COMPx pin to slew up quickly and PWM switching will resume. If the short circuit at the switcher output remains, another hiccup cycle will occur. Hiccups will repeat until the short circuit is removed or the switcher is disabled. If the short circuit is removed, the A8600 will soft start normally and the output voltage will automatically recover to the required level, as shown in figure 20.

BOOT Capacitor Protection

For each buck switcher, the A8600 monitors the voltage across the BOOT capacitor to detect if the capacitor is missing or short circuited. If the BOOT capacitor is missing, the regulator will enter hiccup mode after 7 PWM cycles. If the BOOT capacitor is short circuited, the regulator will enter hiccup mode after 30 PWM cycles. For a BOOT fault, hiccup mode operates similarly to the hiccup mode described for an output short circuit, with SSx ramping up and down as a timer to initiate repeated soft start attempts. A BOOT fault is a non-latched condition, so the A8600 will automatically recover when the fault is corrected.

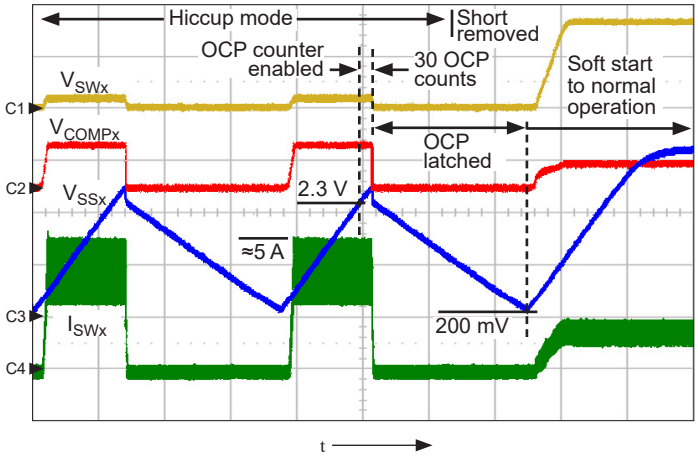

Figure 20. Hiccup mode and recovery to V_{SWx} = 3.3 V at I_{SWx} = 1.6 A; shows V_{SWx} (ch1, 2 V/div), V_{COMPx} (ch2, 2 V/div), V_{SSx} (ch3, 1 V/div), I_{SSSUx} (ch4, 2 A/div); t = 2 ms/div

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Asynchronous Diode Protection

In most high voltage asynchronous buck regulators, if the asynchronous diode is missing or damaged, the LX pin will transition to a very high negative voltage when the upper MOSFET turns off, resulting in damage to the regulator. The A8600 includes protection circuitry to detect when the asynchronous diode is missing or damaged. If the LXx pin becomes more negative than 1.25 V (typ) for more than 50 ns (typ), the A8600 will protect itself to prevent damage. SW1 will enter hiccup mode after 1 missing diode fault. SW2/3/4 will latch off after 1 missing diode fault. After a latched missing diode fault, the latch must be reset by either setting EN/SYNC to a logic low or cycling V_{INx}.

Overvoltage Protection (OVP)

The A8600 provides a basic level of overvoltage protection by monitoring the voltage level at the FBx pin of all four buck switchers. Two overvoltage conditions can be detected. First, if the FBx pin is disconnected from its feedback resistor divider, a tiny internal current source will force the voltage at the FBx pin to rise. When the voltage at the FBx pin exceeds the overvoltage threshold (V_{POKOVx}, 860 mV (typ)), PWM switching will stop. For SW1, the POK pin level is unaffected by overvoltage, but for SW2/3/4 the POK pin will be pulled low.

Second, if a higher external voltage supply is accidently shorted to a switcher output, V_{FBx} will rise above the overvoltage threshold and be detected as an overvoltage condition. PWM switching will stop and the POK pin pulled low (for SW2/3/4). If the condition causing the overvoltage is removed the regulators will automatically recover.

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Table 1: Summary of Fault Mode Operation

Fault Condition	Latched	V_{SSx}	V_{COMPx}	V_{POK}	PWM Switching	S1, S2	Reset
SW1/2/3/4 output shorted to GND	No	Hiccup after 30 or 118 faults	Discharged, then respond to V_{SSx} rise	Depends on V_{SWx}	Active, responds to VCOMPx	Not affected	Auto, remove short
S1/2 output shorted to GND	No	Not affected	Not affected	Not affected	Not affected	Foldback limiting	Auto, remove short
SW1/2/3/4 boot capacitor missing	No	Hiccup, after 7 faults	Discharged, then respond to V_{SSx} rise	Depends on V_{SWx}	Off during hiccup	Not affected	Auto, replace capacitor
SW1/2/3/4 boot capacitor shorted	No	Hiccup, after 30 faults	Discharged, then respond to V_{SSx} rise	Depends on V_{SWx}	Off via UVLO BOOT	Not affected	Auto, unshort capacitor
SW1 asynchronous diode missing	No	Hiccup, after 1 fault	Discharged, then respond to V_{SSx} rise	N/A	Active, responds to VCOMPx	Not affected	Auto, install diode
SW1/2/3/4 asynchronous diode missing	Yes	Discharged after 1 fault	Discharged	Depends on V_{SWx}	Forced off	Not affected	EN/SYNC low [1] or VREG POR via VIN1 UVLO
SW1 asynchronous diode (or LX1) hard short	No	Hiccup after 1 fault	Discharged, then respond to V_{SSx} rise	N/A	Active, responds to VCOMPx	Not affected	Auto, remove short
SW1 asynchronous diode (or LX1) soft short	No	Hiccup after 30 faults	Discharged, then respond to V_{SSx} rise	N/A	Active, responds to VCOMPx	Not affected	Auto, remove short
SW1/2/3/4 asynchronous diode (or LXx) hard short	Yes	Pulled low after 1 fault	Discharged	Depends on V_{SWx}	Forced off	Not affected	EN/SYNC low [1] or VREG POR via VIN1 UVLO
SW1/2/3/4 asynchronous diode (or LXx) soft short	No	Hiccup after 30 faults	Discharged, then respond to V_{SSx} rise	Depends on V_{SWx}	Active, responds to VCOMPx	Not affected	Auto, remove short
SW1/2/3/4 FBx pin open (V_{FBx} floats high)	No	Ramps high for soft start	Low via loop response	SW2/3/4 low via V_{FBx} high (OV)	Off via V_{COMPx} low	Not affected	Auto, connect FBx pin
SW1/2/3/4 overvoltage (V_{FBx} > 107.5%)	No	Ramps high for soft start	Low via loop response	Pulled Low	Forced off	Not affected	Auto, V_{FBx} to normal range
LG4 more than 8.1 V for >400 ns	Yes	Pulled low after 1 fault	Discharged	Depends on V_{SW4}	Latched off	Not affected	EN/SYNC low [1] or VREG POR via VIN1 UVLO
LG4 in high state but < 1 V for >400 ns	Yes	Pulled low after 1 fault	Discharged	Depends on V_{SW4}	Latched off	Not affected	EN/SYNC low [1] or VREG POR via VIN1 UVLO
LG4 in low state but > 1 V for >400 ns	Yes	Pulled low after 1 fault	Discharged	Depends on V_{SW4}	Latched off	Not affected	EN/SYNC low [1] or VREG POR via VIN1 UVLO
Thermal (TSDL)	Yes	Not affected	Not affected	Depends on V_{SWx}	Not affected	Off	EN/SYNC low [1] or ENS low or VREG POR via VIN1 UVLO
SW1 Thermal (TSDH)	Yes	After 2048 PWM cycles, latches in Low IQ mode				Off	EN/SYNC low [1] or VREG POR via VIN1 UVLO
SW2/3/4 Thermal (TSDH)	Yes	Pulled low	Pulled low	Depends on V_{SWx}	Latched off	Off	EN/SYNC low [1] or VREG POR via VIN1 UVLO

[1] EN/SYNC low requires a logic low for 15 clock cycles.

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APPLICATION INFORMATION

Design and Component Selection

Setting the Output Voltage (V_{SWx}, R_{FBAx}, R_{FBBx})

The output voltage of any switcher, SW1 through SW4, is determined by connecting a resistor divider from the switcher output node (V_{SWx}) to the switcher FBx pin as shown in figure 21. There are trade-offs when choosing the value of the feedback resistors. If the series combination (R_{FBAx}+ R_{FBBx}) is relatively low, then the light load efficiency of the regulator will be reduced. So to maximize the efficiency, it is best to choose resistors with higher values. Conversely, if the value of the parallel combination (R_{FBAx}//R_{FBBx}) is too high, then the switcher may be susceptible to noise coupling into the FBx pin.

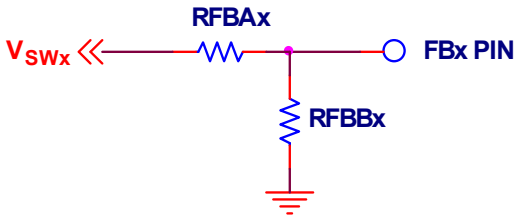

Figure 21. Connecting the feedback divider

Table 2. Recommended Feedback Resistors for Switchers SW2 through SW4

$V_{SW2/3/4}$ (V)	$R_{FBA2/3/4}$ (kΩ)	$R_{FBB2/3/4}$ (kΩ)
1.2	6.04	12.1
1.5	7.50	8.45
1.8	9.09	7.15
2.5	12.4	5.76
3.3	16.5	5.23
5.0	24.9	4.75
7.0	34.8	4.53
8.0	40.2	4.42
9.6	47.5	4.32

In general, the feedback resistors must satisfy the ratio shown in equation 1 to produce a required output voltage:

$$\frac{R_{FBAx}}{R_{FBBx}} = \left(\frac{V_{SWx}}{0.8\ (V)} - 1 \right) \quad (1)$$

Table 2 shows the most common output voltages and recommended feedback resistors assuming less than 0.2% efficiency loss at light load of 100 mA and a parallel combination of 4 kΩ presented to the FBx pin. For optimal system accuracy, it is recommended that the feedback resistors have tolerances of ≤1% .

SW1 presents some unique challenges when determining its feedback resistor divider. This resistor divider must draw minimum current from V_{SW1} or it will raise the input current during Low IQ operation. With this in mind, Allegro recommends the standard ±1% resistor values shown in table 3.

For Low IQ mode operation, a small feed-forward capacitor (CFB1) should be connected in parallel with RFBA1, as shown in figure 22. The purpose of this capacitor is to offset any stray capacitance (C_{STRAY}) from FB1 to ground. Without CFB1, the stray capacitance and the relatively high resistor values used for the SW1 feedback network form a low pass filter and introduce lag to the Low IQ PFM feedback path. The feed-forward capaci-

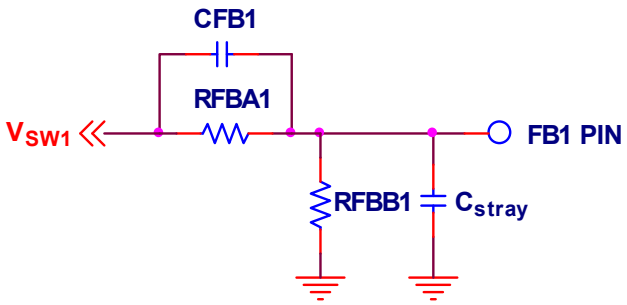

Figure 22. Addition of CFB1 to cancel stray capacitance

Table 3. Recommended Feedback Components for Switcher SW1

V_{SW1} (V)	R_{FBA1} (kΩ)	R_{FBB1} (kΩ)	C_{FB1} (pF)
3.3	163	52.3	7.2 to 12
5.0	249	47.5	4.7 to 8
6.5	365	51.1	3.3 to 6

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tor helps to maintain sensitivity during PFM mode and assure the output voltage ripple is minimized.

In general, CFB1 should be calculated as:

$$C_{FB1} > (1.5\ \ C_{STRAY}) \times (R_{FBB1} / R_{FBA1}) \quad (2)$$

where C_{STRAY} is typically 15 to 25 pF.

Output Inductor (LSWx)

For a peak current mode buck regulator, it is common knowledge that, without adequate slope compensation, the system will become unstable when the duty cycle exceeds approximately 50%. However, the slope compensation in the A8600 is a fixed value ($S_{E(x)}$). Therefore, it is important to calculate an inductor value such that the downward slope of the current (S_{Fx}) approximately matches the A8600 slope compensation. Equations 3 and 4 can be used to calculate a range of values for the output inductor based on the well-known approach of providing slope compensation that matches 50% to 100% of downward slope of the inductor current. In these equations, we assume the minimum value of slope compensation ($S_{E(X)}$ = 300 mA/µs). V_{fx} is the forward voltage of the asynchronous diode:

$$L_{SWx} \geq \frac{V_{SWx}+V_{fx}}{0.6\times10^{-6}} \quad (3)$$

$$L_{SWx} \leq \frac{V_{SWx}+V_{fx}}{0.3\times10^{-6}} \quad (4)$$

More recently, Dr. Raymond Ridley presented a formula to calculate the amount of slope compensation required to critically damp the double poles at half the PWM switching frequency. This formula includes the duty cycle (D), which should be calculated at the minimum input voltage to insure maximum stability:

$$L_{SWx} \geq \frac{V_{SWx}+V_{fx}}{0.45\times10^{-6}}\left(1-0.18\times\frac{(V_{INx}(\min)+V_{fx})}{V_{SWx}+V_{fx}}\right) \quad (5)$$

Also, note that V_{INx}(min) must be approximately 1 to 1.5 V above V_{SWx} when calculating the inductor value with equation 5. Recall that SW4 is a synchronous regulator so V_{fx} = 0 V should be used in equations 3 to 5.

If equations 3 to 5 yield an inductor value that is not a standard value, then the next highest available value should be used. The final inductor value should allow for 5% to 10% of initial tolerance and 10% to 20% of inductor saturation.

The saturation current of the inductor should be higher than the peak current capability of the A8600. Ideally, for output short circuit conditions, the inductor should not saturate given the highest pulse-by-pulse current limit at minimum duty cycle (I_{LIMx}), 4.9 A(max). This may be too costly. At the very least, the inductor should not saturate given the peak operating current according to equation 6. In equation 6, V_{INx}(max) is the maximum continuous input voltage, such as 18 V (not a surge voltage).

$$I_{LIMx} = 4.4 - \frac{0.45\times10^{-6}\times(V_{SWx}+V_{fx})}{f_{SWx}(\max)\times(V_{INx}(\max)+V_{fx})} \quad (6)$$

Starting with equation 6 and subtracting half of the inductor ripple current provides us with an interesting equation to predict the typical DC load capability for any of the buck regulators:

$$I_{SWx(DC)} = 4.4 - \frac{0.45\times10^{-6}\times D}{f_{SWx}} - \frac{V_{SWx}\times\ 1-D}{2\times f_{SWx}\times L_{SWx}} \quad (7)$$

After an inductor is chosen, it should be tested during output short circuit conditions. The inductor current should be monitored using a current probe. A good design would ensure the inductor or the switcher are not damaged when the output is shorted to GND at maximum input voltage and at the highest expected ambient temperature.

Output Capacitors (CSWx)

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

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The output voltage ripple (ΔV_{SWx}) is a function of the output capacitor parameters: ESR_{SWx}, ESL_{SWx}, and C_{SWx}:

$$\Delta V_{SWx} = \Delta I_{LSWx} \times ESR_{SWx} + \frac{V_{INx} - V_{SWx}}{L_{SWx}} \times ESL_{SWx} + \frac{\Delta I_{LSWx}}{8 f_{SWx} C_{SWx}} \quad (8)$$

The type of output capacitors will determine which terms of equation 8 are dominant.

For ceramic output capacitors the ESR and ESL are virtually zero so the output voltage ripple will be dominated by the third term of equation 8:

$$\Delta V_{SWx} = \frac{\Delta I_{LSWx}}{8 f_{SWx} C_{SWx}} \quad (9)$$

To reduce the voltage ripple of a design using ceramic output capacitors simply increase the total capacitance, reduce the inductor current ripple (that is, increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors the value of capacitance will be relatively high so the third term in equation 8 will be minimized and the output voltage ripple will be determined primarily by the first two terms of equation 8:

$$\Delta V_{SWx} = \Delta I_{LSWx} \times ESR_{SWx} + \frac{V_{INx}}{L_{SWx}} \times ESL_{SWx} \quad (10)$$

To reduce the voltage ripple of a design using electrolytic output capacitors, simply decrease the equivalent ESR and ESL by using a high-quality capacitor, and/or add more capacitors in parallel, or reduce the inductor current ripple (that is, increase the inductor value). The ESR of some electrolytic capacitors can be quite high so Allegro recommends choosing a high-quality capacitor with a datasheet that that clearly documents the ESR or the total impedance. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambient, which increases the output voltage ripple and, in many cases, reduces the stability of the system.

The transient response of the A8600 depends on the number and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response.

The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage will change by the amount:

$$\Delta V_{SWx} = \Delta I_{LOADSWx} \times ESR_{SWx} + \frac{di}{dt} ESL_{SWx} \quad (11)$$

After the load transient occurs, the output voltage will deviate for a short time. The time will depend on the system bandwidth, the output inductor value, and output capacitance. After a short delay, the error amplifier will bring the output voltage back to its nominal value.

The speed at which the error amplifier brings the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, with a higher bandwidth system it may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (RZ, CZ, CP) are discussed in more detail in the Compensation Components section of this datasheet.

SW1 Low IQ PFM Ripple Calculation

After choosing an output inductor and output capacitor(s) for SW1, it is important to calculate the output voltage ripple during Low IQ PFM mode. With ceramic output capacitors the output voltage ripple in PWM mode is usually negligible, but that is not the case during Low IQ PFM mode.

First, we need to calculate the MOSFET on and off times. The on-time is defined as the time it takes for the inductor current to reach 800 mA (typ):

$$t_{ON} = \frac{800\ (mA) \times L_{SW1}}{V_{IN1} - V_{SW1} - 800\ (mA) \times (R_{DS(on)HS1} + R_{DCLSW1})} \quad (12)$$

where $R_{DS(on)HS1}$ is the on-resistance of the SW1 high-side MOSFET (150 mΩ (typ)) and R_{DCLSW1} is the DC resistance of the output inductor, L_{SW1}. The on-time during PFM mode is internally limited to approximately 4 µs.

The off-time is defined as the time it takes for the inductor current to decay from 800 mA (typ) to 0 A:

$$t_{OFF} = \frac{800\ (mA) \times L_{SW1}}{V_{SW1} + V_{f1}} \quad (13)$$

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Lastly, the PFM output voltage ripple can be calculated:

$$\Delta V_{SW1(PFM)} = \frac{800\ (mA) \times (t_{ON} + t_{OFF})}{2 \times C_{SW1}} \quad (14)$$

If the PFM output voltage ripple appears to be too high, then the output capacitance of SW1 should be increased. The PFM output voltage ripple will increase as the input voltage decreases.

Notice that t_{ON} will increase as the output to input voltage ratio (V_{SW1} / V_{IN1}) increases. If the V_{SW1} / V_{IN1} ratio is too high, the system will not be able to achieve 800 mA within only 1 PFM pulse. In this case the on-time will be limited to approximately 4 µs and a second PFM pulse will be required, about 300 ns later, as shown in figure 12.

Input Capacitors (CINx)

Three factors should be considered when choosing the input capacitors. First, they must be chosen to support the maximum expected input voltage, with adequate design margin. Second, their rms current rating must be higher than the expected rms input current to the switcher. Third, they must have enough capacitance, and a low enough ESR, to limit the input voltage dV/dt to something much less than the hysteresis of the UVLO circuitry (nominally 400 mV for the A8600) at maximum loading and minimum input voltage.

The input capacitors must deliver the rms current according to:

$$I_{rms} = I_{SWx} \sqrt{D \times (1 - D)} \quad (15)$$

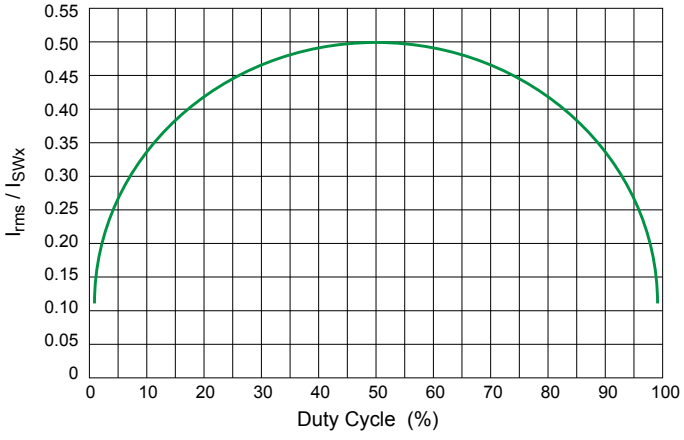

Figure 23. Input capacitor ripple versus duty cycle

where the duty cycle is:

$$D \approx (V_{SWx} + V_{fx}) / (V_{IN} + V_{fx}) \quad (16)$$

and V_{fx} is the forward voltage of the asynchronous diode, D_{SWx}.

Figure 23 shows the normalized input capacitor rms current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.400. Therefore, if the regulator is delivering 2.0 A of steady-state load current, the input capacitor(s) must support 0.400 × 2.0 A or 0.8 A_{rms}.

The input capacitors must limit the voltage deviations at the VINx pin to something significantly less than the A8600 UVLO hysteresis during maximum load and minimum input voltage. Equation 17 allows us to calculate the minimum input capacitance:

$$C_{INx} \geq \frac{I_{SWx} \times D \times (1 - D)}{f_{SWx}(min) \times (\Delta V_{INx}(min)} \quad (17)$$

where $\Delta V_{INx}(min)$ is chosen to be much less than the hysteresis of the V_{INx} UVLO comparator ($\Delta V_{INx}(min) \leq 150$ mV is recommended), and $f_{SW(min)}$ is the lowest expected PWM frequency.

The D × (1–D) term in equation 17 has an absolute maximum value of 0.25 at 50% duty cycle. So for example, a very conservative design, based on I_{SWx} = 2 A, $f_{SW}(min)$ = 325 kHz, D × (1–D) = 0.25, and ΔV_{INx} = 150 mV:

$$C_{INx} \geq \frac{2\ (A) \times 0.25}{325\ (kHz) \times 150\ (mV)} = 10.2\ \mu F$$

A good design accommodates the DC-bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction) so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC-bias effect is even more pronounced on smaller case sizes, so a good design uses the largest affordable case size (such as 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating, in order to accommodate the worst-case transient input voltage (that is, load dump as high as 40 V for automotive applications).

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Equation 17 should be used for each of the four buck switchers to calculate the required amount of ceramic input capacitance for each switcher. In the PCB layout, the input capacitor(s) for each buck switcher should be placed close to the switcher they support.

Asynchronous Diode (DSWx)

There are three requirements for the asynchronous diodes.

First, the asynchronous diode must be able to withstand the regulators input voltage when the high-side MOSFET is on. Therefore, the design should have a diode with a reverse voltage rating (V_{rx}) higher than the maximum expected input voltage (that is, the surge voltage).

Second, the forward voltage of the diode (V_{fx}) should be minimized or the regulator efficiency will suffer. Also, if V_{fx} is too high the missing diode protection in the A8600 could be falsely activated. A Schottky-type diode that can maintain a very low V_f when the regulator output is shorted to ground at the coldest ambient temperature is highly recommended.

Third, the asynchronous diode must conduct the output current when the high-side MOSFET is off. Therefore, the average forward current rating of this diode (I_{favgx}) must be high enough to deliver the load current according to equation 17, such that:

$$I_{favgx} \geq I_{SWx}(max)\,(1 - D) \tag{18}$$

where $I_{SWx}(max)$ is the maximum continuous output current of the regulator, and the minimum duty cycle is:

$$D(min) = (V_{SWx} + V_{fx}) / (V_{INx}(max) + V_{fx}) \tag{19}$$

Even though SW4 is a synchronous controller, it requires an external Schottky diode from LX4 to ground (DSW4), as shown in the Typical Application Circuit diagram. This diode will conduct during the non-overlap time and must clamp the LX4 pin to a relatively low (negative) voltage. Without this Schottky diode the LX4 pin will become more and more negative. Eventually, the negative voltage will forward-bias the substrate parasitic base-emitter junction and/or the LX4 ESD structure, which could lead to malfunction or even destruction of the A8600.

Bootstrap Capacitor (CBOOTx)

A bootstrap capacitor must be connected between the BOOTx and LXx pins to provide floating gate drive to the high-side MOSFET. Usually, SW1/2/3 require only 47 nF. However, for SW4 with its relatively large external MOSFET, 100 nF is recommended. This capacitor should be a high-quality ceramic, such as an X5R or X7R, with a voltage rating of at least 16 V.

For SW1/2/3, the A8600 incorporates a 10 Ω low-side MOSFET to ensure that the bootstrap capacitor is always charged, even when the regulator is lightly loaded or pre-biased.

Soft Start and Hiccup Mode Timing (CSSx)

The soft start time of the A8600 is determined by the value of the capacitance on the SSx pin (CSSx).

When the A8600 is enabled, the voltage at the SSx pin will start from 0 V and be charged by the soft start current, I_{SSSUx}. However, PWM switching will not begin instantly because the voltage at the SSx pin must rise above 400 mV. The soft start delay (t_{dSSx}) can be calculated using:

$$t_{dSSx} = C_{SSx} \times \left(\frac{400\ (mV)}{I_{SSSUx}}\right) \tag{20}$$

If the A8600 is starting into a very heavy load, a very fast soft start time may cause the switcher to exceed the pulse-by-pulse overcurrent threshold. This can occur because the total of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors

$$I_{CO} = C_{SWx} \times V_{SWx} / t_{SS} \tag{21}$$

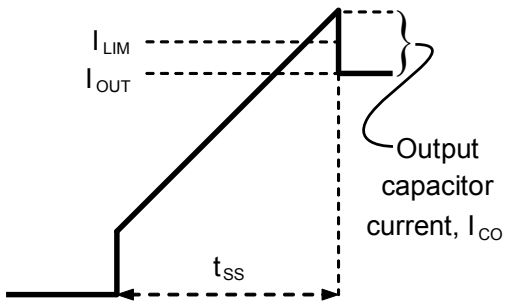

Figure 24. Output current (I_{CO}) during startup

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is higher than the pulse-by-pulse current threshold, as shown in figure 24. This phenomenon is more pronounced when using high value, electrolytic-type output capacitors.

To avoid prematurely triggering hiccup mode, the soft start capacitor, CSSx, should be calculated using the following formula:

$$C_{SSx} \geq \frac{I_{SSSSUx} \times V_{SWx} \times C_{SWx}}{0.8\ (V) \times I_{COx}} \quad (22)$$

where V_{SWx} is the output voltage, C_{SWx} is the output capacitance, I_{COx} is the amount of current allowed to charge the output capacitance during soft start (Allegro recommends an I_{COx} between 0.1 and 0.3 A).

Higher values of I_{CO} result in faster soft start times. However, lower values of I_{CO} ensure that hiccup mode is not falsely triggered. Allegro recommends starting the design with an I_{CO} of 0.1 A and increasing it only if the soft start time is too slow. If a non-standard capacitor value for CSSx is calculated, the next larger value should be used.

The output voltage ramp time, $t_{SSRAMPx}$, can be calculated by using either of the following methods:

$$t_{SSx} = V_{SWx} \times \frac{C_{SWx}}{I_{COx}} \quad (24)$$

or

$$t_{SSx} = 0.8\ (V) \times \frac{C_{SSx}}{I_{SSSUx}} \quad (25)$$

When the A8600 is in hiccup mode, the CSSx capacitor is used as a timing capacitor and sets the hiccup period. The SSx pin charges the CSSx capacitor with I_{SSSUx} during a startup attempt, and discharges the CSSx capacitor with I_{SSHICx} between startup attempts. Because the ratio of the SSx pin currents is 2:1, the time between hiccups will be at least twice as long as the startup time. Therefore, the effective duty-cycle of the A8600 will be very low when the output is shorted to ground, and the junction temperature will be kept low.

SW4 External MOSFET Selections

The external MOSFETs for SW4 must withstand the maximum expected input voltage. In an automotive environment this is usually the 40 V load dump situation. The BOOT4 regulator shown in the Typical Application Circuit diagram, internal gate drivers, and protection circuits were optimized for MOSFETs with less than12 nC of gate charge at V_{GS} = 5 V.

The upper and lower MOSFETs must support the SW4 peak output current according to the following equations:

Upper MOSFET:

$$I_{DHS4} \geq I_{SW4}(peak) \times \left(\frac{V_{SW4}}{V_{IN4}(min)}\right) \quad (26)$$

Lower MOSFET:

$$I_{DHS4} \geq I_{SW4}(peak) \times \left(1 - \frac{V_{SW4}}{V_{IN4}(max)}\right) \quad (27)$$

Examples of several 40 V MOSFETs with less than 12 nC of gate charge are shown in table 4.

SW4 Current Sense Resistor

The current limit of SW4 at its minimum on-time (t_{ON}(min)) is determined by the value of the external sense resistor according to the following equation:

$$I_{SW4}(peak) \text{ at } t_{ON}(min) = \frac{I_{LIM4}}{R_{SENSE4}} = \frac{75\ (mV)\ (typ)}{R_{SENSE4}} \quad (28)$$

Notice that this sets the current limit at t_{ON}(min) only. The actual current limit will depend on the duty cycle and switching frequency as shown in equations 5 and 6. Therefore, the sense resistor should be chosen to support the required load current (plus some margin) at a relatively high duty cycle and minimum switching frequency.

Compensation Components (RZx, CZx, CPx)

To compensate the system, it is important to understand where the buck power stage, load resistance, and output capacitance form their poles and zeros in frequency. Also, it is important to

Table 4: Possible 40 V MOSFETs for SW4

Part Number	Manufacturer	Typical at V_{GS}= 4.5 V (A)	(mΩ)	nC
FDS8449	Fairchild	6.8	26	8
Si4446DY	Vishay	4.9	37	8
DMN4034SSS	Diodes, Inc.	5.5	39	5
NTMS5838NL	ON Semi	7	25	9

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understand that the compensated error amplifier introduces a zero and two more poles, and where these should be placed to maximize system stability, provide a high bandwidth, and optimize the transient response.

First, we will look at the power stage of the A8600, the output capacitors, and the load resistance. This circuitry is commonly referred as the *control-to-output* transfer function. The low frequency gain of this section depends on the COMPx to V_{SWx} node current gain ($g_{mPOWERx}$), and the value of the load resistor (R_{LOADx}). The DC gain (0 Hz) of the control-to-output (CTO) is:

$$g_{CTO(0Hz)x} = g_{mPOWERx} \times R_{LOADx} \quad (29)$$

The control-to-output transfer function has a pole (f_{P1}), formed by the output capacitance (C_{SWx}) and load resistance (R_{LOADx}), at:

$$f_{P1x} = \frac{1}{2\pi \times R_{LOAD} \times C_{SWx}} \quad (30)$$

The control-to-output transfer function also has a zero (f_{Z1}) formed by the output capacitance (C_{SWx}) and its associated ESR:

$$f_{Z1x} = \frac{1}{2\pi \times ESRx \times C_{SWx}} \quad (31)$$

For a design with very low-ESR type output capacitors (such as ceramic or OS-CON™ output capacitors), the ESR zero (f_{Z1}) is usually at a high frequency, so it can be ignored. On the other hand, if the ESR zero falls below or near the 0 dB crossover frequency of the system (such as for electrolytic output capacitors), then it should be cancelled by the pole formed by the CPx capacitor and the RZx resistor (discussed and identified later as f_{P3}).

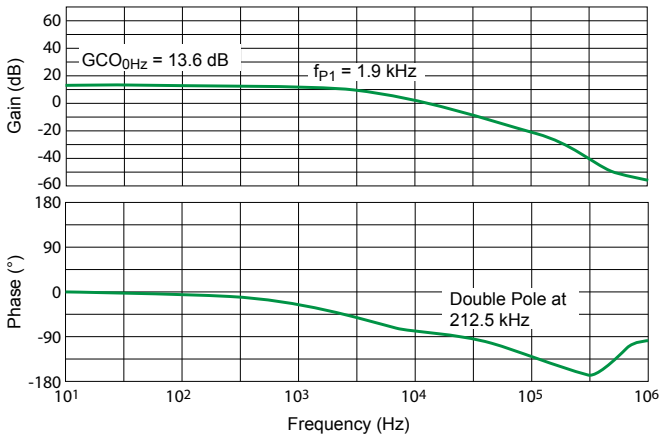

Figure 25. Control-to-output Bode plot for SW3

A Bode plot of the control-to-output transfer function for SW3 as shown in the Typical Application Circuit diagram, with V_{SW3} = 3.3 V, I_{SW3} = 2 A, and R_{LOAD3} = 1.65 Ω) is shown in figure 25. The pole at f_{P1} can be seen at 1.9 kHz while the ESR zero (f_{Z1}) occurs at a very high frequency, 636 kHz (this is typical for a design using ceramic output capacitors). Note, there is more than 90° of total phase shift because of the double-pole at half the switching frequency.

Next, we will look at the feedback resistor divider, (RFBAx and RFBBx), the error amplifier (g_m), and its compensation network RZ-CZ-CP. It greatly simplifies the transfer function derivation if R_{Ox} (error amplifier output impedance) >> R_{Zx}, and C_{Zx} >> C_{Px}. In most cases, R_{Ox} > 2 MΩ, 1 kΩ < R_{Zx} < 50 kΩ, 220 pF < C_{Zx} < 47 nF, and C_{Px} < 100 pF, so the following analysis should be very accurate.

The low frequency gain of the control section (G_{C0Hz}) is formed by the feedback resistor divider and the error amplifier. It can be calculated using:

$$\begin{aligned} G_{C0Hz} &= \frac{R_{FBBx}}{R_{FBAx}+R_{FBBx}} \times g_{mx} \times R_{Ox} \\ &= \frac{V_{FBx}}{V_{SWx}} \times g_{mx} \times R_{Ox} \\ &= \frac{V_{FBx}}{V_{SWx}} \times A_{VOLx} \end{aligned} \quad (32)$$

where V_{SWx} is the output voltage, V_{FBx} is the reference voltage (0.8 V), g_{mx} is the error amplifier transconductance (750 µA/V), and R_{Ox} is the error amplifier output impedance (A_{VOLx}/g_{mx}).

The transfer function of the Type-II compensated error amplifier has a (very) low frequency pole (f_{P2}) dominated by the output error amplifier output impedance R_{Ox} and the CZx compensation capacitor:

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$$f_{P2x} = \frac{1}{2\pi \times R_{Ox} \times C_{Zx}} \quad (33)$$

The transfer function of the Type-II compensated error amplifier also has frequency zero (f_{Z2}) dominated by the RZx resistor and the CZx capacitor:

$$f_{P2x} = \frac{1}{2\pi \times R_{Zx} \times C_{Zx}} \quad (34)$$

Lastly, the transfer function of the Type-II compensated error amplifier has a higher frequency pole (f_{P3}) dominated by the RZx resistor and the CPx capacitor:

$$f_{P3x} = \frac{1}{2\pi \times R_{Zx} \times C_{Px}} \quad (35)$$

A Bode plot of the error amplifier and its compensation network is shown in figure 26, in which f_{P2}, f_{P3}, and f_{Z2} are indicated on the magnitude plot. Notice that the zero (f_{Z2} at 3.8 kHz) has been placed so that it is in the vicinity of the pole at f_{P1} previously shown at 1.9 kHz in the control-to-output Bode plot, figure 25. Placing f_{Z2} just above f_{P1} will result in excellent phase margin, but relatively slow transient recovery time, as we will see later.

Finally, we look at the combined Bode plot of both the control-to-output and the compensated error amplifier; see the red curve shown in figure 27. Careful examination of this plot shows that the magnitude and phase of the entire system (red trace) are simply the sum of the error amplifier response (blue trace) and the control-to-output response (green trace). As shown in figure 27, the bandwidth (f_c) of this system is 36 kHz and the phase margin is 66 degrees.

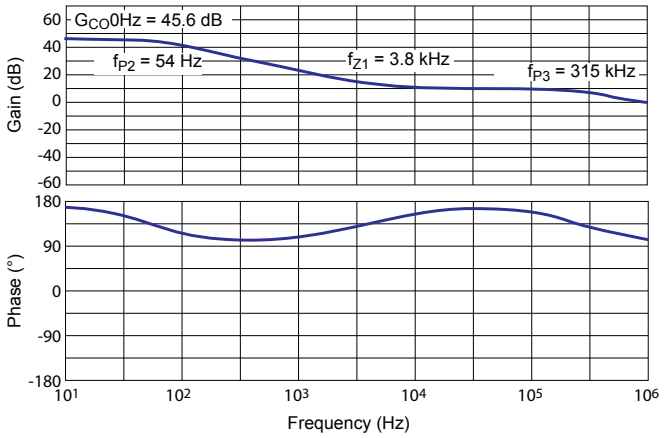

Figure 26. Compensated error amplifier Bode plot (SW3)

A Generalized Tuning Procedure

1) Choose the system bandwidth, f_C, which is the frequency at which the magnitude of the gain will cross 0 dB. Recommended values for f_C, based on the PWM switching frequency, are in the range: $f_{SW} / 20 < f_C < f_{SW} / 10$. A higher value of f_C will generally

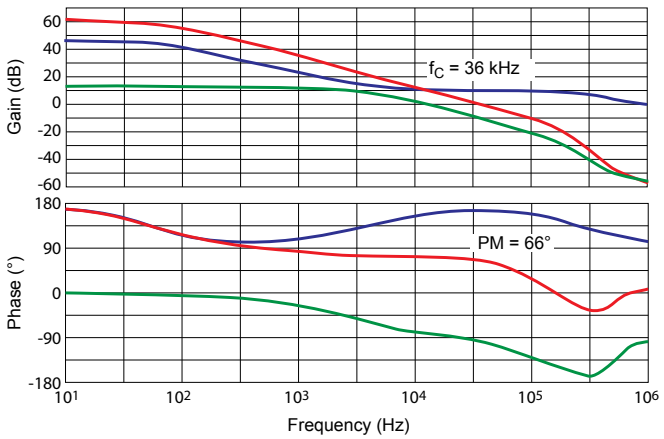

Figure 27. Bode plot of the complete SW3 system (red curve)

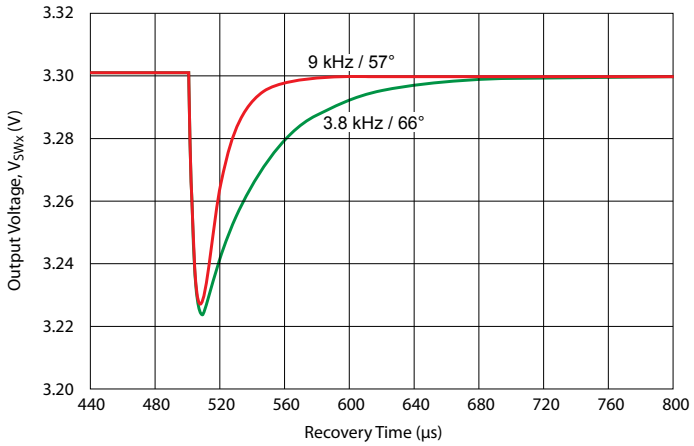

Figure 28. Transient recovery comparison for f_{Z2} at 3.8 kHz / 66° and 9 kHz / 57°

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provide a better transient response, and a lower value of f_C will make it easier to obtain higher gain and phase margins.

2) Calculate the RZx resistor value to set the required system bandwidth (f_C):

$$R_{Zx} = f_C \times \frac{V_{SWx}}{V_{FBx}} \times \frac{2\pi \times C_{SWx}}{g_{mPOWERx} \times g_{mx}} \quad (36)$$

3) Determine the frequency of the pole (f_{P1}) formed by C_{SWx} and R_{LOAD} by using equation 30 (repeated here):

$$f_{P1x} = \frac{1}{2\pi \times R_{LOAD} \times C_{SWx}}$$

4) Calculate a range of values for the CZx capacitor:

$$\frac{4}{2\pi \times R_{Zx} \times f_{Cx}} < C_{Zx} < \frac{1}{2\pi \times R_{Zx} \times 1.5 \times f_{P1x}} \quad (34)$$

To maximize system stability (that is, to have the most gain margin), use a higher value of CZ_X. To optimize transient recovery time, at the expense of some phase margin, use a lower value of CZ_X. Figure 28 shows the output voltage recovery time due to a 1A load transient for the system shown in figure 27 (f_{Z2} = 3.8 kHz, 66° phase margin) and a system with f_{Z2} at $^1/_4$ the crossover frequency, or 9 kHz. The system with f_{Z2} at 9 kHz has 57° of phase margin but recovers about twice as fast as the other system.

5) Calculate the frequency of the ESR zero (f_{Z1}) formed by the output capacitor(s) by using equation 31 (repeated here):

$$f_{Z1x} = \frac{1}{2\pi \times ESRx \times C_{SWx}}$$

5a) If f_{Z1} is at least 1 decade higher than the target crossover frequency (f_C) then f_{Z1} can be ignored. This is usually the case for a design using ceramic output capacitors. Use equation 35 to calculate the value of CPx by setting f_{P3} to either 5 × f_C or f_{SW} / 2, whichever is higher.

5b) Conversely, if f_{Z1} is near or below the target crossover frequency (f_C) then use equation 35 to calculate the value of CPx by setting f_{P3} equal to f_{Z1}. This is usually the case for a design using high ESR electrolytic output capacitors.

Power Dissipation and Thermal Calculations

The power dissipated in the A8600 is the sum of the power dissipated from the V_{IN} supply current (P_{IN}), the power dissipated due to the switching of the internal power MOSFETs ($P_{SW1/2/3}$), the power dissipated due to the rms current being conducted by the internal MOSFET ($P_{COND1/2/3}$), the power dissipated by the four internal gate drivers ($P_{DRIVER1/2/3/4}$), and the power dissipated due to the rms current being conducted by the two high-side switches ($P_{S1/S2}$).

The power dissipated from the V_{IN} supply current can be calculated using the following equation:

$$P_{INTOTAL} = V_{INx} \times I_Q + (V_{INx} - V_{GSx}) \times (3 \times Q_G + Q_{G4}) \times f_{SW} \quad (35)$$

where V_{INx} is the input voltage, I_Q is the input quiescent current drawn by the A8600 (nominally 7.5 mA), V_{GS} is the MOSFET gate drive voltage (typically 5 V), Q_G is the internal MOSFET gate charge (approximately 2.5 nC), Q_{G4} is the external MOSFET gate charge for SW4, and f_{SW} is the PWM switching frequency.

The power dissipated by the internal high-side MOSFET while it is switching can be calculated using the following equation:

$$P_{SW1/2/3} \geq \frac{V_{IN1/2/3} \times I_{SW1/2/3x} \times (t_r + t_f) \times f_{SW}}{2} \quad (36)$$

where V_{INx} is the input voltage, I_{SWx} is the regulator output current, f_{SWx} is the PWM switching frequency, and t_r and t_f are the rise and fall times measured at the V_{LXx} node. The exact rise and fall times at the V_{SWx} node will depend on the external components and PCB layout so each design should be measured at full load. Approximate values for both t_r and t_f range from 5 to 10 ns.

The power dissipated by the internal high-side MOSFETs while they are conducting can be calculated using the following equation:

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$$P_{COND1/2/3} = I^2_{rms(FET)1/2/3} \times R_{DS(on)HS1/2/3} = \left(\frac{V_{SW1/2/3}+V_{f1/2/3}}{V_{IN1/2/3}+V_{f1/2/3}}\right) \times \left(I^2_{LSW1/2/3} + \frac{\Delta I^2_{L1/2/3}}{12}\right) \times R_{DS(on)HS1/2/3} \quad (37)$$

where I_{SWx} is the regulator output current, ΔI_{Lx} is the peak-to-peak inductor ripple current, $R_{DS(on)HSx}$ is the on-resistance of the high-side MOSFET, and V_{fx} is the forward voltage of the asynchronous diode.

The $R_{DS(on)}$of the high-side MOSFET will have some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an $R_{DS(on)}$ with at least a 15% initial tolerance plus 0.39%/°C increase due to temperature.

The sum of the power dissipated by the internal gate driver can be calculated using the following equation:

$$P_{DRIVER} = (3 \times Q_G + Q_{G4}) \times V_{GS} \times f_{SW} \quad (38)$$

where V_{GS} is the gate drive voltage (typically 5 V for all four buck switchers), Q_G is the gate charge to drive internal MOSFET1/2/3 to V_{GS} = 5 V (about 2.5 nC each), Q_{G4} is the gate charge to drive the external MOSFET to V_{GS} = 5 V (this must come from the MOSFET datasheet), and f_{SW} is the PWM switching frequency.

The power dissipated by the high-side switches (S1, S2) can be calculated using th following equation:

$$P_{S1/S2} = I^2_{S1/S2} \times R_{DS(on)S1/S2} \quad (39)$$

where I_x is the DC current through high-side switches S1 and S2, and $R_{DS(on)Sx}$ is the on-resistance of the switch (typically 1 Ω),

Finally, the total power dissipated (P_{TOTAL}) is the sum of the previous equations for all four switchers and the high-side switches:

$$P_{TOTAL} = P_{INTOTAL} + P_{SW1/2/3} + P_{DRIVER} + P_{S1/S2} \quad (40)$$

The average junction temperature can be calculated with the following equation:

$$T_J = P_{TOTAL} + R_{\theta JA} + T_A \quad (41)$$

where P_{TOTAL} is the total power dissipated as described in equation 40, $R_{\theta JA}$ is the junction-to-ambient thermal resistance (23°C/W on a 4-layer PCB), and T_A is the ambient temperature.

The maximum junction temperature will be dependent on how efficiently heat can be transferred from the PCB to ambient air. The thermal pad on the bottom of the IC should be connected to a at least one ground plane using multiple vias for optimum performance. A small amount of airflow can improve the thermal performance considerably.

As with any regulator, there are limits to the amount of power that can be delivered and heat that can be dissipated before risking thermal shutdown. There are tradeoffs between ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will will reduce junction temperature considerably.

PCB Component Placement and Routing

A good PCB layout is critical if the A8600 is to provide clean, stable output voltages. Follow these guidelines to insure good PCB layout. Figure 28 shows a typical buck converter schematic with the critical power paths/loops. Figure 29 shows an example PCB component placement and routing (for SW3) with the same critical power paths/loops from the schematic.

1) By far, the highest di/dt in the asynchronous buck regulator occurs at the instant the upper FET turns on and the capacitance of the asynchronous Schottky diode (200 to 1000 pF) is quickly charged to V_{INx}. The ceramic input capacitors must deliver this fast, short pulse of current. Therefore, the loop from the ceramic input capacitors through the upper FET and into the asynchronous diode to ground should be minimized. Ideally these components are all connected using only the top layer traces (that is, do not use vias to other power or signal layers).

2) When the upper FET is on, current flows from the input supply and capacitors, through the upper FET, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.

3) When the upper FET is off, free-wheeling current flows from ground, through the asynchronous diode, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.

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4) The voltage on the LXx nodes transition from 0 V to V_{INx} very quickly and are the root cause of many noise issues. It is best to place the asynchronous diode and output inductor close to the A8600 to minimize the size of the LXx polygon. Also, keep low-level analog signals (such as FBx and COMPx) away from the LXx polygon.

5) Place the feedback resistor dividers (RFBAx and RFBBx) very close to the FBx pin. Ground this resistor divider as close as possible to the A8600.

6) The two traces to the SW4 sense resistor should be run in parallel back to CSP and CSN.

7) To have the highest output voltage accuracy, the output voltage sense trace (from V_{SWx} to RFBAx) should be connected as close as possible to the load.

8) Place the compensation components (RZx, CZx, and CPx) as close as possible to the COMPx pin. Place vias to the GND plane as close as possible to these components.

9) Place the soft start capacitor (CSSx) as close as possible to the SSx pin. Place a via to the GND plane as close as possible to this component.

10) Place the boot strap capacitor (CBOOTx) near the BOOTx pin and keep the routing to this capacitor as short as possible.

11) When routing the input and output ceramic capacitors, use multiple vias to GND and place the vias as close as possible to the pads of the component.

12) To minimize PCB losses and improve system efficiency, the input and output traces should be as wide as possible and be duplicated on multiple layers, if possible.

13) To improve thermal performance, place multiple vias to the GND plane around the anode of the asynchronous diode.

14) The thermal pad under the A8600 must connect to the GND plane using multiple vias. More vias will ensure the lowest junction temperature and highest efficiency.

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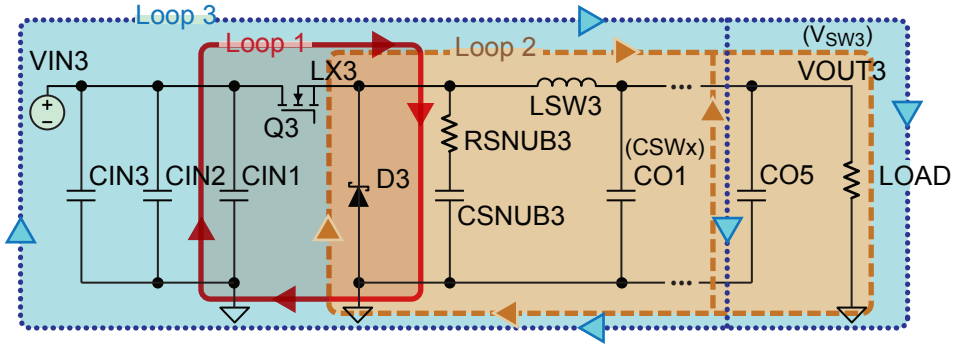

Figure 28. Typical buck converter PCB layout, with critical paths and loops shown

Loop 1 (Red): At the instant Q3 turns on, the Schottky diode D3 (which is very capacitive), must be very quickly charged and shut off. The spike of charging current must come from the input capacitors, CIN1/2/3. This spike of current is quite large and will be an EMI/EMC issue if loop 1 is not minimized. Therefore, the input capacitors and Schottky diode D3 must be placed be on the same (top) layer, be located near each other, and be grounded at virtually the same point on the PCB.
Loop 2 (Brown): When Q3 is off, free-wheeling inductor current must flow from ground through diode D3, into the output inductor, out to the load and return via ground. While Q3 is off, the voltage on the output capacitors will decrease. The output capacitors and Schottky diode D3 must be placed on the same (top) layer, be located near each other, and be grounded at virtually the same point on the PCB.
Loop 3 (Blue): When Q3 is on, current flows from the input supply and input capacitors through the output inductor and into the load. At this time the voltage on the output capacitors will increase.

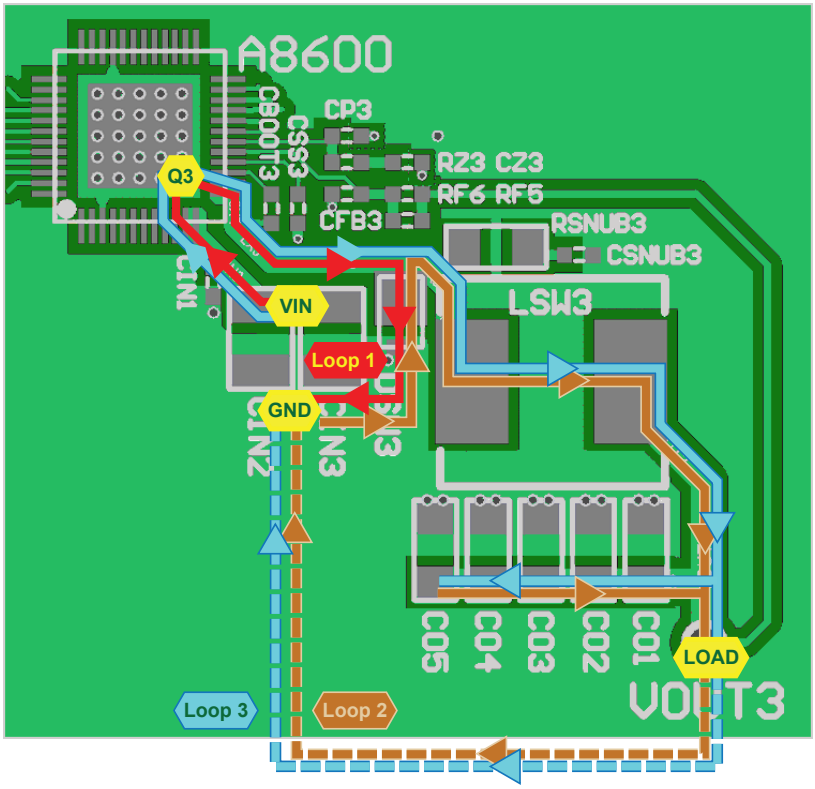

Figure 29. Example PCB component placement and routing, example shows SW3

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Table 5. Pin Descriptions Table

Name	Number	Description	Pin Connection If Pin Function Not Used
General			
EN/SYNC	6	EN/PFM control and PWM synchronization input	((Always used))
BIAS	45	Bias input, supplies internal circuitry when V_{SW1} is high enough	Ground
VREG	4	Internal voltage regulator bypass capacitor pin	(Always used)
POK	23	Power OK open drain output	Open
GND	3	Ground	(Always used)
PAD	–	Exposed pad for enhanced thermal dissipation	(Always used, connect to ground)
Internal Asynchronous Always-On Buck Regulator (SW1)			
VIN1	1	Input supply for buck regulator SW1	(Always used)
LX1	48	Switching node for buck regulator SW1	(Always used)
BOOT1	47	Floating gate drive for buck regulator SW1	(Always used)
FB1	44	Feedback pin for buck regulator SW1	(Always used)
COMP1	43	Error amplifier compensation network for regulator SW1	(Always used)
SS1	46	Soft start programming for regulator SW1	(Always used)
Internal Asynchronous Buck Regulator (SW2)			
VIN2	35	Input supply for buck regulator SW2	Ground
VIN2	36	Input supply for buck regulator SW2	Ground
LX2	37	Switching node for buck regulator SW2	Ground
LX2	38	Switching node for buck regulator SW2	Ground
NC	34	Unused, this pin should be left unconnected	N/A
BOOT2	39	Floating gate drive for buck regulator SW2	Ground
FB2	41	Feedback pin for buck regulator SW2	FB3 or FB4
COMP2	42	Error amplifier compensation network for regulator SW2	Ground
SS2	40	Soft start programming for regulator SW2	Ground
Internal Asynchronous Buck Regulator (SW3)			
VIN3	11	Input supply for buck regulator SW3	V_{IN} supply (or Ground[1])
VIN3	12	Input supply for buck regulator SW3	V_{IN} supply (or Ground[1])
LX3	13	Switching node for buck regulator SW3	BOOT3 (or Ground[1])
LX3	14	Switching node for buck regulator SW3	BOOT3 (or Ground[1])
BOOT3	15	Floating gate drive for buck regulator SW3	LX3 (or Ground[1])
FB3	17	Feedback pin for buck regulator SW3	FB2 or FB4
COMP3	18	Error amplifier compensation network for regulator SW3	Ground
SS3	16	Soft start programming for regulator SW3	Ground

Continued on the next page…

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Table 5. Pin Descriptions Table (continued)

Name	Number	Description	Pin Connection If Pin Function Not Used
External Synchronous Buck Regulator (SW4)			
LX4	30	Switching node for buck regulator SW4	BOOT4 (or Ground [1])
BOOT4	31	Floating gate drive for buck regulator SW4	LX4 (or Ground [1])
HG4	29	High side gate drive for buck regulator SW4	Open (or Ground [1])
LG4	32	Low side gate drive for buck regulator SW4	Open (or Ground [1])
PGND	33	Power ground	(Always used)
CSP	27	Current sense pin for buck regulator SW4	Ground
CSN	26	Current sense pin for buck regulator SW4	Ground
FB4	25	Feedback pin for buck regulator SW4	FB2 or FB3
COMP4	24	Error amplifier compensation network for regulator SW4	Ground
SS4	28	Soft start programming for regulator SW4	Ground
BU, ACC, and Mute Functions			
BUI	10	Input to the BU comparator	Ground
BUO	9	Output of the BU comparator	Open
ACCI	8	Input to the ACC comparator	Ground
ACCO	7	Output of the ACC comparator	Open
CTMR	5	Delay programming for the MUTE pulse circuit	Ground
MUTE	2	Open-drain, active LOW output of the MUTE pulse circuit	Open
High-Side Switches (S1, S2)			
VINS	21	Input to the high-side switches	V_{IN} supply (or Ground [2])
ENS	19	Input to enable/disable both high-side switches	Ground
OUT1	20	High-side switch S1 output	OUT2 or Open (or Ground [2])
OUT2	22	High-side switch S2 output	OUT1 or Open (or Ground [2])

[1] Connect to Ground instead, if also SW3 and SW4 both are not used.
[2] Connect to Ground instead, if also S1 and S2 both are not used.

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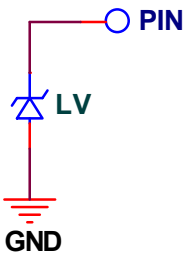
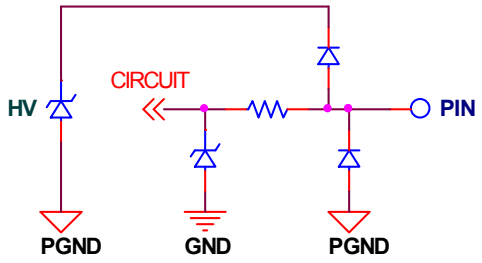
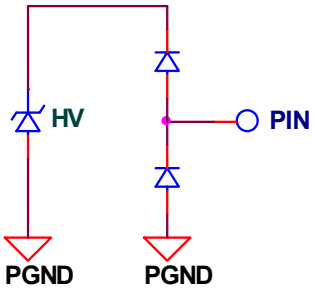
PIN ESD STRUCTURES: (Note: The **HV clamp** is shown where needed, but there is only 1 common HV clamp in the IC)



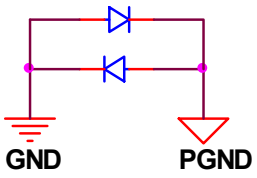
Low Voltage Pins;
FB_X, EN/SYNC, VREG, BIAS, CSP, CSN, LG4, BUQ ACCQ CTMR, ACCI



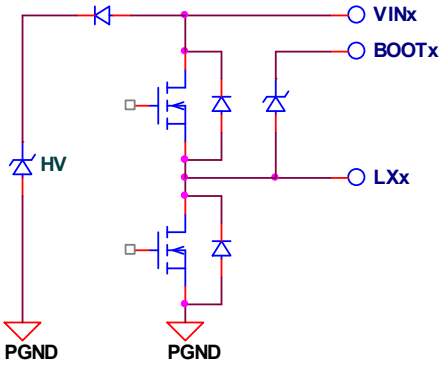
High Voltage Pins with Clamp:
BUI, SS_X, ENS



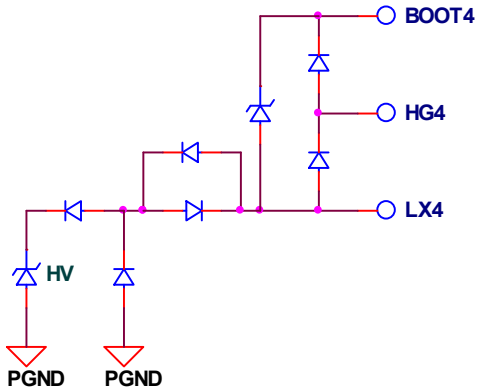
High Voltage Pins;
OUT1, OUT2, VINS, MUTE, POK



GND to PGND



SW1, SW2, and SW3 Power Pins;
VIN1, VIN2, VIN3, LX1, LX2, LX3, BOOT1, BOOT2, BOOT3



SW4 Output Pins; BOOT4, HG4, LX4

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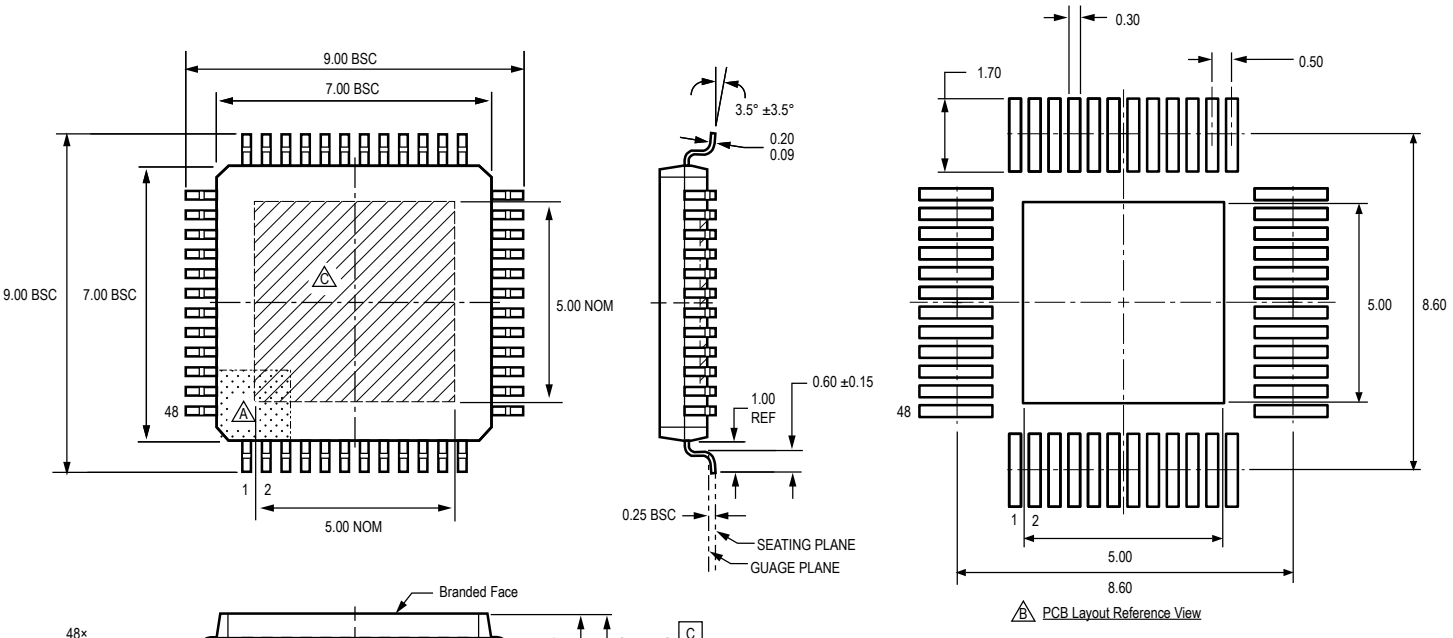
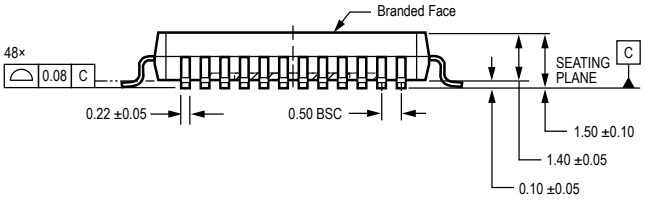
PACKAGE OUTLINE DRAWING

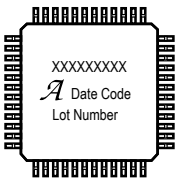
Package JP, 48-Pin LQFP

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000386, Rev. 5 or JEDEC MS-026 BBCHD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown







A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 QFP50P900X900X160-48M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface); exact dimensions may vary with device

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View
Line 1, 2, 3: Maximum 9 characters per line

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Assembly Lot Number

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Revision History

Number	Date	Description
3	December 5, 2012	Editorial changes
4	April 1, 2016	Updated High-Side MOSFET Leakage test conditions in Electrical Characteristics table
5	May 1, 2020	Minor editorial updates
6	April 22, 2022	Updated package drawing (page 51)

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