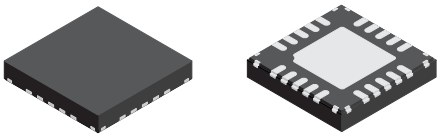
Buck-Boost Controller with Integrated Buck MOSFET

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Wide operating range of 3 to 36 V_{IN}, 40 V_{IN} maximum, covers automotive stop/start, cold crank, double battery, and load dump
- Regulated output can operate up to 2 A DC
- Adjustable PWM switching frequency: 250 kHz to 2.2 MHz
- PWM frequency can be synchronized to external clock: 250 kHz to 2.4 MHz
- Frequency dithering helps reduce EMI/EMC
- Undervoltage protection
- Pin-to-pin and pin-to-ground tolerant at every pin
- Thermal shutdown protection
- Operating junction temperature range −40°C to 150°C

PACKAGES:

20-pin 4 × 4 mm QFN (ES) with wettable flank



Not to scale

DESCRIPTION

The A4450 is a power management IC that can implement either a buck or buck-boost regulator to efficiently convert automotive battery voltages into a tightly regulated voltage. It includes control, diagnostics, and protection functions.

An enable input to the A4450 is compatible to a high-voltage battery level, (EN).

A diagnostic output from the A4450 includes a power-on reset output (NPOR) signal.

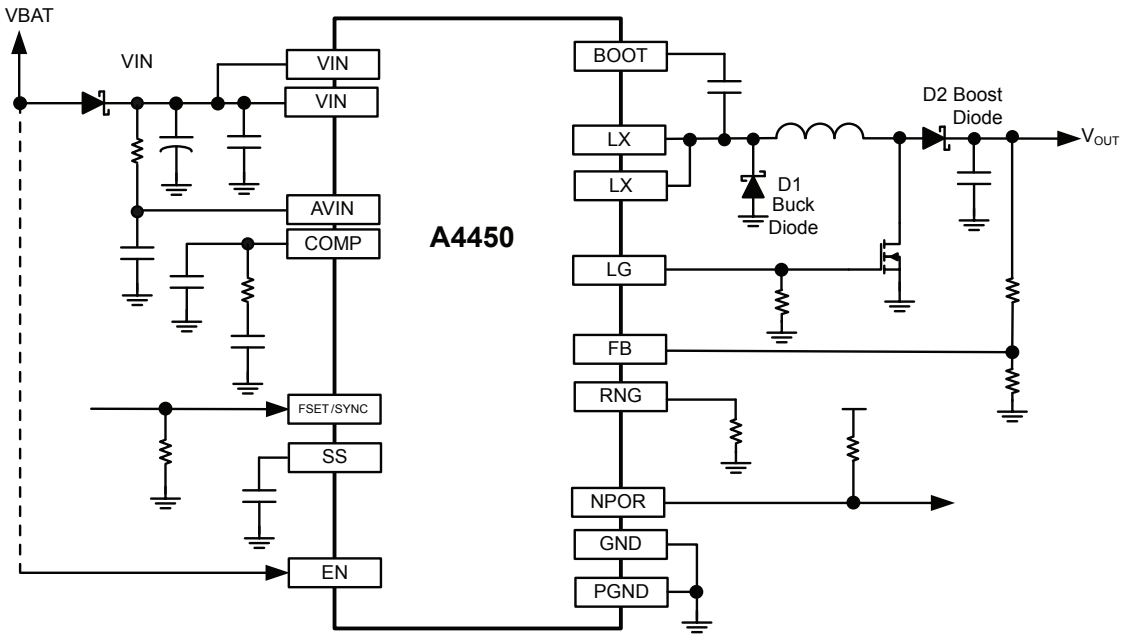
Protection features include pulse-by-pulse current limit, hiccup mode short-circuit protection, LX short-circuit protection, missing freewheeling diode (buck diode at LX node in A4450) protection, and thermal shutdown.

The A4450 is most suitable for applications where the input voltage can vary from less than or greater than the regulated output voltage.

The A4450 is supplied in 4 mm × 4 mm QFN (suffix “ES”) with exposed power pad.

APPLICATIONS

- Infotainment
- Instrument Clusters
- Control Modules



Typical Application Diagram

SELECTION GUIDE

Part Number	Temperature Range	Packing [1]	Package	Lead Frame
A4450KESTR-J	–40°C to 150°C	1500 pieces per 7-inch reel	20-pin QFN with thermal pad and wettable flank	100% matte tin

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V_{IN}		–0.3 to 40	V
AVIN	V_{AVIN}		–0.3 to 40	V
EN	V_{EN}		–0.3 to V_{IN}	V
LX	V_{LX}	continuous	–0.3 to V_{IN} + 0.3	V
		t < 250 ns	–1.5	V
		t < 50 ns	V_{IN} + 3	V
LG	V_{LG}		–0.3 to 8.5	V
BOOT	V_{BOOT}		V_{LX} – 0.3 to V_{LX} + 6	V
All other pins			–0.3 to 7.5	V
Junction Temperature Range	T_J		–40 to 150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	QFN-20 (ES) package, 4-layer PCB based on JEDEC standard	37	°C/W

[3] Additional thermal information available on the Allegro website.

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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
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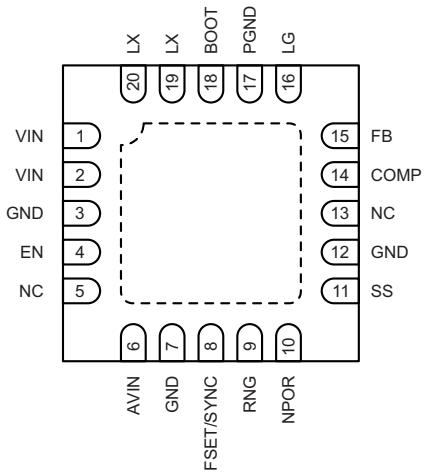
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package ES, 20-Pin QFN Pinout Diagram

Terminal List Table

Symbol	Number	Function
VIN	1, 2	Input voltage; ensure decoupling capacitors are connected directly to this pin.
GND	3, 7, 12	Ground pin for decoupling and ground connection.
EN	4	Enable pin; 40 V rated and logic level compatible; can be connected to VIN or switching battery. Used to turn the regulator on or off: set pin high to turn the regulator on or set pin low to turn the regulator off. Can be used to set UVLO threshold with external resistor divider.
NC	5, 13	No connection.
AVIN	6	Input to internal voltage regulator and boost duty generator; must connect to VIN through a resistor (5 Ω typ) and a capacitor is suggested to be added between AVIN pin and GND to form a RC filter.
FSET/SYNC	8	Frequency setting and synchronization input. Switching frequency is programmed by connecting a resistor from this pin to ground. This pin can also accept a square wave switching signal that synchronizes the converter through internal PLL.
RNG	9	Output range select pin. A resistor connected between RNG pin and GND is selected base on the target V_{OUT}.
NPOR	10	Active-low power-on reset output signal. This pin is an open-drain regulator fault detection output that transitions from low to high impedance after the output has maintained regulator for t_{dNPOR}.
SS	11	A capacitor from this pin to GND sets the soft-start time. This capacitor also determines the hiccup period.
COMP	14	Error amplifier compensation network pin. Connect series RC network from this pin to ground for loop compensation to stabilize the converter.
FB	15	Feedback pin for output. Connect a voltage divider from the output to this pin to program the output voltage.
LG	16	Gate drive output for the external boost switch. Connect a 10 kΩ resistor from this pin to PGND.
PGND	17	Power ground. Provide power ground return for drivers.
BOOT	18	Bootstrap capacitor connection. Connect a capacitor from this pin to LX pin. This pin provides supply voltage for the high-side and low-side gate drivers.
LX	19, 20	Switching node of the regulator; the output inductor and cathode of the buck diode should be connected to this pin with relatively wide traces. The inductor and buck diode should be placed as close as possible to this pin.

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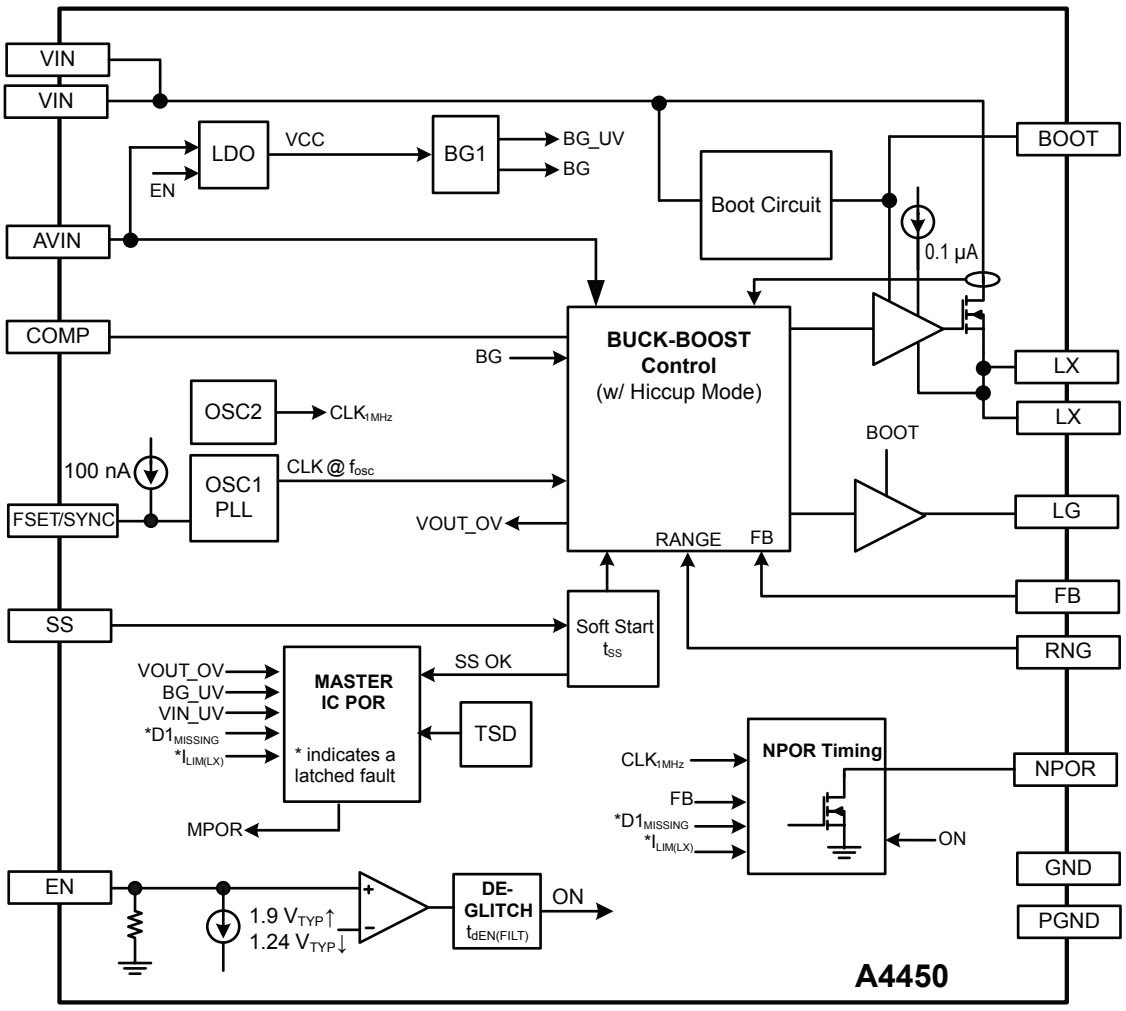
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS: Valid at 3 V ≤ V_{IN} ≤ 36 V and V_{IN} having first reached $V_{INSTART}$, –40°C ≤ T_J ≤ 150°C, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage	V_{IN}	After V_{IN} > $V_{INSTART}$, V_{EN} ≥ 4 V	3.0	13.5	36	V
VIN UVLO Start	$V_{INSTART}$	V_{IN} rising	–	–	4.8	V
VIN UVLO Stop	V_{INSTOP}	V_{IN} falling, when in Buck-Boost mode	–	–	2.9	V
Supply Quiescent Current [1]	I_Q	V_{IN} = 13.5 V, V_{EN} ≥ 4 V, no load	–	4.5	–	mA
	$I_{Q(SLEEP)}$	V_{IN} = 13.5 V, V_{EN} ≤ 1 V, no load	–	–	10	µA
PWM SWITCHING FREQUENCY AND DITHERING						
Switching Frequency	f_{OSC}	R_{FSET} = 7.87 kΩ	1.8	2.0	2.2	MHz
		R_{FSET} = 41.2 kΩ	343	400	457	kHz
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	–	±12	–	%
VIN Dithering START Threshold	$V_{IN(DITHER,ON)}$	V_{IN} rising, R_{NG} = 15 kΩ, target V_{OUT} = 5 V		7.0 [3]		V
		V_{IN} falling	–	16.6	–	V
VIN Dithering STOP Threshold	$V_{IN(DITHER,OFF)}$	V_{IN} falling, R_{NG} = 15 kΩ, target V_{OUT} = 5 V		7.0 [3]		V
		V_{IN} rising	–	18	–	V
VIN Dithering Hysteresis	$V_{IN(DITHER,HYS)}$		–	1.5	–	V
THERMAL PROTECTION						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	160	170	180	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	20	–	°C
OUTPUT VOLTAGE SPECIFICATIONS						
Feedback Voltage Tolerance	V_{FB}	V_{IN} = 13.5 V, EN = high	0.788	0.800	0.812	V
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWMOFFS}$	V_{COMP} for 0% duty cycle	–	400	–	mV
LX Rising Slew Rate [2]	LX_{RISE}	V_{IN} = 13.5 V, 10% to 90%, I_{LX} = 1 A	–	1.5	–	V/ns
LX Falling Slew Rate [2]	LX_{FALL}	V_{IN} = 13.5 V, 10% to 90%, I_{LX} = 1 A	–	1.8	–	V/ns
Buck Minimum On-Time	$t_{ON(MIN,BUCK)}$		–	85	120	ns
Buck Minimum Off-Time	$t_{OFF(MIN,BUCK)}$		–	85	120	ns
Boost Maximum Duty Cycle	$D_{MAX(BST)}$	V_{IN} = 3.5 V, V_{OUT} = 8 V target, R_{NG} = 25.5 kΩ, 2 MHz	–	0.75	–	–
		V_{IN} = 3.5 V, V_{OUT} = 5 V target, R_{NG} = 15 kΩ, 2 MHz	–	0.57	–	–
		V_{IN} = 3.5 V, V_{OUT} = 3 V target, R_{NG} = 9.31 kΩ, 2 MHz	–	0.31	–	–
COMP to LX Current Gain	gm_{POWER}		3.5	4.7	5.9	A/V
Slope Compensation [2]	S_E	f_{OSC} = 2 MHz	1.76	2.2	2.64	A/µs
		f_{OSC} = 400 kHz	0.35	0.44	0.53	A/µs
INTERNAL MOSFET						
MOSFET On Resistance	R_{DSon}	V_{IN} = 13.5 V, T_J = –40°C (2), I_{DS} = 0.1 A	–	60	90	mΩ
		V_{IN} = 13.5 V, T_J = 25°C (2), I_{DS} = 0.1 A	–	80	110	mΩ
		V_{IN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	–	140	170	mΩ
MOSFET Leakage	$I_{FET(LKG)}$	V_{EN} ≤ 1 V, V_{LX} = 0 V, V_{IN} = 13.5 V, –40°C ≤ T_J ≤ 85°C (2)	–	–	10	µA

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ELECTRICAL CHARACTERISTICS (continued): Valid at 3 V ≤ V_{IN} ≤ 36 V and V_{IN} having first reached $V_{INSTART}$, –40°C ≤ T_J ≤ 150°C, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER						
Open-Loop Voltage Gain	AVOL		–	65	–	dB
Transconductance	gm_{EA}		550	750	950	µA/V
Output Current	I_{EA}		–	±75	–	µA
Maximum Output Voltage, Buck-Boost Mode	$V_{EAVO(max)BuckBoost}$		–	1.5	–	V
Maximum Output Voltage, Buck Mode	$V_{EAVO(max)Buck}$		–	1.2	–	V
Minimum Output Voltage	$V_{EAVO(min)}$		150	220	290	mV
BOOST MOSFET (LG) GATE DRIVER						
LG High Output Voltage	$V_{LG(ON)}$	V_{IN} = 7 V	5.0	–	8.0	V
LG Low Output Voltage	$V_{LG(OFF)}$	V_{IN} = 13.5 V	–	–	0.4	V
LG Source Current [1]	$I_{LG(ON)}$	V_{LG} = 1 V	–	−265	–	mA
LG Sink Current [1]	$I_{LG(OFF)}$	V_{LG} = 1 V	–	500	–	mA
SOFT-START						
SS PWM Frequency Foldback (Linear)	$f_{SW(SS)}$	V_{FB} = 0 V	–	0.12 × f_{OSC}	–	–
		V_{FB} = 0.2 V	–	0.43 × f_{OSC}	–	–
		V_{FB} = 0.6 V	–	0.93 × f_{OSC}	–	–
		V_{FB} = 0.8 V	–	f_{OSC}	–	–
Switching Frequency in SYNC Mode with Applied Frequency f_{SYNC}	$f_{SW(SYNC)}$	0 V < V_{FB} < 0.2 V	–	f_{SYNC}/4	–	–
		0.2 V < V_{FB} < 0.4 V	–	f_{SYNC}/2	–	–
		0.4 V < V_{FB}	–	f_{SYNC}	–	–
HICCUP MODE						
Hiccup OCP PWM Counts	$t_{HIC(OCP)}$	V_{FB} < 0.4 V (typical), V_{COMP} = $V_{EAVO(max)}$	–	30	–	PWM cycles
		V_{FB} > 0.4 V (typical), V_{COMP} = $V_{EAVO(max)}$	–	120	–	PWM cycles
Hiccup Mode Recovery Time	$t_{HIC(RECOVER)}$	LX switching stops to LX switching starts, during overcurrent	3.0	–	5.6	ms
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit, Buck-Boost Mode	$I_{LIM(BuckBoost)}$	Buck-Boost mode	3.9	4.5	5.1	A
Pulse-by-Pulse Current Limit, Buck Mode	$I_{LIM(Buck)}$	Buck mode	2.4	2.8	3.4	A
LX Short-Circuit Current Limit	$I_{LIM(LX)}$		6.3	7.4	8.5	A
MISSING BUCK DIODE (D1) PROTECTION						
Detection Level [2]	$V_{D(OPEN)}$		−1.6	−1.4	−1.1	V
Time Filtering [2]	$t_{D(OPEN)}$		50	–	250	ns

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ENABLE (EN) INPUT						
EN Thresholds	$V_{EN(H)}$	V_{EN} rising	–	1.9	2.25	V
	$V_{EN(L)}$	V_{EN} falling	1.0	1.2	–	V
EN Hysteresis	$V_{EN(HYS)}$	$V_{EN(H)} – V_{EN(L)}$	–	700	–	mV
EN Bias Current [1]	$I_{EN(BIAS)}$	V_{EN} = 3.5 V, T_J = 25°C (2)	–	28	45	µA
		V_{EN} = 3.5 V, T_J = 150°C	–	35	55	µA
EN Pulldown Resistance	R_{EN}		–	650	–	kΩ
EN DEGLITCH						
Enable Filter/Deglitch Time	$t_{dEN(FILT)}$		10	20	30	µs
EN SHUTDOWN DELAY						
Shutdown Delay	t_{dOFF}	Measured from the falling edge of EN to the time when LX stops switching	28	32	36	µs
FSET/SYNC INPUT						
FSET/SYNC Pin Voltage	$V_{FSET/SYNC}$	No external SYNC signal	–	640	–	mV
FSET/SYNC Open Circuit (Undercurrent) Detection Time [2]	$V_{FSET/SYNC(UC)}$	PWM switching frequency becomes 1 MHz upon detection	–	3	–	µs
FSET/SYNC Short Circuit (Overcurrent) Detection Time [2]	$V_{FSET/SYNC(OC)}$	PWM switching frequency can rise up to 3.2 MHz_{TYP}	–	3	–	µs
Sync High Threshold [2]	$V_{SYNCVIH}$	V_{SYNC} rising	–	–	2.0	V
Sync Low Threshold [2]	$V_{SYNCVIL}$	V_{SYNC} falling	0.5	–	–	V
Sync Input Duty Cycle	DC_{SYNC}		–	–	80	%
Sync Input Pulse Width	t_{wSYNC}		200	–	–	ns
Sync Input Transition Times [2]	t_{tSYNC}		–	10	15	ns
VFB THRESHOLDS						
NPOR VFB Overvoltage Threshold	$V_{FBNPOROV(H)}$	V_{FB} rising, PWM disabled, NPOR pulled low	840	890	930	mV
NPOR VFB Overvoltage Hysteresis	$V_{FBNPOROV(HYS)}$		–	10	–	mV
VFB Overvoltage Threshold	V_{FBOV}	High-side FET off, LG turns high, NPOR remains high	–	840	–	mV
NPOR VFB Undervoltage Thresholds	$V_{FBNPORUV(H)}$	V_{FB} rising	–	750	–	mV
	$V_{FBNPORUV(L)}$	V_{FB} falling	720	740	760	mV
NPOR VFB Undervoltage Hysteresis	$V_{FBNPORUV(HYS)}$	$V_{FBNPORUV(H)} – V_{FBNPORUV(L)}$	–	10	–	mV
UNDERVOLTAGE/OVERVOLTAGE FILTERING/DEGLITCH						
Undervoltage Filter/Deglitch Times	$t_{dUV(FILT)}$		20	30	40	µs
Overvoltage Filter/Deglitch Times	$t_{dOV(FILT)}$		20	30	40	µs
NPOR OUTPUT						
NPOR Rising Delay	t_{dNPOR}	Time from output in regulation to NPOR rising edge	–	2.1	–	ms
NPOR Low Output Voltage	$V_{NPOR(L)}$	EN High, V_{IN} ≥ 3 V, I_{NPOR} = 4 mA	–	150	400	mV
NPOR Leakage Current	$I_{NPOR(LKG)}$	V_{NPOR} = 5 V	–	–	2	µA

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Threshold is adjustable following the equation R_{NG} (kΩ) / 1.844 (V).

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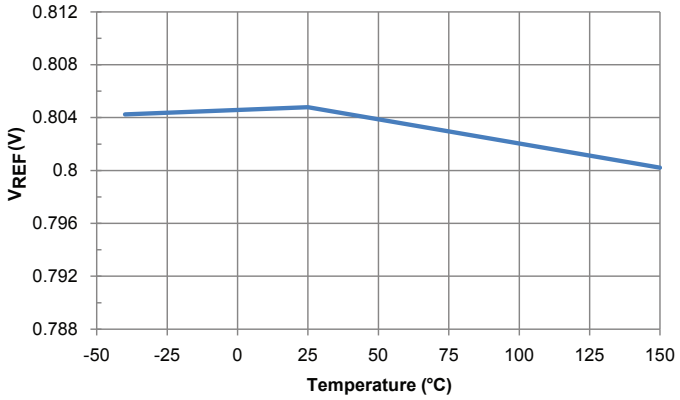
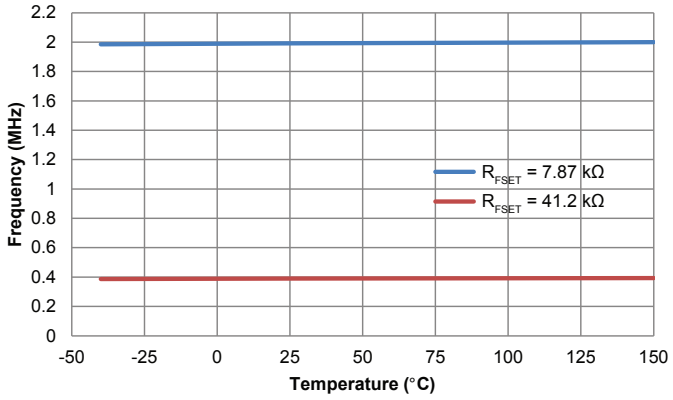
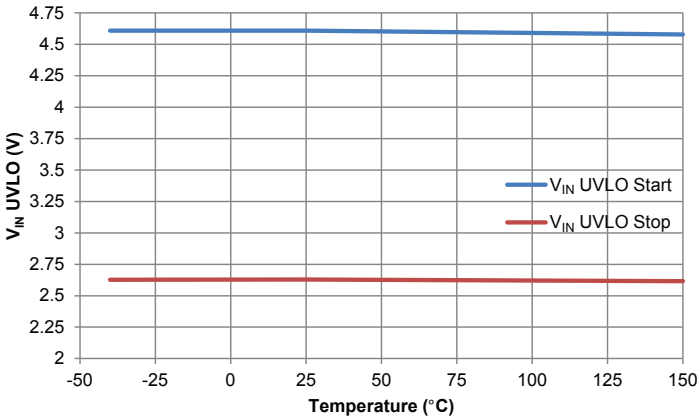
TYPICAL PERFORMANCE CHARACTERISTICS



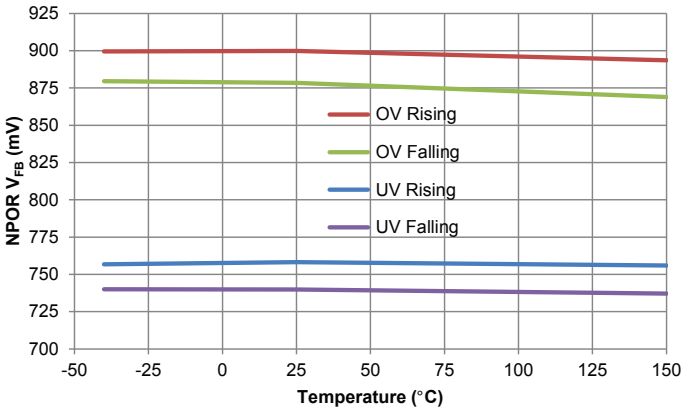
Reference Voltage versus Temperature



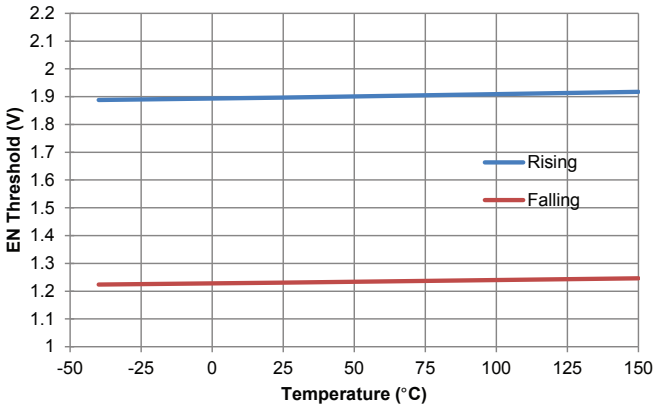
Switching Frequency f_{OSC} versus Temperature



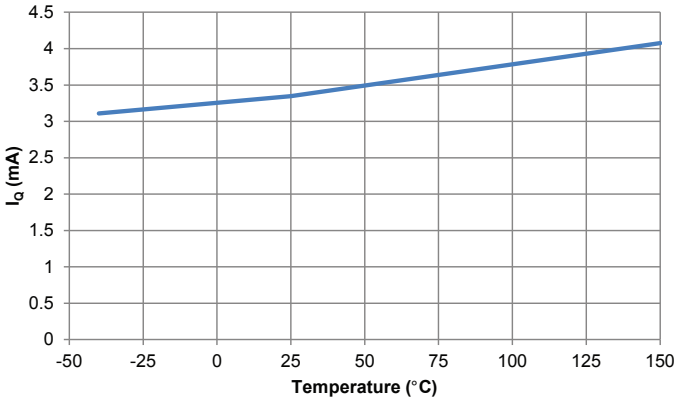
VIN UVLO START and STOP Thresholds versus Temperature



NPOR V_{FB} Overvoltage and Undervoltage versus Temperature



EN Rising and Falling Threshold versus Temperature



Quiescent Current I_Q versus Temperature

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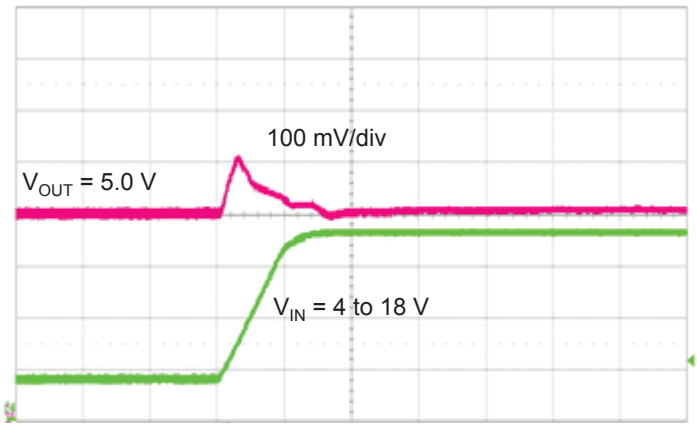
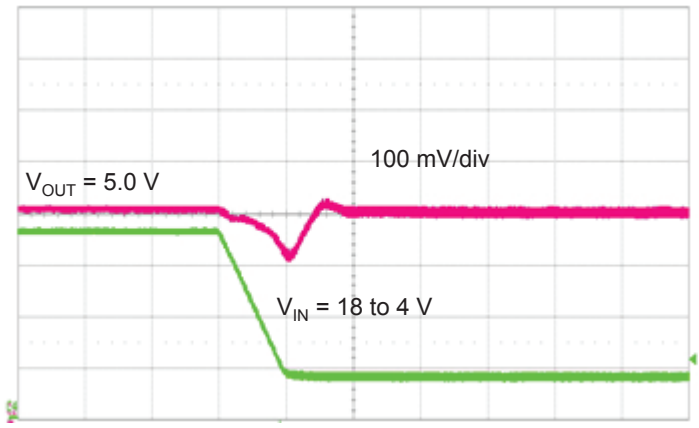
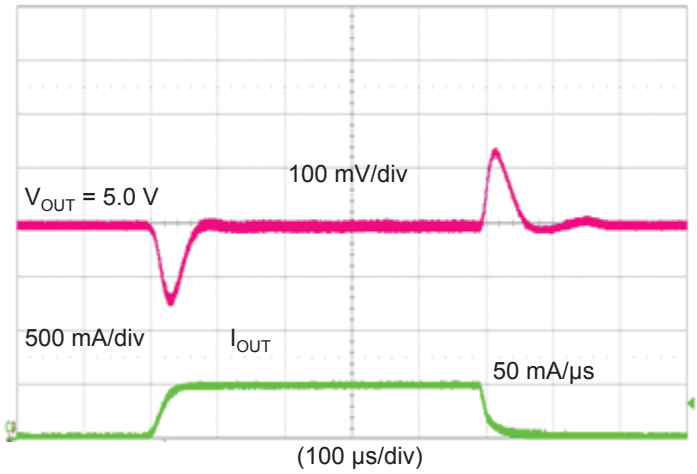


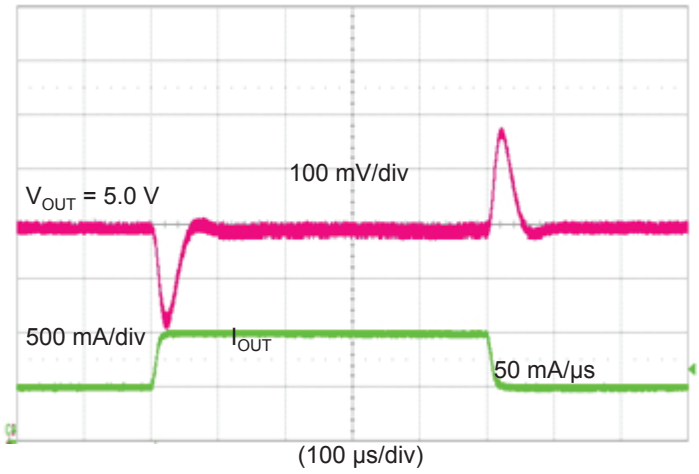
V_{IN} Transient Response: 4 to 18 V at 0.5 A Load for 5 V_{OUT}, 2 MHz design example



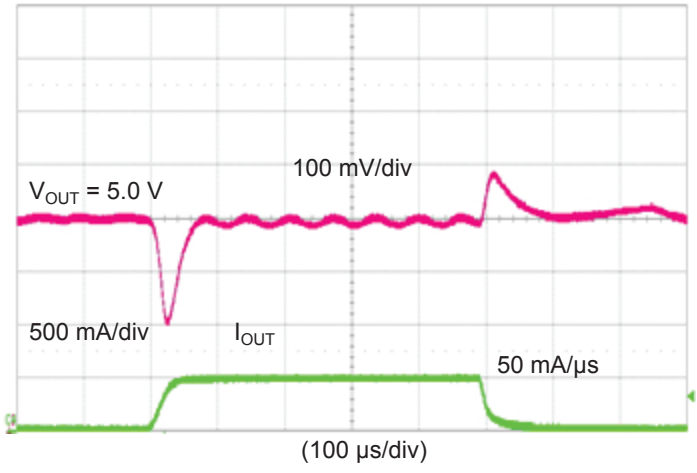
V_{IN} Transient Response: 18 to 4 V at 0.5 A Load for 5 V_{OUT}, 2 MHz design example



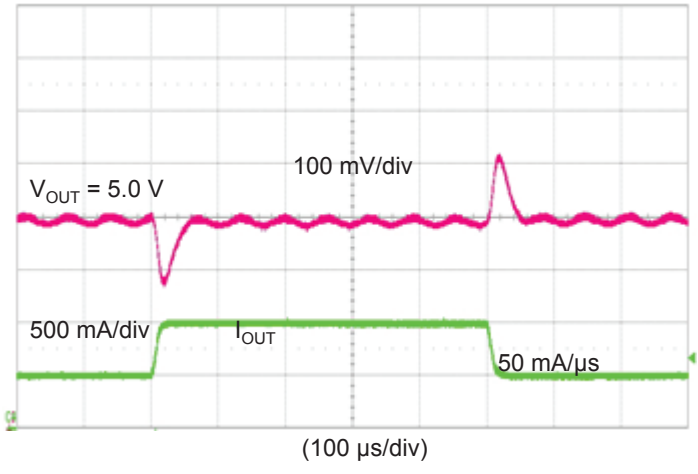
Transient Response 0 to 0.5 A Load Step at V_{IN} = 5 V for 5 V_{OUT}, 2 MHz design example



Transient Response 0.5 to 1 A Load Step at V_{IN} = 5 V for 5 V_{OUT}, 2 MHz design example



Transient Response 0 to 0.5 A Load Step at V_{IN} = 12 V for 5 V_{OUT}, 2 MHz design example



Transient Response 0.5 to 1 A Load Step at V_{IN} = 12 V for 5 V_{OUT}, 2 MHz design example

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FUNCTIONAL DESCRIPTION

Overview

The A4450 features all the necessary functions to implement an efficient buck or buck-boost regulation to convert automobile battery voltage into a tightly regulated voltage. The regulator can smoothly switch between Buck mode operation and Buck-Boost mode operation, allowing the operation with input voltage greater than or less than the output voltage. The A4450 integrates low R_{DSON} high-side N-MOSFET as a controlled buck switch. The A4450 provides a gate driver output for the external boost switch. As shown in Figure 1, the configuration of typical buck-boost regulator consists of an external freewheeling Schottky diode dictated as buck diode, another Schottky diode dictated as boost diode, an external MOSFET as boost switch, inductor, and output capacitor. The A4450 can provide regulated output up to 2 A DC load. The A4450 employs peak current-mode control to provide superior line and load regulation, pulse-by-pulse current limit, fast transient response, and simple compensation.

The A4450 features include a transconductance error amplifier for external compensation network, an enable input (EN), externally set soft-start time, a SYNC/FSET input to set PWM switching frequency or synchronize to external clock, an output voltage range set pin (RNG), a Power-On Reset output (NPOR) pin, and frequency dithering. Protection features of the A4450 include V_{IN} undervoltage lockout, pulse-by-pulse overcurrent protections in Buck-Boost and Buck modes, BOOT capacitor protection, two levels output overvoltage protection, hiccup mode short-circuit protection, LX short-circuit protection, missing buck diode protection, and thermal shutdown. In addition, the A4450 provides open-circuit, adjacent pin short-circuit, and pin-to-ground short-circuit protection at every pin.

The A4450 is available in industry-standard QFN-20 package.

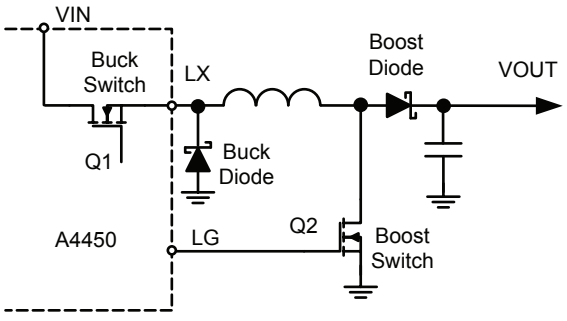

Figure 1: Basic Buck-Boost Regulator Configuration

Operation Modes

A buck-boost regulator can regulate the output voltage with input voltage greater than or less than the output voltage. However, the buck-boost regulator is not as efficient as the buck regulator. The A4450 is designed as a dual mode controller to resolve this challenge so that the regulator can operate efficiently under the Buck mode when the input voltage is greater than the output voltage. Figure 1 shows the basic buck-boost regulator configuration with dual mode controller A4450.

BUCK MODE

In case the input voltage is high compared to the output voltage, the regulator will enter Buck mode: buck switch Q1 turns on and off with duty cycle, D_{Buck}, to maintain regulation while boost switch Q2 is off, according to the following equation:

$$V_{OUT} = D_{Buck} \times V_{IN} \quad (1)$$

where D_{Buck} is the duty cycle of buck switch.

BUCK-BOOST MODE

When the input voltage decreases toward to the output voltage, the duty cycle of the buck switch Q1 will increase to maintain regulation. At the same time, once the programmed boost switch duty cycle, D_{Boost} (shown in the equation below), is greater than 0, the boost switch starts to turn on and off with duty cycle D_{Boost}. The regulator then enters Buck-Boost mode.

The boost switch duty cycle is determined by the equation below:

$$D_{Boost} = max\left(0,1 - \frac{V_{IN} \times 1.844}{R_{NG}}\right) \quad (2)$$

where V_{IN} is in Volts (V) and R_{NG} (kΩ) is the resistor connected between RNG pin and GND.

The Range resistor RNG (kΩ) programs the targeted output voltage, V_{OUT}, following the equation below:

$$R_{NG} = \frac{V_{OUT}(V) \times 1.844}{D_{BUCK0}} \quad (3)$$

where D_{BUCK0} is the preferred buck duty cycle at the instant that the boost switch starts to switch, typically set between 0.60 and 0.65.

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Under the Buck-Boost mode operation, the buck switch duty cycle, D_{Buck}, is controlled through the feedback network to regulate V_{OUT}, as shown in the equation below:

$$V_{OUT} = D_{Buck} / (1 - D_{Boost}) \times V_{IN} \quad (4)$$

This dual mode controller of A4450 enables smooth transition between Buck and Buck-Boost mode over a wide range of input voltages to maintain the regulation of output voltages.

Take as an example, V_{OUT} = 5 V buck-boost regulator, setting D_{BUCK0} = 0.61 results in R_{NG} = 15 kΩ from equation 4. As shown in Figure 2, when V_{IN} is greater than ~8.5 V, the regulator is in Buck mode and the duty cycle of Boost switch is 0; when V_{IN} is less than ~8.5 V, the regulator enters is in Buck-Boost mode with both switches turning on and off. It is recommended that the duty cycle of the buck switch should be larger than that of the boost switch for efficient operation.

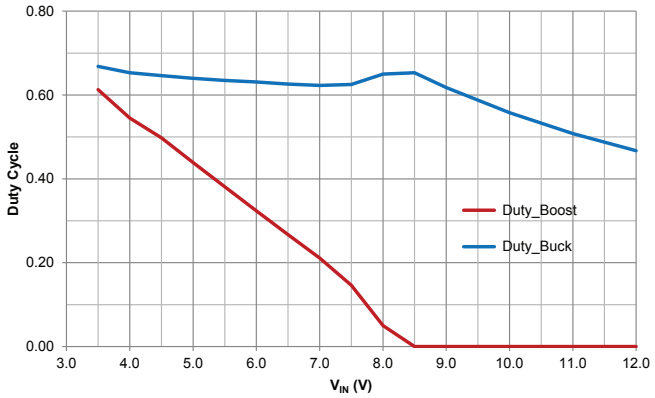

Figure 2: Duty Cycles of Boost and Buck Switches vs V_{IN} for example above with V_{OUT} = 5 V, R_{NG} = 15 kΩ

Reference Voltage

The A4450 incorporates an internal precision reference at 0.8 V (V_{REF}) as the reference of the output voltage feedback divider. The output voltage of the regulator is then programmed with a resistor divider between V_{OUT} and the FB pin of the A4450. After V_{OUT} is set, R_{NG} resistor can be selected based on equation 3. The accuracy of the internal reference is ±1.5% across a –40°C to 150°C temperature range.

Oscillator/Switching Frequency and Synchronization

The PWM switching frequency of the A4450 is adjustable from 250 kHz to 2.2 MHz and has an accuracy of about ±10% over the operating temperature range. A resistor, R_{FSET}, connected from the FSET/SYNC pin to GND, sets the switching frequency. An FSET/SYNC resistor with ±1% tolerance is recommended. A graph of switching frequency versus FSET/SYNC resistor value is shown in the Component Selection section of this datasheet.

The FSET/SYNC pin can also be used as a synchronization input that accepts an external clock to switch the A4450 from 250 kHz to 2.4 MHz; the slope compensation will be scaled according to the applied synchronization frequency. When used as a synchronization input, the applied clock pulses must satisfy the pulse-width duty-cycle requirements shown in the Electrical Characteristics table of this datasheet.

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Frequency Dithering

The A4450 adopts a frequency dithering technique to help reduce EMI/EMC for demanding automotive applications. The A4450 implements the linear triangular dithering of the PWM frequency, spreading the energy above and below the base frequency set by R_{FSET}. A typical fixed-frequency PWM regulator will create distinct "spikes" of energy at f_{OSC}, and at higher frequency multiples of f_{OSC}. Conversely, the A4450 spreads the spectrum around f_{OSC}, thus creating a lower magnitude at any comparative frequency. Frequency dithering is disabled if FSET/SYNC pin is used for external synchronization.

Frequency dithering of A4450 only applies in Buck mode—there is no frequency dithering in Buck-Boost mode. Therefore, when V_{IN} rises from low level to be above the V_{IN} Dithering Start Threshold (see EC table), frequency dithering will be activated where the A4450 enters into Buck mode from Buck-Boost mode. This V_{IN} Dithering Start Threshold is approximately equal to R_{NG} (kΩ) / 1.844 V.

If V_{IN} continues to rise and exceeds the V_{IN} Dithering Stop Threshold at 18 V (typical), frequency dithering will be disabled. Then if V_{IN} starts to fall, frequency dithering will resume again when V_{IN} goes below 16.6 V (typical). When V_{IN} continues to drop below the V_{IN} Dithering Stop Threshold (V_{IN} falling) to trigger the Buck-Boost mode operation, then frequency dithering is disabled. The V_{IN} Dithering Stop Threshold is approximately equal to R_{NG} (kΩ) / 1.844 V.

Refer to Figure 3 and Figure 4 and the PWM Switching Frequency and Dithering specifications in Electrical Characteristics table.

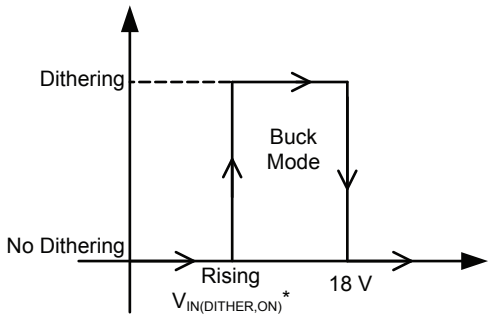

Figure 3: V_{IN} Rising Dithering Threshold

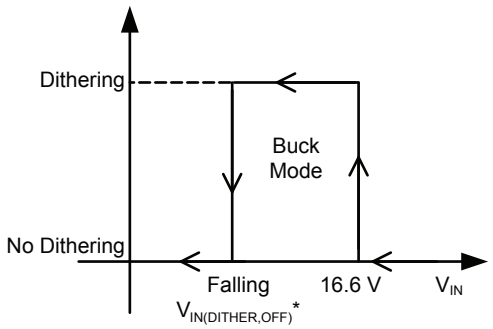

Figure 4: V_{IN} Falling Dithering Threshold, where threshold is adjustable following the equation R_{NG} (kΩ) / 1.844 (V)

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Transconductance Error Amplifier and Compensation Network

The transconductance error amplifier primary function is to control the regulator output voltage. It has three-terminal inputs with two positive inputs and one negative input (as shown in Figure 5). The negative input is connected to the FB pin to sense the feedback output voltage for regulation. The two positive inputs are used for soft-start and steady-state regulation. The error amplifier regulates to the lower value of those two positive inputs. The error amplifier regulates the FB voltage according to the soft-start voltage minus Soft-Start Offset during startup; when the soft-start voltage minus Soft-Start Offset exceeds the internal 0.8 V reference, the error amplifier then "switches over" and regulates the FB voltage to the 0.8 V reference voltage.

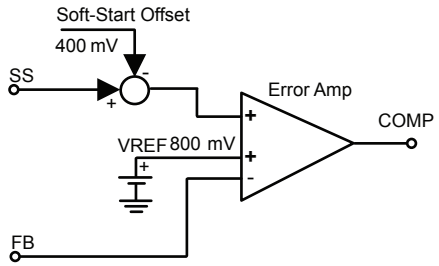

Figure 5: Error Amplifier

To stabilize the regulator, a series RC compensation network (R_Z and C_Z) must be connected from the error amplifier output (the COMP pin) to GND, as shown in the Typical Application Diagram. In most instances, an additional relatively low-value capacitor (C_P) should be connected in parallel with the R_Z-C_Z components to reduce the loop gain at very high frequencies. However, if the C_P capacitor is too large, the phase margin of the converter can be reduced. A general guideline about how to select R_Z, C_Z, and C_P is provided in the Component Selection section of this datasheet.

If a fault occurs or the regulator is disabled, the COMP pin is pulled to GND via approximately 4.5 kΩ and the switching is inhibited.

Slope Compensation

The A4450 incorporates internal slope compensation to allow PWM duty cycles above 50% for a wide range of input/output voltages, switching frequencies, and inductor values. The slope compensation signal of the A4450 is actually subtracted from COMP signal, equivalently being added into the current sense signal. The amount of slope compensation is scaled with the switching frequency when programming the frequency with a resistor or with an external clock.

The value of the output inductor should be chosen such that slope compensation rate, S_E, is theoretically at least greater than half the falling slope of the inductor current (S_F). Because the A4450 will work in the Buck-Boost mode, a larger compensation slope is preferred; refer to Output Inductor section for details.

Enable Input (EN)

An enable pin is available on the A4450. When this pin is low, the A4450 is shut down and enters a "sleep mode", where the internal control circuits will be shut off and draw less current from VIN. If EN goes high, the A4450 will turn on, and provided there are no fault conditions, soft-start will be initiated and V_{OUT} will ramp to its final voltage in a time set by the soft-start capacitor (C_{SS}). To automatically enable the A4450, the EN pin may be connected to VIN through a current-limiting resistor (1 ~10 kΩ). For transient suppression, it is recommended that a 0.1 to 0.22 µF capacitor is placed after the series resistor to form a low-pass filter before the EN pin. Larger external resistance is needed if EN signal rings below GND significantly.

Integrated Buck MOSFET

The A4450 integrates an 80 $m\Omega_{TYP}$ high-side N-channel MOSFET as the buck switch.

Current Sense Amplifier

The A4450 incorporates a high-bandwidth current sense amplifier to monitor the current through the high-side MOSFET. This current signal is used to regulate the peak current when the high-side MOSFET is turned on. The current signal is also used by the protection circuitry for the pulse-by-pulse current limit and hiccup mode short-circuit protection.

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Pulse-Width Modulation (PWM) Mode

The A4450 employs peak current-mode control to provide excellent load and line regulation, fast transient response, and simple compensation.

A high-speed comparator and control logic is included in the A4450. The inverting input of the PWM comparator is the subtraction of the slope compensation signal from the output of the error amplifier. The noninverting input is connected to the sum of the current sense signal, and a DC PWM Ramp offset voltage ($V_{PWMOFFS}$).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop and the high-side buck switch is turned on. When the voltage at the noninverting of the PWM comparator rises above the error amplifier output, COMP, the PWM flip-flop is reset and the high-side buck switch is turned off.

In the A4450, the duty cycle of the buck switch is controlled to regulate the output voltage, regardless of Buck-Boost or Buck mode. This makes control loop analysis easy, and facilitates the compensation to design a stable system without the right-half-plane zero introduced.

As illustrated in Figure 6, in Buck-Boost mode, both Q1 and Q2 are turned on at the beginning of each PWM cycle; Q2 operates with the programmed duty cycle, D_{Boost}:

$$D_{Boost} = 1 - \frac{V_{IN}(V) \times 1.844}{R_{NG}(k\Omega)} \quad (5)$$

and the buck switch Q1 is controlled by the PWM comparator to regulate the output voltage with the duty cycle, D_{Buck}:

$$D_{Buck} = (V_{OUT} / V_{IN}) \times (1 - D_{Boost}) \quad (6)$$

In Buck mode, the boost switch (Q2) is off and the buck switch (Q1) is active.

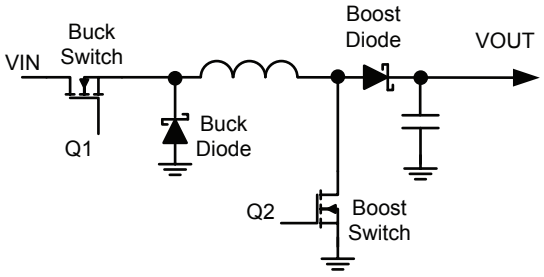

Figure 6: Buck-Boost Regulator

When V_{IN} rises above 18 V, the A4450 starts to linearly foldback the PWM switching frequency, f_{SW}, based on V_{IN}, from the original frequency, f_{SWO}, before foldback, up to about half f_{SWO} at 36 V. In this way, the on-time of the buck switch is relatively extended to ensure the duty cycle regulation is within control.

The test results illustrate the foldback behavior of switching frequency f_{SW} versus V_{IN}, in Figure 7 (where switching frequency f_{SW} is normalized to the original switching frequency f_{SWO} before foldback).

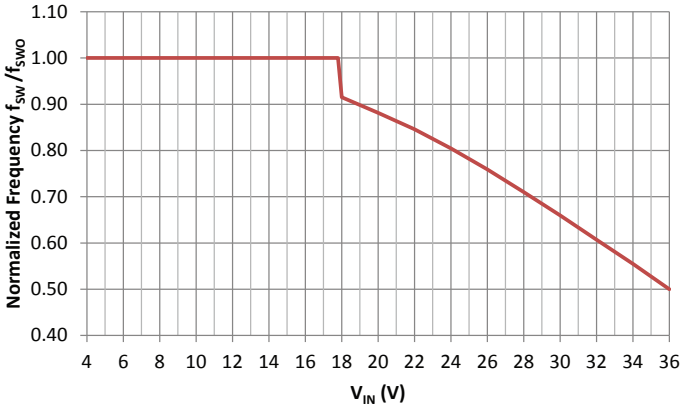

Figure 7: Normalized Switching Frequency f_{SW}/f_{SWO} Foldback vs. V_{IN}

BOOT Regulator

The A4450 includes an internal regulator to charge its boot capacitor. The voltage across the boot capacitor is typically 5 V, which provides voltage for the gate drivers of the buck switch and the boost switch. A 7 Ω bottom MOSFET is also integrated, which is turned on during minimum off-time to help ensure the boot capacitor is always charged. When V_{IN} is below 5 V, to ensure sufficient gate voltage, it is recommended to add an external boot diode, which is connected to a 5 V supply, as shown in Figure 8.

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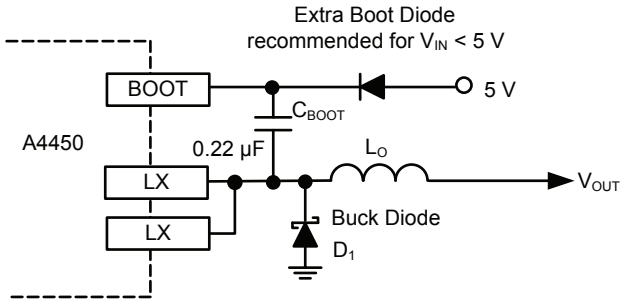

Figure 8: Extra Boot Diode Suggested for V_{IN} < 5 V

If the boot capacitor is missing or shorted, the A4450 will detect such a fault and enter hiccup mode. Also, the boot regulator has a current limit to protect itself during a short-circuit condition.

Soft-Start (Startup) and Inrush Current Control

The soft-start function controls the inrush current at startup. The soft-start pin, SS, is connected to GND via a capacitor. When the A4450 is enabled and all faults are cleared, the soft-start pin will source the charging current and the voltage on the soft-start capacitor C_{SS} will ramp upward from 0 V. When the voltage at the soft-start pin exceeds the Soft-Start Offset (typical 0.4 V), the error amplifier will ramp up its output voltage above the PWM Ramp Offset. At that instant, PWM switching begins.

Once the A4450 begins PWM switching, the error amplifier will regulate the voltage at the FB pin to the soft-start pin voltage minus the Soft-Start Offset. During the active portion of soft-start, the regulator output voltage will rise from 0 V to the targeted output voltage.

When the voltage of the soft-start pin minus the Soft-Start Offset is greater than 0.8 V, the error amplifier will start to regulate the voltage at the FB pin to the A4450 reference voltage, 800 mV. The voltage at the soft-start pin will continue to rise to the internal LDO regulator output voltage.

During normal startup, the PWM switching frequency is linearly scaled from 0.12 × f_{OSC} to f_{OSC} (depending on the FB voltage level) as the voltage at the FB pin ramps from 0 to 800 mV (see the details in the Electrical Characteristics table). Note if the theoretically scaled switching frequencies are less than 100 kHz, then 100 kHz frequency will take over. The scaled scheme is implemented to prevent the output inductor current from climbing to a level that may damage the A4450 regulator when the input voltage is high and the output of the regulator is either shorted or soft-starting a relatively high capacitance or very heavy load. However, during Overcurrent Protection or Hiccup mode, the soft-start PWM switching frequencies will become half of the corresponding linear foldback frequencies during normal startup.

If the A4450 is disabled or a fault occurs, the internal fault latch is set and the capacitor at the SS pin is discharged to ground very quickly through a 2 kΩ pull-down resistor. The A4450 will clear the internal fault latch when the voltage at the SS pin decays to approximately 200 mV. However, if the A4450 enters Hiccup mode, the capacitor at the SS pin is slowly discharged through 10 µA sink current. Therefore, the soft-start capacitor C_{SS} not only controls the startup time but also the time between soft-start attempts in Hiccup mode.

Pre-Biased Startup

If the output of the regulator is pre-biased at a certain output voltage level, the A4450 will modify the normal startup routine to prevent discharging the output capacitors. As described in the Soft-Start (Startup) and Inrush Current Control section, the error amplifier usually becomes active when the voltage at the soft-start pin exceeds the Soft-Start Offset. If the output is pre-biased, the voltage at the FB pin will be non-zero, the Boost diode blocks reverse current from the output, and the A4450 will not start switching until the voltage at SS pin minus the Soft-Start Offset rises to approximately V_{FB}. From then on, the error amplifier becomes active, the voltage at the COMP pin rises, PWM switching starts, and the output voltage will ramp upward from the pre-bias level.

Not Power-On Reset (NPOR) Output

The A4450 has an inverted Power-On Reset Output (NPOR) with a fixed delay of its rising edge (t_{dNPOR}). The NPOR output is an open-drain output, so an external pull-up resistor must be used, as shown in the Typical Application Diagram. NPOR transitions high when the output voltage, sensed at the FB pin, is within regulation.

The NPOR output is immediately pulled low if either a NPOR V_{FB} Overvoltage or Undervoltage condition occurs, or the A4450 junction temperature exceeds the thermal shutdown threshold (TSD). For other faults, NPOR depends on the output voltage.

At power-up, NPOR must be initialized (set to a logic low) when V_{IN} is relatively low. At power-down, NPOR must be held in the logic-low state as long as possible.

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Protection Features

The A4450 was designed to satisfy the most demanding automotive and nonautomotive applications. In this section, a description of protection features is provided.

UNDERVOLTAGE LOCKOUT PROTECTION (UVLO)

An Undervoltage Lockout (UVLO) comparator in the A4450 monitors V_{IN} at the VIN pin and keeps the regulator disabled either if the voltage is below the start threshold, $V_{INSTART}$, while V_{IN} is rising, or if V_{IN} is below the stop threshold, V_{INSTOP}, while V_{IN} is falling in Buck-Boost mode. The UVLO comparator incorporates some hysteresis to help reduce on/off cycling of the regulator due to the resistive or inductive drops in the VIN path during heavy loading or during startup.

OVERCURRENT PROTECTION (OCP)

The A4450 monitors the current through the high-side MOSFET. If this current exceeds the LX Short-Circuit Current Limit, $I_{LIM(LX)}$, for example when LX is hard short to ground (note: high V_{IN} triggers a hard short condition more easily than low V_{IN} case), the high-side MOSFET will be turned off and the regulator stays in the latched-off status unless the regulator is reset. If this current is less than $I_{LIM(LX)}$ but above the pulse-by-pulse current limit $I_{LIM(Buck)}$ while in Buck mode or $I_{LIM(BuckBoost)}$ while in Buck-Boost mode, the A4450 will enter into Hiccup mode. The A4450 includes leading-edge blanking to prevent false triggering the overcurrent protection when the high-side MOSFET is turned on.

An OCP (Overcurrent Pulses) counter and hiccup mode circuit are incorporated to protect the A4450 regulator when the output of the regulator is shorted to ground or when the load current is too high.

If V_{FB} is less than 400 mV_{TYP}, the number of overcurrent pulses is limited to 30; If V_{FB} is greater than 400 mV_{TYP}, the number of overcurrent pulses is increased to 120 to accommodate the possibility of starting into a relatively high output capacitance.

If the OCP counter reaches the preset counts, a hiccup latch is set and the COMP pin is quickly pulled down by a relatively low resistance.

The hiccup latch also enables a small current sink connected to the SS pin. This causes the voltage at the soft-start pin to slowly ramp downward. When the voltage at the soft-start pin decays to a preset low level, the hiccup latch is cleared and the small current sink is turned off. At that instant, the SS pin will begin to source current and the voltage at the SS pin will ramp upward. This marks the beginning of a new, normal soft-start cycle. When the voltage at the soft-start pin exceeds the Soft-Start Offset, the error amplifier will force the voltage at the COMP pin to quickly slew upward and PWM switching will resume. But the PWM switching frequencies during the Hiccup SS upward period are half of the SS PWM Foldback Frequency listed in Electrical Characteristics table. Figure 9 below shows the Overcurrent Hiccup operation.

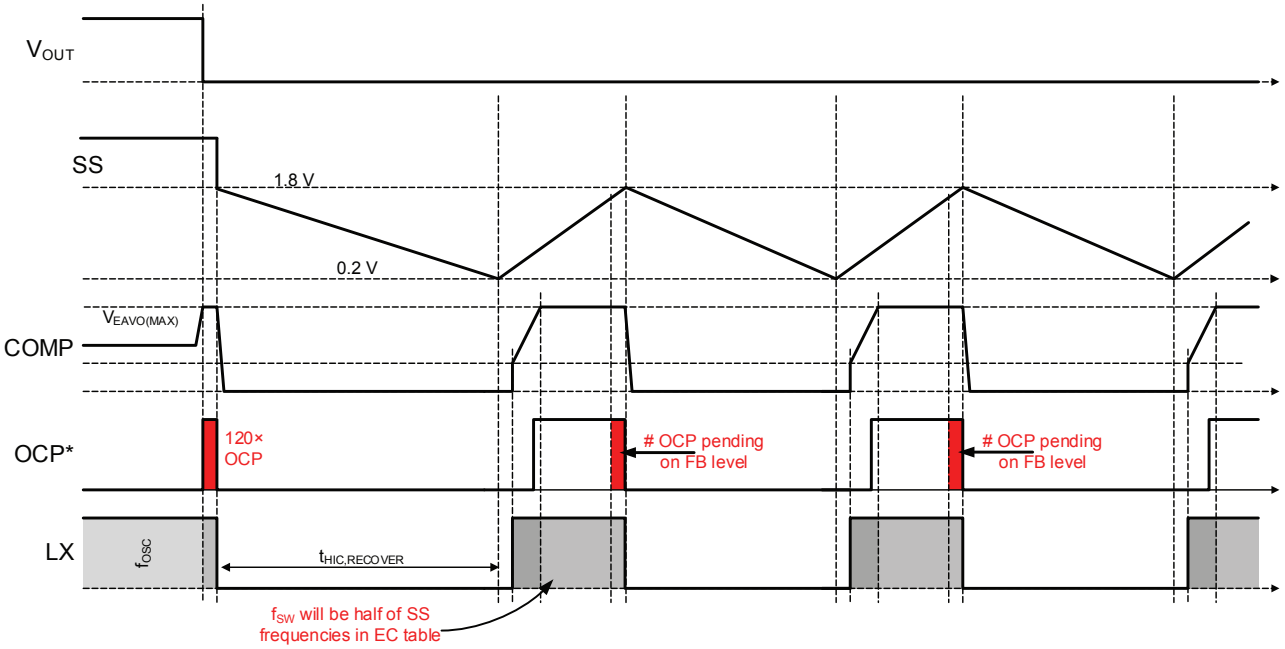

Figure 9: Output Short Circuit to Ground Hiccup Operation

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If the short circuit at the regulator output remains, another hiccup cycle will occur. Hiccups will repeat until the short circuit is removed or the converter is disabled. If the short circuit is removed, the A4450 will soft-start normally and the output voltage will automatically recover to the desired level.

Thus, Hiccup mode is very effective protection for the overload condition. It can avoid false trigger for a short-term overload. For the extended overload, the average power dissipation during Hiccup operation is very low to keep the controller cool and enhance reliability.

BOOT CAPACITOR PROTECTION

The A4450 monitors the voltage across the boot capacitor to detect if the capacitor is missing or short-circuited. If the boot capacitor is missing, the regulator will enter hiccup mode after approximately 14 PWM cycles. If the boot capacitor is shorted to GND, Boot Undervoltage protection will be triggered and the regulator will enter Hiccup mode after about 32 PWM cycles.

For a boot fault, hiccup mode will operate virtually the same as described previously for an output short-circuit fault (OCP), with SS ramping up and down as a timer to initiate repeated soft-start attempts. Boot faults are non-latched conditions, so the A4450 will automatically recover when the fault is corrected.

PROTECTION OF BUCK DIODE AT LX NODE

If the buck diode at LX node is missing or damaged (open), the LX node will be subject to unusually high negative voltages. These negative voltages may cause the A4450 to malfunction and could lead to damage. When the buck diode is missing, the internal ESD diode will carry most of the freewheeling current and will cause thermal shutdown. Also, if this diode is shorted, which is hard short of LX to ground, as described in Overcurrent Protection section, the high-side MOSFET will be turned off and the regulator will stay in latched-off status unless the regulator is reset.

OVERVOLTAGE PROTECTION (OVP)

The A4450 includes two levels of overvoltage comparators that monitor the FB pin voltage, V_{FB}. When rising V_{FB} first exceeds 840 mV (typical, i.e., V_{FBOV}, 105% of 800 mV V_{REF}), the high-side buck switch turns off and the boost gate driver LG turns high, but NPOR still remains high. In this way, the further buildup of output current is inhibited so that it cannot charge the output capacitors further. If V_{FB} keeps rising and exceeds the second overvoltage threshold ($V_{FBNPOROV(H)}$, 110% of V_{REF}), NPOR will be pulled low, the high-side buck switch remains off, and the boost gate driver LG remains high. If the duration of the overvoltage condition is less than OV Deglitch Times, $t_{dOV(FILT)}$ (30 μs_{TYP}), no OV protection event is triggered. When V_{FB} drops below NPOR V_{FB} UV Thresholds specified in Electrical Characteristics table, an NPOR Undervoltage fault is triggered and NPOR will be pulled low.

The error amplifier and its regulation voltage clamp are not effective when the FB pin is disconnected. When the FB pin is disconnected from the feedback resistor divider, a tiny internal current source will force the voltage at the FB pin to rise above the OV threshold and disables the regulator, preventing the load from being significantly over voltage. If the conditions causing the overvoltage are corrected, the regulator will automatically recover.

Figure 10 below shows a timing diagram of UV/OV conditions with respect to NPOR (refer to Electrical Characteristics table).

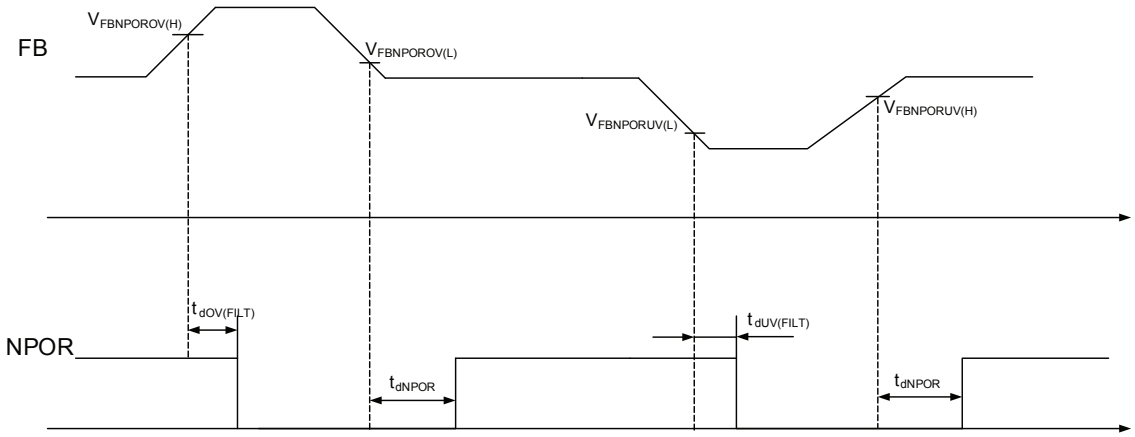

Figure 10: UV/OV Delay Timing Diagram (not scaled)

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THERMAL SHUTDOWN (TSD)

The A4450 protects itself from overheating by monitoring its junction temperature. If the junction temperature exceeds the Thermal Shutdown Threshold (T_{TSD}, 170°C_{TYP}), the A4450 will stop PWM switching and pull NPOR low. TSD is a non-latched fault, so the A4450 will automatically recover if the junction temperature decreases by approximately 20°C from T_{TSD}.

PIN-TO-GROUNDANDPIN-TO-PINSHORTPROTECTIONS

The A4450 was designed to satisfy the most demanding automotive and nonautomotive applications. For example, the A4450 was carefully designed “up front” to withstand a short circuit to ground at each pin without suffering damage.

In addition, care was taken when defining the A4450’s pinout to optimize protection against pin-to-pin adjacent short circuits. For example, logic pins and high-voltage pins were separated as much as possible. Inevitably, some low-voltage pins were located adjacent to high-voltage pins. In these instances, the low-voltage pins were designed to withstand increased voltages, with clamps and/or series input resistance, to prevent damage to the A4450.

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DESIGN AND COMPONENT SELECTION

Setting the Output Voltage

The output voltage of the regulator is determined by a resistor divider from the output node (V_{OUT}) to the FB pin as shown in Figure 11. There are tradeoffs when choosing the value of the feedback resistors. If the series combination (R_{FB1} + R_{FB2}) is too low, then the light load efficiency of the regulator will be reduced. To maximize efficiency, it's best to choose higher values of resistors. If the parallel combination (R_{FB1}//R_{FB2}) is too high, then the regulator may be susceptible to noise coupling onto the FB pin. 1% resistors are recommended to maintain the output voltage accuracy.

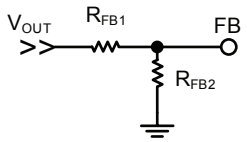

Figure 11: Connecting a Feedback Divider to Set the Output Voltage

The feedback resistors must satisfy the ratio shown in equation below to produce a desired output voltage, V_{OUT}.

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT}}{0.8\ V} - 1 \qquad (7)$$

After the output voltage is set, the range resistor R_{NG} (kΩ) at RNG pin can be calculated from equation 3 found under Operation Modes in the Functional Description section, repeated below:

$$R_{NG} = \frac{V_{OUT}(V) \times 1.844}{D_{BUCK0}}$$

where D_{BUCK0} is the preferred buck duty cycle at the instant when the boost switch starts to switch, typically set at around 0.6 to 0.65.

PWM Switching Frequency (f_{SW}, R_{FSET})

The desired switching frequency (f_{SW}) can be set with a resistor R_{FSET} connected at pin FSET/SYNC to the ground. The recommended R_{FSET} value for various switching frequencies f_{SW} can be obtained from either Table 1 or Figure 12:

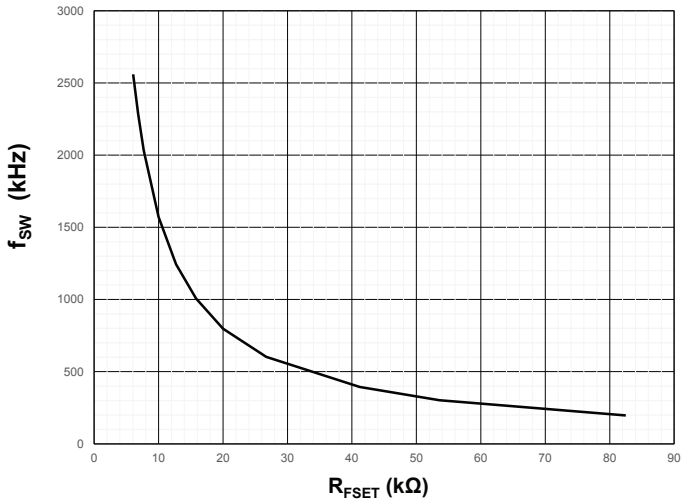

Figure 12: PWM Switching Frequency f_{SW} versus R_{FSET}

Table 1: f_{SW} versus R_{FSET}

f_{SW} (kHz)	R_{FSET} (kΩ)
2500	6.04
2300	6.81
2000	7.87
1500	10.0
1250	12.7
1000	15.8
800	20.0
600	26.7
400	41.2
300	53.6

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Output Inductor (L_O)

For the peak current-mode control, the priority to consider when selecting the inductor is to prevent the subharmonic oscillations when the duty cycle is near or above 50%. To prevent the subharmonic oscillations, the theoretical slope compensation ramp S_E should be at least 50% of the down slope of the inductor current. In the A4450, the inductor value L_O is suggested to start with the equation below, because A4450 will also operate in Buck-Boost mode:

$$L_O \geq 1.5 \times max\left(\frac{V_{OUT} - V_{IN(MIN)}}{S_E}, \frac{0.5 \times V_{OUT}}{S_E}\right) \quad (8)$$

where V_{OUT} is the output voltage, $V_{IN(MIN)}$ is the minimum input voltage, S_E is in A/µs, which scales with the switching frequency and can be estimated by interpolating from Electrical Characteristics table, and L_O is in µH.

Ideally, the inductor should not saturate at the highest pulse-by-pulse current limit. This may be too costly. At the very least, the inductor should not saturate at the peak operating current.

In Buck-Boost mode, the peak inductor current is calculated as:

$$I_{PEAK} = \frac{I_{OUT} + \frac{\Delta I_L}{2} \times (1 - D_{Buck})}{1 - D_{BOOST(MAX)}} \quad (9)$$

where

$$\Delta I_L = max\left\{\frac{V_{IN(MIN)} \times D_{Boost(MAX)}}{f_{SW} \times L_O}, \frac{V_{IN(MIN)} \times D_{Boost(MAX)}}{f_{SW} \times L_O} + \frac{V_{IN(MIN)} - V_{OUT}}{f_{SW} \times L_O} \times (D_{Buck} - D_{Boost(MAX)})\right\}$$

$$D_{Boost(MAX)} = 1 - \frac{V_{IN(MIN)} \times 1.844}{R_{NG}}$$

$$D_{Buck(MAX)} = (1 - D_{Boost(MAX)}) \times \frac{V_{OUT}}{V_{IN(MIN)}}$$

In Buck mode, the peak inductor current is:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (10)$$

where

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L_O}$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure neither the inductor nor the regulator are damaged when the output is shorted to ground at the highest expected ambient temperature.

Buck Diode (D_1) and Boost Diode (D_2)

Schottky diodes with proper ratings should be chosen for the buck diode (D_1) and boost diode (D_2), because of their low forward voltage drop and fast reverse recovery time. The key parameters in D_1 and D_2 selection are the average forward current $I_{f(AVG)}$ and the DC reverse voltage.

The boost diode D_2 should be greater than V_{OUT} with some margin. The average forward current rating of the boost diode should be above the full load current, and the peak current should be above the peak inductor current which is calculated in previous Output Inductor section.

The buck diode D_1 must be able to withstand the input voltage when the high-side buck switch is on. Therefore, the reverse voltage rating should be greater than the maximum expected V_{IN} with some margin.

When the buck switch is off, the buck diode D_1 must conduct the output current. The average forward current rating of the buck diode should be above the full load current.

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External Boost Switch

The A4450 requires a N-channel MOSFET as the external boost switch to form the buck-boost configuration. A suitable boost switch should have low gate charge, small on-resistance, break-down voltage greater than V_{OUT}, and maximum gate driver voltage greater than 8 V. The maximum current $I_{DS(MAX)}$ should be larger than the peak inductor current calculated in Output Inductor section. STL10N3LLH5 from STMicroelectronics and NVTFS4823N from ON Semiconductor are good examples. A 10 $k\Omega_{TYP}$ resistor must be added at LG pin to ground to avoid false turn-on from coupling noise.

Output Capacitors

In Buck-Boost mode, the output capacitors must supply the entire output current when the boost switch is on. The output capacitors are chosen based on the Buck-Boost mode instead of the Buck mode where the demand is much less when the application runs through both operation modes.

The output capacitance in Buck-Boost mode is selected to limit the output voltage ripple to meet the specification requirement, and is calculated according to the equation below for the given output ripple voltage ΔV_{OUT}:

$$C_{OUT(MIN)} = \frac{I_{OUT} \times D_{Boost(MAX)}}{f_{SW} \times \Delta V_{OUT}} \quad (11)$$

where

$$D_{Boost(MAX)} = 1 - \frac{V_{IN(MIN)}\,(V) \times 1.844}{R_{NG}\,(k\Omega)}$$

The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

In Buck-Boost mode, the output voltage ripple (ΔV_{OUT}) is mainly due to the voltage drop across the ESR of output capacitors, ESR_{CO}, and the ESR requirements can be obtained from:

$$ESR_{CO} = \frac{\Delta V_{OUT}}{I_{OUT}} \quad (12)$$

The ESR requirement can usually be met by simply using multiple capacitors in parallel or by using higher quality capacitors. Ceramic capacitors have good ESR characteristics and are good choices for output capacitors. It should be noted that the effective capacitance of the ceramic capacitors decreases due to the DC bias effect.

For larger bulk values of capacitance, a high quality low ESR electrolytic output capacitor can be used; however, electrolytic capacitors have poor tolerance, especially over temperature. The ESR of electrolytic capacitors usually increases significantly at cold ambients, as much as 10×, which increases the output voltage ripple and, in most cases, reduces the stability of the system.

The transient response of the regulator depends on the number and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. At the instant of a fast load transient (di/dt), the output voltage will change by the amount:

$$\Delta V_{OUT} = \Delta I_{LOAD} \times ESR_{CO} + di/dt \times ESL_{CO} \quad (13)$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and the output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, with a higher bandwidth system it may be more difficult to obtain acceptable gain and phase margins.

Input Capacitors

Selection of input capacitors should meet these three requirements: first, they must support the maximum expected input surge voltage with adequate design margin; second, the capacitor's RMS current rating must be higher than the expected RMS input current to the regulator; third, they must have enough capacitance and a low enough ESR to limit the input voltage deviation to something much less than the VIN UVLO hysteresis at maximum loading and minimum input voltage.

The RMS current of the input capacitors depends on the operation mode. During the Buck mode, the input capacitors must deliver the RMS current according to:

$$I_{RMS} = I_{OUT} \times \sqrt{D_{Buck} \times (1 - D_{Buck})} \quad (14)$$

where D_{Buck} is the duty cycle of Buck switch.

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The $D_{Buck} \times (1 - D_{Buck})$ term in equation 14 above has an absolute maximum value of 0.25 at 50% duty cycle.

During Buck-Boost mode, the RMS current of input capacitors is:

$$I_{RMS} = \frac{I_{OUT}}{1 - D_{Boost}} \times \sqrt{D_{Buck} \times (1 - D_{Buck})} \quad (15)$$

Thus, the RMS currents of both operation modes should be checked to ensure the input capacitors are able to handle the larger ripple current of the two.

The input capacitor(s) must limit the voltage deviations at the VIN pin to a value significantly less than UVLO hysteresis during maximum load and minimum input voltage. For Buck operation mode, the minimum input capacitance can be calculated as follows:

$$C_{IN} \geq \frac{I_{OUT} \times D_{Buck} \times (1 - D_{Buck})}{0.85 \times f_{SW} \times \Delta V_{IN(MIN)}} \quad (16)$$

For Buck-Boost mode, the required minimum input capacitance becomes:

$$C_{IN} \geq \frac{I_{OUT} \times D_{Buck} \times (1 - D_{Buck})}{(1 - D_{Boost}) \times 0.85 \times f_{SW} \times \Delta V_{IN(MIN)}} \quad (17)$$

where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the VIN UVLO comparator ($\Delta V_{IN(MIN)} \leq 150$ mV is recommended), and f_{SW} is the nominal PWM frequency.

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction) so these types should be avoided. The X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size (i.e., 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in voltage rating to accommodate the worst-case transient input voltage (such as a load dump as high as 40 V for automotive applications).

Bootstrap Capacitor

A bootstrap capacitor must be connected between the BOOT and LX pins to provide the gate drives for the buck and boost switches. A 220 nF, 50 V, X7R ceramic capacitor is recommended in A4450 applications.

Soft-Start and Hiccup Mode Timing (C_{SS})

The soft-start time of the A4450 is determined by the value of the capacitance at the soft-start pin, C_{SS}.

When the A4450 is enabled, the voltage at the soft-start pin will start from 0 V and will be charged by the soft start current, I_{SSSU}. However, PWM switching will not begin instantly because the voltage at the soft-start pin must rise above 400 mV (Soft-Start Offset). The soft-start delay ($t_{SS(DELAY)}$) can be calculated using equation 18:

$$t_{SS(DELAY)} = C_{SS} \times \left(\frac{400\ mV}{I_{SS(SU)}}\right) \quad (18)$$

If the A4450 is starting with a very heavy load, a very fast soft-start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. This occurs because the sum of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors ($I_{CO} = C_{OUT} \times V_{OUT}/t_{SS}$) is higher than the pulse-by-pulse current threshold.

To avoid prematurely triggering the pulse-by-pulse current limit, a larger soft-start capacitance can be used. The soft-start capacitor, C_{SS}, should be calculated according to equation 19:

$$C_{SS} \geq \frac{I_{SS(SU)} \times V_{OUT} \times C_{OUT}}{0.8\ V \times I_{CO}} \quad (19)$$

where V_{OUT} is the output voltage, C_{OUT} is the output capacitance, I_{CO} is the amount of current allowed to charge the output capacitance during soft-start (recommend 0.1 A < I_{CO} < 1 A). Higher values of I_{CO} result in faster soft-start times. However, lower values of I_{CO} ensure that hiccup mode is not falsely triggered. It is recommended to start the design with an I_{CO} of 0.1 A and to increase I_{CO} only if the soft-start time is too slow.

The output voltage ramp time, t_{SS}, can be calculated by using either of the following methods:

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$$t_{SS} = V_{OUT} \times \frac{C_{OUT}}{I_{CO}} \text{ or } 0.8\ V \times \frac{C_{SS}}{I_{SS(SU)}} \qquad (20)$$

When the A4450 is in hiccup mode, the soft-start capacitor is used as a timing capacitor and sets the hiccup period. The soft-start pin charges the soft-start capacitor with $I_{SS(SU)}$ during a startup attempt and discharges the same capacitor with smaller current than $I_{SS(SU)}$ between startup attempts. Therefore, the effective duty cycle will be very low and the junction temperature will be kept low.

Compensation Components (R_Z, C_Z, C_P)

To compensate the system, it is important to understand the overall control loop response in frequency domain. The A4450 simplified control loop, consisting of power stage and transconductance error amplifier, is shown in Figure 13 for compensation analysis. The error amplifier uses a Type II compensation network to ensure system stability and to optimize transient response with desirable phase margin and gain margin.

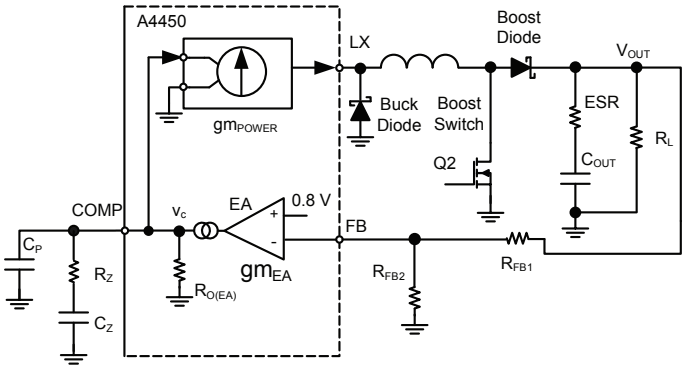

Figure 13: Simplified Overall Current-Mode Control Loop

Figure 14 is a simplified small signal model of the A4450 power stage. The power stage is approximated as a voltage-controlled current source to provide current to the load and output capacitor. Because the duty cycle of boost switch Q2 is programmed with R_{NG} resistor at pin RNG and the inductor provides current to the output only during off-time of Q2, the transconductance of the voltage-controlled current source is expressed as $(1 - D_{Boost}) \times gm_{POWER}$.

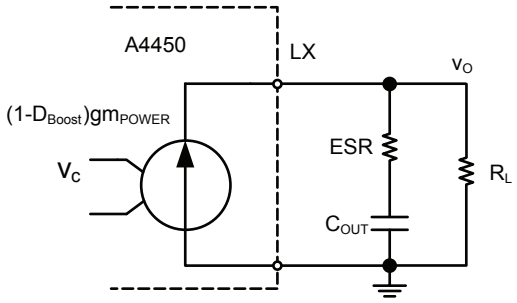

Figure 14: Simplified Small Signal Model of A4450 Power Stage

where gm_{POWER} is COMP to LX Current Gain (see Electrical Characteristics table), i.e. the transconductance of power stage; D_{Boost} is the duty cycle of boost switch,

$$D_{Boost} = \begin{cases} 0, & \text{in Buck mode} \\ 1 - \dfrac{V_{IN(MIN)}\ (V) \times 1.844}{R_{NG}\ (k\Omega)}, & \text{in Buck-Boost mode} \end{cases}$$

The control-to-output transfer function of the power stage is shown in equation 21 and consists of a DC gain, one dominant pole, and one ESR zero.

$$\frac{v_o}{v_c}\ \Big|\ power = G_{DC(power)} \times \frac{1 + \dfrac{s}{2\pi \times f_{ESR(z)}}}{1 + \dfrac{s}{2\pi \times f_{power(p)}}} \qquad (21)$$

where

$G_{DC(power)}$ is the DC gain of the power stage,

$G_{DC(power)} = (1 - D_{Boost}) \times gm_{POWER} \times R_L$,

$f_{ESR(z)}$ is the ESR zero of the power stage,

$$f_{ESR(z)} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$f_{power(p)}$ is the dominant pole of the power stage,

$$f_{power(p)} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

R_L is the load resistance,

ESR is the equivalent series resistance of the output capacitor,

C_{OUT} is the output capacitance.

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For a design with very low-ESR-type output capacitors (i.e. ceramic or OSCON output capacitors), the ESR zero is usually at a very high frequency, so it can be ignored. If the ESR zero falls below or near the 0 dB crossover frequency of the system (as is the case with electrolytic output capacitors), then it should be cancelled by the pole formed by the C_P capacitor and the R_Z resistor (identified and discussed later as $f_{EA(p2)}$).

The feedback loop includes a feedback output voltage divider (R_{FB1} and R_{FB2}), the error amplifier (gm_{EA}), and the compensation network (R_Z, C_Z, and C_P). The transfer function of the feedback can be derived and simplified if $R_{O(EA)} \gg R_Z$, and $C_Z \gg C_P$. In most cases, $R_{O(EA)} > 2$ MΩ, 1 kΩ < R_Z < 100 kΩ, 220 pF < C_Z < 47 nF, and C_P < 50 pF, so the following equations are very accurate:

$$\left|\frac{v_c}{v_o}\right|_{feedback} = G_{DC(EA)} \times \frac{1 + \frac{s}{2\pi \times f_{EA(z)}}}{\left(1 + \frac{s}{2\pi \times f_{EA(p1)}}\right)\left(1 + \frac{s}{2\pi \times f_{EA(p2)}}\right)} \quad (22)$$

where

$G_{DC(EA)}$ is the DC gain of the feedback loop,

$$G_{DC(EA)} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times gm_{EA} \times R_{O(EA)}$$

gm_{EA} is the error amplifier transconductance (see EC table),

$R_{O(EA)}$ is the output resistance of the error amplifier (the small output capacitance of the error amplifier is neglected), and

$$RO_{(EA)} = AVOL / gm_{EA}$$

AVOL is the error amplifier open-loop voltage gain (see EC table),

$f_{EA(z)}$ is the low-frequency zero of the error amplifier compensation network,

$$f_{EA(z)} = \frac{1}{2\pi \times R_Z \times C_Z}$$

$f_{EA(p1)}$ is the low-frequency pole of the error amplifier compensation network,

$$f_{EA(p1)} = \frac{1}{2\pi \times R_{O(EA)} \times C_Z}$$

$f_{EA(p2)}$ is the high-frequency pole of the error amplifier compensation network,

$$f_{EA(p2)} = \frac{1}{2\pi \times R_Z \times C_P}$$

Placing $f_{EA(z)}$ just above $f_{power(p)}$ will result in excellent phase margin, but relatively slow transient recovery time.

The sum of power stage control-to-output response equation 21 and the feedback loop response equation 22, including error amplifier, is the overall loop frequency response of the entire system. The goal of compensation design is to shape the transfer function of the overall loop to get a stable converter with the desired loop gain and phase margin.

A Generalized Tuning Procedure

1. Choose the system bandwidth, f_C, the frequency at which the magnitude of the gain will cross 0 dB. Recommended values for f_C are $f_{SW}/20 < f_C < f_{SW}/7.5$. A higher value of f_C will generally provide a better transient response, while a lower value of f_C will be easier to obtain higher gain and phase margins.
2. Calculate the R_Z resistor value to set the desired system bandwidth (f_C),

$$R_Z = f_C \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times \frac{2 \times \pi \times C_{OUT}}{gm_{POWER} \times gm_{EA}}$$

3. Calculate the dominant pole frequency of power stage ($f_{power(p)}$) formed by C_{OUT} and R_L.

$$f_{power(p)} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

4. Calculate a range of values for the C_Z capacitor and set the compensation zero below the one fourth of the crossover frequency f_C,

$$\frac{4}{2 \times \pi \times R_Z \times f_C} < C_Z < \frac{1}{2 \times \pi \times R_Z \times 1.5 \times f_{power(p)}}$$

To maximize system stability (i.e., have the most gain margin), use a higher value of C_Z. To optimize transient recovery time at the expense of some phase margin, use a lower value of C_Z.

5. Calculate the frequency of the ESR zero ($f_{ESR(z)}$) formed by the output capacitor(s).

$$f_{ESR(z)} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

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A. If $f_{ESR(z)}$ is at least 1 decade higher than the target crossover frequency (f_C), then $f_{ESR(z)}$ can be ignored. This is usually the case for a design using ceramic output capacitors. Use equation below to calculate the value of C_P by setting $f_{EA(p2)}$ to either $5 \times f_C$ or $f_{SW}/2$, whichever is higher.

$$f_{EA(p2)} = \frac{1}{2\pi \times R_Z \times C_P}$$

B. If $f_{ESR(z)}$ is near or below the target crossover frequency (f_C) then use equation above to calculate the value of C_P by setting $f_{EA(p2)}$ equal to $f_{ESR(z)}$. This is usually the case for a design using high ESR electrolytic output capacitors.

Typical design examples are provided for V_{OUT} = 5 V and V_{OUT} = 8 V with f_{SW} = 400 kHz and 2 MHz respectively.

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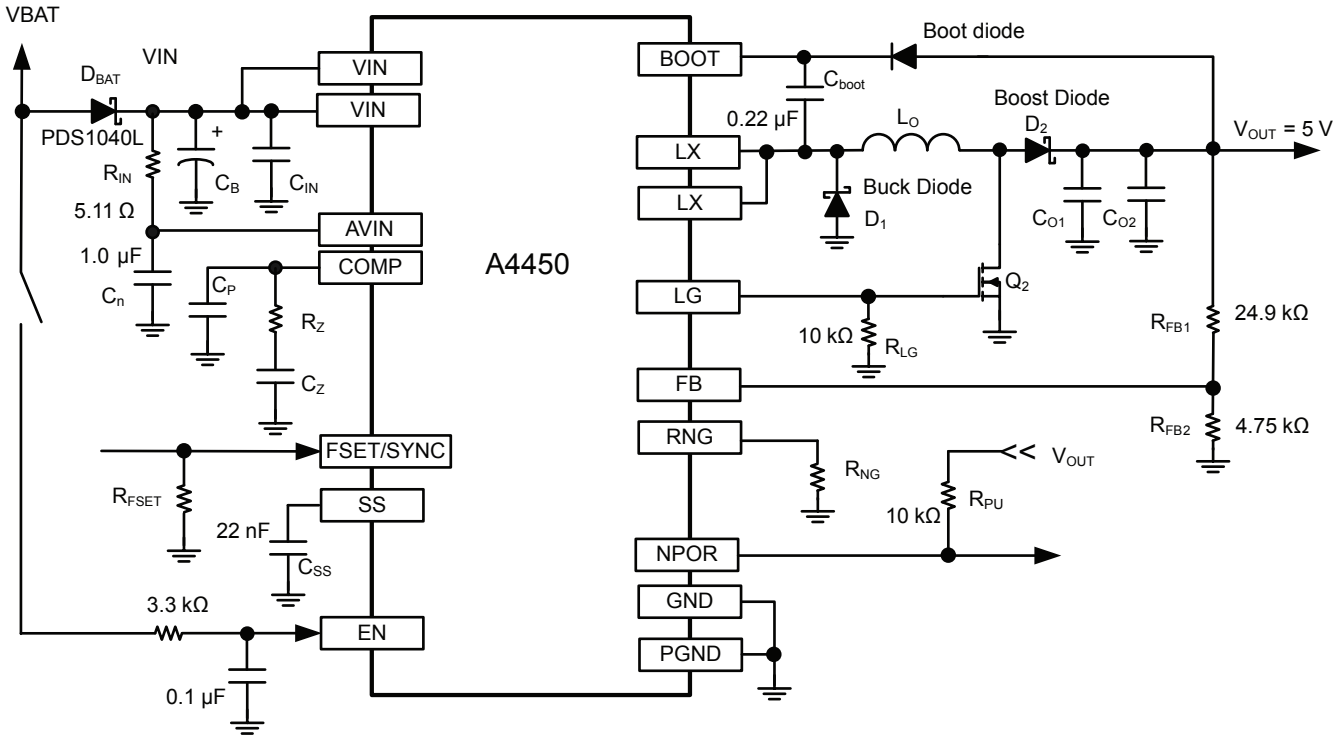

Figure 15: Schematic of 5 V_{OUT} Design Example at 400 kHz and 2 MHz

Table 2: Recommended Key Components of 5 V_{OUT} at 400 kHz and 2 MHz Designs

Reference	Description	Manufacturer/Part Number
Q2 – Boost Switch	NFET, 20 V/30 V, 25 mΩ and 14 nC_{MAX} @ 4.5 V_{GS}	ST, STL10N3LLH5
		OnSemi, NVTFS4823N
D_1, D_2	Schottky 3 A, 40 V	Vishay, SS3P4-M3/84A
C_B	47 µF, electrolytic capacitor, 50 V	Panasonic, EEE-FK1H470XP
C_{IN}	Total ~10 µF, ceramic capacitors, X7R, ≥50 V	TDK, Murata, Taiyo Yuden
2 MHz 5 V_{OUT} (R_{FSET} = 7.87 kΩ, R_{NG} = 15 kΩ)		
$(R_Z+C_Z)//C_P$	(7.32 kΩ + 2.2 nF)//33 pF	–
L_O	10 µH, I_R = 5.2 A, I_{SAT} = 12.5 A, 27 mΩ	Wurth, 74437368100
C_O	Total ~20 µF, ceramic, X7R, ≥16 V	TDK, Murata, Taiyo Yuden
Boot Diode	BAS16	NXP, Vishay
400 kHz 5 V_{OUT} (R_{FSET} = 41.2 kΩ, R_{NG} = 15 kΩ)		
$(R_Z+C_Z)//C_P$	(9.31 kΩ + 5.6 nF)//10 pF	–
L_O	33 µH, I_R = 4.2 A, I_{SAT} = 5.5 A, 45 mΩ	Wurth, 7447709330
C_O	Total ~30 µF, ceramic, X7R, ≥16 V	TDK, Murata, Taiyo Yuden
Boot Diode	BAS16	NXP, Vishay

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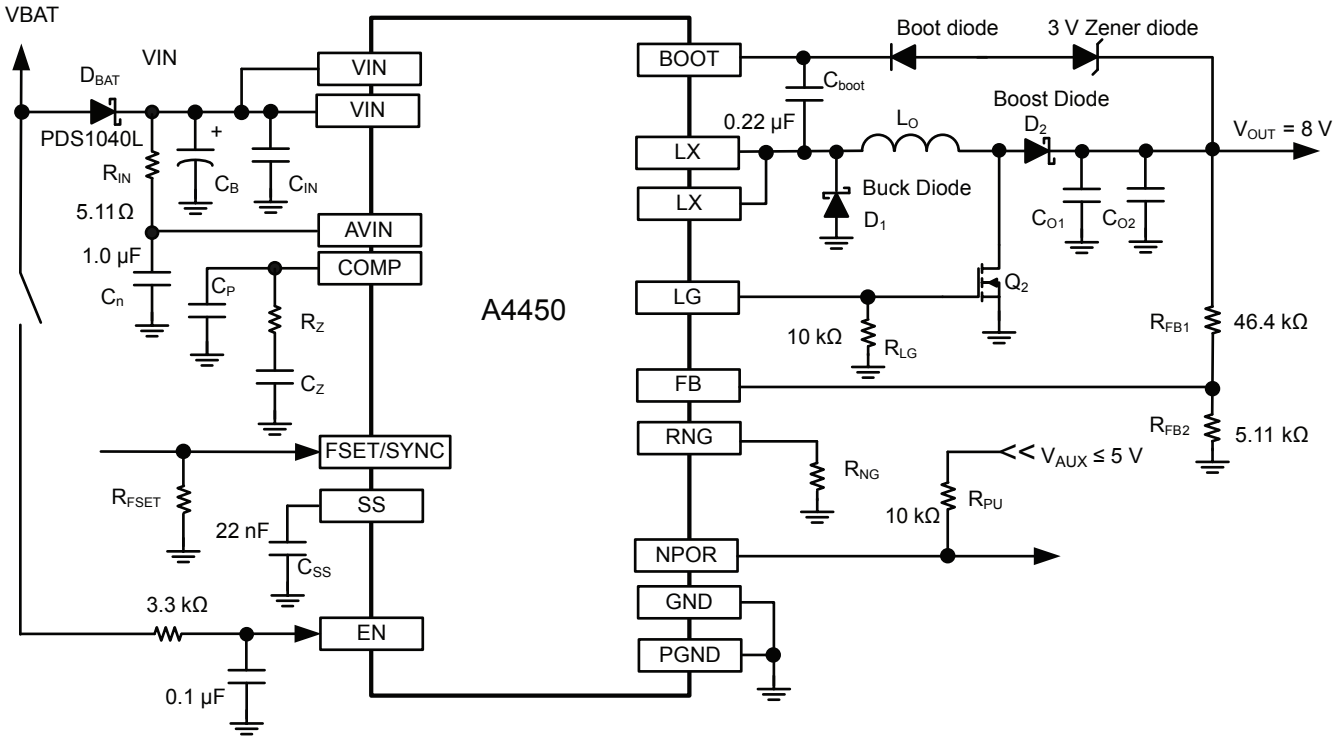

Figure 16: Schematic of 8 V_{OUT} Design Example at 400 kHz

Table 3: Recommended Key Components of 8 V_{OUT} at 400 kHz Design

Reference	Description	Manufacturer/Part Number
400 kHz 8 V_{OUT} (R_{FSET} = 41.2 kΩ, R_{NG} = 23.2 kΩ)		
$(R_Z+C_Z)//C_P$	(20.5 kΩ + 3.3 nF)// 10 pF	–
L_O	47 µH, I_R = 3.8 A, I_{SAT} = 4.5 A, 60 mΩ	Wurth, 7447709470
C_O	Total ~55 µF, ceramic, X7R, ≥16 V	TDK, Murata, Taiyo Yuden
Boot Diode	BAS16	NXP, Vishay
Zener Diode	3 V Zener Diode BZT52C3V0T-7	Diodes Inc.

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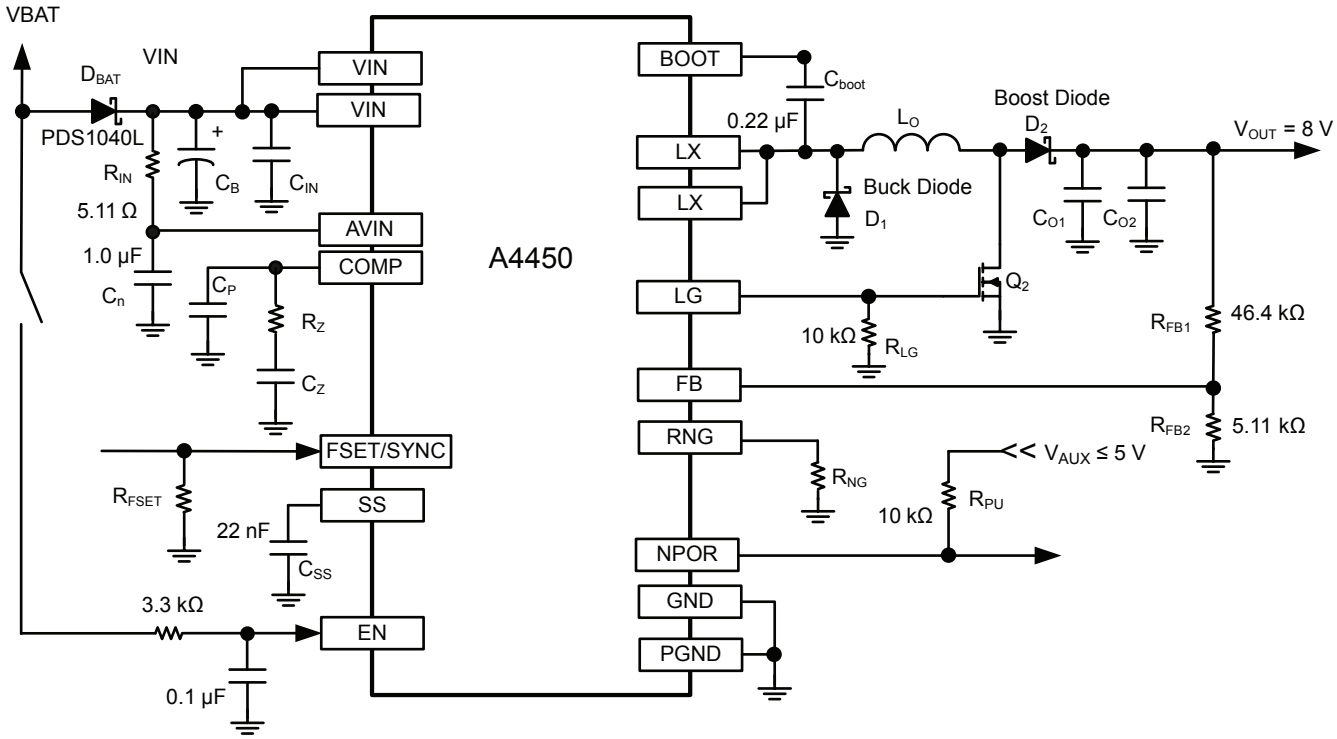

Figure 17: Schematics of 8 V_{OUT} Design Example at 2 MHz

Table 4: Recommended Key Components of 8 V_{OUT} at 2 MHz Design

Reference	Description	Manufacturer/Part Number
2 MHz 8 V_{OUT} (R_{FSET} = 7.87 kΩ, R_{NG} = 23.2 kΩ)		
$(R_Z+C_Z)//C_P$	(20 kΩ + 2.2 nF)//10 pF	–
L_O	10 µH, I_R = 5.2 A, I_{SAT} = 12.5 A, 27 mΩ	Wurth, 74437368100
C_O	Total ~20 µF, ceramic, X7R, ≥16 V	TDK, Murata, Taiyo Yuden

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The following are some guidelines to determine the appropriate output and input ranges.

First, when the A4450 operates under buck-boost mode, the peak inductor current, I_{PEAK}, which happens at minimum V_{IN}, should be below the Pulse-by-Pulse Current Limit at Buck-Boost Mode, $I_{LIM(BUCKBOOST)}$:

$$I_{PEAK} = \frac{I_{OUT} + \frac{\Delta I_L}{2} \times (1 - D_{Buck})}{1 - D_{Boost\_MAX}} < I_{LIM(BUCKBOOST)} \rightarrow$$

$$I_{OUT} + \frac{\Delta I_L}{2} \times (1 - D_{Buck}) < I_{LIM(BUCKBOOST)} \times (1 - D_{Boost\_MAX})$$

For practical application, some margin—for example 15% or higher—should be added:

$$I_{OUT} + \frac{\Delta I_L}{2} \times (1 - D_{Buck}) \le I_{LIM(BUCKBOOST)} \times \frac{V_{IN\_MIN}}{V_{OUT}} \times D_{Buck0} \times 85\%$$

Minimum $I_{LIM(BUCKBOOST)}$ = 3.9 A, and it is recommended to choose D_{Buck0} = 0.65 (for Buck minimum Off-Time at 2 MHz) or D_{Buck0} = 0.80 or lower (for Buck minimum Off-Time at 400 kHz and below); also choose ΔI_L = 40% × I_{OUT}. Then the outputs should meet the following criteria:

$$1.07 \times I_{OUT} \le I_{LIM(BUCKBOOST)} \times \frac{V_{IN\_MIN}}{V_{OUT}} \times D_{Buck0} \times 85\% \quad \textbf{for 2 MHz}$$

$$1.04 \times I_{OUT} \le I_{LIM(BUCKBOOST)} \times \frac{V_{IN\_MIN}}{V_{OUT}} \times D_{Buck0} \times 85\% \quad \textbf{for 400 kHz and below}$$

$$I_{OUT} \times V_{OUT} \le 2.0 \times V_{IN\_MIN} \quad \textbf{for 2 MHz}$$

$$I_{OUT} \times V_{OUT} \le 2.5 \times V_{IN\_MIN} \quad \textbf{for 400 kHz and below}$$

Second, when the A4450 operates under Buck mode, the peak inductor current should not go beyond the Pulse-by-Pulse Current Limit at Buck Mode, $I_{LIM(BUCK)}$:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \le I_{LIM(BUCK)}$$

Minimum $I_{LIM(BUCK)}$ = 2.4 A, and if the chosen ΔI_L = 40% × I_{OUT}, then:

$$I_{OUT} \le 2.0A$$

Thus, the rated output current should not go above 2 A. At the same time, the rated output voltage, V_{OUT}, and rated output current, I_{OUT}, will also depend on the selected minimum input voltage, V_{IN_MIN}. See Figure 18 and Figure 19.

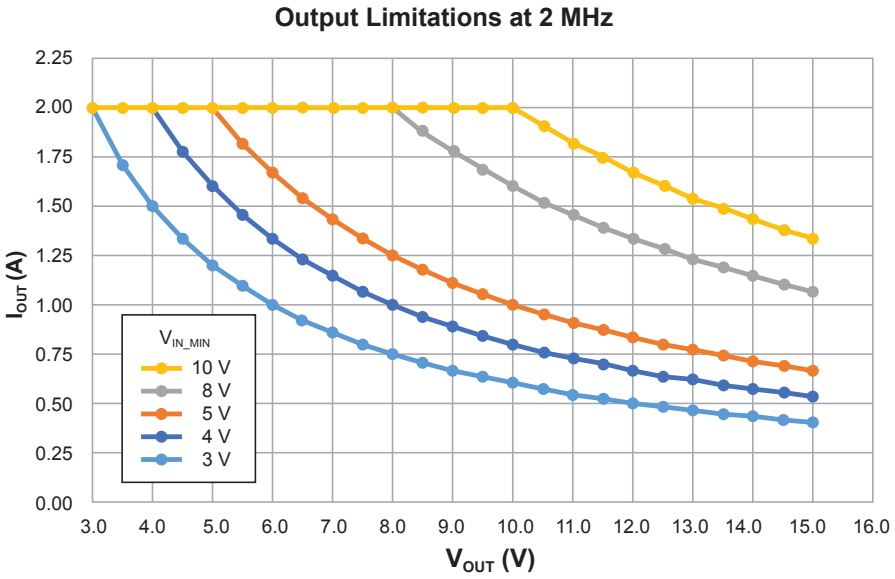

Figure 18: Selection of rated I_{OUT} versus rated V_{OUT} for different V_{IN_MIN} at 2 MHz

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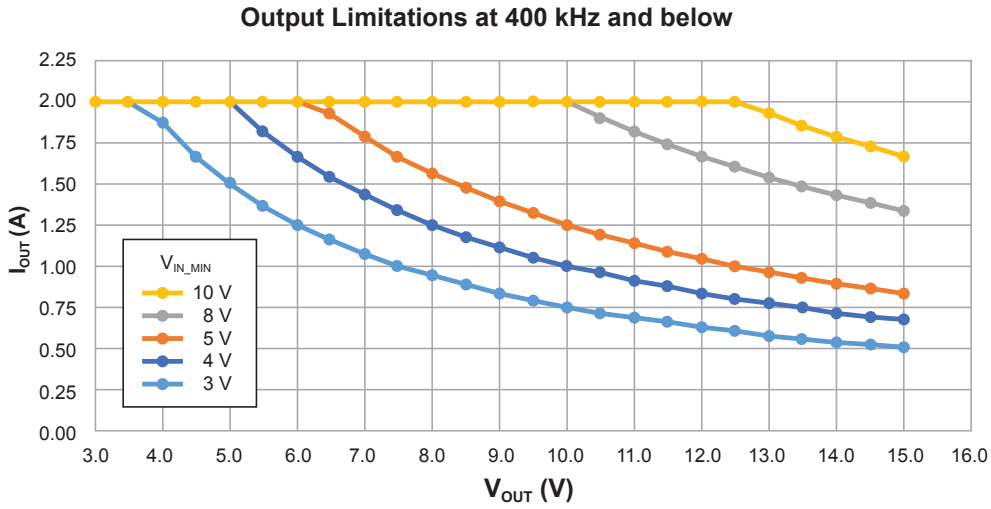

Figure 19: Selection of rated I_{OUT} versus rated V_{OUT} for different V_{IN_MIN} at 400 kHz and below

In actual application, it is important to check actual Buck duty cycle, D_{Buck}, at V_{IN_MIN} to ensure that D_{Buck} is not saturated to avoid dropout operation. If D_{Buck} is saturated, it is suggested to reduce D_{Buck0} or increase V_{IN_MIN}.

For example, when V_{OUT} = 12 V and I_{OUT} = 0.8 A at 400 kHz, and D_{Buck0} = 0.8, then $V_{IN\_MIN} \geq 3.84$ V. However, the actual Buck duty cycle at V_{IN} = 5 V is 0.95, which is close to saturation; therefore, it is better to set $V_{IN\_MIN} > 5.5$ V, where measured D_{Buck} = 0.92. The other option is to choose lower D_{Buck0} = 0.72; then $V_{IN\_MIN} \geq 4.3$ V, and the actual Buck duty cycle at V_{IN} = 5 V becomes 0.875. At V_{IN} = 4.3 V, actual Buck duty cycle will be 0.92. $V_{IN\_MIN} > 5$ V is suggested for some margin in the actual application.

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POWER DISSIPATION AND THERMAL CALCULATIONS

The power dissipated in the A4450 is the sum of the power dissipated from the V_{IN} supply current (P_{IN}), the switching power dissipation of the integrated buck switch (P_{SW1}), the conduction power dissipation of the integrated Buck switch (P_{COND1}), and the power dissipated by both gate drivers (P_{DRIVER}).

The power dissipated from the V_{IN} supply current can be calculated using equation 23,

$$P_{IN} = V_{IN} \times I_Q + (V_{IN} - V_{GS1}) \times Q_{G1} \times f_{SW} + P_{IN2} \quad (23)$$

where

$$P_{IN2} = \begin{cases} (V_{IN} - V_{GS2}) \times Q_{G2} \times f_{SW}, & \text{in Buck-Boost mode} \\ 0, & \text{in Buck mode} \end{cases}$$

V_{IN} is the input voltage,

I_Q is the input quiescent current drawn by the A4450 (see Electrical Characteristics table),

V_{GS1} is the MOSFET gate drive voltage of high-side buck switch (typically 5 V),

Q_{G1} is the internal high-side buck switch gate charges (approximately 5.7 nC),

Q_{G2} is the external boost switch gate charges, and

f_{SW} is the PWM switching frequency.

The switching power dissipation of the high-side buck switch can be calculated using equation 24,

$$P_{SW1} = \frac{1}{2} \times V_{IN} \times \frac{I_{OUT}}{1 - D_{Boost}} \times (t_r + t_f) \times f_{SW} \quad (24)$$

where

V_{IN} is the input voltage,

I_{OUT} is the regulator output current,

D_{Boost} is the duty cycle of the boost switch,

f_{SW} is the PWM switching frequency, and

t_r and t_f are the rise and fall times measured at the SW node.

The exact rise and fall times at the LX node will depend on the external components and PCB layout, so each design should be measured at full load. Approximate values for both t_r and t_f range from 5 to 20 ns.

The power dissipated by the high-side Buck switch while it is conducting can be calculated using equation 25,

$$P_{COND1} = I^2_{RMS(FET)} \times R_{DS(ON)HS} = \left(\frac{D_{Buck}}{(1 - D_{Boost})^2}\right) \times \left(I^2_{OUT} + \frac{\Delta I_L^2}{12}\right) \times R_{DS(ON)HS} \quad (25)$$

where

I_{OUT} is the regulator output current,

ΔI_L is the peak-to-peak inductor ripple current,

D_{Boost} is the duty cycle of the boost switch,

D_{Buck} is the duty cycle of the buck switch, and

$R_{DS(ON)HS}$ is the on-resistance of the high-side buck switch MOSFET.

The $R_{DS(ON)HS}$ of the high-side buck switch has some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an $R_{DS(ON)}$ with at least a 15% initial tolerance plus 0.39%/°C increase due to temperature.

The sum of the power dissipated by both gate drivers of the integrated buck switch and the external boost switch is,

$$P_{DRIVER} = P_{G1} + P_{G2} \quad (26)$$

where

$$P_{G1} = Q_{G1} \times V_{GS1} \times f_{SW}$$

$$P_{G2} = \begin{cases} Q_{G2} \times V_{GS2} \times f_{SW}, & \text{in Buck-Boost mode} \\ 0, & \text{in Buck mode} \end{cases}$$

Finally, the total power dissipated by the A4450 (P_{TOTAL}) is the sum of the previous equations,

$$P_{TOTAL} = P_{IN} + P_{SW1} + P_{COND1} + P_{DRIVER} \quad (27)$$

The average junction temperature can be calculated with the equation 28,

$$T_J = P_{TOTAL} \times R_{\theta JA} + T_A \quad (28)$$

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where

P_{TOTAL} is the total power dissipated from equation 27,

$R_{\theta JA}$ is the junction-to-ambient thermal resistance of QFN-20 package (37°C/W on a 4-layer PCB), and

T_A is the ambient temperature.

The maximum junction temperature will be dependent on how efficiently heat can be transferred from the PCB to the ambient air.

It is critical that the thermal pad on the bottom of the IC should be connected to at least one ground plane using multiple vias.

As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are trade-offs between ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will reduce the junction temperature considerably.

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PCB COMPONENT PLACEMENT AND ROUTING

A good PCB layout is critical for the A4450 to provide clean, stable output voltages. Follow these guidelines to ensure a good PCB layout. Figure 20 shows a typical buck-boost converter schematic with the critical power paths/loops.

1. Place the ceramic input capacitors C_{IN} as close as possible to the VIN pin and GND pins to minimize the area of the critical Loop 1 (shown in Figure 20); and the traces of the input capacitors to VIN pin should be short and wide to minimize the inductance. The larger input capacitor can be located further away from VIN pin. The input capacitors and A4450 IC should be on the same side of the board with traces on the same layer.
2. The critical Loop 2 consisting of boost diode, output capacitor C_{OUT}, and the external boost switch Q2 should be minimized with relatively wide traces.
3. The Loop 3 shows the external boost switch gate driver current loop. It is supplied from the bootstrap capacitor, C_{boot}. Ensure that the gate driver Loop 3 is small and place the traces parallel with small gap.
4. Ideally, the output capacitors, output inductor, buck diode, boost diode, boost switch, and the controller IC should be on the same layer. Connect these components with fairly wide traces. A solid ground plane should be used as a very low-inductance connection to the GND.
5. Place the output inductor (L_O) as close as possible to the LX pin with short and wide traces. The LX and LXb nodes have high dv/dt rate, which are the root cause of many noise issues. It is suggested to minimize the copper area to minimize the coupling capacitance between these nodes and other noise-sensitive nodes; However, the nodes' area cannot be too small in order to conduct high current. A ground copper area can be placed beneath the node to provide additional shielding. Also, keep low-level analog signals (like FB, COMP) away from the LX and LXb polygons.
6. Place the feedback resistor divider (R_{FB1} and R_{FB2}) very close to the FB pin. Make the ground side of R_{FB2} as close as possible to the A4450.
7. Place the compensation components (R_Z, C_Z, and C_P) as close as possible to the COMP pin. R_Z should be in COMP pin side and C_Z in GND side. Also make the ground side of C_Z and C_P as close as possible to the IC.
8. Place the FSET resistor as close as possible to the SYNC/FSET pin; place the soft-start capacitor C_{SS} as close as possible to the SS pin.
9. The output voltage sense trace (from V_{OUT} to R_{FB1}) should be connected as close as possible to the load to obtain the best load regulation.
10. Place the bootstrap capacitor (C_{boot}) near the BOOT pin and keep the routing from this capacitor to the LX polygon as short as possible.
11. When connecting the input and output ceramic capacitors, use multiple vias to GND and place the vias as close as possible to the pads of the components. Do not use thermal reliefs around the pads for the input and output ceramic capacitors.
12. To minimize PCB losses and improve system efficiency, the input and output traces should be as wide as possible and be duplicated on multiple layers, if possible.
13. The thermal pad under the IC should be connected to the GND plane (preferably on the top and bottom layer) with as many vias as possible. Allegro recommends vias with an approximately 0.25 to 0.30 mm hole and a 0.13 mm and 0.18 mm ring.
14. EMI/EMC issues are always a concern. Allegro recommends having locations for an RC snubber from LX to ground. The resistor should be 0805 or 1206 size.

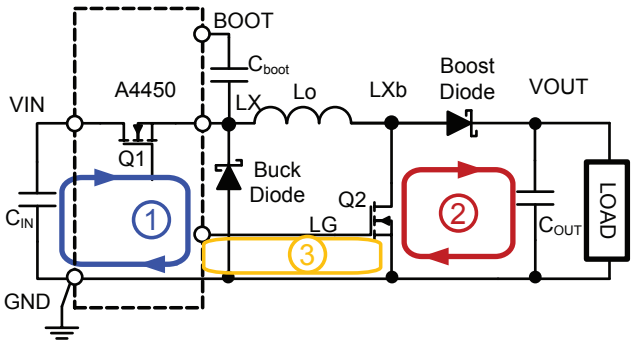

Figure 20: Typical Buck-Boost Regulator

A single-point ground is recommended, which could be the exposed thermal pad under the IC.

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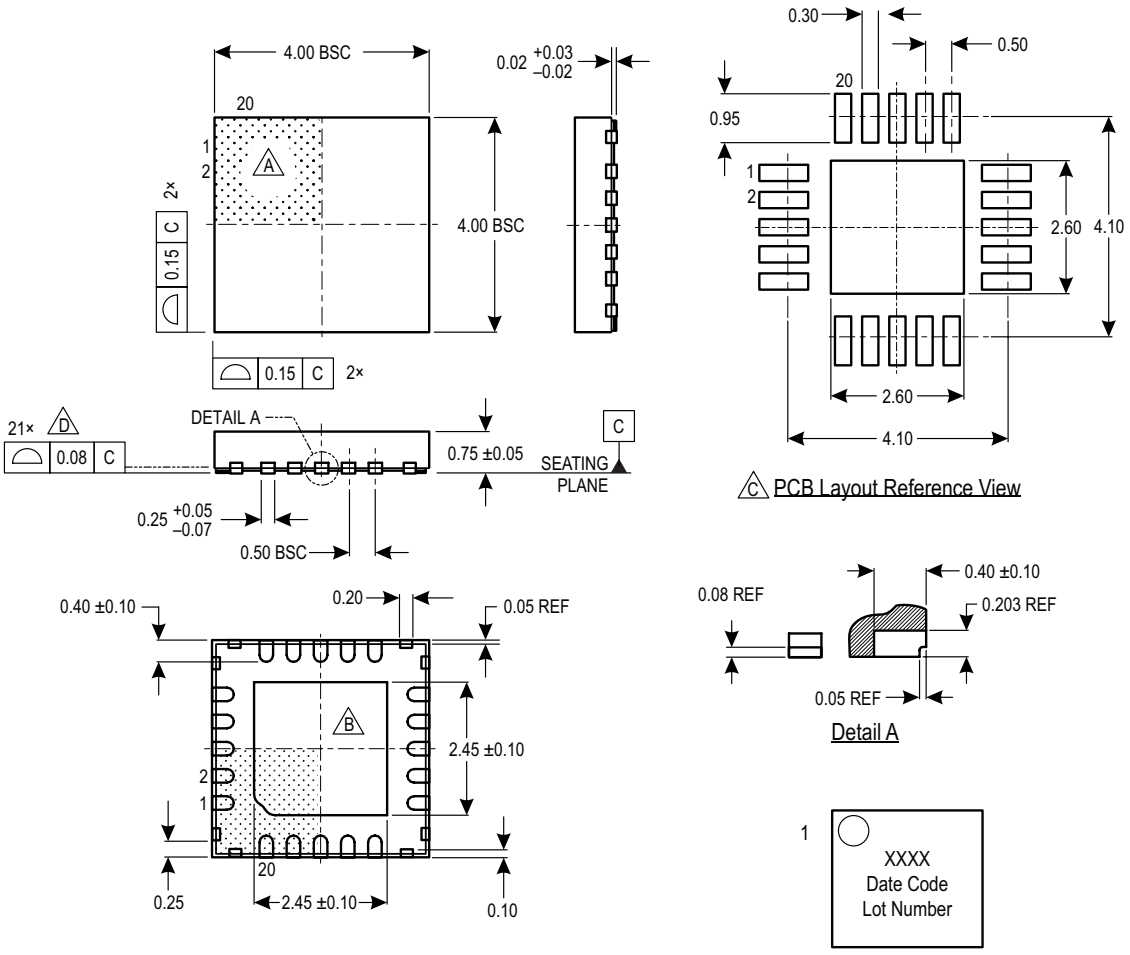
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area.

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Coplanarity includes exposed thermal pad and terminals.

E Branding scale and appearance at supplier discretion.

E Standard Branding Reference View

Line 1: Part Number
Line 2: 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

Figure 21: Package ES, 20-Pin QFN with Exposed Thermal Pad and Wettable Flank

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Revision Table

Number	Date	Description
–	June 29, 2016	Initial release
1	March 28, 2017	Added guidelines to determine the appropriate output and input ranges (page 29-30)
2	June 6, 2017	Added Table of Contents (page 3); updated Functional Description Overview (page 11)
3	June 20, 2018	Minor editorial updates
4	July 2, 2019	Minor editorial updates
5	July 5, 2022	Updated package drawing (page 35) and minor editorial updates

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