ExpressLane PEX 8604-BA
4-Lane, 4-Port PCI Express Gen 2 Switch
Data Book

Version 1.3

March 2011

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Revision History

Version	Date	Description of Changes
1.0	July, 2009	Production Release, Silicon Revision BA.
1.1	May, 2010	Production update, Silicon Revision BA. Added support for Industrial temperature, and added new order part number.
1.2	September, 2010	Production update, Silicon Revision BA. Corrected Link widths listed for STRAP_PORTCFG[1:0] in Table 3-6.
1.3	March, 2011	Production update, Silicon Revision BA. Applied miscellaneous corrections and enhancements throughout the data book.

Copyright Information

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Preface

The information in this data book is subject to change without notice. This PLX data book to be updated periodically as new information is made available.

Audience

This data book provides functional details of PLX Technology's ExpressLane PEX 8604-BA 4-Lane, 4-Port PCI Express Gen 2 Switch, for hardware designers and software/firmware engineers.

Supplemental Documentation

This data book assumes that the reader is familiar with the following documents:

- PLX Technology, Inc. (PLX), www.plxtech.com

  The PLX PEX 8604 Toolbox includes this data book and other supporting documentation, *such as* errata, and design and application notes.

- The Institute of Electrical and Electronics Engineers, Inc. (IEEE), www.ieee.org
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
  - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*
- Intel Corporation, www.intel.com
  - *PHY Interface for the PCI Express Architecture, Version 2.00*
- NXP Semiconductors, www.standardics.nxp.com
  - *The I2C-Bus Specification, Version 2.1*
- PCI Special Interest Group (PCI-SIG), www.pcisig.com
  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI Bus Power Management Interface Specification, Revision 1.2*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2*
  - *PCI Express Base Specification, Revision 1.0a*
  - *PCI Express Base Specification, Revision 1.1*
  - *PCI Express Base Specification, Revision 2.0*
  - *PCI Express Base Specification, Revision 2.0 Errata*
  - *PCI Express Card Electromechanical Specification, Revision 2.0*
  - *PCI Express Mini Card Electromechanical Specification, Revision 1.1*
  - *PCI Express Architecture PCI Express Jitter and BER White Paper, Revision 1.0*
- Personal Computer Memory Card International Association (PCMCIA), www.pcmcia.org
  - *ExpressCard Standard Release 1.0*
- PXI Systems Alliance (PXI), www.pxisa.org
  - *PXI-5 PXI Express Hardware Specification, Revision 1.0*
- SBS Implementers Forum, smbus.org
  - *System Management Bus (SMBus) Specification, Version 2.0*

Note: *In this data book, shortened titles are associated with the previously listed documents. The following table lists these abbreviations.*

Abbreviation	Document
PCI r3.0	*PCI Local Bus Specification, Revision 3.0*
PCI Power Mgmt. r1.2	*PCI Bus Power Management Interface Specification, Revision 1.2*
PCI-to-PCI Bridge r1.2	*PCI to PCI Bridge Architecture Specification, Revision 1.2*
PCI Express Base r1.0a	*PCI Express Base Specification, Revision 1.0a*
PCI Express Base r1.1	*PCI Express Base Specification, Revision 1.1*
PCI Express Base r2.0	*PCI Express Base Specification, Revision 2.0*
PCI ExpressCard CEM r2.0	*PCI Express Card Electromechanical Specification, Revision 2.0*
PCI ExpressCard Mini CEM r1.1	*PCI Express Mini Card Electromechanical Specification, Revision 1.1*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*
IEEE Standard 1149.6-2003	*IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*
I^2C Bus v2.1 *I2C Bus v2.1*[a]	*The I^2C-Bus Specification, Version 2.1*
SMBus v2.0	*System Management Bus (SMBus) Specification, Version 2.0*

a. Due to formatting limitations, the specification name may appear without the superscripted "2" in its title.

Terms and Abbreviations

The following table lists common terms and abbreviations used in this data book. Terms and abbreviations defined in the *PCI Express Base r2.0* are not included in this table.

Terms and Abbreviations	Definitions
8b/10b	Data-encoding scheme used on data transferred across a Link that is operating at either Gen 1 or Gen 2 Link speed (2.5 or 5.0 GT/s, respectively).
ACK	Acknowledge Control Packet. Control packet used by a destination to acknowledge data packet receipt. Signal that acknowledges signal receipt.
AMCAM	Address-mapping CAM that determines a memory Request route. Contains mirror copies of the PCI-to-PCI bridge **Memory Base** and **Memory Limit** registers in the switch.
ARI	Alternative Routing-ID Interpretation.
BAR	Base Address register.
BER	Bit error rate.
BusNoCAM	Bus Number-mapping CAM that determines the Completion route. Contains mirror copies of the PCI-to-PCI bridge **Secondary Bus Number** and **Subordinate Bus Number** registers in the switch.
CAM	Content-Addressable Memory.
CDR	Clock Data Recovery.
CRC	Cyclic Redundancy Check.
CSRs	Configuration Space registers.
DLL	Data Link Layer.
DMA	Direct Memory Access.
Downstream Device	Device that is connected to a downstream Port.
Downstream Port	Port that is used to communicate with a device below it within the system hierarchy. A switch can have one or more downstream Ports.
ECC	Error-Correcting Code.
ECRC	End-to-end Cyclic Redundancy Check.
EIOS	Electrical Idle Ordered-Set.
Electrical Idle	Transmitter is in a High-Impedance state (+ and - are both at common mode voltage).
EP	Endpoint.
FC	Flow Control.
Field	Multiple register bits that are combined for a single function.
GPIO	General-Purpose Input/Output.
GT/s	Giga-Transfers per second.
Half Station	Internal hardware processing partition of Even- or Odd-numbered (Even or Odd) Ports.
INCH	Ingress Credit Handler.
InitFC	Initialization Flow Control.
IOCAM	I/O Address-mapping CAM that determines an I/O Request route. Contains mirror copies of the PCI-to-PCI bridge **I/O Base** and **I/O Limit** registers in the switch.
JTAG	Joint Test Action Group.
Lane	A bidirectional pair of differential PCI Express I/O signals.
LCRC	Link Cyclic Redundancy Check.

Terms and Abbreviations	Definitions
Link Interface	Primary side of the NT Port, connects to external device pins. The secondary side of the NT Port is called the *NT Port Virtual Interface*, and connects to the internal virtual PCI Express interface.
Local	Reference to PCI Express attributes (*such as* credits) that belong to the PCI Express Link logic.
LTSSM	Link Training and Status State Machine.
LUT	Lookup Table.
MRL	Manually operated Retention Latch.
NACK	Negative Acknowledge. Used in the SMBus-related content.
NAK	Negative Acknowledge.
N_FTS	Number of Fast Training Sequences field in Training Sets.
NT	Non-Transparent. A bridging technique used in the PCI Express Switch to isolate Memory spaces by presenting the processor as an endpoint rather than another memory system. The PEX 8604 supports one NT Port.
Partial Completion	In PCI Express, a single Read can have one or more Completions with data. If more than one Completion is returned, they are referred to as *Partial Completions*.
PCI Express Link Logic	Functional unit that provides the PCI Express conforming system interface. Includes the Serializer/De-Serializer (SerDes) hardware interface modules and PCI Express interface, which provides the Physical Layer (PHY), Data Link Layer (DLL), and Transaction Layer (TL) logic.
PEC	Packet Error Code.
PEX	PCI Express.
PHY	Physical Layer.
PIPE	PHY Interface for PCI Express architecture.
PLL	Phase-Locked Loop.
PM	Power Management.
PME	Power Management Event.
Port	Interface to a group of SerDes and supporting logic that is capable of creating a Link, for communication with another Port.
P-P	PCI-to-PCI.
PRBS	Pseudo-Random Bit Sequence.
QoS	Quality of Service.
RAS	Reliability, Availability, and Serviceability.
RoHS	Restrictions on the use of certain Hazardous Substances (RoHS) Directive.
RR	Round-Robin scheduling.
Rx	Receiver.
SerDes	Serializer/De-Serializer. A high-speed differential-signaling parallel-to-serial and serial-to-parallel conversion logic attached to Lane pads.
SMBus	System Management Bus.
SPI	Serial Peripheral Interface.
SSC	Spread-Spectrum Clock.

Terms and Abbreviations	Definitions
Sticky Bits	Register bits in which the current values are unchanged by a Hot Reset, Link Down event, or Secondary Bus Reset, while the switch is powered. Sticky bits are reset to default values by a Fundamental Reset. Applies to ROS, RW1CS, and RWS CSR types, and sometimes HwInit. (Refer to Table 13-5, "Register Types, Grouped by User Accessibility," for CSR type definitions.)
Sticky State	Condition that causes a state machine to be stuck in a particular state, unable to make forward progress.
TC	Traffic Class.
TL	Transaction Layer.
TLC	Transaction Layer Control. The module performing PCI Express Transaction Layer functions.
TLP	Transaction Layer Packet. PCI Express packet formation and organization.
Transparent	Refers to standard PCI Express upstream-to-downstream routing protocol.
TS1	Type 1 Training Sequence Ordered-Set.
TS2	Type 2 Training Sequence Ordered-Set.
Tx	Transceiver.
UI	Unit Interval – 400 ps at 2.5 GT/s, 200 ps at 5.0 GT/s.
Upstream Device	Device that is connected to the upstream Port.
Upstream Port	Port that is used to communicate with a device above it within the system hierarchy.
UTP	User Test Pattern.
VC	Virtual Channel. The PEX 8604 supports two Virtual Channels, VC0 and VC1.
VCO	Voltage-Controlled Oscillator.
Vector	Address and data.
Virtual Interface	Secondary side of the NT Port, connects to the internal virtual PCI Express interface.
WRR	Weighted Round-Robin scheduling.

Data Book Notations and Conventions

Notation / Convention	Description
Blue text	Indicates that the text is hyperlinked to its description elsewhere in the data book. Left-click the blue text to learn more about the hyperlinked information. This format is often used for register names, register bit and field names, register offsets, chapter and section titles, figures, and tables.
PEX_XXXn[*x*] PEX_XXXp[*x*]	When the signal name appears in all CAPS, with the primary Port description listed first, field [*x*] indicates the number associated with the signal balls/ pads assigned to a specific SerDes module/Lane. The lowercase "n" (negative) or "p" (positive) suffix indicates the differential pair of signals, which are always used together.
# = Active-Low signals	Unless specified otherwise, Active-Low signals are identified by a "#" appended to the term (*for example*, PEX_PERST#).
`Program/code samples`	`Monospace font` (*`program or code samples`*) is used to identify code samples or programming references. These code samples are case-sensitive, unless specified otherwise.
`command_done`	Interrupt format.
Command/Status	Register names.
Parity Error Detected	Register parameter [bit or field] or control function.
Upper Base Address[31:16]	Specific Function in 32-bit register bounded by bits [31:16].
Number multipliers	k = 1,000 (10^3) is generally used with frequency response. K = 1,024 (2^{10}) is used for Memory size references. KB = 1,024 bytes. M = meg. = 1,000,000 when referring to frequency (decimal notation) = 1,048,576 when referring to Memory sizes (binary notation)
255d	d = Suffix that identifies decimal values.
1Fh	h = Suffix that identifies hex values. Each prefix term is equivalent to a 4-bit binary value (Nibble). Legal prefix terms are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.
1010b	b = suffix which identifies binary notation (*for example*, 01b, 010b, 1010b, and so forth). Not used with single-digit values of 0 nor 1.
0 through 9	Decimal numbers, or single binary numbers.
byte	Eight bits – abbreviated to "B" (*for example*, 4B = 4 bytes).
LSB	Least-Significant Byte.
lsb	Least-significant bit.
MSB	Most-Significant Byte.
msb	Most-significant bit.
DWord	Double-Word (32 bits) is the primary register size in these devices.
QWord	Quad-Word (64 bits).
Reserved	Do not modify ***Reserved*** bits and words. Unless specified otherwise, these bits read as 0 and must be written as 0.
word	16 bits.

Contents

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Registers

Transparent Port Registers

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NT Port Link Interface Registers – NT Mode Only

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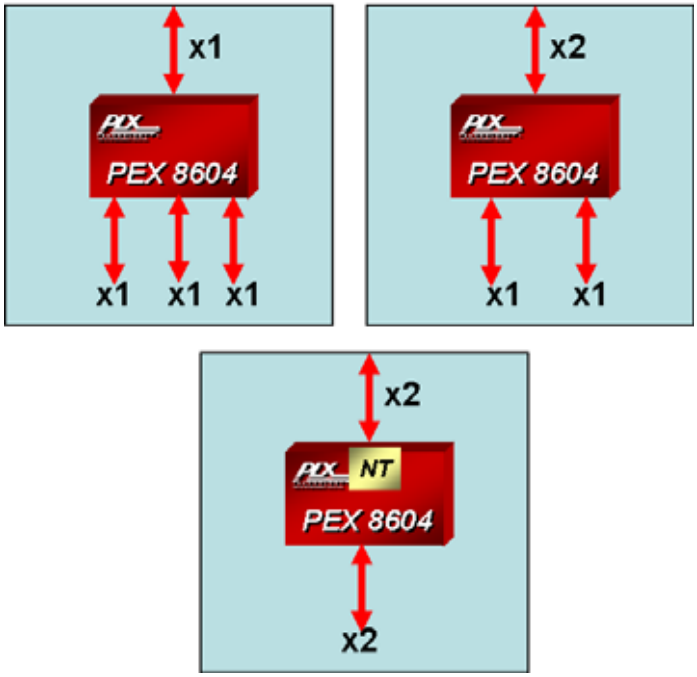
Chapter 1 Introduction

1.1 Overview

This data book describes PLX Technology's ExpressLane™ PEX 8604, a fully non-blocking, low-latency, low-cost, and low-power 4-Lane, 4-Port PCI Express Gen 2 Switch. Conforming to the *PCI Express Base r2.0*, the PEX 8604 enables users to add scalable, high-bandwidth I/O to various products, including communications platforms, servers, storage systems, embedded systems, and intelligent I/O modules. The PEX 8604's flexible hardware configuration and software programmability allows the switch to be tailored for a wide variety of applications, including fan-out, aggregation, and peer-to-peer applications.

The PEX 8604 supports multiple Port configuration options, to provide flexible solutions for optimal product design. (Refer to Figure 1-1.)

Figure 1-1. Port Configuration



1.2 Features

The PEX 8604 supports the following features:

- 4-Port PCI Express switch
  - 4 Lanes with integrated on-chip SerDes
  - Low-power SerDes (under 90 mW per Lane)
  - Port configuration
    - 4 independent Ports
    - Choice of Link width (quantity of Lanes) per unique Link/Port – x1 or x2
    - Configurable with serial EEPROM, I^2C, SMBus, and/or Host software
    - Designate any Port as the *upstream Port* (Port 0 is recommended)
- High Performance
  - 40 GT/s aggregate bandwidth (5.0 GT/s/Lane x 4 SerDes x 2 (full duplex))
  - Integrated 5.0 GT/s SerDes speed negotiation, for each Port
  - Full line rate on all Ports
  - Cut-Thru latency – 190 ns for Link widths of x4 to x1
  - Non-blocking Crossbar Switch interface supports TLP bandwidth capacity of each x2 Link
  - Maximum Payload Size – 512 bytes
- *performance*PAK™
  - Read Pacing™ (intelligent bandwidth allocation)
  - Dual Cast™
  - Dynamic Buffer Pool Architecture for faster credit updates
- *vision*PAK™
  - Performance Monitoring
    - Per-Port Payload and Header Counters
    - Per-traffic type (Write, Read, Completion) Counters
  - Error Injection and Pseudo-Random Bit Sequence (PRBS)
  - SerDes Loopback
  - SerDes Eye Capture
- Access Control Services (ACS) – Protection mechanisms for added data integrity in peer-to-peer transactions
- Alternative Routing-ID Interpretation (ARI) – Enables virtualized systems and/or highly integrated multi-function devices
- Quality of Service (QoS) support
  - Two Virtual Channels (VC0 and VC1), per Port
  - Eight Traffic Classes (TC[7:0]), per Port
  - Weighted Round-Robin (WRR) Port and Virtual Channel (VC) arbitration
- Non-Transparent Bridging
  - Configurable Non-Transparent Port
  - Moveable *upstream Port*
  - Enables Dual-Host, Dual-Fabric, Host-Failover applications
  - Cross-link Port capability

- Reliability, Availability, Serviceability (RAS) features
  - All Transparent downstream Ports are Hot Plug-capable, through I^2C (Serial Hot Plug Controller on every Port)
  - End-to-end Cyclic Redundancy Check (ECRC) and Poison bit support
  - Data path protection
  - Memory (RAM) error correction
  - Advanced Error Reporting support
  - Lane Status bits and GPIO available
  - Per-Port error diagnostics
  - Joint Test Action Group (JTAG) AC/DC boundary scan
- Spread-Spectrum Clock isolation
  - Dual-clock domain
- INTA# (PEX_INTA#) and FATAL ERROR (FATAL_ERR#) (Conventional PCI SERR# equivalent) ball support
- 19 General-Purpose Input/Output (GPIO) balls, which can be used for GPIO and/or Interrupt inputs
- Lane Status balls (PEX_LANE_GOOD[5, 4, 1, 0]#)
- Other PCI Express Capabilities
  - Lane reversal
  - Polarity reversal
  - Conventional PCI-compatible Link Power Management states – L0, L0s, L1, L2/L3 Ready, and L3 (with Vaux ***not supported***)
  - Conventional PCI-compatible Device Power Management states – D0 and D3hot
  - Active State Power Management (ASPM)
  - Dynamic speed (2.5 or 5.0 GT/s) negotiation, for each Port
  - Dynamic Link width negotiation
- Out-of-Band Initialization options
  - Serial EEPROM
  - I^2C and SMBus (7-bit Slave address with 100 Kbps)
- Testability – JTAG support for DC
- 15 x 15 mm^2, 196-ball Plastic Ball Grid Array (PBGA) package
- Typical power – 1.10W (Gen 1, 2.5 GT/s) or 1.29W (Gen 2, 5.0 GT/s)
- Microsoft® Windows® Logo (WHQL)-compliant
- Compliant to the following specifications:
  - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
  - *PCI Bus Power Management Interface Specification, Revision 1.2 (PCI Power Mgmt. r1.2)*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2 (PCI-to-PCI Bridge r1.2)*
  - *PCI Express Base Specification, Revision 1.1 (PCI Express Base r1.1)*
  - *PCI Express Base Specification, Revision 2.0 (PCI Express Base r2.0)*
  - *PCI Express Base Specification, Revision 2.0 Errata*

- *PCI Express Card Electromechanical Specification, Revision 2.0 (PCI ExpressCard CEM r2.0)*
- *PCI Express Mini Card Electromechanical Specification, Revision 1.1 (PCI ExpressCard Mini CEM r1.1)*
- *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Standard 1149.1-1990)*
- *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
- *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
- *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions (IEEE Standard 1149.6-2003)*
- *The I^2C-Bus Specification, Version 2.1 (I^2C Bus v2.1)*
- *System Management Bus (SMBus) Specification, Version 2.0 (SMBus v2.0)*

Chapter 2 Features and Applications

2.1 Flexible and Feature-Rich 4-Lane, 4-Port Switch

2.1.1 Highly Flexible Port Configurations

The PLX ExpressLane PEX 8604 PCI Express Gen 2 Switch offers a maximum of four configurable Ports. To support specific bandwidth needs, Link widths can be individually configured as any power-of-two, from x1 to x2, through auto-negotiation, hardware strapping, Host software configuration, an optional serial EEPROM, and/or the I^2C Slave interface. Flexible buffer allocation, along with the PEX 8604's **flexible packet flow control**, maximizes throughput for applications where more traffic flows in the downstream, rather than upstream, direction.

The PEX 8604 supports several Port configurations. *For example*, the PEX 8604 can be used in a fan-out application, where any one Port is the upstream Port and the remaining available Lanes are divided among one, two, or three downstream Ports, of varying Link widths. Any one Port can be designated as, or dynamically changed to be, the upstream Port (Port 0 is recommended).

2.1.2 Non-Blocking Crossbar Switch Architecture

The Non-Blocking Crossbar Switch architecture is an on-chip interconnect switching fabric, which is built upon the existing PLX Switch Fabric Architecture technology. In addition to addressing simultaneous multiple flows, the Crossbar Switch architecture incorporates functions required to support an efficient PCI Express switch fabric, including:

- Deadlock avoidance
- Priority preemption
- PCI Express Ordering rules
- Packet fair queuing
- Oldest first scheduling

The Crossbar Switch interconnect physical topology is that of a packet-based Crossbar Switch fabric (internal fabric). The Crossbar Switch protocol is sufficiently flexible and robust to support a variety of embedded system requirements. The Crossbar Switch architecture basic features include:

- Multiple concurrent Data transfers
- Global ordering within the PEX 8604
- Three types of transactions – Posted, Non-Posted, and Completion (P, NP, and Cpl, respectively) – meet PCI and PCI Express Ordering and Deadlock Avoidance rules
- Optional weighting of source Ports, to support Source Port arbitration

2.1.3 Low Packet Latency and High Performance

The PEX 8604 architecture supports packet Cut-Thru with a maximum latency of 190 ns for Link widths of x4 to x1. This, combined with large Packet memory and Non-Blocking Internal Switch architecture, provides full line rate on all Ports for low-latency applications, *such as* communications and servers. The low latency enables applications to achieve high throughput and performance. In addition to low latency, the PEX 8604 supports a 512-byte Maximum Payload Size.

2.1.3.1 Data Payloads

The Data Payloads are variable length with a maximum of 512 bytes, as defined by the *Maximum Payload Size* field (available sizes are 128, 256, and 512, depending upon the quantity of enabled Ports). Read Requests ***do not*** include a Data Payload.

Note: *Refer to the* ***Device Control*** *register Maximum Payload Size field (offset 70h[7:5]) for Maximum Payload Size Port limitations.*

2.1.3.2 Cut-Thru

Cut-Thru mode can reduce latency, especially for longer packets, because the entire packet does not need to be stored before being forwarded. Instead, after the Header is decoded, the packet can be immediately forwarded. The PEX 8604 is designed to cut through TLPs, to and from every Port. By default, all Ports are enabled for Cut-Thru. Cut-Thru mode can be disabled for all Ports, by Clearing the **Debug Control** register *Cut-Thru Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[21]).

Cut-Thru mode, if enabled, is supported for the PEX 8604's NT Port Link Interface, if the PEX 8604 is configured for NT mode.

Note: *The* ***Debug Control*** *register Cut-Thru Enable bit affects the entire switch. If Cut-Thru is enabled, all Ports use Cut-Thru. If Cut-Thru is* ***not*** *enabled, no Ports use Cut-Thru.*

Caution: ***One of the drawbacks to using Cut-Thru mode is that the TLP is not known to be good until the last byte. If the TLP proves to be bad, the Cut-Thru packet must be discarded. If the TLP has already been forwarded to another device, that TLP will be framed with an EDB (End Data Bad), as opposed to the standard END.***

2.1.4 Virtual Channels and Traffic Classes

The PEX 8604 supports two Virtual Channels (VC0 and VC1) and eight Traffic Classes (TC[7:0]). VC0 and TC0 are required by the *PCI Express Base r2.0*, and configured at device start-up.

For further details, refer to Section 8.2, "Virtual Channel Support."

2.1.5 Port Arbitration

The PEX 8604 supports hardware-fixed and Weighted Round-Robin (WRR) Ingress Port Arbitration. This allows fine-tuning of Quality of Service (QoS) and efficient use of Packet buffers, for better system performance. The PEX 8604 also supports:

- RR VC arbitration on the ingress Ports
- WRR VC arbitration on the egress Ports, that select between VC0 and VC1, for each egress Port

For further details, refer to Section 8.2, "Virtual Channel Support."

2.1.6 End-to-End Packet Integrity

To enable designs that require **guaranteed error-free packets**, the PEX 8604 provides **End-to-end Cyclic Redundancy Check** (ECRC) protection and **Poison** bit support, as well as **Error-Correcting Code** (ECC) protection on the internal data paths and memory (RAM). ECC maintains packet integrity through the PEX 8604, by providing automatic correction of any 1-bit errors. These features are optional in the *PCI Express Base r2.0*; however, PLX provides them across its entire ExpressLane PCI Express Gen 2 switch product line.

2.1.7 Configuration Flexibility

The PEX 8604 provides several ways to configure its operations. *For example*, the PEX 8604 can be configured through Strapping balls, CPU Configuration Requests, an optional serial EEPROM, and/or the I^2C Slave interface. Additionally, the I^2C Slave interface allows for easy debug during the development phase, performance monitoring during the operation phase, and driver or software upgrade.

2.1.8 Interoperability

The PEX 8604 is designed to be fully compliant with the *PCI Express Base r2.0*, and is backward-compatible to the *PCI Express Base r1.1* and *PCI Express Base r1.0a*. Additionally, the switch supports **auto-negotiation**, **Lane reversal**, and **polarity reversal**, for maximum board design and board layout flexibility. All PLX ExpressLane devices undergo thorough interoperability testing at PLX's **Interoperability Lab** and compliance testing at the **PCI-SIG Compliance Workshop**, to ensure compatibility with PCI Express devices in the market.

2.1.9 Low Power with Granular SerDes Control

The PEX 8604 provides **low-power** capability that is fully compliant with the *PCI Express Base r2.0* and *PCI Power Mgmt. r1.2* Power Management (PM) specifications. Unused SerDes are automatically powered down, to further reduce power consumption.

The PEX 8604 supports **SerDes output software control**, to allow power and signal strength optimization within a system. The PLX SerDes implementation supports four power levels – *Off*, *Low*, *Typical*, and *High*. The SerDes block also supports **Loopback modes** and **Advanced Error Reporting**, which enables efficient system debug and management.

2.1.10 Dynamic Lane Reversal

The PEX 8604 supports dynamic Lane reversal during the Link training process. Lane reversal capability allows flexibility in determining board routing, so that PCI Express components can be connected without having to crisscross wires. If the wiring of Lanes to a device is reversed (on both Transmitters and Receivers), only one of the two connected devices must support Lane reversal.

Either of the outside Lanes (Transmitter and Receiver pairs) of the PEX 8604 programmed Link width must be identified as being Lane 0. During Link training, both devices on the Link negotiate the Lane numbering. During the Link Training and Status State Machine (LTSSM)'s *Configuration* state, the upstream device sends TS1 Ordered-Sets, in which each connected Lane is identified by a consecutive Lane Number, starting with Lane 0 corresponding to the physical Lane Number associated with the Port.

The Port reverses its Lane Numbers and attempts to re-train when any of the following conditions occur:

- No Receiver is detected on preferred Lane 0
- No valid Training Sets are received on preferred Lane 0 during the LTSSM's *Polling* state
- TS1 with a non-zero Lane Number Port is received on the Port's Lane 0

To confirm successful Lane Number negotiation, both devices exchange TS2 Ordered-Sets with identical Lane Numbers on each connected Lane.

2.1.11 *performance*PAK

Exclusive to PLX, *performance*PAK is a suite of unique and innovative performance features that enable PLX's Gen 2 switches to be the highest-performing Gen 2 switches available in the market today. The *performance*PAK features consist of Read Pacing, Dual Cast, and Dynamic Buffer Pool.

2.1.11.1 Read Pacing

The Read Pacing feature allows users to throttle the quantity of Read Requests being made by downstream devices. When a downstream device requests several long Reads back-to-back, the Root Complex services the Read Requests from this downstream Port in a sequential order. If this Port has a narrow Link and is therefore slow in receiving these Read packets from the Root Complex, other downstream Ports may become starved, thus negatively impacting performance. This feature enhances performance by allowing for the adequate servicing of all downstream devices, by intelligent handling of Read Requests.

For further details, refer to Section 9.6, "Read Pacing."

2.1.11.2 Dual Cast

The Dual Cast feature allows for the copying of data (packets) from one ingress Port to two egress Ports, in a single transaction, allowing for higher performance in storage, security, and mirroring applications. The feature relieves the CPU from having to conduct two separate transactions, resulting in higher system performance.

For further details, refer to Section 9.7, "Dual Cast."

2.1.11.3 Dynamic Buffer Pool

The PEX 8604 uses a dynamic buffer pool for FC management, which uses a common pool of FC Credits that is shared among other Ports within a Half-Station. This shared buffer pool is user-programmable, so FC credits can be allocated among the enabled Ports, as needed. Not only does this prevent wasted buffers and inappropriate buffer assignments, any un-allocated buffers remain in the common buffer pool, which can then be used by other Ports within the same Half-Station, for faster FC credit updates.

For further details, refer to Section 9.3.2, "Dynamic Buffering."

2.1.12 *vision*PAK

Another PLX exclusive, *vision*PAK is a debug diagnostics suite of integrated hardware and software instruments that users can use to help bring their systems to market faster. *vision*PAK features consist of Performance Monitoring, Error Injection, SerDes Loopback, SerDes Eye Capture, and more.

2.1.12.1 Performance Monitoring

The PEX 8604's real-time performance monitoring allows users to literally "see" ingress and egress performance on each Port as traffic passes through the switch, using PLX's Software Development Kit (SDK). The monitoring is completely passive, and therefore, has no effect on overall system performance. Internal counters provide extensive granularity down to traffic and packet type, and even allow for the filtering of traffic (*that is*, count only Memory Writes).

2.1.12.2 Error Injection

Using the PEX 8604's Error Injection feature, users can inject malformed packets and/or Fatal errors into their system, then evaluate the system's ability to detect and recover from such errors.

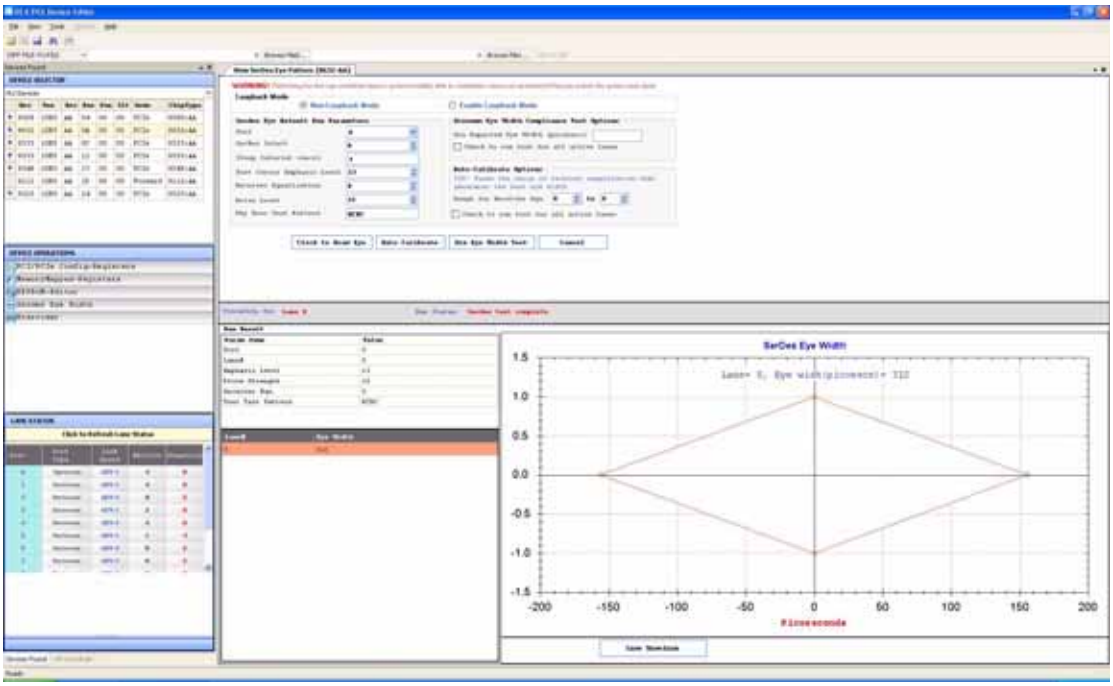
2.1.12.3 SerDes Loopback

The PEX 8604 supports External Tx, Recovered Clock, and Recovered Data Loopback modes.

2.1.12.4 SerDes Eye Capture

Users can evaluate their system's signal integrity at the Physical Layer (PHY), using the PEX 8604's SerDes Eye Capture feature. Using PLX's SDK, users can view the Receiver eye width of any Lane on the PEX 8604. Users can then modify SerDes Settings and see the impact on the Receiver eye. Figure 2-1 presents a screen shot of the SDK's SerDes Eye Capture feature.

Figure 2-1. PLX SDK SerDes Eye Capture Feature



2.1.13 Hot Plug for High Availability

Hot Plug capability allows users to replace hardware modules and perform maintenance, without having to power down the system. The PEX 8604 Hot Plug Capability and Advanced Error Reporting features make the switch suitable for **High-Availability (HA) applications**. If the PEX 8604 is used in an application where one or more of its downstream Ports connect to PCI Express slots, each Port's Serial Hot Plug Controller can be used to manage the Hot Plug event of its associated slot. Each PEX 8604 Transparent downstream Port is equipped with a **Hot Plug Control/Status** register, to support Hot Plug capability through external logic (by way of the I^2C Master interface).

For further details, refer to Chapter 11, "Hot Plug Support."

2.1.14 Fully Compliant Power Management

The PEX 8604 supports Link (L0, L0s, L1, L2/L3 Ready, and L3) and Device (D0 and D3hot) PM states, in compliance with the *PCI Express Base r2.0* and *PCI Power Mgmt. r1.2* PM specifications.

For further details, refer to Chapter 12, "Power Management."

2.1.15 General-Purpose Input/Output Signals

The PEX 8604 contains 19 General-Purpose Input/Output (GPIO) balls and associated registers, that can be programmed to function as GPIO and/or Interrupt inputs. Default functionality is GPIO inputs; however, serial EEPROM, I^2C/SMBus, and/or software can program the GPIO registers to define functionality for each I/O.

For further details, refer to the GPIO[30, 29, 16:0] signal descriptions in Section 3.4.7, "Device-Specific Signals," and Section 10.5, "General-Purpose Input/Output."

2.1.16 Non-Transparent Dual Host and Failover Support – NT Mode Only

The PEX 8604 supports full Non-Transparent Bridging (NTB) functionality, to allow implementation of **multi-Host systems** and **intelligent I/O modules** in applications that require redundancy support, *such as* **communications**, **storage**, and **servers**.

NT bridges allow systems to isolate Host memory domains, by presenting the processor subsystem as an endpoint, rather than another memory system:

- **Base Address** registers (BARs) are used to translate addresses
- **Doorbell** registers are used to signal interrupts between the address domains
- **Scratchpad** registers are accessible from both address domains, to allow inter-processor communication

For further details, refer to Chapter 14, "Non-Transparent Bridging – NT Mode Only."

2.1.17 Spread-Spectrum Clock Isolation

The PEX 8604 supports Dual Clock domains. This feature allows the buffer inside the PEX 8604 to become part of two systems with different system clocks, one of which can implement Spread-Spectrum Clocking. The constant clock input must follow the clock requirements defined in the *PCI Express Base r2.0* (±300 ppm).

For further details, refer to Chapter 17, "Dual Clocking Support."

2.2 Applications

The PEX 8604 allows user-specific tuning to a variety of **Host-centric**, as well as **peer-to-peer**, **applications**.

2.2.1 Host-Centric Fan-Out

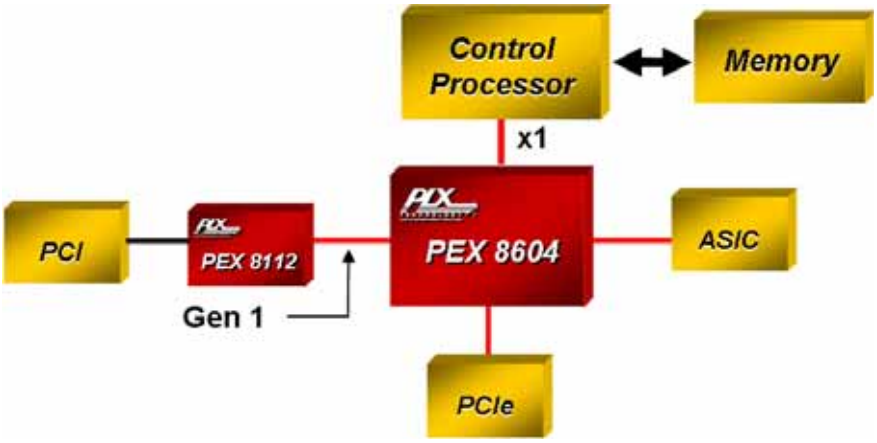
The PEX 8604, with its versatile symmetric or asymmetric Lane configuration capability, allows user-specific tuning to a variety of Host-centric applications.

Figure 2-2 illustrates a typical fan-out design, where the processor provides a PCI Express Link that must be expanded into a larger quantity of smaller Ports for a variety of I/O functions. In this example, the PEX 8604 has a 1-Lane upstream Port, and as many as three downstream Ports. The downstream Ports provide x1 PCI Express connectivity to the endpoints.

With its four Ports, the PEX 8604 can provide fan-out connectivity to up to three PCI Express devices.

The PEX 8604 can also be used to create PCI Express Gen 1 (2.5 GT/s) Ports. The PEX 8604 is backward-compatible with Gen 1 devices. Therefore, the PEX 8604 enables a PCI Express Gen 2 native chipset to fan-out to Gen 1 endpoints. In Figure 2-2, the PCI Express slots connected to the PEX 8604's downstream Ports can be populated with either Gen 1 or Gen 2 devices. Conversely, the PEX 8604 can also be used to create Gen 2 Ports on a Gen 1 native Chip Set in the same manner.

Figure 2-2. Fan-In/Fan-Out Usage



2.2.2 I/O Integration

Figure 2-3 and Figure 2-4 describe how some of the Ports can be used to bridge to PCI Express Gen 1 devices. Specifically, Figure 2-3 illustrates a PEX 8604 Port being used with a PCI-to-PCI Express Gen 1 bridge. In this usage model, the remaining PEX 8604 Ports continue to function at Gen 2 Link speed (5.0 GT/s).

Similarly, Figure 2-4 illustrates the PEX 8604 being used to bridge a PCI Express x2 Gen 1 endpoint to a Gen 2-enabled system. Each PEX 8604 Port can independently function at Gen 1 or Gen 2 Link speed (2.5 or 5.0 GT/s, respectively), according to the endpoint capabilities.

Figure 2-3. PEX 8604 Used with PCI-to-PCI Express Gen 1 Bridge

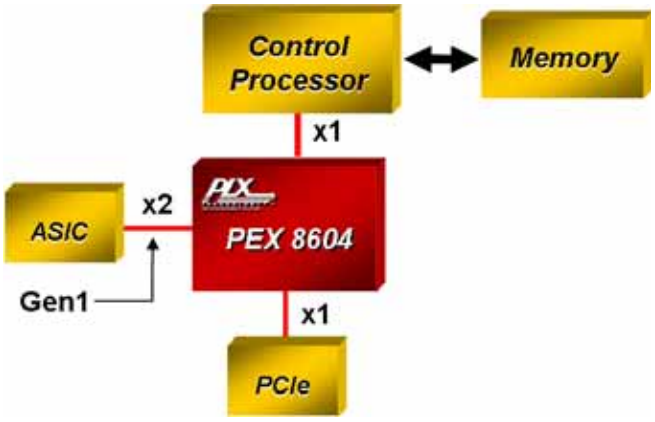
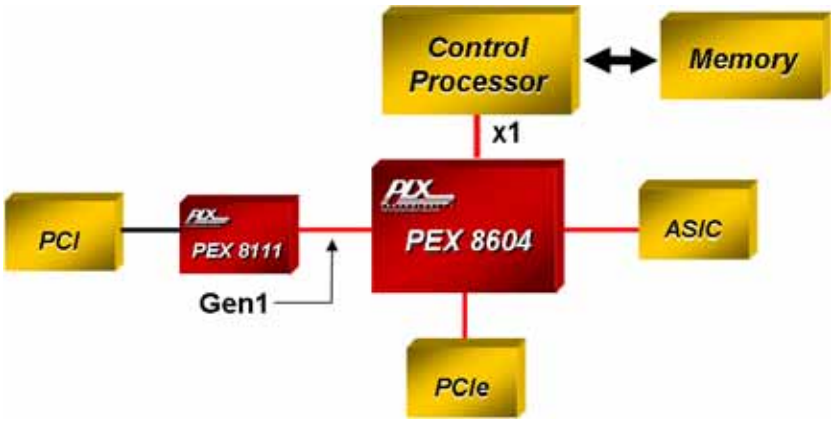


Figure 2-4. PEX 8604 Used to Bridge PCI Express x2 Gen 1 Endpoint to Gen 2-Enabled System



2.2.3 Embedded Mobile Applications

The PEX 8604 is ideal for mobile applications. Its small footprint and low power consumption make it an ideal candidate for mobile applications. Figure 2-5 illustrates a mobile application in which the PEX 8604 is used to connect a wireless radio, USB, and eSATA for storage. The upstream Port can connect to the Root Complex through a variety of forms, including external cable.

Figure 2-5. Embedded Mobile Applications

2.3 Software Usage Model

From the system model viewpoint, each PCI Express Port is a virtual PCI-to-PCI bridge, with its own set of PCI Express Configuration registers. The recommended upstream Port is Port 0; however, any Port can be configured as the upstream Port through optional configuration, by way of a serial EEPROM, the I^2C Slave interface, and/or Strapping balls. The BIOS and/or Host can configure the other Ports, by way of the upstream Port, using Conventional PCI enumeration.

2.3.1 System Configuration

The virtual PCI-to-PCI bridges within the PEX 8604 are compliant to the PCI and PCI Express system models. The Configuration Space registers (CSRs) in a virtual primary/secondary PCI-to-PCI bridge are accessible by Type 0 or Type 1 Configuration Requests, through the virtual primary bus interface (matching Bus Number, Device Number, and Function Number). Assuming the Bus Number for the upstream Port is 1, the PEX 8604's BDF (Bus, Device, Function) for F0 and F1 is 1/0/0 and 1/0/1, respectively.

2.3.2 Interrupt Sources and Events

The PEX 8604 supports the INT*x* Interrupt Message type (compatible with *PCI r3.0* Interrupt signals) or Message Signaled Interrupts (MSIs), when enabled. The PEX 8604 generates interrupts/Messages for the following:

- Hot Plug or Link State events
- PCI Express Hot Plug events
- Device-Specific errors
- GPIO-generated events
- NT Doorbell-generated events
- Baseline and Advanced Error Reporting

Internally generated interrupts and interrupts forwarded from downstream Ports are re-mapped and collapsed at the upstream Port.

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Chapter 3 Signal Ball Description

3.1 Introduction

This chapter provides descriptions of the 196 PEX 8604 signal balls. The signal name, type, location, and a brief description are provided for each signal ball. A map of the PEX 8604's physical layout is also provided.

3.2 Abbreviations

The following abbreviations are used in the signal tables provided in this chapter.

Table 3-1. Ball Assignment Abbreviations

Abbreviation	Description
#	Active-Low signal
A	Analog Input signal
APWR	Power (VDD10A) balls for SerDes Analog circuits
CMLCLK_CFCn[a]	Spread-Spectrum differential low-voltage, high-speed, CML negative Clock inputs
CMLCLK_CFCp[a]	Spread-Spectrum differential low-voltage, high-speed, CML positive Clock inputs
CMLCLKn[a]	Differential low-voltage, high-speed, CML negative Clock inputs
CMLCLKp[a]	Differential low-voltage, high-speed, CML positive Clock inputs
CMLRn	Differential low-voltage, high-speed, CML negative Receiver inputs
CMLRp	Differential low-voltage, high-speed, CML positive Receiver inputs
CMLTn	Differential low-voltage, high-speed, CML negative Transmitter outputs
CMLTp	Differential low-voltage, high-speed, CML positive Transmitter outputs
CPWR	1.0V Power (VDD10) balls for low-voltage Core circuits
GND	Common Ground (VSS) for all circuits
I	Input
I/O	Bidirectional (Input or Output)
I/OPWR	2.5V Power (VDD25) balls for Input and Output interfaces
O	Output
OD	Open Drain output
PLLPWR	2.5V Power (VDD25A) balls for Phase-Locked Loop (PLL) circuits
PU	Weak internal pull-up resistor
SerDes	Serializer/De-Serializer differential low-voltage, high-speed, I/O signal pairs (negative and positive)
STRAP	Signals used for PEX 8604 configuration, operational mode setting, and ***Factory Test***; these signals generally are not toggled at runtime

a. For REFCLK input, CML source is recommended; however, LVDS source is supported.

3.3 Internal Pull-Up Resistors

The PEX 8604 contains I/O buffers that have weak internal pull-up resistors, indicated in this chapter by PU in the signal ball tables (**Type** column). If a signal with this notation is used and no board trace is connected to the ball, the internal resistor is usually sufficient to keep the signal from toggling. However, if a signal with this notation is not used, but is connected to a board trace and is not used nor driven by an external source at all times, the internal resistors might not be sufficiently strong to hold the signal in the inactive state. In cases such as these, it is recommended that the signal be pulled or tied High to VDD25 or Low to Ground (VSS), as appropriate, through a 3KΩ to 10KΩ resistor.

Table 3-2 lists the internal pull-up resistor values.

Table 3-2. Internal Resistor Values

Internal Resistor	Minimum	Typical	Maximum	Units
PU	74K	111K	178K	Ω

3.4 Signal Ball Descriptions

Note: *If there is more than one ball per signal name that includes a numbered range, the locations are listed in the same sequence in which the range is listed, starting at the top row, from left to right. For example, PEX_PERn5 is located at B10, PEX_PERn4 is located at B12, and so forth.*

If there is more than one ball per signal name that does not include a numbered range (such as VDD10), the locations are listed in ascending alphanumeric order.

The PEX 8604 signals are divided into the following groups:

- PCI Express Signals
- Serial Hot Plug Signals
- Serial EEPROM Signals
- Strapping Signals
- JTAG Interface Signals
- I^2C/SMBus Slave Interface Signals
- Device-Specific Signals
- External Resistor Signals
- No Connect Signals
- Power and Ground Signals

3.4.1 PCI Express Signals

Table 3-3 defines the PCI Express SerDes and Control signals.

Table 3-3. PCI Express Signals – 21 Balls

Signal Name	Type	Location	Description
PEX_PERn[5, 4, 1, 0]	CMLRn	B10, B12, N5, N3	**Negative Half of PCI Express Receiver Differential Signal Pairs (4 Balls)**
PEX_PERp[5, 4, 1, 0]	CMLRp	A10, A12, P5, P3	**Positive Half of PCI Express Receiver Differential Signal Pairs (4 Balls)**
PEX_PERST#	I PU	H13	**PCI Express Reset** Used to cause a Fundamental Reset. (Refer to Chapter 5, "Reset and Initialization," for further details.)
PEX_PETn[5, 4, 1, 0]	CMLTn	B9, B11, N6, N4	**Negative Half of PCI Express Transmitter Differential Signal Pairs (4 Balls)**
PEX_PETp[5, 4, 1, 0]	CMLTp	A9, A11, P6, P4	**Positive Half of PCI Express Transmitter Differential Signal Pairs (4 Balls)**
PEX_REFCLKn	CMLCLKn	P8	**Negative Half of 100-MHz PCI Express Reference Clock Input Signal Pair** When Dual Clocking is enabled, the PEX_REFCLKn and PEX_REFCLKp signal balls become the Spread-Spectrum Clocking (SSC) domain Clock signals. PEX_REFCLKn must be AC-coupled. Use a 0.01 to 0.1 µF capacitor. Refer to Chapter 17, "Dual Clocking Support," for further details.
PEX_REFCLKp	CMLCLKp	N8	**Positive Half of 100-MHz PCI Express Reference Clock Input Signal Pair** When Dual Clocking is enabled, the PEX_REFCLKn and PEX_REFCLKp signal balls become the SSC domain Clock signals. PEX_REFCLKn must be AC-coupled. Use a 0.01 to 0.1 µF capacitor. Refer to Chapter 17, "Dual Clocking Support," for further details.
PEX_REFCLK_CFCn	CMLCLK_ CFCn	A7	**Negative Half of 100-MHz PCI Express Spread-Spectrum Reference Clock Input Signal Pair** When Dual Clocking is enabled, the PEX_REFCLK_CFCn and PEX_REFCLK_CFCp signal balls become the Constant Frequency Clocking (CFC) domain Clock signals. Due to internal biasing, the CFC Clock input requires an AC-coupling capacitor. Use a 0.01 to 0.1 µF capacitor. Refer to Chapter 17, "Dual Clocking Support," for further details.
PEX_REFCLK_CFCp	CMLCLK_ CFCp	B7	**Positive Half of 100-MHz PCI Express Spread-Spectrum Reference Clock Input Signal Pair** When Dual Clocking is enabled, the PEX_REFCLK_CFCn and PEX_REFCLK_CFCp signal balls become the CFC domain Clock signals. Due to internal biasing, the CFC Clock input requires an AC-coupling capacitor. Use a 0.01 to 0.1 µF capacitor. Refer to Chapter 17, "Dual Clocking Support," for further details.

3.4.2 Serial Hot Plug Signals

Transparent downstream Ports can implement Hot Plug, by using external I^2C I/O Expanders (one 16-pin Maxim MAX7311, NXP PCA9555, or TI PCA9555 per slot –or– one 40-pin NXP PCA9698 per two slots, provided that the PEX 8604 serial EEPROM Sets the **Power Management Hot Plug User Configuration** register *40-Pin I/O Expander Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1E0h[17]). All Transparent downstream Ports that implement Serial Hot Plug must use the same type of I/O Expander (either 16- or 40-pin, but not both concurrently).

Table 3-4 defines the three signal balls that support Serial Hot Plug. Additionally, the PEX 8604 supports external Serial Hot Plug signals on the I^2C I/O Expander. (Refer to Section 11.6.2, "I^2C I/O Expander Parts Selection and Pin Definition.")

Hot Plug signals are enabled, configured, and accessed through the Port's **Slot Capability** and **Slot Status and Control** registers (offsets 7Ch and 80h, respectively). Also, each Port's **Power Management Hot Plug User Configuration** register provides additional Device-Specific configuration and control.

These signals are active only for Hot Plug-capable Ports configured at start-up. For further details regarding Hot Plug, refer to Chapter 11, "Hot Plug Support."

Table 3-4. Serial Hot Plug Signals – 3 Balls

Signal Name	Type	Location	Description
I2C_SCL1	OD	F13	**I^2C Serial Clock Line for Serial Hot Plug Support** I^2C Clock source. Used with the external I^2C I/O Expander, and must be bused to each I/O Expander's Clock (SCL) pin. In combination with I2C_SDA1, forms the PEX 8604 I^2C Master interface. **I2C_SCL1 requires an external pull-up resistor.**
I2C_SDA1	OD	E14	**I^2C Serial Data Output for Serial Hot Plug Support** Transmits and receives I^2C data. Used with the external I^2C I/O Expander, and must be bused to each I/O Expander's Data (SDA) pin. In combination with I2C_SCL1, forms the PEX 8604 I^2C Master interface. **I2C_SDA1 requires an external pull-up resistor.**
SHPC_INT#	I PU	C14	**Serial Hot Plug Controller Interrupt Input** Active-Low interrupt input from external I^2C I/O Expanders. Used only by Serial Hot Plug-enabled Transparent downstream Ports. The I/O Expander asserts its INT# output whenever any of its inputs change state, and de-asserts its INT# output when the corresponding Input Port Data register (that changed state) is read. When the SHPC_INT# Interrupt input (connected to the INT# output of all I/O Expanders) is asserted, the I^2C Master interface begins reading the Input Port registers of all I/O Expanders, and copies the values to the appropriate bits in the corresponding Port's **Slot Status** register (offset 80h). The I^2C Master interface halts the reading of I/O Expander registers when the SHPC_INT# input de-asserts. **SHPC_INT# requires an external pull-up resistor.** ***Note:*** *SHPC_INT# is internally de-bounced, but must remain stable for at least 10 ms.*

3.4.3 Serial EEPROM Signals

The PEX 8604 includes four signals for interfacing to a serial EEPROM, defined in Table 3-5. For information regarding serial EEPROM use, refer to Chapter 6, "Serial EEPROM Controller."

Table 3-5. Serial EEPROM Signals – 4 Balls

Signal Name	Type	Location	Description
EE_CS#	I/O PU	J13	**Active-Low Serial EEPROM Chip Select Output** ***Note:*** *Although this is an I/O signal, its logical operation is output.*
EE_DI	O	K14	**PEX 8604 Output to Serial EEPROM Data Input**
EE_DO	I/O PU	H14	**PEX 8604 Input from Serial EEPROM Data Output** Should be pulled High to VDD25. ***Note:*** *Although this is an I/O signal, its logical operation is input.*
EE_SK	I/O PU	J14	**Serial EEPROM Clock Frequency Output** Programmable, by way of the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 268h[2:0]), to the following: • 1 MHz (default) • 1.98 MHz • 5 MHz • 9.62 MHz • 12.5 MHz • 15.6 MHz • 17.86 MHz ***Note:*** *Although this is an I/O signal, its logical operation is output.*

3.4.4 Strapping Signals

The PEX 8604 Strapping signals, defined in Table 3-6, Set the configuration of upstream Port and NT Port assignment, Link width, Spread-Spectrum clocking, and various setup and test modes. These balls must be pulled or tied High to VDD25 or Low to VSS (GND), as indicated in the table.

After a Fundamental Reset, the **Link Capability** (offset 74h, in each Port), and **Debug Control** and **Port Configuration** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 1DCh and 574h, respectively) capture ball status. Strapping ball Configuration data can be changed by writing new data to these registers from the serial EEPROM. I^2C can also change Strapping ball Configuration data; however, it should first Set the Port's **Even/Odd Port Disable** register *Disable Port x* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[2, 0], and Odd Ports, offset 234h[2, 0]), to prevent linkup and Host enumeration. Then, when I^2C programming is complete, I^2C should lastly Clear the upstream Port's *Disable Port x* bit, to enable linkup and allow subsequent Host enumeration.

Table 3-6. Strapping Signals – 28 Balls

Signal Name	Type	Location	Description
STRAP_DEBUG_SEL0	I	J11	***Factory Test Only*** Must be pulled or tied High to VDD25.
STRAP_FAST_BRINGUP#	I	C3	***Factory Test Only*** Must be pulled or tied High to VDD25.
STRAP_NT_ENABLE#	I	H12	**Enable NT Mode** Active-Low input that enables and disables NT mode. The STRAP_NT_ENABLE# input can be overridden by serial EEPROM and/or I^2C programming of the **Debug Control** register *NT Mode Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[18]). **If the register is programmed by serial EEPROM and/or I^2C, that must be the first serial EEPROM entry, or the first register written by I^2C, with one exception. (Refer to the Note.)** I^2C can select a Port to be the upstream NT Port, by writing to the **Debug Control** register, after the upstream Port Link is brought down, by Setting the upstream device's **Link Control** register *Link Disable* bit (PCI Express Capability, offset 10h[4]). After I^2C configures the PEX 8604, the upstream Link can be restored by Clearing the *Link Disable* bit in the device connected to the upstream Port. Software can enable or disable NT mode, by writing to the **Debug Control** register, if the register's *Hardware/ Software Configuration Mode Control* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[15]) is already Set. The mode will change, following subsequent Hot Reset (or DL_Down condition) at the PEX 8604's upstream Port. L = Enables NT mode H = Disables NT mode (default, if input is not connected)

Table 3-6. Strapping Signals – 28 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_NT_P2P_EN#	I PU	G1	**NT PCI-to-PCI Bridge Enable** ***Note:*** *If NT mode is enabled (STRAP_NT_ENABLE#=L), this input should be pulled or tied Low to VSS (GND), unless the NT PCI-to-PCI bridge between the internal Virtual PCI Bus and the NT Port Virtual Interface must be disabled for software compatibility to earlier NT mode switches.* *If NT mode is not enabled, optionally, this input can remain unconnected, because the internal pull-up resistor holds the input High.* Allows the NT function to be logically placed on the internal Virtual PCI Bus, or behind the PCI-to-PCI bridge for that Port. This input maps to the **Debug Control** register *NT P2P Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[6]). This signal and its corresponding register bit must ***not*** be toggled at runtime. **It is important that STRAP_NT_P2P_EN# is pulled or tied High or Low with a resistor. Active drivers should not be used, because STRAP_NT_P2P_EN# is used as an output in certain modes of operation.** L = Enables NT PCI-to-PCI bridge mode, if NT mode is enabled (pulled or tied Low to VSS (GND)) H = Disables NT PCI-to-PCI bridge mode, if NT mode is enabled (default; the PEX 8604 is in Legacy NT mode, if NT mode is enabled) (pulled or tied High to VDD25)

Table 3-6. Strapping Signals – 28 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_NT_UPSTRM_PORTSEL[3:0]	I	M3, K3, J2, J3	**Select Upstream Non-Transparent Port (4 Balls)** Select any Port as the upstream NT Port. The STRAP_NT_UPSTRM_PORTSEL[3:0] inputs can be overridden by the serial EEPROM value for the **Debug Control** register *NT Port Number* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[27:24]). **If the Debug Control register is programmed by serial EEPROM, that must be the first serial EEPROM entry.** I^2C can also change which Port is configured to be the NT Port, by writing to the **Debug Control** register. I^2C should first Set the Port's **Even/Odd Port Disable** register *Disable Port x* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[2, 0], and Odd Ports, offset 234h[2, 0]), to prevent linkup and Host enumeration. After I^2C re-configures the PEX 8604, I^2C should lastly Clear the upstream Port's *Disable Port x* bit, to enable linkup and allow subsequent Host enumeration. Software can also change which Port is configured to be the NT Port, by writing to the **Debug Control** register, if the register's *Hardware/Software Configuration Mode Control* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[15]) is already Set. All other encodings are ***reserved***. Refer to Section 14.10, "Port Programmability," for further details. LLLL = Port 0 LLLH = Port 1 LHLL = Port 4 LHLH = Port 5 ***Note:*** *If NT mode is not used (STRAP_NT_ENABLE#=H) and/or the serial EEPROM and/or I^2C programs NT mode (**Debug Control** register NT Mode Enable bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[18]) is Set (overriding STRAP_NT_ENABLE#)), value should be HH and/or if the **Debug Control** register is programmed by serial EEPROM (overriding STRAP_NT_UPSTRM_PORTSEL[3:0]), field [27:24] should be programmed to Fh.*
STRAP_PLL_BYPASS#	I	M12	***Factory Test Only*** Must be pulled or tied High to VDD25.

Table 3-6. Strapping Signals – 28 Balls *(Cont.)*

<table>
<tr><th>Signal Name</th><th>Type</th><th>Location</th><th>Description</th></tr>
<tr><td>STRAP_PORTCFG[1:0]</td><td>I</td><td>B2, A1</td><td>Strapping Signals to Select Port Configuration (Quantity of Enabled Ports (2, 3, or 4), and Maximum Quantity of Lanes for Each Specific Port) (2 Balls)
Defines the enabled Port Numbers and their Link widths. Programs the Port Configuration register Port Configuration field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0]) default value.
LL = x1, x1, x1, x1
LH = x2, x1, x1
HL = x2, x2
HH = Reserved
All other encodings are reserved.</td></tr>
<tr><td>STRAP_PROBE_MODE#</td><td>I</td><td>K13</td><td>Factory Test Only
Must be pulled or tied High to VDD25.</td></tr>
<tr><td>STRAP_RESERVED17#</td><td>I</td><td>F4</td><td>Factory Test Only
Must be pulled or tied High to VDD25.</td></tr>
<tr><td>STRAP_RESERVED16</td><td>I</td><td>D13</td><td>Factory Test Only
Must be tied directly to VSS (GND).</td></tr>
<tr><td>STRAP_SERDES_MODE_EN#</td><td>I</td><td>C4</td><td>Factory Test Only
Must be pulled or tied High to VDD25.</td></tr>
<tr><td>STRAP_SMBUS_EN#</td><td>I
PU</td><td>L1</td><td>System Management Bus Enable
Selects the I²C or SMBus protocol, and defines the default SMBus Configuration register SMBus Enable bit (Port 0, offset 344h[0], respectively) value, as listed below.
<table>
<tr><th>STRAP_SMBUS_EN# Input State</th><th>SMBus Enable Value</th></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td></tr>
</table>
When pulled or tied Low to Ground, enables SMBus Slave protocol on the I2C_SCL0 and I2C_SDA0 2-wire bus. ARP is enabled if I2C_ADDR2 is Low when sampled at the time PEX_PERST# input de-asserts.
When pulled or tied High to VDD25, enables I²C Slave protocol on the I2C_SCL0 and I2C_SDA0 2-wire bus.</td></tr>
<tr><td>STRAP_SPARE1#</td><td>I/O
PU</td><td>L2</td><td>Factory Test Only
Pull or tie High to VDD25 for standard operation.</td></tr>
<tr><td>STRAP_SPARE0#</td><td>O
PU</td><td>K2</td><td>Factory Test Only
Do not connect this ball to board electrical paths.</td></tr>
</table>

Table 3-6. Strapping Signals – 28 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_SSC_ISO_ENABLE#	I	M4	**Spread Spectrum Clocking (SSC) Crossing Enable** Allows the SSC REFCLK clock source on upstream Port 0, with a x2 Link width and Constant Frequency Clocking (CFC) REFCLK source on downstream devices. (Refer to Chapter 17, "Dual Clocking Support," for further details.) L = Enabled (pulled or tied Low to VSS (GND)) H = Disabled (pulled or tied High to VDD25)
STRAP_TESTMODE[3:0]	I	N13, M14, N14, P13	***Factory Test Only* (4 Balls)** Must be pulled or tied High to VDD25.
STRAP_UPCFG_TIMER_EN#	I PU	C1	**Link Upconfigure Timer Enable** This input maps to the **Debug Control** register *UPCFG Timer Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[4]). STRAP_UPCFG_TIMER_EN# and the *UPCFG Timer Enable* bit must ***not*** be toggled at runtime. When STRAP_UPCFG_TIMER_EN# is pulled or tied High to VDD25, the Data Rate Identifier symbol in the TS Ordered-Sets always advertises support for both the Gen 2 data rate and Autonomous Change. When STRAP_UPCFG_TIMER_EN# is pulled or tied Low to VSS (GND), if this Link training sequence fails during the Configuration state, the next time the LTSSM exits the *Detect* state, TS Ordered-Sets advertise only the Gen 1 data rate, and no Autonomous Change support. If Link training continues to fail when the LTSSM is in the *Configuration* state, the LTSSM continues to alternate between Gen 1 and Gen 2 advertisement every time it exits the *Detect* state. ***Note: This feature should be enabled only if a non-compliant device will not linkup if these Data Rate Identifier bits are Set.***

Table 3-6. Strapping Signals – 28 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_UPSTRM_PORTSEL[3:0]	I	G2, H2, F1, F3	**Strapping Signals to Select Upstream Port (4 Balls)** The STRAP_UPSTRM_PORTSEL[3:0] inputs can be overridden by the serial EEPROM value for the **Debug Control** register *Upstream Port ID* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[11:8]). **If the Debug Control register is programmed by serial EEPROM, that must be the first serial EEPROM entry.** I^2C can also change which Port is configured to be the upstream Port, by writing to the **Debug Control** register. I^2C should first Set the Port's **Even/Odd Port Disable** register *Disable Port x* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[2, 0], and Odd Ports, offset 234h[2, 0]), to prevent linkup and Host enumeration. After I^2C re-configures the PEX 8604, I^2C should lastly Clear the upstream Port's *Disable Port x* bit, to enable linkup and allow subsequent Host enumeration. Software can also change which Port is configured to be the upstream Port, by writing to the **Debug Control** register, if the register's *Hardware/Software Configuration Mode Control* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[15]) is already Set. All other encodings are ***reserved***. Refer to Section 14.10, "Port Programmability," for further details. LLLL = Port 0 LLLH = Port 1 LHLL = Port 4 LHLH = Port 5

3.4.5 JTAG Interface Signals

The PEX 8604 includes five signals for performing Joint Test Action Group (JTAG) boundary scan, defined in Table 3-7. The JTAG interface is described in Section 18.8, "JTAG Interface."

Table 3-7. JTAG Interface Signals – 5 Balls

Signal Name	Type	Location	Description
JTAG_TCK	I	E13	**JTAG Test Clock Input** JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 20 MHz.
JTAG_TDI	I	D12	**JTAG Test Data Input** Serial input to the JTAG TAP Controller, for test instructions and data.
JTAG_TDO	O	E12	**JTAG Test Data Output** Serial output from the JTAG TAP Controller test instructions and data.
JTAG_TMS	I	D14	**JTAG Test Mode Select** Input decoded by the JTAG TAP Controller, to control test operations.
JTAG_TRST#	I	C13	**JTAG Test Reset** Active-Low input used to reset the Test Access Port. When JTAG functionality is not used, the JTAG_TRST# input should be driven Low, or pulled Low to VSS (GND) through a 1.5KΩ resistor, to place the JTAG TAP Controller into the *Test-Logic-Reset* state, which disables the test logic and enables standard logic operation. Alternatively, if JTAG_TRST# input is High, the JTAG TAP Controller can be placed into the *Test-Logic-Reset* state by initializing the JTAG TAP Controller's **Instruction** register to contain the *IDCODE* instruction, or by holding the JTAG_TMS input High for at least five rising edges of the JTAG_TCK input.

3.4.6 I2C/SMBus Slave Interface Signals

Table 3-8 defines the five signals that support the I2C/SMBus Slave interface. For further details, refer to Chapter 7, "I2C/SMBus Slave Interface Operation."

Table 3-8. I2C/SMBus Slave Interface Signals – 5 Balls

<table>
<tr><th>Signal Name</th><th>Type</th><th>Location</th><th>Description</th></tr>
<tr><td>I2C_ADDR[2:0]</td><td>I</td><td>G14, F11, G13</td><td>
I2C/SMBus Slave Address Bits 2 through 0 Inputs (3 Pins)

Used to define the default value of the three least significant bits of the PEX 8604 I2C/SMBus 7-bit Slave address, which is programmable in the I2C Configuration register Slave Address field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 294h[2:0], default value is 38h). If I2C or SMBus configuration is used, I2C_ADDR[2:0] should be strapped to a unique address, to avoid an address conflict with any other I2C/SMBus devices (on the same I2C Bus/SMBus segment) that have the upper four bits of their 7-bit I2C/SMBus Slave address also defined as value 0111b.

If I2C_ADDR[2:0] are left unconnected, the value of the lowest three bits is 111b (due to the internal pull-up resistors), and the 7-bit Slave address defaults to value 0111_111b. The eight possible default values for the Slave address are listed below.
<table>
<tr><th>I2C_ADDR[2:0] Values</th><th>Offset 294h[2:0] Value</th><th>Offset 294h[6:3] Value</th><th>I2C/SMBus Slave Address</th></tr>
<tr><td>000</td><td>000b</td><td rowspan="8">0111b</td><td>0111_000b</td></tr>
<tr><td>001</td><td>001b</td><td>0111_001b</td></tr>
<tr><td>010</td><td>010b</td><td>0111_010b</td></tr>
<tr><td>011</td><td>011b</td><td>0111_011b</td></tr>
<tr><td>100</td><td>100b</td><td>0111_100b</td></tr>
<tr><td>101</td><td>101b</td><td>0111_101b</td></tr>
<tr><td>110</td><td>110b</td><td>0111_110b</td></tr>
<tr><td>111</td><td>111b</td><td>0111_111b</td></tr>
</table>

When SMBus is enabled (SMBus Configuration register SMBus Enable bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 344h[0]) is Set (the default value when STRAP_SMBUS_EN# is sampled and latched Low at PEX_PERST# input de-assertion):

I2C_ADDR[1:0] define the two least significant bits of the SMBus Slave Address,
Bit 2 of the SMBus Slave Address defaults to value 0, and
I2C_ADDR0 input defines the default value of the SMBus Configuration register ARP Disable bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 344h[8]), to enable (0) or disable (1) SMBus Address Resolution Protocol (ARP).

I2C_ADDR[2:0] require external pull-up or pull-down termination resistors. If I2C is not used, external termination is strongly recommended, to prevent possible Input buffer oscillation.
</td></tr>
</table>

Table 3-8. I²C/SMBus Slave Interface Signals – 5 Balls *(Cont.)*

Signal Name	Type	Location	Description
I2C_SCL0	OD	F14	**I²C/SMBus Serial Clock Line** I²C/SMBus Clock line. Data on the I²C Bus can be transferred at rates of up to 100 kbit/s (Standard mode). **I2C_SCL0 requires an external pull-up resistor.** ***Note:*** *The PEX 8604 I²C/SMBus Slave Interface can stretch the Low period of the I²C/SMBus clock while a simultaneous in-band Request that also targets PEX 8604 registers is being processed.*
I2C_SDA0	OD	F12	**I²C/SMBus Serial Data I/O** Transmits and receives I²C/SMBus data during I²C/SMBus accesses to PEX 8604 registers. **I2C_SDA0 requires an external pull-up resistor.**

3.4.7 Device-Specific Signals

Table 3-9 defines the Device-Specific signals – signals that are unique to the PEX 8604.

Table 3-9. Device-Specific Signals – 26 Balls

Signal Name	Type	Location	Description
FATAL_ERR#	O	B13	**Fatal Error Output** Asserted Low when a Fatal error is detected in the PEX 8604 and the following conditions exist (all the same conditions that are required to send a Fatal Error Message to the Host): • Specific error is defined as *Fatal* in the **Uncorrectable Error Severity** register (offset FC0h), and • Reporting of the specific error condition is enabled, not masked by the **Uncorrectable Error Mask** register's (offset FBCh) corresponding *Interrupt Mask* bit, and • **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]) –or– **PCI Command** register *SERR# Enable* bit (offset 04h[8]) is Set The **Device Status** register *Fatal Error Detected* bit (offset 70h[18]) is Set, and the specific error is flagged in the **Uncorrectable Error Status** register (offset FB8h).
GPIO[30, 29, 16:0]	I/O PU	A2, D3, K12, N2, M2, L3, P1, P2, M1, K1, H1, J1, J4, F2, E1, E2, E3, D1, D2	**General-Purpose I/O (19 Balls)** Default functionality is determined at Fundamental Reset; however, functionality can be switched by programming the **GPIO** registers by way of serial EEPROM, I^2C/SMBus, and/or software. GPIO[30, 29, 16:0] provide GPIO input functionality, by default, when the STRAP_TESTMODE[3:0] inputs, sampled at Fundamental Reset (PEX_PERST# input de-assertion), are a value of 1111b (Fh). Alternatively, when the STRAP_TESTMODE[3:0] inputs, sampled at Fundamental Reset, are a value of 1100b (Ch), GPIO[5, 4, 1, 0] function as Serial Hot Plug PERST# Reset outputs, by default, for the corresponding Ports that include an external I^2C I/O Expander. If an external I^2C I/O Expander is not present for a Port, the corresponding GPIO[5, 4, 1, 0] output remains Low (the Serial Hot Plug PERST# output for that Port is ***not*** de-asserted). If Serial Hot Plug is implemented (using external I^2C I/O Expanders), it is recommended that the GPIO[5, 4, 1, 0] signals be strapped as Serial Hot Plug PERST# Reset outputs and routed to the slots, rather than using the PERST# outputs from the I^2C I/O Expanders.

Table 3-9. Device-Specific Signals – 26 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_INTA#	OD	J12	**Interrupt Output** PEX_INTA# Interrupt output is enabled if: • INT*x* Messages are enabled (**PCI Command** register *Interrupt Disable* bit, offset 04h[10], is Cleared), and MSIs are disabled (**MSI Control** register *MSI Enable* bit, offset 48h[16], is Cleared) • PEX_INTA# output (**ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for x Interrupt* bit(s), offset 1C8h[7, 6, 5, and/or 4]) is enabled (refer to the register description, for Port associations) The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources: • Conventional PCI INT*x* Message generation • Native MSI transaction generation • Device-Specific PEX_INTA# assertion PEX_INTA# assertion (Low) indicates that one or more of the following events and/or errors (if not masked) were detected: • Hot Plug or Link State events • PCI Express Hot Plug events • General-Purpose Input Interrupt events • Device-Specific errors • Device-Specific NT Port Link Interface errors and events • NT-Virtual Doorbell events • NT-Link Doorbell events Refer to Section 10.4, "PEX_INTA# Interrupts," for details.
PEX_LANE_GOOD[5, 4, 1, 0]#	I/O PU	B14, B1, M13, P14	**Active-Low PCI Express Lane Status Indicator Outputs for Lanes [5, 4, 1, 0] (4 Balls)** Directly drives the common-anode LED module. PEX_LANE_GOOD[5, 4, 1, 0]# LED behavior: • **Off** – Lane is disabled • **On** – Lane is enabled, 5.0 GT/s • **Blinking, 0.5 seconds On, 0.5 seconds Off** – Lane is enabled, 2.5 GT/s, reduced Lanes are up
PEX_NT_RESET#	O	L13	**Active-Low Output Used to Propagate Reset in NT Mode** Pulse width is 1 µs.

3.4.8 External Resistor Signals

Table 3-10. External Resistor Signals – 4 Balls

Signal Name	Type	Location	Description
REXT_A[1:0]	A	B8, P7	**External Resistor Balls (2 Balls)** One pair per SerDes block (paired with the "B" signal). **An external 1.43KΩ 1% resistor must be attached between each REXT_A and REXT_B pair.** **Do not connect to any other signal, power, nor ground.**
REXT_B[1:0]	A	A8, N7	**External Resistor Balls (2 Balls)** One pair per SerDes block (paired with the "A" signal). **An external 1.43KΩ 1% resistor must be attached between each REXT_A and REXT_B pair.** **Do not connect to any other signal, power, nor ground.**

3.4.9 No Connect Signals

Caution: ***Do not connect these balls to board electrical paths. These balls are internally connected to the device.***

Table 3-11. No Connect Signals – 25 Balls

Signal Name	Type	Location	Description
N/C	***Reserved***	A3, A4, A5, A6, A14, B3, B4, B5, B6, C2, C7, L12, L14, M8, N1, N9, N10, N11, N12, P9, P10, P11, P12	**No Connect (23 Balls)** Do not connect these balls to board electrical paths.
THERMAL_DIODEn	***Reserved***	C12	**No Connect** ***Factory Test Only*** Do not connect this ball to board electrical paths.
THERMAL_DIODEp	***Reserved***	A13	**No Connect** ***Factory Test Only*** Do not connect this ball to board electrical paths.

3.4.10 Power and Ground Signals

Table 3-12. Power and Ground Signals – 75 Balls

Signal Name	Type	Location	Description
VDD10	CPWR	D5, D6, D9, D10, E4, E11, G4, G11, H4, H11, K4, K11, L5, L6, L9, L10	**1.0V ±5% Power for Core and SerDes Digital Logic (16 Balls)**
VDD10A	APWR	D7, D8, L7, L8	**1.0V ±5% Power for SerDes Analog Circuits (4 Balls)**
VDD25	I/OPWR	D4, D11, L4, L11	**2.5V ±10% Power for I/O Logic Functions (4 Balls)**
VDD25A	PLLPWR	C8, G3, G12, M7	**2.5V ±10% Power for Phase-Locked Loop (PLL) Circuits (4 Balls)**
VSS	GND	C5, C6, C9, C10, C11, H3, M5, M6, M9, M10, M11	**Ground Connections (11 Balls)**
VSS_THERMAL	Thermal-GND	E5, E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10	**Thermal-Ball Ground Connection (36 Balls)**

3.5 Physical Layout

Figure 3-1. PEX 8604 Physical Ball Assignment (See-Through Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	STRAP_PORTCFG0	GPIO30	N/C	N/C	N/C	N/C	PEX_REFCLK_CFCn	REXT_B1	PEX_PETp5	PEX_PERp5	PEX_PETp4	PEX_PERp4	THERMAL_DIODEp	N/C	A
B	PEX_LANE_GOOD4#	STRAP_PORTCFG1	N/C	N/C	N/C	N/C	PEX_REFCLK_CFCp	REXT_A1	PEX_PETn5	PEX_PERn5	PEX_PETn4	PEX_PERn4	FATAL_ERR#	PEX_LANE_GOOD5#	B
C	STRAP_UPCFG_TIMER_EN#	N/C	STRAP_FAST_BRINGUP#	STRAP_SERDES_MODE_EN#	VSS	VSS	N/C	VDD25A	VSS	VSS	VSS	THERMAL_DIODEn	JTAG_TRST#	SHPC_INT#	C
D	GPIO1	GPIO0	GPIO29	VDD25	VDD10	VDD10	VDD10A	VDD10A	VDD10	VDD10	VDD25	JTAG_TDI	STRAP_RESERVED16	JTAG_TMS	D
E	GPIO4	GPIO3	GPIO2	VDD10	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VDD10	JTAG_TDO	JTAG_TCK	I2C_SDA1	E
F	STRAP_UPSTRM_PORTSEL1	GPIO5	STRAP_UPSTRM_PORTSEL0	STRAP_RESERVED17#	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	I2C_ADDR1	I2C_SDA0	I2C_SCL1	I2C_SCL0	F
G	STRAP_NT_P2P_EN#	STRAP_UPSTRM_PORTSEL3	VDD25A	VDD10	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VDD10	VDD25A	I2C_ADDR0	I2C_ADDR2	G
H	GPIO8	STRAP_UPSTRM_PORTSEL2	VSS	VDD10	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VDD10	STRAP_NT_ENABLE#	PEX_PERST#	EE_DO	H
J	GPIO7	STRAP_NT_UPSTRM_PORTSEL1	STRAP_NT_UPSTRM_PORTSEL0	GPIO6	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	STRAP_DEBUG_SEL0	PEX_INTA#	EE_CS#	EE_SK	J
K	GPIO9	STRAP_SPARE0#	STRAP_NT_UPSTRM_PORTSEL2	VDD10	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VSS_THERMAL	VDD10	GPIO16	STRAP_PROBE_MODE#	EE_DI	K
L	STRAP_SMBUS_EN4#	STRAP_SPARE1#	GPIO13	VDD25	VDD10	VDD10	VDD10A	VDD10A	VDD10	VDD10	VDD25	N/C	PEX_NT_RESET#	N/C	L
M	GPIO10	GPIO14	STRAP_NT_UPSTRM_PORTSEL3	STRAP_SSC_ISO_ENABLE#	VSS	VSS	VDD25A	N/C	VSS	VSS	VSS	STRAP_PLL_BYPASS#	PEX_LANE_GOOD1#	STRAP_TESTMODE2	M
N	N/C	GPIO15	PEX_PERn0	PEX_PETn0	PEX_PERn1	PEX_PETn1	REXT_B0	PEX_REFCLKp	N/C	N/C	N/C	N/C	STRAP_TESTMODE3	STRAP_TESTMODE1	N
P	GPIO12	GPIO11	PEX_PERp0	PEX_PETp0	PEX_PERp1	PEX_PETp1	REXT_A0	PEX_REFCLKn	N/C	N/C	N/C	N/C	STRAP_TESTMODE0	PEX_LANE_GOOD0#	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

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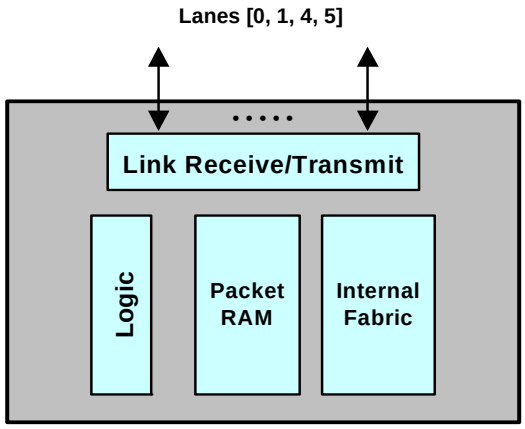
Chapter 4 Functional Overview

4.1 Hardware Architecture

The PEX 8604 is designed with a flexible, modular architecture. The four PCI Express Lanes are connected to one another by the internal fabric to the central RAM. Figure 4-1 provides a block diagram of the PEX 8604.

Figure 4-1. PEX 8604 Block Diagram



4.1.1 Port Functions

Each Port implements the *PCI Express Base r2.0* Physical, Data Link, and Transaction Layers (PHY, DLL, and TL, respectively). The PEX 8604 supports four integrated Serializer/De-Serializer (SerDes) modules, which provide the four PCI Express hardware interface Lanes. The Lanes can be combined, for a total of two to four Ports.

4.1.1.1 Port Configurations

The upstream and downstream Ports' Link widths are initially defined by the STRAP_PORTCFG[1:0] inputs, which are pulled or tied High to VDD25 or Low to VSS (GND). The serial EEPROM option can be used to re-configure the Ports, with the options defined in Table 4-1. Serial EEPROM configuration occurs following a Fundamental Reset, and overrides the configuration defined by the STRAP_PORTCFG[1:0] inputs at that time. Port configuration can also be changed through the I^2C Slave interface. The final Link width can be automatically negotiated down from the programmed width, through Link-width negotiation for linkup to a device with fewer Lanes. The narrowest Port on one end of the Link determines the maximum Link width. Additionally, if a connection is broken on one of the Lanes, the training sequence removes the broken Lane and negotiates to a narrower Link width. A x2 Port can negotiate down to x1.

If the Port cannot train to x1 (Lane 0 is broken), the Port reverses its Lanes and attempts to retrain. *For example*, a x2 Port that cannot train to x2 attempts to negotiate down to x1; if x1 linkup fails, the Port reverses its Lanes and re-attempts linkup negotiation. Either the lowest Lane (Lane 0) or highest Lane (if Lanes are reversed) of the programmed Link width must connect to the other device's Lane 0.

Each Port can run independently at Gen 1 (2.5 GT/s) or Gen 2 (5.0 GT/s) Link speed.

Table 4-1 defines the PEX 8604 Port and Lane configurations. The Lanes are assigned to each enabled Port, in sequence. Ports that are not configured nor enabled are invisible to software.

Table 4-1. Port Configurations

STRAP_PORTCFG[1:0]	Port 0	Port 1	Port 4	Port 5
(default) 00b	x1	x1	x1	x1
(Lane)	0	4	1	5
01b	x2	x1		x1
(Lane)	0-1	4		5
10b	x2	x2		
(Lane)	0-1	4-5		

4.1.1.2 Port Numbering

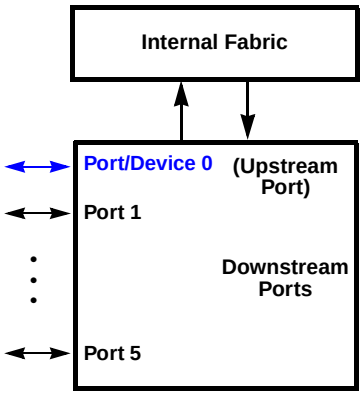
The Port Numbers are 0, 1, 4, and 5, as defined in Table 4-1 and illustrated in Figure 4-2. (Refer to Section 4.1.1.1.)

The Port Numbers have a direct relationship to the downstream Ports for the PCI Device Number assigned to the internal PCI-to-PCI bridges on the internal virtual PCI Bus. *For example*, if Port 1 is a downstream Port, the PCI-to-PCI bridge associated with that Port is Device Number 1. Each downstream Device Number matches its corresponding Port Number. *For example*, if Port 0 is the upstream Port, Ports 1, 4, and 5 are the available downstream Ports, when all Ports are enabled. The Device Numbers for the PCI-to-PCI bridges implemented on the downstream Ports are 1, 4, and 5, respectively.

Any PEX 8604 Port can be configured as, or dynamically changed to be, the upstream Port (Port 0 is recommended). The PCI-to-PCI bridge implemented on the upstream Port does not assume a Device Number – it accepts the Device Number assigned by the upstream device. Generally, the upstream device assigns Device Number 0, according to the *PCI Express Base r2.0*.

Note: *In Figure 4-2, the downstream Port Numbers are only those defined in Table 4-1.*

Figure 4-2. Port Numbering Convention Example (When Port 0 Is Upstream Port)



4.2 PCI Express Link Functional Description

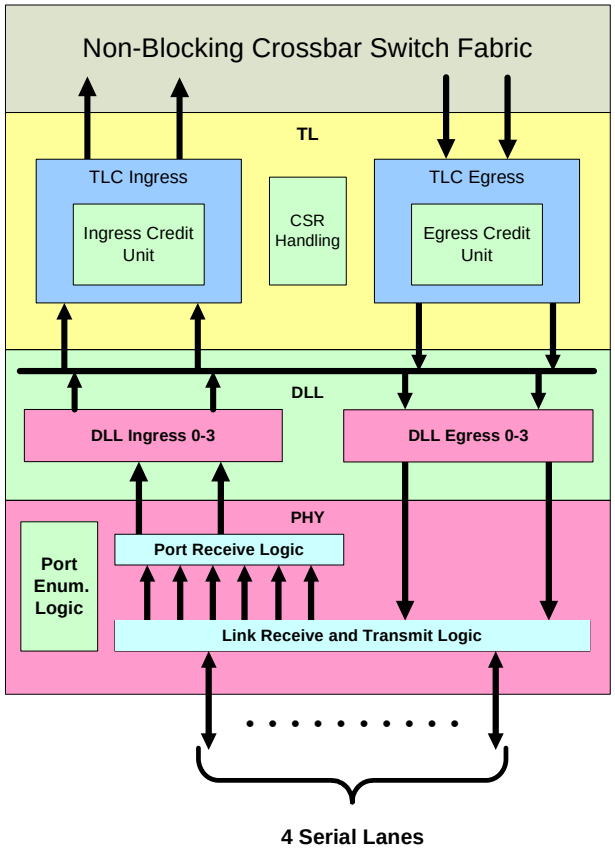
The PEX 8604 groups four SerDes together, which can comprise a total of two to four Ports. (Refer to Table 4-1.) The Ports forward ingress packets to the internal fabric and central RAM, and pull egress packets from the central RAM to send out of the PEX 8604.

The PEX 8604 implements the PCI Express PHY and DLL functions for each of its Ports, and aggregates traffic from these Ports onto a transaction-based, non-blocking internal crossbar fabric. All packet queuing and ordering aspects of this layer are handled by the Crossbar Switch Control blocks.

During system initialization, software initiates Configuration Requests that set up the PCI Express interfaces, Device Numbers, and Address maps across the various Ports. These maps are used to direct traffic between Ports during standard system operation. Traffic flow between Ports is supported through the central internal fabric.

At the top level, the PEX 8604 has a layered organization consisting of the PHY, DLL, and TL blocks, as illustrated in Figure 4-3. The PHY and DLL blocks have Port-specific data paths (one per PCI Express Port) that operate independently of one another. The Transaction Layer Control (TLC) ingress section of the TL block aggregates traffic for all ingress Ports, then sends the traffic to the internal crossbar fabric. The TLC egress section of the TL block accepts packets, by way of the internal crossbar fabric, from all ingress Ports, and schedules them to be sent out the appropriate egress Port.

Figure 4-3. PCI Express Block Diagram



4.3 Physical Layer

The Physical Layer (PHY) converts information received from the DLL into an appropriate serialized format and transmits it across the PCI Express Link. The PHY also receives the serialized input from the Serializer/De-Serializer (SerDes), converts it to parallel data (internal Data Bus), then writes it to the Transaction Layer Control (TLC) Ingress buffer.

The PHY includes all circuitry for PCI Express Link Interface operation, including:

- Driver and Input buffers
- Parallel-to-serial and serial-to-parallel conversion
- Phase-Locked Loops (PLLs) and clock circuitry
- Impedance Matching circuitry
- Interface Initialization and Maintenance functions

4.3.1 Physical Layer Features

The PHY module interfaces to the PCI Express Lanes and implements the PHY functions. The quantity of available PCI Express Ports is two to four, with a cumulative Lane bandwidth of x4. PHY functions include:

- SerDes modules, which provide all functions required by the *PCI Express Base r2.0*
- User-configurable Port division
- Link widths – x1 or x2
- Link speeds supported
  - 2.5 GT/s
  - 5.0 GT/s
- Hardware Link training and initialization
- Hardware detection of polarity reversal
- Hardware detection of Lane reversal
- Hardware Autonomous Speed Control supported
- Dynamic Link speed control supported
- Dynamic Link width supported
- Data scrambling/de-scrambling and 8b/10b encode/decode
- Packet framing
- Loopback Master and Slave support
- Programmable test pattern with SKIP Ordered-Set insertion and return data checking
- Receiver error checking (Elastic buffer over/underflow, disparity, and symbol encoding)
- Modified Compliance Pattern support with Receiver Error Counters, per Lane
- Link state Power Management (PM) – Supports L0, L0s, L1, L2/L3 Ready, and L3 Link PM states
- Supports cross-linked upstream Port and downstream Ports

4.3.2 Physical Layer Status and Command Registers

The PHY operating conditions are defined in:

- Section 13.14.2, "Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)"
- Section 13.16.13, "Device-Specific Registers – Physical Layer (Offsets B80h – C30h)"
- Section 13.16.15, "Device-Specific Registers – Physical Layer (Offsets E40h – EFCh)"

The System Host can track the Link operating status and re-configure Link parameters, by way of these registers.

4.3.3 Hardware Link Interface Configuration

The PHY can include up to four integrated SerDes modules, which are distributed among two SerDes quads (Quads 0 and 2) and provide the PCI Express hardware interface Lanes. The SerDes modules also provide all physical communication controls and functions required by the *PCI Express Base r2.0*, as well as the Links (clustered into Ports) that connect the PEX 8604 to other PCI Express devices.

The quantity of enabled Ports, and Link widths associated with those Ports, are configurable, on a Port-by-Port basis. Initial Port configuration is determined by the STRAP_PORTCFG[1:0] inputs, serial EEPROM, and/or auto Link-width negotiation. If the PEX 8604 Ports are configured using the auto-negotiation process, the Link widths can narrow or widen (by combining multiple adjacent Lanes).

4.4 Transaction Layer

The upper layer of the architecture is the Transaction Layer (TL). The TL assembles and disassembles TLPs, which are used to communicate transactions, *such as* Read and Write, as well as certain types of events. The TL also manages credit-based Flow Control (FC) for TLPs.

The TL supports four Address spaces – it includes the three PCI Address spaces (Configuration, Input/Output, and Memory) and adds a Message space. (Refer to Table 4-2.) This specification uses Message space to support all prior sideband signals, *such as* interrupts, Power Management (PM) Requests, and so forth, as in-band Message transactions. PCI Express Message transactions are considered *virtual wires* that support *virtual pins*. As virtual wires, Assert and De-assert Messages are sent when a triggering event changes the wire's state.

Table 4-2. Address Spaces Support Differing Transaction Types

Address Space	Transaction Types	Transaction Functions
Configuration	Read/Write	Device configuration or setup
Input/Output		Transfers data from/to an I/O space
Memory		Transfers data from/to a memory location
Message	Baseline/Virtual Wires	General-purpose Messages Event signaling (status, interrupts, and so forth)

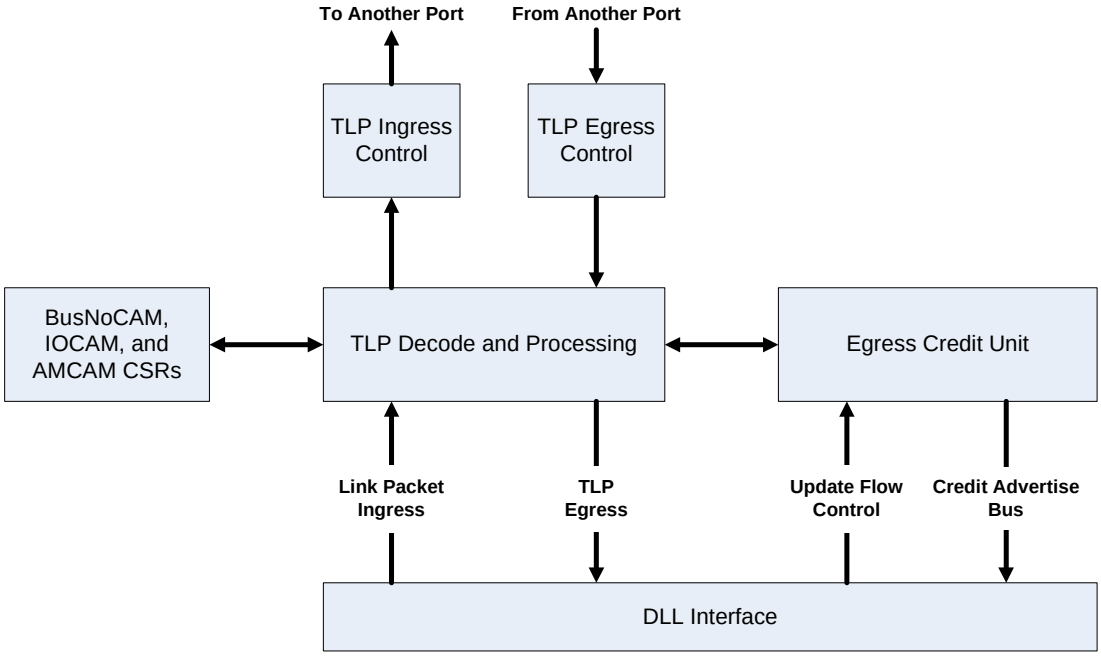
All Request packets requiring a Response packet are implemented as Split Transactions. Each packet has a unique identifier that enables Response packets to be directed to the correct originator. The packet format supports various forms of addressing, depending upon the transaction type – *Memory*, *I/O*, *Configuration*, or *Message*.

TL functions include:

- Decoding and checking rules for the incoming TLP
- Memory-Mapped Configuration Space register (CSR) access
- Checking incoming packets for malformed or unsupported packets
- Data Poisoning and end-to-end data integrity detection
- End-to-end Cyclic Redundancy Check (ECRC) of incoming packets
- Error logging and reporting for incoming packets
- TLP dispatching
- Write control to the packet RAM and packet Link List RAM
- Destination lookup and TC-VC mapping
- Shadow CSRs for BusNoCAM/IOCAM/AMCAM/TC-VC mapping
- Credit-based scheduling
- Pipelined full Split Transaction protocol
- PCI/PCI-X-compatible ordering
- Interrupt handling (INT*x* or Message Signaled Interrupts (MSIs))
- Power Management (PM) support
- Hot Plug and PCI Express Hot Plug event support
- Link State event support
- QoS support
- Ordering
- Ingress and Egress credit management

The hardware functions provided by the PEX 8604 to implement the *PCI Express Base r2.0* TL requirements are illustrated in Figure 4-4. The blocks provide a combination of ingress and egress control, as well as the data management at each stage within the flow sequence.

Figure 4-4. TL Controller



4.4.1 Locked Transactions

The PEX 8604 understands Locked transactions; however, it does not lock the resources. This is consistent with limitations for Locked transaction use, as outlined in the *PCI r3.0* (Appendix F, "Exclusive Accesses"), and prevents potential deadlock, as well as serious performance degradation, that could occur with Locked transaction use.

4.4.2 Relaxed Ordering

The PEX 8604 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, then that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled, by Setting the **Ingress Control Shadow** register *No Special Treatment for Relaxed Ordering Traffic* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 664h[5]).

4.4.3 TL Transmit/Egress Protocol – End-to-End Cyclic Redundancy Check

End-to-End Cyclic Redundancy Check (*ECRC*) is an optional 32-bit field appended to the end of the outgoing packet. ECRC is calculated over the entire packet, starting with the Header and including the Data Payload, except for the *EP* bit and bit 0 of the *Type* field, which are always considered to be a value of 1 for ECRC calculations. The *ECRC* field is transmitted, unchanged, as it moves through the fabric to the Completer device. The PEX 8604 checks the ECRC on all incoming TLPs, if enabled (Port's **Advanced Error Capabilities and Control** register *ECRC Check Enable* bit (offset FCCh[8]) is Set), and can optionally report detected errors. (When the ECRC is detected, the **Uncorrectable Error Status** register *ECRC Error Status* bit (offset FB8h[19]) can be used to log ECRC errors.)

Additionally, the PEX 8604 can optionally append ECRC to the end of internally generated TLPs, *such as* Interrupt and Error Messages, if enabled (Port's **Advanced Error Capabilities and Control** register *ECRC Generation Enable* bit, offset FCCh[6], is Set).

4.4.4 TL Receive/Ingress Protocol

The ingress side TL collects and stores inbound TLP traffic in the packet RAM. The incoming data is checked for ECRC errors, valid type field, length matching the Header *Transfer Size* field, and other TLP-specific errors defined by the *PCI Express Base r2.0*.

Header and Data Payload information is forwarded to the Source Scheduler, to be routed across the internal fabric, to the egress Port. When ECRC errors are detected, the packet is discarded.

4.4.5 Flow Control Credit Initialization

The initial quantity of VC0 Flow Control (FC) credits is advertised as programmed for each type of Header and Payload. After VC0 FC initialization is complete, the FC credits received are transferred to the TL egress. The TL ingress must schedule an UpdateFC Data Link Layer Packet (DLLP) for transmission, to increase the quantity of advertised credits. When enabled, the TL initiates flow credit initialization for VC1, following VC0 initialization.

4.4.6 Flow Control Protocol

The PEX 8604 implements FC protocol that ensures that the switch:

- Does not transmit a TLP over a Link to a remote Receiver, unless the receiving device has sufficient VC Buffer space to accommodate the packet
- Generates FC credit updates to the remote Transmitter, to replace credits used to send TLPs to the PEX 8604

This FC is automatically managed by the hardware, and is transparent to software. Software is used only to enable additional Buffer space, to supplement the initial default buffer assignment.

The initial default FC credits, which are enabled after Link training, allow TLP traffic immediately after Link training completes. The Configuration transactions are the first transactions to use the default VC credits, to set up the initial device operating modes and capabilities.

The TL Ingress Credit Unit transmits DLLPs (referred to as *FC packets*) that update the FC to the remote Transmitter device, on a periodic basis. The DLLPs contain FC credit information that updates the Transmitter regarding the amount of available Buffer space in the PEX 8604.

The TL Egress Credit Unit receives DLLPs from the remote device, indicating the amount of Buffer space available in the remote Receiver. The unit uses this credit information to schedule the sending of TLPs to the remote device.

4.5 PCI-Compatible Software Model

The PEX 8604 can be thought of as a hierarchy of PCI-to-PCI bridges, with one upstream PCI-to-PCI bridge and one or more downstream PCI-to-PCI bridges connected by an internal virtual bus. (Refer to Figure 4-5.) PCI-to-PCI bridges are compliant with the PCI and PCI Express system models. Figure 4-5 illustrates the concept of hierarchical PCI-to-PCI bridges, with the bus in the middle being the internal virtual PCI Bus. The Configuration Space registers (CSRs) in the upstream PCI-to-PCI bridge are accessible by Type 0 Configuration Requests that target the upstream bus interface. The upstream Port captures the Type 0 Configuration Write Target Bus Number and Device Number. The upstream Port uses this Captured Bus Number and Captured Device Number as part of the Requester ID and Completer ID for the Requests and Completions generated by the upstream Port.

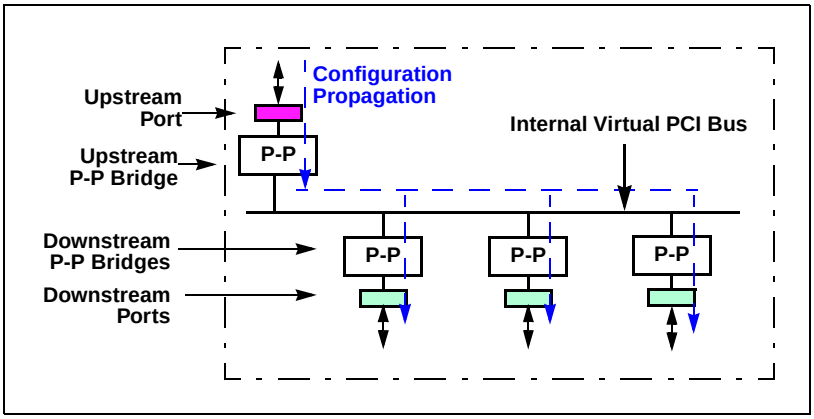
The CSRs in the downstream Port PCI-to-PCI bridges are accessible by Type 1 Configuration Requests received at the upstream Port that target the internal virtual PCI Bus, by having a Bus Number value that matches the upstream bridge's Secondary Bus Number value. Each downstream bridge is associated with a unique Device Number, as explained in Section 4.1.1.2.

The CSRs of downstream devices are hit in two ways. If the Configuration Request matches the PEX 8604 downstream Port Secondary Bus Number, the PEX 8604 converts the Type 1 Configuration Request into a Type 0 Configuration Request. However, if the Bus Number does ***not*** match the Secondary Bus Number, but falls within the Subordinate Bus Number range, the Type 1 Configuration Request is forwarded out of the PEX 8604, unchanged. A Type 1 Configuration Request that targets a Bus Number that is not within range is invalid, and is terminated by the PEX 8604 upstream Port as an Unsupported Request (UR).

After all PCI devices have been located and each assigned a Bus Number and Device Number, software can assign a Memory map and I/O map. Requests (Memory or I/O) go downstream if they fall within a bridge's Base and Limit range. In the PEX 8604, each downstream bridge has its own Base and Limit. Alternatively, Requests (Memory or I/O) go upstream if they do not target anything within the upstream bridge's Base and Limit range.

Completions are routed by the Bus Number established in the Configuration registers. If the Bus Number is in the Secondary or Subordinate range, the packet goes downstream; otherwise, the packet goes upstream.

Figure 4-5. PEX 8604 System Configuration Propagation



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Chapter 5 Reset and Initialization

5.1 Reset

This section describes the resets that the PEX 8604 supports. (Refer to Table 5-1.) *Reset* is a mechanism that returns a device to its initial state. Reset is propagated from upstream to downstream. Hardware or software mechanisms can trigger three different levels of reset – Fundamental, Hot, or Secondary Bus (each is described in the sections that follow). The re-initialized states following a reset vary, depending upon the reset type.

Table 5-1. Reset Summary

PCI Express Definition	Reset Source	Impact to Different Internal Components (upon De-Assertion)	Impact to Internal Registers
Fundamental Reset • Cold Reset • Warm Reset	PEX_PERST# input assertion	• Initializes everything • Serial EEPROM contents are loaded • HwInit types are evaluated	All registers are initialized
Hot Reset	• TS Ordered-Set *Hot Reset* bit is Set, at the upstream Port • Upstream Port enters the *DL_Down* state	• Initializes all Half-Station Ports • Initializes internal credits and queues • Selectively reloads serial EEPROM contents	All registers, except: • Port Configuration registers • All Sticky bits not affected by Hot Reset (HwInit, ROS, RW1CS, RWS)
Secondary Bus Reset	Downstream Port's **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) is Set	• Downstream Port PHY generates a Hot Reset • Downstream Port Data Link Layer (DLL) is down • Downstream Port Transaction Layer (TL) is initialized, exhibits DL_Down behavior, and TLP Requests to that Port are dropped • Upstream Port and downstream Ports drain traffic, corresponding to the DL_Down condition on the downstream Port, and initialize credits corresponding to that downstream Port	Does not affect registers (other than to initialize credits)
	Upstream Port's **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) is Set	• All downstream Ports propagate a Hot Reset • DLL of each downstream Port is down • TL of each downstream Port is initialized, exhibits DL_Down behavior, and drops TLP Requests that target downstream Ports • Upstream Port TL exhibits DL_Up behavior	Initializes downstream Ports registers to default values

5.1.1 Fundamental Reset

Fundamental Reset is a hardware mechanism defined by the *PCI Express Base r2.0*, Section 6.6. Fundamental Reset input, through the PEX_PERST# signal, resets all Port states and Configuration registers to default conditions. Reset remains asserted, until the Port's bit is Cleared.

5.1.2 Hot Reset

Hot Reset is an in-band Reset that propagates from an upstream PCI Express Link to all its Transparent downstream Ports, through the Physical Layer (PHY) mechanism. The PHY mechanism communicates a reset to downstream devices through a training sequence (TS1/TS2 Ordered-Set, in which the *Hot Reset* Training Control Bit is Set). Hot Reset is also referred to as a *Soft Reset*.

A Hot Reset initializes all Ports, resets registers that are not defined as Sticky, and resets the serial EEPROM logic to reload registers (except Port Configuration registers) from serial EEPROM, if present[a]. Hot Reset does not reset the Clock logic, and can be caused by any of the following:

- Upstream Port PHY receives two consecutive TS1 Ordered-Sets in which the *Hot Reset* Training Control Bit is Set. Hot Reset is generated from an upstream device, *such as* by Setting its **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).
- Upstream Port unexpectedly enters the *DL_Down* state.

  Exception – If the upstream Port Link is in the L2 Link PM state and the Link goes down, the downstream Ports do ***not*** generate Hot Reset.
- Upstream Port PHY enters either the *Loopback* or *Disabled* state, upon receiving two consecutive TS1 or TS2 Ordered-Sets in which either the *Loopback* or *Disable Link* Training Control Bit is Set, respectively. An upstream device can generate the *Disable Link* sequence, by Setting its **Link Control** register *Link Disable* bit (offset 78h[4]).

5.1.3 Secondary Bus Reset

Any virtual upstream or downstream PCI-to-PCI bridge within the PEX 8604 can reset its downstream hierarchy, by Setting the **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).

When the *Secondary Bus Reset* bit is Set on the upstream Port, all the downstream Ports are initialized to their default states, as defined by the *PCI Express Base r2.0*. Each of the Transparent downstream Ports generates an in-band Hot Reset onto its downstream Links (the NT Port Link Interface does not generate Hot Reset). In addition, writable registers defined by the *PCI Express Base r2.0*, in all downstream Ports, are initialized to default values (upstream Port registers are not reset, and the serial EEPROM does not reload registers).

When the *Secondary Bus Reset* bit is Set on a downstream Port, that Port is reset to its default state as defined by the *PCI Express Base r2.0*, and generates an in-band Hot Reset onto its downstream Link. The registers of that downstream Port are not affected.

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*a. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its Status register. This value is copied to the **Serial EEPROM Status** register Status Data from Serial EEPROM fields (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 260h[31:24]). Serial EEPROM presence is reported in the register's EepPrsnt[1:0] field [17:16]; a value of 01b or 11b indicates that the serial EEPROM is present.*

5.1.4 Register Bits that Affect Hot Reset

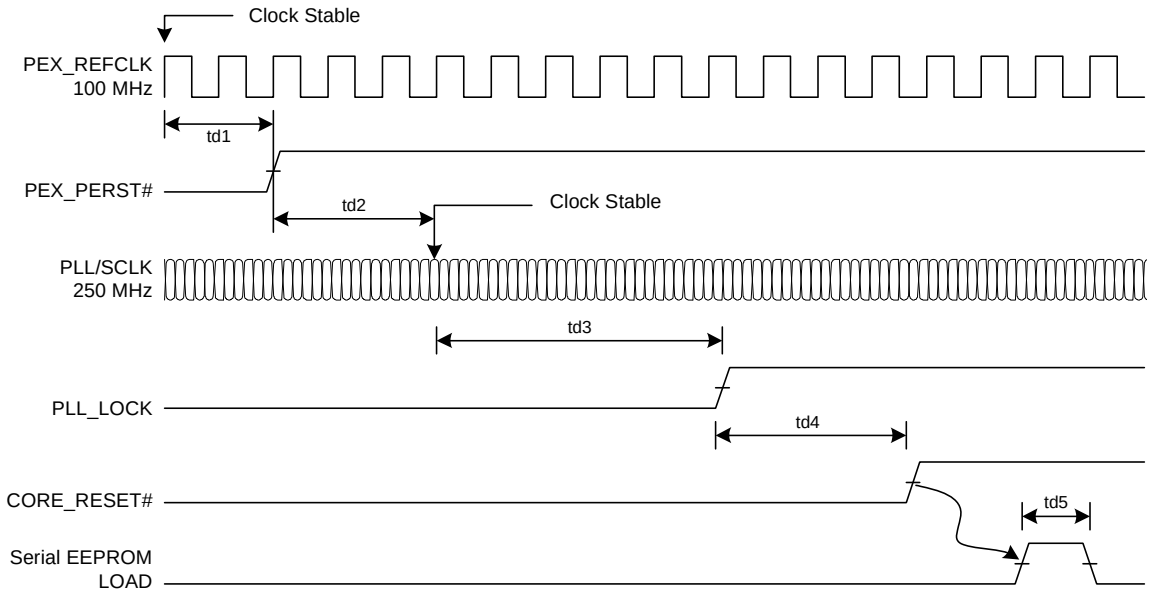
Setting the **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) generates a Hot Reset to downstream Ports and downstream devices.

5.1.5 Reset and Clock Initialization Timing

Table 5-2. Reset and Clock Initialization Timing

Symbol	Description	Typical Delay
td1	REFCLK stable to PEX_Reset release time	100 µs
td2	PEX_Reset release to Reset de-bounce	1.32 ms
td3	Reset de-bounce to Phase-Locked Loop (PLL) Lock	105 µs
td4	Reset de-bounce to Core Reset release	2.63 ms
td5	Serial EEPROM load time with no serial EEPROM present	17 µs

Figure 5-1. Reset and Clock Initialization Timing



5.2 Initialization Procedure

The PEX 8604 initialization process starts upon exit from a Fundamental Reset. There are two or more steps in the process, depending upon the availability of an external initialization serial EEPROM and I^2C.

The initialization sequence executed is as follows:

1. PEX 8604 reads the Strapping inputs, to determine the upstream Port (STRAP_UPSTRM_PORTSEL[3:0]) and Lane configuration (STRAP_PORTCFG[1:0]) of each enabled Port.
2. If a serial EEPROM is present, serial EEPROM data is downloaded to the PEX 8604 Configuration registers. The configuration from the Strapping inputs can be changed by serial EEPROM data.

   Alternatively, I^2C can be used to program all the registers (the same as would be done with the serial EEPROM), except, if PHY or DLL register values that affect SerDes parameters or Link initialization need to be changed, those registers must be programmed by serial EEPROM, so that the values are loaded prior to initial Link training. Because I^2C is relatively slow, the Links are usually up by the time the first I^2C Write occurs. The first I^2C command might be to block system access while the configuration is being changed, by disabling the upstream Port; Ports can be disabled by Setting the Port's **Even/Odd Port Disable** register *Disable Port x* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[2, 0] and Odd Ports, 234h[2, 0], respectively).

   Switch configuration, including Port Configuration (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0]) and/or upstream Port designation (**Debug Control** register *Upstream Port ID* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[11:8])) can be changed:

   – At runtime, by software, if the **Debug Control** register *Hardware/Software Configuration Mode Control* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[15]) is Set
   – By I^2C and/or serial EEPROM reload

   If the **Debug Control** register *Upstream Port ID* field value is to be changed, the register must be written twice, with *Factory Test Only* bit 7 Set in the first Write, and Cleared in the second Write. Changes take effect upon subsequent Hot Reset.

Note: *As described in Chapter 7, "I^2C/SMBus Slave Interface Operation," an external I^2C Master can send the register Read/Write Requests to PEX 8604 after reset. To prevent conflict, first disable the upstream Port, by Setting the Port's Disable Port x bit. Restoration of the upstream Port should be the last register Write of the entire I^2C programming procedure.*

3. After configuration from the Strapping inputs, serial EEPROM, and/or I^2C is complete, the PHY of the configured Ports attempts to bring up the Links. After both components on a Link enter the initial Link Training state, the components proceed through PHY Link initialization and then through Flow Control initialization for VC0 and VC1, preparing the DLL and TL to use the Link. following Flow Control initialization for VC0 and VC1, it is possible for VC0 and VC1 TLPs and DLL Packets (DLLPs) to be transmitted across the Link.

5.2.1 Default Port Configuration

The default upstream Port selection and overall Link width configuration is determined by Strapping inputs, which must be pulled or tied High to VDD25 or Low to Ground (VSS), to define the default device configuration. (Refer to Section 3.4.4, "Strapping Signals.") The configuration defined by the Strapping inputs can be changed by downloading serial EEPROM data, and/or by I^2C programming followed by a Hot Reset.

5.2.2 Default Register Initialization

Each PEX 8604 Port defined in the Port Configuration process has a set of assigned registers that control Port activities and status during standard operation. These registers are programmed to default/ initial values, as defined in:

- Chapter 13, "Transparent Port Registers"
- Chapter 15, "NT Port Virtual Interface Registers – NT Mode Only"
- Chapter 16, "NT Port Link Interface Registers – NT Mode Only"

Following a Fundamental Reset, the basic PCI Express Support registers are initially programmed to the values specified in the *PCI Express Base r2.0*. The Device-Specific registers are programmed to the values specified in their register description tables. These registers can be changed by loading new data with the attached serial EEPROM, the I^2C Slave interface, and/or by CSR accesses using Configuration or Memory Writes; however, registers identified as Read-Only (RO) ***cannot*** be modified by Configuration nor Memory Write Requests.

The Transparent Ports and NT Port support the following mechanisms for accessing registers by way of the TL, as described in:

- Section 13.4.1, "PCI r3.0-Compatible Configuration Mechanism"
- Section 13.4.2, "PCI Express Enhanced Configuration Access Mechanism"
- Section 13.4.3, "Device-Specific Memory-Mapped Configuration Mechanism"

For NT mode, refer also to Section 15.3.3 or Section 16.3.3, "Device-Specific Cursor Mechanism."

5.2.3 Device-Specific Registers

The Device-Specific registers are unique to the PEX 8604, and are not referenced in the *PCI Express Base r2.0*. The registers are organized into the following sections:

- Section 13.14, "Device-Specific Registers (Offsets 1C0h – 51Ch)"
- Section 13.16, "Device-Specific Registers (Offsets 530h – F8Ch)"

5.2.4 Serial EEPROM Load Time

Serial EEPROM initialization loads only the Configuration register data that is specifically programmed into the serial EEPROM. Registers that are not included in the serial EEPROM data are initialized to default register values.

Each register entry in the serial EEPROM consists of two Address bytes and four Data bytes (refer to Section 6.4, "Serial EEPROM Data Format"); therefore, each register entry (6 bytes, or 48 bits) requires 48 serial EEPROM clocks to download. Thus, at the serial EEPROM clock default frequency of 1 MHz, after initial overhead to read the **Serial EEPROM Status** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 260h) (16 serial EEPROM clocks, or 16 µs), plus another 40 serial EEPROM clocks (40 µs) to begin reading the register data, each register entry in the serial EEPROM requires 48 µs to download. A serial EEPROM containing 50 register entries (typical configuration, assuming the serial EEPROM is programmed only with non-default register values) and clocked at 1 MHz takes approximately 5.2 ms to load (16 + 40 + 48) x 50 µs (5,200 µs).

To reduce the serial EEPROM initialization time, the first register entry in the serial EEPROM can increase the clock frequency, by programming the **Serial EEPROM Clock Frequency** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 268h), to a value of 2h (5 MHz), or 3h (9.62 MHz), if the serial EEPROM supports the higher frequency at the serial EEPROM supply voltage (typically 2.5 to 3.3V). At 5-MHz clocking, the serial EEPROM load time for 50 register entries can be reduced to approximately 575 µs. Because the *PCI Express Base r2.0* allows a 20-ms budget for system hardware initialization, the default 1-MHz serial EEPROM clock is often sufficient when the quantity of Ports and registers programmed by serial EEPROM is relatively small.

For further details, refer to Chapter 6, "Serial EEPROM Controller."

5.2.5 I^2C Load Time

Initialization using I^2C is slower than serial EEPROM initialization, because the I^2C Slave interface operates at a lower clock frequency (100 KHz maximum) and the quantity of bits per Register access is increased (because the Device address is included in the bit stream). Writing one register using 100-KHz clocking takes approximately 830 µs (83 clock periods).

For further details, refer to Section 7.2, "I^2C Slave Interface."

Chapter 6 Serial EEPROM Controller

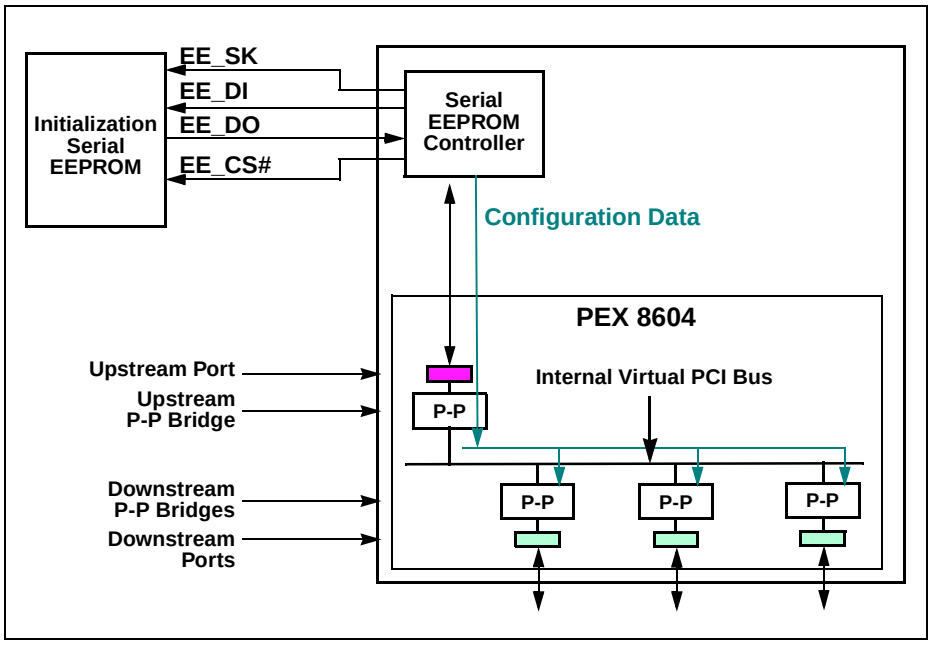
6.1 Overview

The PEX 8604 provides a Serial EEPROM Controller and interface to Serial Peripheral Interface (SPI)-compatible serial EEPROMs, as illustrated in Figure 6-1. This interface consists of a Chip Select, Clock and Write Data outputs, and a Read Data input, and operates at a programmable frequency of up to 17.86 MHz. The PEX 8604 supports serial EEPROMs that use 1-, 2-, or 3-byte addressing (2-byte addressing is recommended); the PEX 8604 automatically determines the appropriate addressing mode.

The controller provides access to non-volatile memory. This external memory can be used for three different purposes:

- The serial EEPROM can be used to store register data, for switch configuration and initialization. When a serial EEPROM device is connected to the PEX 8604, immediately after reset, the Serial EEPROM Controller reads data from the serial EEPROM that is used to update the PEX 8604 register default values.
- System or application data can be stored into, and read from, the serial EEPROM, by software, I^2C and/or SMBus, initiating random-access Read or Write Requests to the serial EEPROM.
- In NT mode, the serial EEPROM can provide up to 32 KB of Expansion ROM, for the NT Port Link Interface (default) or NT Port Virtual Interface. When software reads the Expansion ROM (starting at the Expansion ROM Base Address), the PEX 8604 reads from the serial EEPROM, to return the requested ROM image.

Figure 6-1. Serial EEPROM Connections



6.2 Features

- Detection of whether a serial EEPROM is present/not present
- Supports high-speed serial EEPROMs with Serial Peripheral Interface (SPI) interface
- Non-volatile storage for register default values loaded during Power-On Reset
- 4-byte Write/Read access to the serial EEPROM, through the upstream Port
- Serial EEPROM data format allows for loading registers by Port/Address location
- Required serial EEPROM size is dependent upon the quantity of registers being changed
- Automatic support for 1-, 2-, or 3-byte-addressable serial EEPROMs
- Manual override for quantity of serial EEPROM Address bytes
- Programmable serial EEPROM clock frequency
- Programmable serial EEPROM clock-to-chip select timings
- No Cyclic Redundancy Check (CRC), single *Valid* byte at start of serial EEPROM memory
- Supports Expansion ROM for the NT Port (***not supported*** for 1-byte address serial EEPROMs)

6.3 Serial EEPROM Load following Upstream Port Reset

The Serial EEPROM Controller performs a serial EEPROM download when the following conditions exist:

- Serial EEPROM is present[a], and
- Validation signature (first byte read from the serial EEPROM) value is 5Ah, and
- One of the following events occur:
  - PEX_PERST# is returned High, following a Fundamental Reset (*such as* a Cold or Warm Reset to the entire chip)
  - Hot Reset is received at the upstream Port (downloading upon this event can be optionally disabled, by Setting the **Debug Control** register *Disable Serial EEPROM Load on Hot Reset* and/or *Upstream Hot Reset Control* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[17 and/or 16], respectively))
  - Upstream Port exits a *DL_Down* state (downloading upon this event can be optionally disabled, by Setting the **Debug Control** register *Upstream Port and NT-Link DL_Down Reset Propagation Disable* and/or *Upstream Hot Reset Control* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[20 and/or 16], respectively))

*a. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its Status register. This value is copied to the **Serial EEPROM Status** register Status Data from Serial EEPROM fields (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 260h[31:24]). Serial EEPROM presence is reported in the register's EepPrsnt[1:0] field [17:16]; a value of 01b or 11b indicates that the serial EEPROM is present.*

6.4 Serial EEPROM Data Format

The data in the serial EEPROM is stored in the format defined in Table 6-1. The Validation Signature byte is located in the first address. The Serial EEPROM Controller reads this byte to determine whether a valid serial EEPROM image exists versus a blank image. REG_BYTE_COUNT[15:0] contains the quantity of bytes of serial EEPROM data to be loaded. It is equal to the quantity of registers to be loaded times 6 (6 serial EEPROM bytes, per register). If the REG_BYTE_COUNT[15:0] value is not a multiple of 6, the last incomplete register entry is ignored.

For the remaining register-related locations, data is written into a 2-byte address that represents the Configuration register offset and Port Number, and the 4 bytes following are the data loaded for that Configuration register. Only Configuration register data specifically programmed into the serial EEPROM is loaded after the PEX 8604 exits reset.

Table 6-2 defines the Configuration register Address format (REGADDR[15:0] from Table 6-1):

- Bits [9:0] represent bits [11:2] of the Register address
- Bits [15:10] represent the Port Number of the register selected to be programmed by serial EEPROM

Because the PEX 8604 Serial EEPROM Controller always accesses 4 bytes of serial EEPROM data (for DWord-aligned Register addresses), register offsets are stored in the serial EEPROM as DWord address values.

To determine the 2-byte serial EEPROM value that represents the PEX 8604 Port and register offset, shift the register offset 2 bits to the right (divide by 4), then OR the resulting value with the appropriate Port Identifier value from Table 6-2.

For example, to load Port 4 register offset 1F8h, shift the address to the right by 2 bits (this becomes 07Eh) and concatenate 0001_00b. The resulting DWord address in the serial EEPROM will be 0001_0000_0111_1110b, which is 107Eh.

Table 6-1. Serial EEPROM Data

Location	Value	Description
0h	5Ah	Validation Signature
1h	00h	***Reserved***
2h	REG_BYTE_COUNT (LSB)	Configuration register Byte Count (LSB)
3h	REG_BYTE_COUNT (MSB)	Configuration register Byte Count (MSB)
4h	REGADDR (LSB)	1st Configuration Register Address (LSB)
5h	REGADDR (MSB)	1st Configuration Register Address (MSB)
6h	REGDATA (Byte 0)	1st Configuration Register Data (Byte 0)
7h	REGDATA (Byte 1)	1st Configuration Register Data (Byte 1)
8h	REGDATA (Byte 2)	1st Configuration Register Data (Byte 2)
9h	REGDATA (Byte 3)	1st Configuration Register Data (Byte 3)
Ah	REGADDR (LSB)	2nd Configuration Register Address (LSB)
Bh	REGADDR (MSB)	2nd Configuration Register Address (MSB)
Ch	REGDATA (Byte 0)	2nd Configuration Register Data (Byte 0)
Dh	REGDATA (Byte 1)	2nd Configuration Register Data (Byte 1)
Eh	REGDATA (Byte 2)	2nd Configuration Register Data (Byte 2)
Fh	REGDATA (Byte 3)	2nd Configuration Register Data (Byte 3)
…	…	…
FFFFh	REGDATA (Byte 3)	Last Configuration Register Data (Byte 3)

Note: *The first Configuration register programmed by the serial EEPROM **must** be the **Debug Control** register (Port 0, offset 1DCh), serial EEPROM locations 4h through 9h, as listed in Table 6-1.*

Table 6-2. Configuration Register Address Format

Port Number	REGADDR Bits [15:10] Value[a]	Port Identifier
Port 0	0000_00b	0000h
Port 1	0000_01b	0400h
Port 4	0001_00b	1000h
Port 5	0001_01b	1400h
NT Port Link Interface	1100_00b	C000h
NT Port Virtual Interface[b]	00XX_XXb	XX00h
NT PCI-to-PCI Bridge	1100_01b	C400h

*a. Encodings not listed are **reserved**.*

*b. For NT Port Virtual Interface registers, use the value for the Port Number that is configured as the NT Port (as designated by the STRAP_NT_UPSTRM_PORTSEL[3:0] inputs or **Debug Control** register NT Port Number field (Port 0, offset 1DCh[27:24])).*

6.5 Serial EEPROM Initialization

After the device Reset is de-asserted, the PEX 8604 determines whether a serial EEPROM is present. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its **Status** register. This value is copied to the **Serial EEPROM Status** register *Status Data from Serial EEPROM* fields (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 260h[31:24]). Serial EEPROM presence is reported in the register's *EepPrsnt[1:0]* field [17:16]; a value of 01b or 11b indicates that the serial EEPROM is present. A pull-up resistor on the EE_DO input produces a value of FFh if a serial EEPROM is not installed.

If a serial EEPROM is detected, the first byte (validation signature) is read. If a value of 5Ah is read, it is assumed that the serial EEPROM is programmed for the PEX 8604. The serial EEPROM address width is determined while the first byte is read. If the first byte's value is not 5Ah, the serial EEPROM is blank or programmed with invalid data. In this case, no more data is read from the serial EEPROM, and the **Serial EEPROM Status** register *EepAddrWidth* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 260h[23:22]) reports a value of 00b (undetermined width).

If the *EepAddrWidth* field reports a value of 00b, any subsequent accesses to the serial EEPROM (through the PEX 8604 Serial EEPROM registers) default to a serial EEPROM address width of 1 byte unless the **Serial EEPROM Status** register *EepAddrWidth Override* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 260h[21]) is Set. The *EepAddrWidth* field is usually Read-Only (RO); however, it is writable if the *EepAddrWidth Override* bit is Set (both can be programmed by a single Write instruction).

If the serial EEPROM contains valid data, the REG_BYTE_COUNT values in Bytes 2 and 3 determine the quantity of serial EEPROM locations that contain Configuration register addresses and data. Each Configuration register entry consists of 2 bytes of register Address and 4 bytes of register Write data. The REG_BYTE_COUNT must be a multiple of 6.

The EE_SK output clock frequency is determined by the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 268h[2:0]). The default clock frequency is 1 MHz. At this clock rate, it takes approximately 48 µs per DWORD during Configuration register initialization. For faster loading of large serial EEPROMs that support a faster clock, the first Configuration register load from the serial EEPROM could be to the **Serial EEPROM Clock Frequency** register.

6.6 PCI Express Configuration, Control, and Status Registers

The PCI Express Configuration, Control, and Status registers that can be initialized are detailed in:

- Chapter 13, "Transparent Port Registers"
- Chapter 15, "NT Port Virtual Interface Registers – NT Mode Only"
- Chapter 16, "NT Port Link Interface Registers – NT Mode Only"

6.7 Serial EEPROM Registers

The Serial EEPROM register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 260h through 26Ch) parameters defined in Section 13.14.2, "Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)," can be changed, using the serial EEPROM. It is recommended that the first serial EEPROM entry (after the **Debug Control** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh) entry, if programmed), be used to change the **Serial EEPROM Clock Frequency** register (offset 268h) value, to increase the clock frequency, and thereby reduce the time needed for the remainder of the serial EEPROM load. When the NT Port Expansion ROM feature is used, the serial EEPROM clock frequency must be 5 MHz or higher. At the last serial EEPROM entry, the **Serial EEPROM Status and Control** register (offset 260h) can be programmed to issue a Write Status (WRSR) command, to enable the Write Protection feature(s) within the serial EEPROM data, if needed.

6.8 Serial EEPROM Random Write/Read Access

To access the serial EEPROM, a PCI Express, I^2C, and/or SMBus Master uses the following registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port):

- **Serial EEPROM Status and Control** (offset 260h)
- **Serial EEPROM Buffer** (offset 264h)
- **Serial EEPROM 3rd Address Byte** (offset 26Ch)

Note: *To help streamline the text in the following subsections, the specific Port location/access of each register offset is not repeated – only the offset location is mentioned.*

The Master can only access the serial EEPROM on a DWord basis (4 bytes aligned to one DWord address).

6.8.1 Writing to Serial EEPROM

To write a DWord to the serial EEPROM:

1. If the 3rd Address byte (Address bits [23:16]) is needed (when the **Serial EEPROM Status** register *EepAddrWidth* field bits (offset 260h[23:22]) are both Set), write the value to the *Serial EEPROM 3rd Address Byte* field (offset 26Ch[7:0]).
2. Write the 32-bit data into the **Serial EEPROM Buffer** register (offset 264h).
3. Issue a Write Enable instruction to the serial EEPROM (Command = 110b, Set Write Enable Latch), by writing the value 0000_C000h into the **Serial EEPROM Status and Control** register (offset 260h).
4. Calculate and write the combined Address and Command value to write into the **Serial EEPROM Control** register (offset 260h), by combining the serial EEPROM 3-bit Write Data instruction (value 010b) as the *EepCmd[2:0]* field [15:13], together with the serial EEPROM address. Serial EEPROM Address bits [14:2] must be programmed into the **Serial EEPROM Control** register *EepBlkAddr* field [12:0], and serial EEPROM Address bit 15 must be programmed into the **Serial EEPROM Status** register *EepBlkAddr Upper Bit* bit (*that is*, Set offset 260h[20] if the serial EEPROM address is in the upper 32 KB of any 64-KB address block within the serial EEPROM). The data in the **Serial EEPROM Buffer** register is written to the serial EEPROM when the **Serial EEPROM Status and Control** register is written.
5. The serial EEPROM Write operation is complete when a subsequent read of the **Serial EEPROM Status** register *EepCmdStatus* bit (offset 260h[18]) returns 0. At this time, another serial EEPROM access can be started.

Because each PEX 8604 Port and Register address value (REGADDR; refer to Section 6.5), and its corresponding data value (REGDATA), require 6 bytes of serial EEPROM memory, and the PEX 8604 serial EEPROM interface accesses 4 bytes at a time, two serial EEPROM Writes may be needed to store each set of REGADDR (one word) and REGDATA (1 Dword) entries into the serial EEPROM. To avoid overwriting a word of another set of 6-byte REGADDR and REGDATA values, one of the two Serial EEPROM Writes might need to be a Read-Modify-Write type of operation (preserving one word read from the serial EEPROM, and writing the value back along with a new word value).

6.8.2 Reading from Serial EEPROM

To read a DWord from the serial EEPROM:

1. If the 3rd Address byte (Address bits [23:16]) is needed (when the **Serial EEPROM Status** register *EepAddrWidth* field bits (offset 260h[23:22]) are both Set), write the value to the **Serial EEPROM 3rd Address Byte** register *Serial EEPROM 3rd Address Byte* field (offset 26Ch[7:0]).
2. Calculate the combined Address and Command value to write into the **Serial EEPROM Control** register (offset 260h), by combining the serial EEPROM 3-bit Read Data instruction (value 011b) as the *EepCmd[2:0]* field [15:13], together with the serial EEPROM address. Serial EEPROM Address bits [14:2] must be programmed into the **Serial EEPROM Control** register *EepBlkAddr* field [12:0], and serial EEPROM Address bit 15 must be programmed into the **Serial EEPROM Status** register *EepBlkAddr Upper Bit* bit (*that is*, Set offset 260h[20] if the serial EEPROM address is in the upper 32 KB of any 64-KB address block within the serial EEPROM).
3. Poll the **Serial EEPROM Status** register until the *EepCmdStatus* bit (offset 260h[18]) is Cleared, which signals that the transaction is complete.
4. Read the four bytes of serial EEPROM data from the **Serial EEPROM Buffer** register (offset 264h).

   For example, to read the first DWord in the serial EEPROM, write the value 0000_6000h to Port 0, register offset 260h, and then read Port 0, register offset 264h.

6.8.3 Programming a Blank Serial EEPROM

The PEX 8604 supports 1-, 2-, or 3-byte serial EEPROM addressing. 8-Kbit to 512-Kbit SPI EEPROMs use 2-byte addressing. The PEX 8604 requires that the first byte in the serial EEPROM must be the value 5Ah (ASCII Z), as a Validation Signature.

The 2nd and 3rd bytes contain the quantity of bytes within the serial EEPROM image, beginning with the first register entry at serial EEPROM address 04h. If this Byte Count value exceeds the actual quantity of register entries times 6 (*such as* if the first DWord is programmed to the value 5A00_FFFFh), the system could hang. To simplify programming of a blank EEPROM (*such as* in a typical production build), the serial EEPROM could be pre-programmed with the first DWord, program to 0000_005Ah.

A 2-byte address serial EEPROM that is blank (or corrupted) can be programmed according to the following procedure (when the PEX 8604 is in 1-Byte Address mode).

To program a blank serial EEPROM:

1. Write the value 0000_005Ah into the **Serial EEPROM Buffer** register at address [upstream Port **BAR0** + 264h].
2. Issue a Write Enable instruction (Command = 110b, Set Write Enable Latch, and enable 2-byte addressing, by writing the value 00A0_C000h into the **Serial EEPROM Status and Control** register (offset 260h).
3. Copy this data value to serial EEPROM location 0, by writing the value 00A0_4000h into the **Serial EEPROM Status and Control** register. At this point, the first four bytes in the serial EEPROM now contain the value 0000_005Ah.
4. Reboot the system, to reset the PEX 8604 so that it re-detects the serial EEPROM.

6.9 Serial EEPROM Loading of NT Port Link Interface Registers – NT Mode Only

The **Debug Control** register *Load Only EEPROM NT-Link on Hot Reset* and *Inhibit EEPROM NT-Link Load on Hot Reset* bits (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[31:30], respectively) control whether the serial EEPROM is to load registers following a Soft Reset (Hot Reset or DL_Down) to the upstream Port or NT Port Link Interface, as defined in Table 6-3.

Table 6-3. Serial EEPROM Loading of NT Port Link Interface Registers (Offset 1DCh[31:30] Values)

Bit 31 Value	Bit 30 Value	Action
0	0	Load all registers from the serial EEPROM.
0	1	Load all registers, except the NT Port Link Interface registers, from the serial EEPROM.
1	0	Load only NT Port Link Interface registers from the serial EEPROM.
1	1	Disable serial EEPROM loading of all registers.

6.10 NT Port Expansion ROM – NT Mode Only

The PEX 8604 NT Port Virtual and Link Interfaces support Expansion ROM, as defined in the *PCI r3.0*. Expansion ROM can be implemented for either Port, but not both concurrently. The Expansion ROM image is stored in the serial EEPROM, and its size can be either 16 KB (default, bit is Cleared) or 32 KB (maximum), based upon the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 268h[16]) value. When the Expansion ROM feature is used, the serial EEPROM clock frequency must be 5 MHz or higher.

By default, the Expansion ROM is enabled on the NT Port Link Interface; however, it can be enabled instead for the NT Port Virtual Interface, by Setting the **Ingress Control** register *Expansion ROM Virtual Side* bit (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 660h[23]). The **Expansion ROM Base Address** register (BAR) must be enabled, by Setting the register's *Expansion ROM Enable* bit, in either the NT Port Virtual Interface (offset 30h[0]) or NT Port Link Interface (offset 30h[0]).

The Expansion ROM's location in the serial EEPROM is programmed in the **Serial EEPROM 3rd Address Byte** register *Expansion ROM Base Address* field (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 26Ch[31:16]), of which the lower six bits, [21:16], map to serial EEPROM byte Address bits [15:10] (aligned to a 256-DWord (1-KB) boundary). The Expansion ROM must not straddle a 64-KB boundary within the serial EEPROM.

The default serial EEPROM Base Address value is as follows:

- **16-KB Expansion ROM (*Expansion ROM Size* bit is Cleared)** – The value is 0020h, which corresponds to serial EEPROM Byte address 2000h (8 KB). The serial EEPROM size must be at least 32 KB.
- **32-KB Expansion ROM (*Expansion ROM Size* bit is Set)** – The value is 0040h, which corresponds to serial EEPROM byte address 4000h (16 KB). The serial EEPROM size must be at least 64 KB.

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Chapter 7 I²C/SMBus Slave Interface Operation

7.1 Introduction

This chapter discusses the I²C Slave Interface and SMBus Slave Interface.

7.2 I²C Slave Interface

7.2.1 I²C Support Overview

Note: *This section applies to the I²C Slave interface, which uses the I2C_ADDR[2:0], I2C_SCL0, and I2C_SDA0 signals for PEX 8604 register access by an I²C Master. The I2C_SCL1 and I2C_SCL1 signals form the PEX 8604 I²C Master interface, which is used only for Serial Hot Plug operation. (Refer to Chapter 11, "Hot Plug Support.")*

Inter-Integrated Circuit (I²C) is a bus used to connect Integrated Circuits (ICs). Multiple ICs can be connected to an I²C Bus, and I²C devices that have I²C mastering capability can initiate a Data transfer. I²C is used for Data transfers between ICs at relatively low rates (100 Kbps), and is used in a variety of applications. For further details regarding I²C Buses, refer to the *I2C Bus, v2.1*.

The PEX 8604 is an I²C Slave. Slave operations allow the PEX 8604 Configuration registers to be read from or written to by an I²C Master, external from the device. I²C is a sideband mechanism that allows the device Configuration registers to be programmed, read from, or written to, independent of the PCI Express upstream Link.

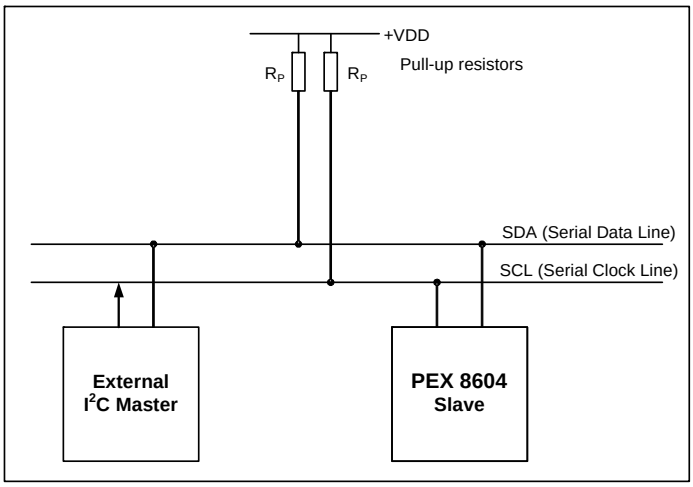
With I²C, users have the option of accessing all PEX 8604 registers through the I²C Slave interface. I²C provides an alternative to using a serial EEPROM. I²C can also be used for debugging, such as if the PEX 8604 upstream Port fails to linkup.

Accordingly, it is recommended that both I²C/SMBus access, and the serial EEPROM (or at least its footprint), be included in designs.

The I2C_SCL0 and I2C_SDA0 signals can be brought out to a 2x2 pin header on the board, to allow PLX software (*for example*, running on a laptop computer) to access the PEX 8604 registers, using an Aardvark USB-I²C adapter connected to this header. (Refer to the *PEX 8604 RDK Hardware Reference Manual* for the header pin design.)

Figure 7-1 provides a block diagram that illustrates how standard devices connect to the I2C Bus.

Figure 7-1. Standard Devices to I2C Bus Connection Block Diagram



7.2.2 I2C Addressing – Slave Mode Access

To access the PEX 8604 Configuration registers through the I2C Slave interface, the PEX 8604 I2C Slave address must be configured.

The PEX 8604 supports a 7-bit I2C Slave address. The 7-bit I2C Address bits can be configured by the serial EEPROM (recommended, if the default address must be changed), or by a Memory Write, in the **I2C Configuration** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 294h, default value 38h), with the lower three bits of the address derived from the I2C_ADDR[2:0] inputs. Bits [6:0] correspond to Address Byte bits [7:1], with bit 0 of the byte indicating a Write (0) or Read (1).

The I2C_ADDR[2:0] inputs can be pulled or tied High or Low, to select a different Slave address. Up to eight PEX 8604 devices can share the same I2C Bus segment without conflict, provided that each PEX 8604 has its I2C_ADDR[2:0] inputs strapped to a unique state. More than eight PEX 8604 devices can share the I2C Bus, however, if the upper Address bits are programmed in the serial EEPROM.

7.2.3 I2C Slave Interface Register

The **I2C Slave Interface** register, **I2C Configuration**, is described in Section 13.14.5, "Device-Specific Registers – I2C Slave Interface (Offsets 290h – 2C4h)." The default I2C Slave address can be changed in the **I2C Configuration** register to a different value, using the serial EEPROM or a Memory Write.

The I2C Slave address must not be changed by an I2C Write command. (Refer to Section 7.2.2.)

Other I2C Slave interface registers exist; however, they are for ***Factory Test Only***.

7.2.4 I2C Command Format

An I2C transfer starts as a packet with Address Phase bytes, followed by four Command Phase bytes, and one or more Data Phase bytes. The I2C packet Address Phase Byte format is illustrated in Figure 7-2a. The Command Phase portion must include 4 bytes of data that contain the following:

- I2C Transfer type (Read/Write)
- PCI Express Configuration Register address
- PEX 8604 Port Number being accessed
- Byte Enable(s) of the register data being accessed

When the I2C Master is writing to the PEX 8604, the I2C Master must transmit the Data bytes to be written to that register within the same packet that contains the Command bytes. Table 7-2 describes each I2C Command byte for Write access. Figure 7-2b illustrates the Command phase portion of an I2C Write packet.

When the I2C Master is reading from the PEX 8604, the I2C Master must separately transmit a Command Phase packet and Data Phase packet. Table 7-6 describes each I2C Command byte for Read access. Figure 7-4b illustrates the Command phase portion of an I2C Read packet.

Each I2C packet must contain 4 bytes of data. Pad unused packet Data bytes with zeros (0) to meet this requirement.

7.2.5 I2C Register Write Access

The PEX 8604 Configuration registers can be read from and written to, based upon I2C register Read and Write operations, respectively. An I2C Write packet consists of Address Phase bytes and Command Phase bytes, followed by one to four additional I2C Data bytes. Table 7-1 defines mapping of the I2C Data bytes to the Configuration register Data bytes. Figure 7-2c illustrates the I2C Data byte format.

The I2C packet starts with the *S* (START condition) bit. Data bytes are separated by the *A* (Acknowledge Control Packet (ACK)) or *N* (Negative Acknowledge (NAK)) bit. The packet ends with the *P* (STOP condition) bit.

If the Master generates an invalid command, the targeted PEX 8604 register is not modified.

The PEX 8604 considers the 1st Data byte of the 4-byte Data phase, following the four Command bytes in the Command phase, as register Byte 3 (bits [31:24]). The next three Data bytes access register Bytes 2 through 0, respectively. Four Data bytes are required, regardless of the Byte Enable Settings in the Command phase. The Master can then generate either a STOP condition (to finish the transfer) or a repeated START condition (to start a new transfer). If the I2C Master sends more than the four Data bytes (violating PEX 8604 protocol), the PEX 8604 returns a NAK for the extra Data byte(s). (For further details regarding I2C protocol, refer to the *I2C Bus, v2.1*.)

Table 7-2 describes each I2C Command byte for Write access. In the packet described in Figure 7-2, Command Bytes 0 through 3 for Writes follow the format specified in Table 7-2.

Table 7-1. I2C Register Write Access

I2C Data Byte Order	PCI Express Configuration Register Bytes
0	Written to register Byte 3
1	Written to register Byte 2
2	Written to register Byte 1
3	Written to register Byte 0

Table 7-2. I2C Command Format for Write Access

Byte	Bit(s)	Description
1st (0)	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 011b = Write register Do not use other encodings for Writes.
2nd (1)	7:4	***Reserved*** Should be Cleared.
	3:0	**Port Selector, Bits [4:1]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Selector.
3rd (2)	7	**Port Selector, Bit 0** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Selector. *Port Selector*, bits [4:0] select the Port to access. 00h – 0Fh for 4 Ports (including NT Port Virtual Interface, if NT mode is enabled) 10h for NT Port Link Interface 11h for NT PCI-to-PCI Bridge 14h – 1Fh are ***reserved***.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8604 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8604 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8604 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8604 register bits [31:24]) 0 = Corresponding PEX 8604 register byte will not be modified 1 = Corresponding PEX 8604 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8604 Register Address [11:10]**
4th (3)	7:0	**PEX 8604 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I2C byte Writes.*

Figure 7-2. I2C Write Packet

Figure 7-2a I2C Write Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

Figure 7-2b I2C Write Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

Figure 7-2c I2C Write Packet Data Phase Bytes

Write Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Data Byte 0 (to selected register Byte 3)	A	Data Byte 1 (to selected register Byte 2)	A	Data Byte 2 (to selected register Byte 1)	A	Data Byte 3 (to selected register Byte 0)	A	P

7.2.5.1 I2C Register Write

The following tables illustrate a sample I2C packet for writing the PEX 8604 **MSI Upper Address** register (offset 50h) for Port 4, with data 1234_5678h.

Note: *The PEX 8604 has a default I2C Slave address [6:0] value of 38h, with the I2C_ADDR[2:0] inputs having a value of 000. The byte sequence on the I2C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I2C Master frames the transfer.*

Table 7-3. I2C Register Write Access Example – 1st Cycle

Phase	Value	Description
Address	70h	**Bits [7:1] for PEX 8604 I2C Slave Address (38h)** Last bit (bit 0) for Write = 0.

Table 7-4. I2C Register Write Access Example – Command Cycle

Byte	Value	Description
0	03h	[7:3] ***Reserved*** Should be Cleared. [2:0] **Command** 011b = Write register
1	00h for Port 1	[7:4] ***Reserved*** Should be Cleared. [3:0] **Port Selector, Bits [4:1]**
2	BCh for Port 1	7 **Port Selector, Bit 0** 6 ***Reserved*** Should be Cleared. [5:2] **Byte Enables** All active. [1:0] **PEX 8604 Register Address, Bits [11:10]**
3	14h	[7:0] **PEX 8604 Register Address, Bits [9:2]**

Table 7-5. I2C Register Write Access Example – Write Cycle

Byte	Value	Description
0	12h	**Data to Write for Byte 3**
1	34h	**Data to Write for Byte 2**
2	56h	**Data to Write for Byte 1**
3	78h	**Data to Write for Byte 0**

Figure 7-3. I2C Write Command Packet Example

Figure 7-3a I2C Write Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address 0111_000b	Read/Write Bit 0 0 = Write	A

Figure 7-3b I2C Write Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK
Command Byte 0 0000_0011b	A	Command Byte 1 0000_0010b	A	Command Byte 2 1011_1100b	A	Command Byte 3 0001_0100b	A

Figure 7-3c I2C Write Packet Data Phase Bytes

Write Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Data Byte 0 0001_0010b	A	Data Byte 1 0011_0100b	A	Data Byte 2 0101_0110b	A	Data Byte 3 0111_1000b	A	P

7.2.6 I2C Register Read Access

When the I2C Master attempts to read a PEX 8604 register, two packets are transmitted. The 1st packet consists of Address and Command Phase bytes to the Slave. The 2nd packet consists of Address and Data Phase bytes.

According to the *I2C Bus, v2.1*, a Read cycle is triggered when the Read/Write bit (bit 0) of the 1st cycle is Set. The Command phase reads the requested register content into the internal buffer. When the I2C Read access occurs, the internal buffer value is transferred on to the I2C Bus, starting from Byte 3 (bits [31:24]), followed by the subsequent bytes, with Byte 0 (bits [7:0]) being transferred last. If the I2C Master requests more than four bytes, the PEX 8604 re-transmits the same byte sequence, starting from Byte 3 of the internal buffer.

The 1st and 2nd I2C Read packets (illustrated in Figure 7-4 and Figure 7-5, respectively) perform the following functions:

- **1st packet** – Selects the register to read
- **2nd packet** – Reads the register (sample 2nd packet provided is for a 7-bit PEX 8604 I2C Slave address)

Although two packets are shown for the I2C Read, the I2C Master can merge the two packets together into a single packet, by not generating the STOP at the end of the first packet (Master does not relinquish the bus) and generating REPEAT START.

Table 7-6 describes each I2C Command byte for Read access. In the packet described in Figure 7-4, Command Bytes 0 through 3 for Reads follow the format specified in Table 7-6.

Table 7-6. I²C Command Format for Read Access

Byte	Bit(s)	Description
1st (0)	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 100b = Read register Do not use other encodings for Reads.
2nd (1)	7:4	***Reserved*** Should be Cleared.
	3:0	**Port Selector, Bits [4:1]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Selector.
3rd (2)	7	**Port Selector, Bit 0** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Selector. *Port Selector*, bits [4:0] select the Port to access. 00h – 0Fh for 4 Ports (including NT Port Virtual Interface, if NT mode is enabled) 10h for NT Port Link Interface 11h for NT PCI-to-PCI Bridge 14h – 1Fh are ***reserved***.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8604 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8604 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8604 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8604 register bits [31:24]) 0 = Corresponding PEX 8604 register byte will not be modified 1 = Corresponding PEX 8604 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8604 Register Address [11:10]**
4th (3)	7:0	**PEX 8604 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I²C byte Writes.*

Figure 7-4. I2C Read Command Packet (1st Packet)

Figure 7-4a I2C Read Command Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

Figure 7-4b I2C Read Command Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	STOP
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	P

Figure 7-5. I2C Read Data Packet (2nd Packet)

Figure 7-5a I2C Read Data Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit, 1 = Read	A

Figure 7-5b I2C Read Data Packet Data Phase Bytes

Read Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

7.2.6.1 I2C Register Read Address Phase and Command Packet

The following is a sample I2C packet for reading the PEX 8604 **Serial EEPROM Buffer** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 264h) for Port 4, assuming the register value is ABCD_EF01h.

Note: *The PEX 8604 has a default I2C Slave address [6:0] value of 38h, with the I2C_ADDR[2:0] inputs having a value of 000. The byte sequence on the I2C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I2C Master frames the transfer.*

Table 7-7. I2C Register Read Access Example – 1st Packet

Phase	Value	Description
Address	70h	**Bits [7:1] for PEX 8604 I2C Slave Address (38h)** Last bit (bit 0) for Write = 0.

Table 7-8. I2C Register Read Access Example – Command Cycle

Byte	Value	Description
0	04h	[7:3] ***Reserved*** Should be Cleared. [2:0] **Command** 100b = Read register
1	00h for Port 1	[7:4] ***Reserved*** Should be Cleared. [3:0] **Port Selector, Bits [4:1]**
2	BCh for Port 1	7 **Port Selector, Bit 0** 6 ***Reserved*** Should be Cleared. [5:2] **Byte Enables** All active. [1:0] **PEX 8604 Register Address, Bits [11:10]**
3	99h	[7:0] **PEX 8604 Register Address, Bits [9:2]**

7.2.6.2 I2C Register Read Data Packet

Note: *The PEX 8604 has a default I2C Slave address [6:0] value of 38h, with the I2C_ADDR[2:0] inputs having a value of 000. The byte sequence on the I2C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I2C Master frames the transfer.*

Table 7-9. I2C Register Read Access Example – 1st Cycle

Phase	Value	Description
Address	71h	**Bits [7:1] for PEX 8604 I2C Slave Address (38h)** Last bit (bit 0) for Read = 1.
Read	ABh	**Byte 3 of Register Read**
	CDh	**Byte 2 of Register Read**
	EFh	**Byte 1 of Register Read**
	01h	**Byte 0 of Register Read**

Figure 7-6. 1st Packet – I2C Command Phase

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address 0111_000b	Read/Write Bit 0 = Write	A

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	STOP
Command Byte 0 0000_0100b	A	Command Byte 1 0000_0010b	A	Command Byte 2 0011_1110b	A	Command Byte 3 1001_1001b	P

Figure 7-7. 2nd Packet – I2C Read Phase

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1] 0111_000b	Read/Write Bit 1 = Read	A

Read Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	STOP
Register Byte 3 1010_1011b	A	Register Byte 2 1100_1101b	A	Register Byte 1 1110_1111b	A	Register Byte 0 0000_0001b	P

7.3 SMBus Slave Interface

7.3.1 SMBus Features

- Compliant to the *SMBus v2.0*
- Supports the SMBus Slave function only
- PEX 8604 internal registers can be read and written, through the SMBus Slave interface
- Supports Address Resolution Protocol (ARP-capable)
- Strapping inputs, serial EEPROM, software, or ARP Set the Slave address
- Supports Block Read, Block Write, and Block Read - Block Write Process Call commands to access the registers
- Supports Packet Error Checking
- 10 to 100 KHz Bus operation frequency range

7.3.2 SMBus Operation

Based upon I2C's principles of operation, SMBus is a two-wire bus used for communication between IC components and the remainder of the system. Electrically, I2C and SMBus devices are compatible, and both protocol devices can co-exist on the same bus. Multiple devices, both Masters and Slaves, can be connected to an SMBus segment. PCI Express cards have two optional SMBus pins defined on the connector – SMCLK and SMDAT.

The PEX 8604 implements an *SMBus v2.0*-compliant Slave device, and is used to read and write PEX 8604 registers, through SMBus commands. The PEX 8604 SMBus uses the same SDA data and SCL clock balls that are used for I2C, and the I2C_ADDR[1:0] inputs, to define address assignment (I2C_ADDR2 is not used as an Address bit in SMBus mode). At any time, either the I2C or SMBus feature is enabled, dependent upon the **SMBus Configuration** register *SMBus Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 344h[0]) state, which is latched (at Fundamental Reset) to the inverse value of the STRAP_SMBUS_EN# input. Software can toggle this bit to switch between I2C and SMBus functionality.

The PEX 8604 SMBus Slave interface supports three command protocols for register access:

- Block Write
- Block Read
- Block Read - Block Write Process Call

The PEX 8604 SMBus logic also supports the commands that are required to support ARP. ARP is a feature specific to *SMBus v2.0*, through which an SMBus ARP Master can dynamically assign a unique address to each of the SMBus Targets residing on the same bus. Although ARP is an optional feature of the *SMBus v2.0*, PCI and PCI Express cards are required to support ARP. The ARP feature is enabled when the **SMBus Configuration** register *ARP Disable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 344h[8]) is Cleared; this bit is initially latched (at Fundamental Reset) to the value of the I2C_ADDR2 input.

If ARP is disabled, by I2C_ADDR2 input being pulled or tied High, the SMBus Slave Address bits [6:2] default to value 001_10b. Address bits [1:0] are initially latched (at Fundamental Reset) to the I2C_ADDR[1:0] input values, which allow a maximum of four SMBus-enabled PEX 8604s to co-exist on the same SMBus segment. Software can change the SMBus Slave address, by programming the **SMBus Configuration** register *SMBus Device Address* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 344h[7:1]).

The PEX 8604 also supports Packet Error Checking and Packet Error Code (PEC) generation, as explained in the *SMBus v2.0*. The *SMBus v2.0* optional feature, *Notify ARP Master* (which requires Master capability on the SMBus) is ***not*** supported.

7.3.3 SMBus Commands Supported

For register access, the SMBus logic supports three commands:

- Block Write (command BEh) is used to write the registers
- Block Write (command BAh), followed by Block Read (command BDh), can be used to read the registers
- Block Read - Block Write Process Call (commands BAh, CDh) can also be used to read registers

SMBus Commands that are not supported by the PEX 8604 (Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read Word, and Process Call), are NACKed.

7.3.3.1 SMBus Block Write

The Block Write command is used to write to the PEX 8604 registers. General SMBus Block Writes are illustrated in Figure 7-8 and Figure 7-9. The sequence of Bytes include the following, in the sequence listed:

- 7-bit address,
- Command Code that indicates it is Block Write,
- *Byte Count* field with a value of 8h that indicates 4 bytes to set up the register to write (Port Number, register address, Command Byte Enable, and so forth), followed by
- 4 bytes of data to be written into the register

Figure 7-10 explains the elements used in Figure 7-8 and Figure 7-9, and Figure 7-11 indicates the Data Bytes written.

Figure 7-8. SMBus Block Write Command Format, to Write to a PEX 8604 Register without PEC

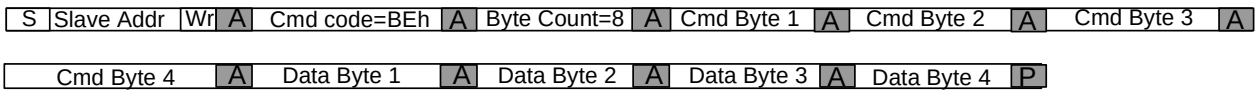


Figure 7-9. SMBus Block Write Command Format, to Write to a PEX 8604 Register with PEC

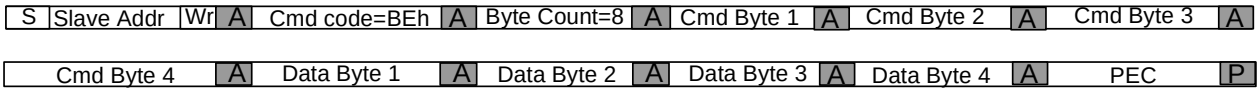


Figure 7-10. SMBus Packet Protocol Diagram Element Key

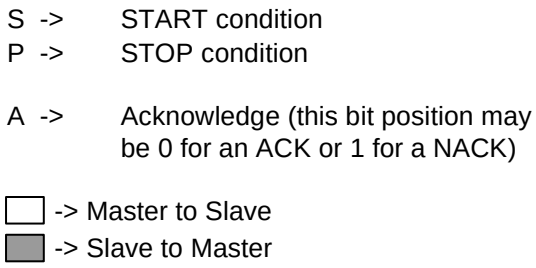


Figure 7-11. SMBus Block Write Bytes, as Written to Register

31:24	23:16	15:8	7:0
Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4

Note: *In each byte, the Most Significant Byte (MSB) is transmitted first.*

Table 7-10 provides a description of bytes for an SMBus Block Configuration Space register (CSR) Write.

Block Write transactions that are received with incorrect byte Settings are NACKed, starting from the wrong byte Setting, and including subsequent bytes in the packet. *For example*, if the Byte Count value is not 8, the PEX 8604 NACKs the byte corresponding to the Byte Count value, as well as any Data bytes following within the same packet.

The byte after Data Byte 4, if present, is taken as the PEC byte, and if present, the PEC is checked. If a packet fails Packet Error Checking, the PEX 8604 drops the packet (ignores the Write), and returns NACK for the PEC byte, to the SMBus Master. Packet Error Checking can be disabled, by Setting the **SMBus Configuration** register *PEC Check Disable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 344h[9]). The Byte Count value, by definition, does not include the PEC byte.

Table 7-10. Bytes for Block CSR Write on SMBus

Field (Byte) On Bus	Bit(s)	Value/Description
Command Code	7:0	BEh for **B**lock Writ**E**.
Byte Count	7:0	08h = 8 bytes to follow (4 Command and 4 Data bytes). The PEC byte is not counted.
Command Byte 1	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 011b = Write register 100b = Read register All other encodings are ***reserved***. ***Do not use.***
Command Byte 2	7:4	***Reserved*** Should be Cleared.
	3:0	**Port Selector, Bits [4:1]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Selector.
Command Byte 3	7	**Port Selector, Bit 0** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Selector. *Port Selector*, bits [4:0] select the Port to access. 00h – 0Fh for 4 Ports (including NT Port Virtual Interface, if NT mode is enabled) 10h for NT Port Link Interface 11h for NT PCI-to-PCI Bridge 14h – 1Fh are ***reserved***.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8604 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8604 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8604 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8604 register bits [31:24]) 0 = Corresponding PEX 8604 register byte will not be modified 1 = Corresponding PEX 8604 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8604 Register Address [11:10]**
Command Byte 4	7:0	**PEX 8604 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I^2C byte Writes.*

Sample Register Write Byte Sequence Using SMBus Block Write

An SMBus Block Write packet to write to the **MSI Upper Address** [63:32] register (offset 50h) in Port 3, is listed in Table 7-11. The register value is 1234_5678h, with all Bytes enabled, and without PEC. The default SMBus Device Address is 001_100b.

Table 7-11. Sample SMBus Block Write Byte Sequence

Byte Number	Byte Type	Value	Description
1	Address	70h	Bits [7:1] for the PEX 8604 default Slave address of 38h, with bit 0 Cleared to indicate a Write.
2	Command Code	BEh	Command Code for register Write, using a Block Write.
3	Byte Count	08h	Byte Count. Four Command Bytes and Four Data Bytes.
4	Command Byte 1	03h	For Write command.
5	Command Byte 2	01h	Bits [2:0] – Port Selector [3:1].
6	Command Byte 3	BCh	Bit 7 is Port Selector LSB. Bit 6 is ***reserved***. Bits [5:2] are the four Byte Enables; all are active. Bits [1:0] are register Address bits [11:10].
7	Command Byte 4	14h	PEX 8604 Register Address bits [9:2] (for offset 50h).
8	Data Byte 1	12h	Data MSB.
9	Data Byte 2	34h	Data Byte for register bits [23:16].
10	Data Byte 3	56h	Data Byte for register bits [15:8].
11	Data Byte 4	78h	Data LSB.

7.3.3.2 SMBus Block Read

A Block Read command is used to read PEX 8604 registers. Similar to register Reads using I^2C, an SMBus Write sequence must first be performed to select the register to read, followed by an SMBus Read of the corresponding register. There are two ways a PEX 8604 register can be read:

- Use a Block Write, followed by a Block Read. The Block Write sets up the parameters including Port Number, register address and Byte Enables, and the Block Read performs the actual Read operation.
- Use a Block Read - Block Write Process Call. This command is defined by the *SMBus v2.0*, and performs a Block Write and Block Read, using a single command. The Block Write portion of the message sets up the register to be read, and then a repeated START followed by the Block Read portion of the message returns the register data specified by the Block Write.

Note: *There is no STOP condition before the repeated START condition.*

Register Read Using SMBus Block Write, Followed by SMBus Block Read

A general SMBus Block Write and Block Read sequence is illustrated in Figure 7-12.

Table 7-12 describes the Byte definitions for a Block Write bus protocol, to prepare for a subsequent Block Read of the PEX 8604 register.

The PEX 8604 always NACKs any incorrect command sequences, starting with the wrong Byte. Upon receiving the Block Read command, the PEX 8604 returns a PEC to the Master if, after the 4th byte of register data, the Master still requests one more Byte. As a Slave, the PEX 8604 recognizes the end of the Master's Read cycle, by observing the Master's NACK response for the last Data Byte transmitted by the PEX 8604.

Incorrect command sequences are always NACKed, starting with the byte that is incorrect. (Refer to Table 7-13.) On the Block Read command, a PEC is returned to the Master, if after the 4th byte of CSR data, the return Master still requests for one additional byte. As a Slave, the PEX 8604 will know the end of the Master Read cycle, by observing the NACK for the last byte read from the Master.

Figure 7-12. SMBus Block Write to Set up Read, and Resulting Read that Returns CSR Value

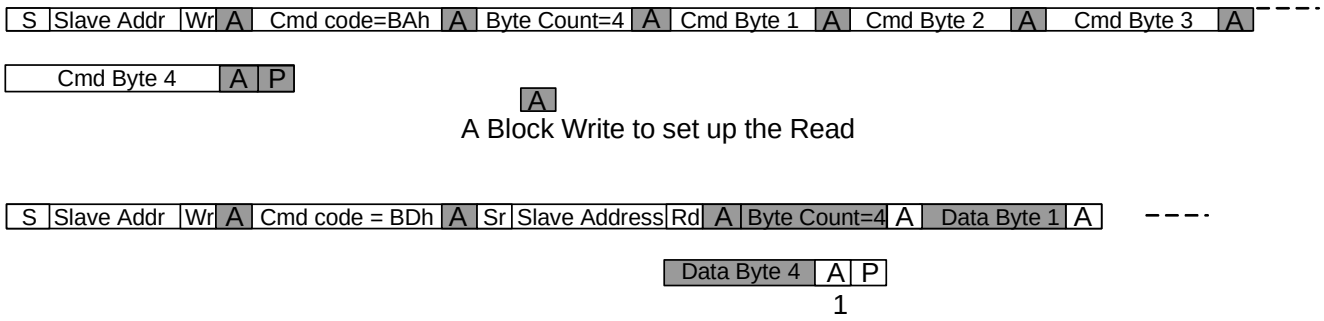


Table 7-12. SMBus Block Read Bytes

Field (Byte) On Bus	Bit(s)	Value/Description
Command Code	7:0	BAh, to set up the Read, using Block Writes.
Byte Count	7:0	04h = 4 Command bytes.
Command Byte 1	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 011b = Write register 100b = Read register All other encodings are ***reserved***. ***Do not use.***
Command Byte 2	7:4	***Reserved*** Should be Cleared.
	3:0	**Port Selector, Bits [4:1]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Selector.
Command Byte 3	7	**Port Selector, Bit 0** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Selector. *Port Selector*, bits [4:0] select the Port to access. 00h – 0Fh for 4 Ports (including NT Port Virtual Interface, if NT mode is enabled) 10h for NT Port Link Interface 11h for NT PCI-to-PCI Bridge 14h – 1Fh are ***reserved***.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8604 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8604 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8604 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8604 register bits [31:24]) 0 = Corresponding PEX 8604 register byte will not be modified 1 = Corresponding PEX 8604 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8604 Register Address [11:10]**
Command Byte 4	7:0	**PEX 8604 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I2C byte Writes.*

Table 7-13. Command Format for SMBus Block Read

Field (Byte) On Bus	Bit(s)	Value/Description
Cmd Code	7:0	CDh, for Block Read (Process **C**all Rea**D**).

Sample CSR Read Byte Sequence, Using SMBus Block Write Followed by SMBus Block Read

An SMBus sequence to write and read the **MSI Upper Address** [63:32] register (offset 50h) in Port 3, is listed in Table 7-14 and Table 7-15, respectively. The register value is ABCD_EF01h, and without PEC. The Block Write sets up the Port Numbers, Register address and Byte Enables, and the Block Read performs the real Read operation. The default SMBus Device Address is 001_100b.

Table 7-14. SMBus Block Write Portion

Byte Number	Byte Type	Value	Description
1	Address	70h	Bits [7:1] value for the PEX 8604 Slave address of 38h, with bit 0 Cleared to indicate a Write.
2	Block Write Command Code	BAh	Command Code for register Read setup, using a Block Write.
3	Byte Count	04h	Byte Count. Four Command Bytes.
4	Command Byte 1	04h	Write command.
5	Command Byte 2	01h	Bit 3 = 0, **Port Selector [3:0]** = *Port Selector* bits (2nd Command byte, bits [3:0] and 3rd Command byte, bit 7).
6	Command Byte 3	BCh	Bit 7 is Port Selector LSB. Bit 6 is ***reserved***. Bits [5:2] are the four Byte Enables; all are active. Bits [1:0] are register Address bits [11:10].
7	Command Byte 4	9Dh	PEX 8604 Register Address bits [9:2] (for offset 50h).

Table 7-15. SMBus Block Read Portion

Byte Number	Byte Type	Value	Description
1	Address	70h	Bits [7:1] value for the PEX 8604 Slave address of 38h, with bit 0 Cleared to indicate a Write.
2	Block Read Command Code	BDh	Command code for Block Read of PEX 8604 registers.

Table 7-16. SMBus Read Command following Repeat START from Master

Byte Number	Byte Type	Value	Description
1	Address	71h	Bits [7:1] value for the PEX 8604 Slave address of 38h, with bit 0 Set to indicate a Read.

Table 7-17. PEX 8604 SMBus Return Bytes

Byte Number	Byte Type	Value	Description
1	Byte Count	04h	Four Bytes in register.
2	Data Byte 1	ABh	Register data MSB.
3	Data Byte 2	CDh	Register data [23:16].
4	Data Byte 3	EFh	Register data [15:8].
5	Data Byte 4	01h	Register data LSB.

7.3.3.3 CSR Read, Using SMBus Block Read - Block Write Process Call

A general SMBus Block Read - Block Write Process Call sequence is illustrated in Figure 7-13. Alternatively, a general SMBus Block Read - Block Write Process Call with PEC sequence is illustrated in Figure 7-14.

Using this command, the register to be read can be set up and read back with one SMBus cycle (a transaction with a START and ending in STOP). There is no STOP condition before the repeated START condition. The command format for the Block Write part of this command has the same sequence as in Table 7-14, except that the Command Code changes to CDh, as illustrated below. Other Bytes remain the same as used in the sequence for SMBus Block Write followed by Block Read.

Table 7-18 lists the Command format for Block Read.

Figure 7-13. CSR Read Operation Using SMBus Block Read - Block Write Process Call

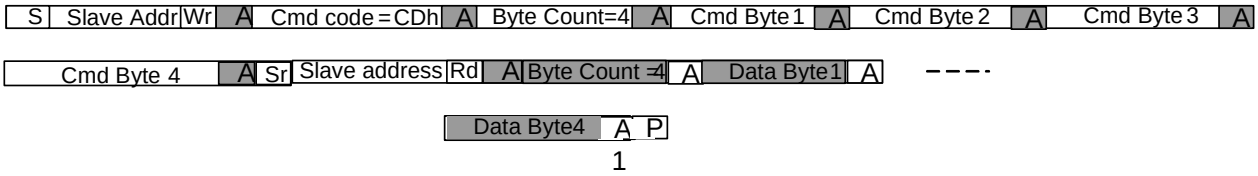


Figure 7-14. CSR Read Operation Using SMBus Block Read - Block Write Process Call with PEC

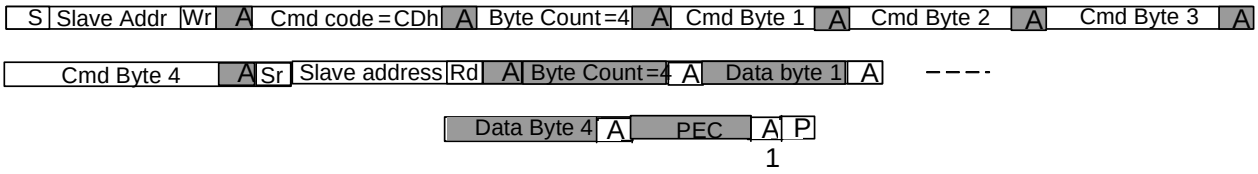


Table 7-18. Command Code for SMBus Block Read

Field (Byte) On Bus	Bit(s)	Value/Description
Cmd Code	7:0	CDh, for Block Read (Process **C**all Rea**D**).

7.3.4 SMBus Address Resolution Protocol

Address Resolution Protocol (ARP) is a protocol by which SMBus devices that implement an assignable Slave address feature are enumerated and dynamically assigned non-conflicting Slave addresses, rather than using a fixed Slave address. Although optional in the *SMBus v2.0*, it is mandatory per the *PCI r3.0* for add-in boards, to support ARP. This feature avoids conflicts with addresses used by other devices on a motherboard. ARP also allows multiple devices of the same type to co-exist on the same bus segment, without address conflicts.

To support this feature, a Slave device must implement a unique 128-bit ID, called *Unique Device Identifier (UDID)*. The fields of this ID are provided in Figure 7-15. All ARP commands use the default Device Address, 1100_001b. There are also two flags that the SMBus devices must implement to support the ARP process:

- **Address Resolved flag (AR)** – A flag bit or device internal state that indicates whether the ARP Master has resolved the device's Slave address
- **Address Valid flag (AV)** – A flag bit or device internal state that indicates whether the device's Slave address is valid

The process of assigning a Slave address starts with the ARP Master issuing a Reset Device or Prepare to ARP command, using the default Device Address. This Clears the AR flag in the Slave device (both flags are Cleared by a Reset Device command). The Master then issues a general Get UDID command. This causes all devices that support ARP to start driving their UDID onto the serial bus. A Target that loses the SMBus arbitration, backs off. Arbitration loss means that a device keeps the SMDAT line floating and it detects 0 driven by another device on the bus. Slave devices that lose arbitration issue NACK in response to further Bytes transmitted on the bus. After the ARP Master finishes the Get UDID sequence, it issues a Set Address command to the Slave device, using the Slave's UDID. All Slave devices on the bus monitor the UDID that is transmitted by the ARP Master, but only the particular device that has the matching UDID adopts the new Slave address, and Sets its own AV and AR flags. After the Slave device sets its AR flag, that device no longer responds to a general Get UDID command, which allows other devices to participate in the ARP process. All ARP commands require PEC checking and generation.

7.3.4.1 SMBus UDID

The 128-bit UDID is comprised of the following fields, as illustrated in Figure 7-15 (not to scale). Each UDID field and its default value implemented in the PEX 8604 and meaning are explained in the tables that follow.

Figure 7-15. 128-Bit SMBus UDID

8 bits	8 bits	16 bits	16 bits	16 bits	16 bits	16 bits	32 bits
127:120	119:112	111:96	95:80	79:64	63:48	47:32	31:0
Device Capability	Version/ Revision	Vendor ID	Device ID	Interface	Subsystem Vendor ID	Subsystem Device ID	Vendor-Specific ID

Table 7-19. SMBus Device Capability [127:120]

Field	Name	Default Value	Description
0	PEC Supported	1	By default, PEC generation and checking are enabled.
5:1	***Reserved***	00_000b	
7:6	Address Type	10b	Defaults to 10b. The PEX 8604 SMBus Address Type is implemented as Dynamic and volatile. 00b = Fixed address 01b = Dynamic and persistent 10b = Dynamic and volatile 11b = Random number device

Table 7-20. SMBus Version/Revision [119:112]

Field	Name	Default Value	Description
2:0	Silicon Revision ID	010b	PEX 8604, Silicon Revision BA.
5:3	UDID Version	001b	UDID version defined for *SMBus v2.0*.
7:6	***Reserved***	00b	

Table 7-21. SMBus Vendor ID [111:96]

Field	Name	Default Value	Description
15:0	Vendor ID	10B5h	PLX Vendor ID.

Table 7-22. SMBus Device ID [95:80]

Field	Name	Default Value	Description
15:0	Device ID	8604h	PEX 8604 default Device ID value.

Table 7-23. SMBus Interface [79:64]

Field	Name	Default Value	Description
3:0	SMBus Version	0100b	*SMBus v2.0*.
15:4	***Reserved***	000h	Supported protocols.

Table 7-24. SMBus Subsystem Vendor ID [63:48]

Field	Name	Default Value	Description
15:0	Subsystem Vendor ID	10B5h	PLX Vendor ID.

Table 7-25. SMBus Subsystem Device ID [47:32]

Field	Name	Default Value	Description
15:0	Subsystem Device ID	8604h	PLX part number for the PEX 8604.

Table 7-26. SMBus Vendor-Specific ID [31:0]

Field	Name	Default Value	Description
31:0	Vendor-Specific ID	Depends upon I2C_ADDR[1:0] input levels. The four combinations provide the following ID values: 00b = 7000_0000h 01b = B000_0000h 10b = D000_0000h 11b = E000_0000h	The Vendor-Specific ID is used to provide a unique ID for functionally equivalent devices. This is for devices that would otherwise return identical UDIDs for the purpose of dynamic address assignment. The combination of two Address bits produces four unique Vendor-Specific ID values, for a maximum of four SMBus-enabled PEX 8604s to co-exist on the same SMBus segment.

7.3.4.2 SMBus Supported ARP Commands

The PEX 8604 supports all ARP Slave commands. The Notify ARP Master command, which requires Master functionality, is ***not*** supported. Table 7-27 explains the PEX 8604 response to each received ARP command.

Table 7-27. SMBus Supported ARP Commands, Format, and Actions

ARP Command	SMBus Command Format	Slave Address	Command Code	Action
Prepare to ARP (Only General)	Send Byte (Refer to Figure 7-16)	SMBus default Device Address 1100_001b	01h	Clear the *AR Flag* and prepare for the ARP process. *AV Flag* will have no change.
Reset Device (General)	Send Byte (Refer to Figure 7-16)	SMBus default Device Address 1100_001b	02h	Clear the *AR Flag* and *AV Flag*.
Reset Device (Directed)	Send Byte (Refer to Figure 7-16)	SMBus default Device Address 1100_001b	Target Device Address[7:1] + 0	If the *AV Flag* is Set, Set ACK and Clear the *AR Flag* and *AV Flag*; else, NACK/REJECT.
Get UDID (General)	Block Read (Refer to Figure 7-17)	SMBus default Device Address 1100_001b	03h	Respond only if the *AR Flag* is Cleared; else, NACK/REJECT. *AR Flag* and *AV Flag* are not changed. Address returned is all ones (1), if the *AV Flag* is Cleared.
Get UDID (Directed)	Block Read	SMBus default Device Address 1100_001b	Target Device Address[7:1] + 1	*AR Flag* and *AV Flag* are not changed. ACK if *AV Flag*=1; else, NACK/REJECT. Data Byte 17 returned will be the SMBus Slave address.
Assign Address ARP	Block Write (Refer to Figure 7-18)	SMBus default Device Address 1100_001b	04h	Always ACK and Set the *AR Flag* and *AV Flag*, if the UDID matches.

Figure 7-16. Prepare SMBus ARP Command and SMBus Reset Device Command Format

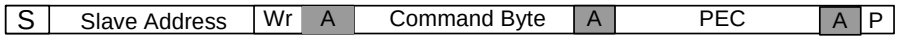
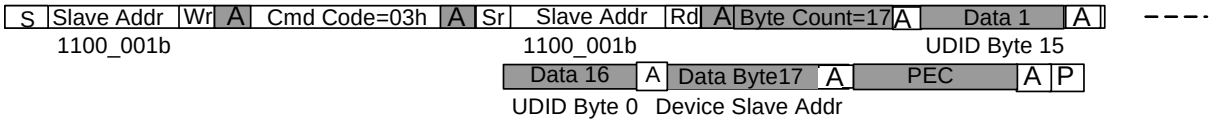
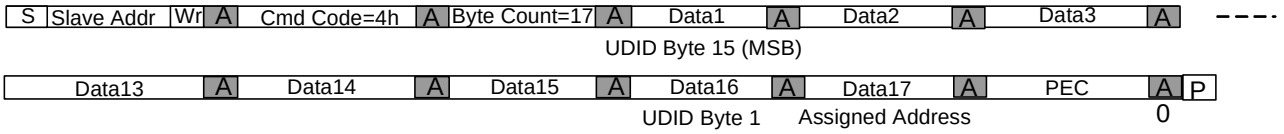


Figure 7-17. Get SMBus UDID Command Format (General Get UDID Command with PEC)



Note: *If the **SMBus Configuration** register AR Flag bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 344h[11]) is Cleared, the device returns the Slave Address field as 1111_111b; otherwise, it returns the device Slave address. Bit 0 (LSB) in the Data Byte 17 field should be 1.*

Figure 7-18. Assign SMBus Address ARP Command Format



Note: *Bit 0 (LSB) of the Data 17 field is ignored in the Assign Address command field.*

7.3.5 SMBus PEC Handling

The PEX 8604 supports the optional *SMBus v2.0* PEC generation and checking feature. This feature is required for the ARP process; however, it is optional for standard data transfer operation. The PEX 8604 supports PEC Cyclic Redundancy Check (CRC) generation and checking during ARP, as well as during Read/Write transfers to the PEX 8604 registers. The CRC polynomial used for PEC calculation is:

$$C(x) = x^8 + x^2 + x + 1$$

An 8-bit parallel CRC is implemented. The PEC calculation does not include ACK, NACK, START, STOP, nor repeated START bits. An SMBus Master can determine whether a Slave device supports PEC, from the UDID value returned by the Slave device, in response to a Get UDID command.

As a Slave device, the PEX 8604 checks the PEC, if the Master transmits the additional PEC byte and the PEX 8604 PEC checking feature is enabled (default). PEC checking can be disabled, by Setting the **SMBus Configuration** register *PEC Check Disable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 344h[9]).

Additionally, when PEC is enabled, packets received with an incorrect PEC value are dropped. If PEC checking is disabled and a received PEC byte value is incorrect, the PEX 8604 accepts the packet. During a register Read, if the Master requests the additional PEC byte, the PEX 8604 generates and transmits the PEC byte after the register data.

7.3.6 Addressing PEX 8604 SMBus Slave

By default, the PEX 8604 supports ARP when the I2C_ADDR2 input is tied Low, and expects the ARP Master to Set the PEX 8604 SMBus Device Address. If ARP is disabled by I2C_ADDR2 input being pulled High, the default Slave address is 38h (Address bits [7:1] are 0111_000b, with Address bit [1:0] values loaded from the I2C_ADDR[1:0] inputs). The two Address bits allow a maximum of four PEX 8604 SMBus Slaves to co-exist without address conflict on the SMBus, using SMBus Address byte values of 70h, 72h, 74h, and 78h. The I2C_ADDR[2:0] inputs are loaded immediately after Fundamental Reset, and any subsequent change of input value does not affect functionality.

If the **SMBus Configuration** register *UDID Address Type* field is programmed as Fixed Address (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 344h[13:12], are both Cleared) without disabling ARP, the PEX 8604 still participates in ARP, but does not Set the Device Address after ARP successfully completes.

The SMBus Slave Address can be changed at any time, by using software to write to the register's *SMBus Device Address* field (offset 344h[7:1]). ARP can also be enabled or disabled at runtime, by writing to the register's *ARP Disable* bit (offset 344h[8]). If ARP is disabled by software after initially being enabled, the default address (70h) is not used for subsequent transactions. In this case, software must program a Slave address into the *SMBus Device Address* field. When software writes the Device Address, it must also Set the register's *AR Flag* and *AV Flag* bits (offset 344h[11:10], respectively), to indicate that the address is valid and resolved.

Whenever software changes the register's *AV Flag*, *ARP Disable*, and/or *SMBus Device Address* values, software must also Set the register's *SMBus Parameter Reload* bit (offset 344h[15]). Writes to this register bit take effect only when the register's *SMBus Command In-Progress* bit (offset 344h[28]) is Cleared, which indicates that the PEX 8604 SMBus interface is in the Idle state.

7.3.7 SMBus Timeout

Unlike I2C, where the Slave or Master can indefinitely hold the I2C_SCL0 line Low, SMBus has a timeout condition. No device is allowed to hold the I2C_SCL0 line Low for more than 25 ms. When the PEX 8604, as a Slave-Transmitter, detects that it has pulled the I2C_SCL0 line Low for more than 25 ms, the PEX 8604 releases I2C_SCL0, and the logic returns to its default state and waits for another START condition. This can also occur when the Master pulls the I2C_SCL0 line Low for more than 25 ms during any single Clock Low interval within a transfer in progress, or during the ACK phase, if the Master pulls the I2C_SCL0 line Low to process a task. Generally, the PEX 8604 pulls the I2C_SCL0 line Low if SMBus access to registers is delayed by internal arbitration for register access.

7.4 Switching between SMBus and I2C Bus Protocols

The PEX 8604's I2C implementation allows switching between the SMBus and I2C protocols, by toggling the **SMBus Configuration** register *SMBus Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 344h[0]).

When operating in SMBus mode, Clearing this bit, using the SMBus Block Write protocol, enables I2C protocol for subsequent register accesses. This SMBus Block Write can be transmitted from an SMBus or I2C Master, provided that the Block Write Byte sequence conforms to the sequence explained in Section 7.3.3.1. In I2C mode, writing 1 to the *SMBus Enable* bit turns On the SMBus protocol, immediately after the Write operation is complete.

Chapter 8 Virtual Channels and Port Arbitration

8.1 Quality of Service Support

Quality of Service (QoS) is a feature offered by PCI Express that was not available before in PCI. *QoS* refers to being able to guarantee preferential treatment for a particular application or for traffic coming from a particular source. The PEX 8604 provides two methods for acquiring QoS:

- Virtual Channel support
- Port arbitration

8.2 Virtual Channel Support

The PEX 8604 supports up to two Virtual Channels (VCs) that act as two completely independent paths through the switch, as defined in the *PCI Express Base r2.0*. Although the two VCs of a Port share the same physical wire/Links, the PEX 8604 has separate queues and separate credit mechanisms for each VC. At the egress stage of each Port, the PEX 8604 has three arbitration methods for determining which TLP from which VC to send on the wire/Link.

The elements of these features are described in the following subsections.

8.2.1 Traffic Class to Virtual Channel Mapping

The Traffic Class to Virtual Channel (TC/VC) mapping is Port-specific and must be configured and enabled for each Port. The default configuration for a PEX 8604 Port maps all TC[7:0] bits to VC0, as defined in the Port's **VC0 Resource Control** register *TC/VC0 Map* bits (offset 15Ch[7:1, 0]). Any of the TC IDs (except TC0) can be mapped to the second VC (*that is*, VC1), by removing them from the *TC/VC0 Map* bits and adding them to the Port's **VC1 Resource Control** register *TC/VC1 Map* field for TC[7:1] (offset 168h[7:1]). If any TCs are mapped to VC1, in addition to performing all steps outlined in Section 8.4 (to set up PCI Express credits for VC1), VC1 must be enabled (**VC1 Resource Control** register *VC1 Enable* bit (offset 168h[31]) is Set).

Note: *The actual VC ID of the second VC is Set by the **VC1 Resource Control** register VC1 ID field (offset 168h[26:24]).*

8.2.2 Ingress VC Arbitration

The PEX 8604 supports hardware-fixed Round-Robin arbitration on the ingress Ports. Round-Robin servicing is performed between the two VCs, per Port. If any ingress Ports are targeting a congested Egress queue (Egress queue depth is greater than its programmable threshold), that ingress Port removes itself from the arbitration pool.

8.2.3 Egress VC Arbitration

The PEX 8604 supports three methods of arbitration on the egress Ports:

- Fixed-Priority VC Arbitration
- Round-Robin VC Arbitration
- Weighted Round Robin Arbitration

Each method is described in the sections that follow.

8.2.3.1 Fixed-Priority VC Arbitration

The *PCI Express Base r2.0* defines the default Hardware-Fixed Strict Priority scheme based upon the inherent priority of the VC IDs, where VC1 has higher priority than VC0. The VC IDs alone determine the sequence in which transactions are sent. For this Arbitration scheme, the **Port VC Capability 1** register *Low-Priority Extended VC Counter* field (offset 14Ch[6:4]) must be Cleared.

8.2.3.2 Round-Robin VC Arbitration

If the **Port VC Capability 1** register *Low-Priority Extended VC Counter* field (offset 14Ch[6:4]) is programmed to 001b (default), VC0 and VC1 share the same Low-Priority Virtual Channel group. As a result, the PEX 8604 alternates selecting VC0 and VC1 in a fair, Round-Robin manner.

8.2.3.3 Weighted Round Robin Arbitration

The PEX 8604 also supports a Weighted Round-Robin (WRR) Arbitration scheme between the two VCs, as defined by the upstream Port's **VC WRR *x*** registers (Upstream Port, offsets 530h and 534h). Each Port has an 8-way time-slice [7:0], whose Setting determines which of the VCs take that time slot. (Refer to Section 13.16.1, "Device-Specific Registers – Virtual Channel Weighted Round Robin Arbitration (Offsets 530h – 540h).")

8.3 Queue Handling

The PEX 8604 implements queues at the ingress and egress Ports. There is arbitration capability for both Ingress and Egress queues. By default, the PEX 8604 attempts to send every packet on the Ingress queue to the Egress queue, until the Egress buffer fills. That results in optimum use of the PEX 8604 on chip buffering; however, it might create a situation in which one high-priority Port takes too much latency.

The packets within each Port's Egress queue are serviced on a first-in, first-out basis within each VC and Type (without violating Conventional PCI Ordering rules). The amount of queuing in the egress side is programmable, per VC. The **Port Egress TLP Threshold** register (offset F10h) establishes a range (minimum and maximum) for the Egress queue depth, for each VC. By reducing the thresholds, the Egress queue size is constrained. A smaller Egress queue means that newly arriving packets from a high-priority source do not have to wait as long for any earlier arriving packets from another source in the same VC, because the quantity of earlier arriving packets is reduced.

Each Port's Egress queue size is programmable, using the **Port Egress TLP Threshold** register fields. The *Port Upper TLP Counter* field (offset F10h[26:16]) allow for a maximum queuing of TLPs in the egress Port. If that maximum is crossed, the destination backpressures any source attempting to write to the destination queue. After the programmed minimum (established by the *Port Lower TLP Counter* field (offset F10h[10:0]) is crossed, the backpressure releases and the source can once again forward TLPs to that destination.

8.4 VC1 Ingress Credit

TLPs consume PCI Express credits (and RAM space) upon entering the PEX 8604. When the TLPs are sent out of the PEX 8604 and an ACK is received, these credits (and Buffer space) are released. When a TLP enters the PEX 8604 and the internal credit engine has free credits available, an UpdateFC DLLP is generated, to replenish the credits used by the Transmitter. If there are no credits available, the credit engine waits until an ACK is received from a sent TLP before generating an UpdateFC DLLP.

Refer to Section 13.16.12, "Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch)," for the default PCI Express credits of various Ports, based upon their Link widths.

8.4.1 VC1

A key element of enabling and using VC1 on a Port/Link is providing for PCI Express credits associated with the VC1 queues.

To enable, and program the credits for, VC1:

1. The PEX 8604 VC1 Global Enable defaults to a value of 1 (VC1 support is disabled) at reset.

   To enable the VC1 capability, Clear the **Miscellaneous Control** register *VC1 (2nd VC) Disable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 28Ch[0]).

   This enables the PEX 8604 to support a second VC, but does not actually enable the VC.

2. Program the VC1 Credit Threshold registers, starting at offset A0Ch. (Refer to Section 13.16.12, "Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch).")

3. Set the **VC1 Resource Control** register *VC1 Enable* bit (offset 168h[31]).

   VC1 is now enabled.

8.4.1.1 VC1 Threshold Registers

The default values of Credit fields in the various VC1 Credit Threshold registers (in the offset A0Ch through A8Ch range) are zero (0), which equates to infinite credits. Because the PEX 8604 cannot support infinite credits, except for Non-Posted Payloads, it is ***very*** important that the Threshold registers are re-programmed before enabling VC1. The minimum value is 1 Header credit and 1 Payload credit or 1 MPS Payload credits (The Posted and Completion Payload minimum is 1 MPS. The Non-Posted Payload credit minimum is 1). Depending upon the Port configuration and MPS, it is possible that even using the minimum VC1 credits, more credits will be advertised then are actually available in the PEX 8604. If this is the case, the Credit Threshold registers for VC0 will also need to be re-programmed, to a smaller value, to compensate for the credits assigned to VC1.

Note: *Enabling VC1 and programming the VC1 Credit Threshold registers can have a direct effect on the PEX 8604 and system performance. Because of this possible side effect and the possibility of advertising too many credits, contact PLX Technology Technical Support for assistance, as seen needed, when using VC1.*

8.4.1.2 Programming the VC1 Global Enable and Threshold Registers

The Global Enable (offset 28Ch[0]) and Threshold (offsets A0Ch to A2Ch) registers can be programmed in three ways, using:

- Serial EEPROM
- I^2C
- CPU (software)

If the serial EEPROM is used to Set the Global Enable bit and the VC1 Threshold Registers, nothing further is needed. However, if I^2C and/or the CPU is used, a Hot Reset to the PEX 8604's upstream Port must be generated after the PEX 8604 Credit Threshold registers are programmed. The Hot Reset is required, to allow the internal Credit Engine to account for the new credits assigned to VC1.

8.4.1.3 Usage Example

The simplest example is if only Non-Posted TLPs, or Posted TLPs with a small Payload length, are used. In the example that follows, each Port and type is given two Headers. If one Header is preferred, it is necessary to re-program the appropriate **INCH Threshold VC1** register *UpdateFC High-Priority Threshold for Header Credit* fields.

Example configuration:

- MPS = 128 bytes
- Upstream Port = Port 0
- Downstream Port 1 needs VC1

Registers to write:

1. Program offset A0Ch (Port 0, Posted) to 408h.
2. Program offset A10h (Port 0, Non-Posted) to 401h.
3. Program offset A14h (Port 0, Completion) to 408h.
4. Program offset A24h (Port 1, Posted) to 408h.
5. Program offset A28h (Port 1, Posted) to 401h.
6. Program offset A2Ch (Port 1, Completions) to 408h.
7. Clear offset 28Ch[0], to enable support for VC1.

Following a Fundamental or Hot Reset, a value of 1 is written to the Port 0 and Port 1 **VC1 Resource Control** register *VC1 Enable* bit (offset 168h[31]).

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Chapter 9 Performance Features

9.1 Introduction

This chapter discusses guidelines for programming on-chip registers, to boost performance beyond that provided by the general-purpose default values, specifically:

- DLLP Policies
- Ingress Resources
- Latency
- Queuing Options
- Read Pacing
- Dual Cast

9.2 DLLP Policies

DLLP rates can vary from 0 to 2 or more DLLPs/TLP. The PEX 8604 allows programming to affect the DLLP rate. An increase in DLLPs reduces the total TLP throughput. Therefore, for designs that require high performance, it would be beneficial to minimize DLLP rates. Transmitting fewer DLLPs, however, can result in credit starvation or Replay buffer overfill, which can have a detrimental effect on TLP bandwidth. Care must be taken when changing the default PEX 8604 DLLP transmission rate.

Typically, TLPs have higher transmission priority on the wire than DLLPs. The PEX 8604, however, allows DLLPs to have higher priority under certain conditions, meaning that DLLPs can transmit before starting a new TLP. The decision to transmit a DLLP ahead of a TLP is referred to as *DLLP policy.*

The PEX 8604 can be programmed to alter its default DLLP policies, to emphasize improved TLP throughput, faster acknowledgement, more credit, or simplest behavior. The PEX 8604 default policies are designed to achieve optimal performance for most applications. Programmable choices for a DLLP policy, however, allow for further optimization.

9.2.1 ACK DLLP Policy

An *ACK DLLP* is a response indicating to the TLP Transmitter that the Receiver received a "good" copy of the TLP, meaning that it acknowledged receipt of the TLP. The simplest policy is to send 1 Acknowledge Control Packet (ACK) for every received TLP, resulting in a 1 DLLP/TLP rate for ACK alone. What an ACK means to the TLP Transmitter is that the TLP Transmitter can remove any stored copy of that TLP, because it is unnecessary to resend the TLP. ACK DLLPs can be combined, so that one ACK DLLP can serve to acknowledge multiple TLPs. This collapsing of ACKs is the basis of the ACK DLLP policy choices. Less-frequent, more-collapsed ACKs have the least impact on TLP transmit bandwidth, meaning that less-frequent ACKs result in less than 1 DLLP/TLP.

The PEX 8604 ACK policy consists of two parts – a Timer and TLP Counter. The default ACK Timer policy/value varies according to the negotiated Link width, operating Link speed, and Maximum Packet Size, as recommended in the *PCI Express Base r1.1* or *PCI Express Base r2.0*. The values provided in Table 9-1 define some of the possible default values, in symbol times.

Note: *The values listed in Table 9-1 have been adjusted to be different than the PCI Express Base r2.0 values, to compensate for hardware-specific latencies.*

Table 9-1. Sample PEX 8604 ACK Latency Timer Values

Maximum Payload Size (Bytes)	x2 Gen 2 (Symbol Times)	x1 Gen 2 (Symbol Times)
128	89	288
256	134	466
512	170	610

The ACK Transmission Latency Timer loads the appropriate value when a TLP is received and known to be good, meaning a few clocks after the END framing symbol is received. The Timer counts down each symbol time (every 4 ns (*PCI Express Base r1.1*) or 2 ns (*PCI Express Base r2.0*)). When the Timer reaches 0, an ACK DLLP takes higher priority over new TLPs (*that is*, an ACK DLLP is transmitted before a new TLP is started). The ACK DLLP transmitted acknowledges all TLPs, up to the most recently arrived good TLP.

The TLP Counter counts down on each TLP arrival until it reaches 0, then schedules a high-priority ACK DLLP. The default initialization value for the TLP Counter is 16, meaning a high-priority ACK is scheduled upon the arrival of 16 TLPs. The **Ingress Control Shadow** register *ACK TLP Counter Timeout* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 664h[10:9]) value controls the Counter, as follows:

- 00b – Allows 16 TLPs before a high-priority ACK (default)
- 01b – Allows 8 TLPs before a high-priority ACK
- 10b – Allows 4 TLPs before a high-priority ACK
- 11b – Disables the Counter

Either the Latency Timer or TLP Counter mechanism can cause a high-priority ACK DLLP to be scheduled, and the first one to do so re-initializes both mechanisms to their starting parameters. *For example*, the time for 16 TLPs can be less than the ACK Timer above, in which case an ACK is sent earlier. The TLP Counter is useful for any system with a large programmed MPS (resulting in a large Timer value), that is capable of sending short TLPs (*such as* 12-byte Memory Reads). Rather than require the Transmitter to save possibly 100+ small TLPs, it need only save 16, plus whatever else arrives during the round-trip time.

If there is no TLP traffic being transmitted (*that is*, the Transmit Link is idle), an ACK DLLP can be transmitted immediately, before the Latency Timer expires. This is an opportunistic, low-priority ACK because it does not contend with a TLP in transmission. When an opportunistic, low-priority ACK is transmitted, both the Latency Timer and TLP Counter re-initialize, waiting for a new TLP to arrive to begin counting again.

The PEX 8604 allows a programmable override of the default Ack_Latency_Timer value, on a per-Port basis, by programming the **ACK Transmission Latency Limit** register *ACK Transmission Latency Limit* field (offset 1F8h[11:0]). The value in this register is loaded when a new TLP arrives and a high-priority ACK DLLP is attempted when the Timer reaches 0. For fastest ACK response, this Timer can be programmed to 000h, resulting in one DLLP ACK transmitted immediately per each TLP received. For less impact on Transmit TLP bandwidth, a larger value can be programmed, resulting in less-frequent ACKs.

In general, a slower ACK response does not impact the Receive TLP stream, and aids the TLP Transmit stream. Every PCI Express device contains storage (Retry buffer) for storing TLPs while waiting for ACKs. The amount of Retry buffer storage a device contains is vendor-dependent. The quantity of TLPs the PEX 8604 can store depends upon the type and size of TLPs received. (Refer to Section 9.3.) The PEX 8604 holds TLPs in the Retry buffer while waiting for an ACK. At some point, if the Retry buffer storage fills, no new TLPs can be sent until a new received ACK frees up space. In this case, the ACK can become a performance bottleneck.

9.2.2 UpdateFC DLLP Policy

An *UpdateFC DLLP* is transmitted in response to a received TLP. The UpdateFC DLLP replenishes the connected device with additional credit, to allow the Transmitter to transmit more TLPs of that type. Each TLP that arrives consumes credit, and eventually, a stream of TLPs consume all the available credit, unless an UpdateFC DLLP provides additional credit. However, if the connected device has sufficient credit to transmit more TLPs, it is not necessary to transmit UpdateFC DLLPs to it. The UpdateFC policy determines how and when to transmit an UpdateFC DLLP.

There are two parts to the UpdateFC policy – frequency of transmitting the updates and credit amount. This section discusses only the frequency. Refer to Section 9.3 for details regarding credit amounts.

If the PEX 8604 is not transmitting TLPs (*that is*, the Transmit Link is idle), and credit to replenish the credit used becomes available, the PEX 8604 immediately transmits an UpdateFC DLLP to the connected device. This is an opportunistic, low-priority UpdateFC DLLP.

However, if the PEX 8604 is busy transmitting TLPs to the connected device, the PEX 8604 does not transmit an UpdateFC DLLP until a programmed threshold is crossed. The PEX 8604 provides four threshold options – 100%, 75% (default), 50%, and 25%. Whenever the remaining credit drops below the programmed threshold, an UpdateFC DLLP is given high priority, meaning that the UpdateFC DLLP is transmitted before a new TLP is started. There is a separate threshold for Header and Payload credits, for each TLP type – Posted, Non-Posted, and Completion – for each Half-Station Port, located in the **Ingress Credit Handler (INCH) Threshold** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets A00h through A8Ch).

The example of UpdateFC options (provided in Table 9-2) chart how, for the various options, an UpdateFC is triggered. This example is for a traffic stream of six back-to-back, 256-byte Posted TLPs, using a x2 Port, where the maximum Posted Header credit is 25 and the maximum Posted Payload credit is 128. A 256-byte Payload requires 16 credits (1 credit per 16 bytes). Therefore, each TLP in this case consumes 1 Header and 16 Payload credits.

Once a high-priority UpdateFC is triggered, if there are sufficient on-chip resources to do so, the running credit deficit is fully restored. For most non-congested applications, it is likely that ample chip resources will exist, to fully restore credit with every UpdateFC. However, if resources are running low, only a portion of the running credit is restored. If the threshold for transmitting an UpdateFC remains crossed, then, as more resources become available, a subsequent DLLP is transmitted until the deficit is satisfied.

Selecting the 100% policy results in a high-priority UpdateFC for every TLP received. By itself, this policy results in 1 DLLP/TLP, without factoring in the ACK policy. The 75% policy triggers 1 DLLP for every 2 TLPs for this traffic load, which results in 0.5 DLLP/TLP without the ACK. The 50% policy results in 0.25 DLLP/TLP, and the 25% policy results in 0.16 DLLP/TLP.

Table 9-2. Example UpdateFC Options

TLP Received	Running Credit Header, Payload Consumed/Total	25% Remains Triggers when 6 Header or 32 Payload Credits Remain	50% Remains Triggers when 12 Header or 64 Payload Credits Remain	75% Remains Triggers when 18 Header or 96 Payload Credits Remain	Less than 100% Remains Update ASAP
TLP0	24/25, 112/128	–	–	–	UpdateFC
TLP1	23/25, 96/128	–	–	UpdateFC	UpdateFC
TLP2	22/25, 80/128	–	–	UpdateFC	UpdateFC
TLP3	21/25, 64/128	–	UpdateFC	UpdateFC	UpdateFC
TLP4	20/25, 48/128	–	UpdateFC	UpdateFC	UpdateFC
TLP5	19/25, 32/128	UpdateFC	UpdateFC	UpdateFC	UpdateFC

9.2.3 Unidirectional DLLP Policies

For unidirectional traffic, the PEX 8604 DLLP policies allow the most-frequent DLLPs, because DLLPs do not interfere with TLPs. (DLLPs flow in the opposite direction of TLPs.)

The PEX 8604 can transmit a DLLP ACK almost immediately upon receiving and verifying a TLP. A faster ACK results in fast Transmitter de-allocation of the TLP, and can therefore allow a shallow TLP Replay buffer. The default values can be overwritten, to increase or decrease the ACK DLLP rate. For unidirectional traffic, a small number, *such as* 1, is recommended.

The number programmed into the **ACK Transmission Latency Limit** register *ACK Transmission Latency Limit* field (offset 1F8h[11:0]) Sets the ACK Transmission Latency Timer, to count the quantity of symbol times after receiving a TLP, before transmitting an ACK.

Similar to the ACK programmability, the PEX 8604 can immediately transmit an UpdateFC after receiving only the TLP Header. By transmitting an UpdateFC earlier, the total credit advertised can be minimized. By programming fewer credits and having a fast UpdateFC policy, the system does not run out of credits and the PEX 8604 does not waste Buffer space on reservations that do not arrive. The following are the recommended Settings:

- Set the UpdateFC policy for unidirectional traffic to 100%
- Set the credits to be sufficient to allow 3 to 4 TLPs

9.3 Ingress Resources

Note: *This section of the data book introduces the concept of Half Stations (which is sometimes mentioned, but not often, in the other chapters within this data book). Its use is necessary here, however, to "illustrate" their function.*

The PEX 8604 manages ingress credit on an even- and odd-numbered-Port basis; therefore, there are separate Credit Handler engines for the Even and Odd Ports. An internal hardware processing partition of Even or Odd Ports is referred to as a *Half Station*. All even-numbered-Ports belong to Half Station 0. All odd-numbered-Ports belong to Half Station 1.

For each Half Station, there are two central resources of on-chip ingress credit RAM – Header and Payload. The total Half-Station Header RAM size is 256 Header credits. The total Half-Station Payload RAM size is 512 Payload credits. A Header credit reserves 4 DWords of RAM storage, regardless of whether the Header size is 3 or 4 DWords. By design, a PEX 8604 Half Station reserves 12 Header credits and 32 Payload credits out of the RAM totals, for special hardware-specific storage needs.

The STRAP_PORTCFG[1:0] inputs configure the quantity of enabled Ports, and the Link width of each Port. At initialization, the PEX 8604 optimally assigns the credits, based upon the selected Port configuration.

Header RAM stores TLP Headers, meaning that every Header credit advertised reserves one Header RAM location, and every TLP received on the PEX 8604 uses one Header RAM location. After subtracting the reserved operational Half Station Header RAM locations, there remains a net total of 244 Header entries available.

Payload RAM stores TLP Payload. A Payload credit is in units of 16 bytes. Of the 2,016 user-configurable entries, 4 credits must be allocated for each Posted and Completion Header credit advertised. These credits are used internally, for linking Posted and Completion TLP Payload to their respective Header.

Every Port receives and transmits the following three traffic types (packets):

- Posted (P)
- Non-Posted (NP)
- Completions (Cpl)

Each Port can be assigned to one or two Virtual Channels (VC0 or VC1).

All three traffic types and each Virtual Channel (VC0 and/or VC1) needs credit, for each Port. The **INCH Threshold** register bit fields (refer to Table 9-6) allocate the credit to be reserved (and advertised) for each Port VC, and traffic type. Once allocated, the credits remain dedicated to each Port, VC, and traffic type.

As TLPs arrive, they are stored on the PEX 8604, until an ACK is received from the final destination. Until the ACK is received, each TLP stored consumes credit, and continues to occupy RAM until released. The RAM/credit is released only after the Receiver has acknowledged to the sender the arrival of the TLP, without any errors per ACK/Negative Acknowledge (NAK) policy. The total quantity of TLPs stored, but not yet forwarded to, and acknowledged by, the next PCI Express device, depends upon congestion and the next PCI Express device's ACK policy.

There are trade-offs between the quantity of credits allocated for a particular traffic type and Port combination, perhaps more for one system configuration than another. To alleviate these trade-offs, the PEX 8604 contains an innovative Dynamic Buffering design that allows a programmable-sized portion of the RAM to store any of the three traffic-type TLPs from any Half-Station Port. The credits that remain, after allocating credits for each of the three traffic types and VC for each Port, become part of a *Dynamic buffer*. The Dynamic buffer is essentially a common pool of Half-Station credits, and is discussed in detail in Section 9.3.2 and Section 9.3.3.

The PEX 8604 default credit allocation values, which create a variable-sized Dynamic buffer for each of the possible Port configurations, are optimal for most applications. Detailed tables of the default initial credit allocation for all three TLP types, and an explanation of the common credit pool, are addressed in the following sections.

9.3.1 Initial Credit Allocation

The PEX 8604 default credit allocation values depend upon the strapped Link width, not the negotiated Link width. The initial credit values that the Initialization Flow Control (InitFC) DLLP advertises on a per-Port basis, which the PEX 8604 transmits after Linkup, are listed in Table 9-3 (in credits) and Table 9-4 (in bytes).

The amount of credit that a Port initially advertises is controlled by the **INCH Threshold** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets A00h through A8Ch). (Refer to Section 9.3.3.) The default value of these registers changes, depending upon the STRAP_PORTCFG[1:0] input levels. Because of the way the hardware links the default **INCH Threshold** register credit values into actual reserved RAM storage, in some cases, one or two additional initial Payload credits are allocated out of the Half-Station common pool. If this occurs, the Port advertises this additional initial credit in its InitFC DLLPs.

Note: *The default initial credits for VC1 are all infinite. If VC1 is enabled, the user must calculate and program the needed optimal VC1 initial credit values. These values should be programmed into the **INCH Threshold** register fields, using a serial EEPROM.*

Table 9-3. Initial Port Credit Allocation (*where* 1 Header credit means storage is available for one Header of any size, and 1 Payload Credit = 16 bytes)

Configured Port Link Width	Posted Header/Payload	Non-Posted Header/Payload	Completion Header/Payload
VC0			
x2	26/256	26/infinite	26/224
x1	7/64	7/infinite	5/64
VC1			
x2	infinite/infinite	infinite/infinite	infinite/infinite
x1	infinite/infinite	infinite/infinite	infinite/infinite

Table 9-4. Initial Port Credit Allocation for Header/Payload (*where* 1 Header credit means that storage is available for one Header, in bytes; Payload credits are listed in bytes)

Configured Port Link Width	Posted Header/Payload	Non-Posted Header/Payload	Completion Header/Payload
VC0			
x2	416/4,096	416/infinite	416/3,584
x1	112/1,024	112/infinite	80/64
VC1			
x2	infinite/infinite	infinite/infinite	infinite/infinite
x1	infinite/infinite	infinite/infinite	infinite/infinite

9.3.2 Dynamic Buffering

The PEX 8604 default credit values are optimal for most applications, to maintain back-to-back TLP traffic indefinitely, without running out of credit. After any of the initial credit (storage space) is used, more resources are automatically made available from the Half-Station Dynamic buffer, to maintain the initial credit allotment. These additional resources, taken from the Dynamic buffer, are not pre-reserved. Therefore, they can be used for either Virtual Channel or any of the three TLP types – Posted, Non-Posted, or Completion (P, NP, or Cpl, respectively). Because the TLP type is not pre-specified, these extra resources are termed a *common credit pool*.

When credit is actually replenished depends upon the UpdateFC DLLP policy (refer to Section 9.2.2), which is controlled by Setting the **INCH Threshold** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets A00h through A8Ch[19:18, 17:16], as appropriate). These thresholds are relative to the initial credits allocated to a Port. Common Pool credits that are allocated to a Port. Common Pool credits that are allocated to a Port before a high-priority UpdateFC DLLP is sent can be de-allocated, if the Port's initial credits are restored before the UpdateFC DLLP is sent.

The common credit pool for Header and Payload credit is as follows:

- **Common Header pool** – What remains in the Header RAM space, after subtracting the advertised Header credits of each Half-Station Port for each of the three TLP types, plus one or two VCs. Figure 9-1 illustrates the way in which the initial allocation of the PEX 8604 Header RAM is partitioned (by default) for a Half-Station x2 Port, with only VC0 in use.
- **Common Payload pool (Common Payload/Completion pool)** – What remains after subtracting the following from the Payload RAM:
  - 4 credits for each Posted and Completion Header Credit advertised, for each Half-Station Port
  - Posted (Payload) credits advertised for each VC and Half-Station Port
  - Completion credits advertised for each VC and Half-Station Port

  Figure 9-2 illustrates the way in which the PEX 8604 Payload (and Completion) RAM is partitioned (by default) for one Half-Station x2 Port.

Figure 9-1. One x2 Port Default Configuration of Header RAM (256 Total Credits)

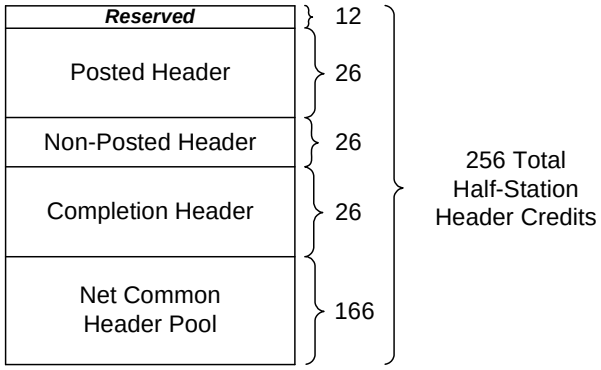
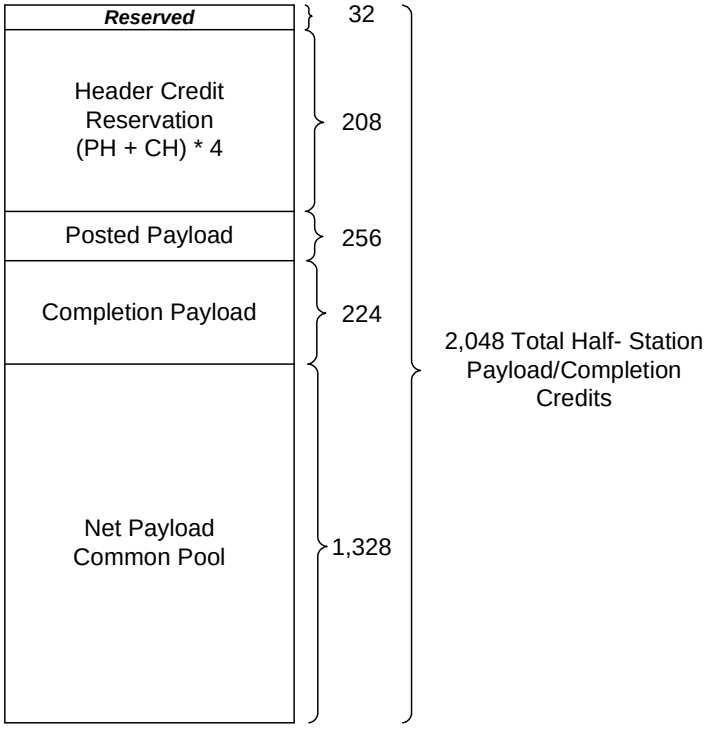


Figure 9-2. One x2 Port Payload/Completion RAM Default Configuration of 2,048 Credits



A larger common pool allows the most flexibility for handling any possible instantaneous traffic stream, without backpressuring ingress flows. The PEX 8604's initial credit allocation default Settings leave sufficient on-chip RAM to accommodate numerous large TLPs in the common pool, after default values for the initial credits are subtracted. Table 9-5 summarizes the common pool default allotment for several Half-Station Port configurations.

Table 9-5. Half-Station Port Configuration Common Pool Default Allotments

Half-Station Port Configuration	Common Pool Header Credits	Common Pool Payload Credits
x1x1x1x1	168	1,312
x2	166	1,328

Notes:

1. *Actual RAM usage for TLP and Header storage and linking is variable.*
2. *The subtraction of 4 credits for each Posted and Completion Header credit advertised, for each Port, is a simplification – the Common Pool credit values can be larger.*

9.3.3 Ingress Credit Handler Threshold Registers (Offsets A00h through A8Ch)

Note: *Although the entire end range of the **INCH Threshold** registers is included in the register reference, only those offsets associated with active Ports are used. All others are either **reserved** or **Factory Test Only**, as identified in Section 13.16.12, "Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch)."*

For each Port, there are six sets of **INCH Threshold** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets A00h through A8Ch) – Posted, Non-Posted, and Completion – one each, per VC. Table 9-6 lists the lower 16 bits for each register. (To view the complete register set, refer to Section 13.16.12, "Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch).")

The Non-Posted credits for Payload are Cleared, which equates to infinite credits. Because Non-Posted TLPs only have a 1-DWord Payload, they will never be longer than 5 DWords. Because the Header RAM is 5 DWords wide, only one Non-Posted Header credit is necessary to store a Non-Posted TLP.

Table 9-6. INCH Threshold Registers (Offsets A00h through A8Ch), Payload and Header Credit Fields

Ports and VC	Register Offset	Type	Payload		Header	
			Bit(s)	Description	Bit(s)	Description
Port 0, VC0	A00h	Posted	8:3	Payload Credit	15:9	Header Credit
	A04h	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A08h	Completion	8:3	Payload Credit	15:9	Header Credit
Port 0, VC1	A0Ch	Posted	8:3	Payload Credit	15:9	Header Credit
	A10h	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A14h	Completion	8:3	Payload Credit	15:9	Header Credit
Port 1, VC0	A18h	Posted	8:3	Payload Credit	15:9	Header Credit
	A1Ch	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A20h	Completion	8:3	Payload Credit	15:9	Header Credit
Port 1, VC1	A24h	Posted	8:3	Payload Credit	15:9	Header Credit
	A28h	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A2Ch	Completion	8:3	Payload Credit	15:9	Header Credit
Port 4, VC0	A60h	Posted	8:3	Payload Credit	15:9	Header Credit
	A64h	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A68h	Completion	8:3	Payload Credit	15:9	Header Credit
Port 4, VC1	A6Ch	Posted	8:3	Payload Credit	15:9	Header Credit
	A70h	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A74h	Completion	8:3	Payload Credit	15:9	Header Credit
Port 5 VC0	A78h	Posted	8:3	Payload Credit	15:9	Header Credit
	A7Ch	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A80h	Completion	8:3	Payload Credit	15:9	Header Credit
Port 5 VC1	A84h	Posted	8:3	Payload Credit	15:9	Header Credit
	A88h	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A8Ch	Completion	8:3	Payload Credit	15:9	Header Credit

9.3.4 Adjusting Initial Credit Values (Ingress Resources)

The default Initial Credit values listed in Table 9-3 and Table 9-4 can be changed; however, to do so, the values must be changed by serial EEPROM and/or I^2C, before the initial advertisement. It is also possible to use software to program the Credit registers over the Link; however, if the Link is up, credit cannot be removed, and values can only be increased. The Credit registers are sticky – a Hot Reset preserves any programmed values, and thereby allows any of the available programming methods to program credits at any time, even after the Link is up, if a Hot Reset is issued afterward to re-run the InitFC sequence.

When changing any credit value, follow the rules outlined in this section; otherwise, the credit can be incorrectly issued and data can be lost.

Credit is partitioned/programmed on a Half-Station basis. All even-numbered-Ports belong to Half Station 0. All odd-numbered-Ports belong to Half Station 1. Per the *PCI Express Base r2.0*, the minimum initial credit must be sufficient to meet the credit requirements of the MPS. To meet this requirement with a 512-byte MPS, the minimum credit value assigned to a Port, for both Posted and Completion TLPs, must be 128 credits each (one credit represents 16 bytes of storage).

Additionally, because each TLP may not optimally fill each location in the internal RAM, the Header credit affects the Payload credit used to store the Payloads. Therefore, for every Posted or Completion Header credit reserved, 4 credits from the Payload/Completion RAM must also be held in reserve.

The following abbreviations are used in the rules outlined in this section:

- *PH* is the total Posted Header credits that are advertised or can be stored
- *NPH* is the total Non-Posted Header credits that are advertised or can be stored
- *CH* is the total Completion Header credits that are advertised or can be stored
- *MPS* is the Maximum Payload Size
- *Hmax* is the maximum quantity of Header credits that can be assigned, per Half Station
- *Pmax* is the maximum quantity of Payload and Completion credits

The total credit advertised, per Half Station, must follow these rules:

1. Sum of all Header credits $\leq$ Hmax = 244.
   Sum of all Header credits = sum (all Ports PH + NPH + CH).
2. Payload and Completion credit must be sufficient for 1 MPS, for each Port.

   Note: *Non-Posted Payload credit is infinite and Read-Only.*
3. Sum of all Payload and Completion credits assigned, per Half Station,
   is $\leq$ Pmax = 2,016 $\leq$ (Advertised Posted Payload + Advertised Completion Payload + (4 x (sum of all Ports PH + CH))).

9.3.5 Credit Allocation When Common Pool Is Consumed

A Half Station's common credit pool is consumed by any Port's Ingress or Egress queue for that Half Station, on a first-come, first-served basis. If the Half Station's common pool is completely consumed (and therefore, each Half-Station Port's credit), the PEX 8604 Half Station is in a congested state. In the congested state, the Half Station is unable to provide additional credit to any of its Ports, until credit is released. Credit is released only after the Receiver acknowledges the packet with an ACK. In this state, the following register fields provide a method for users to weight each Port's Request for more credit, from the Half Station's internal credit allocation logic:

- **INCH Threshold Port x VC0 Posted** register *Congested Port Weight* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets A00h, A18h, A60h, A78h[22:20])
- **INCH Threshold Port x VC1 Posted** register *Congested Port Weight* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets A0Ch, A24h, A6Ch, A84h[22:20])

In the congested state, the Half Station's internal credit allocation logic decides which Port will receive the next available credit, by evaluating the following:

- Each VC and Port's *Congested Port Weight* field Setting
- Quantity of Common Pool credits that the Port has already consumed
- History of which Ports have recently received credit

Table 9-7, By default, the *Congested Port Weight* field for each VC and Port is Cleared. The default value is called an *effective rate Setting*. For the default case, if a Half Station is configured into five Ports (x4, x1, x1, x1, x1), each Port receives credit updates based upon on the Port's negotiated Link width. The x4 Port would receive 50% of the credit updates, and the four x1 Ports would each receive effectively 1/8th of the remaining credits as they become available.

Table 9-7 defines the *Congested Port Weight* field values. Requests are weighted, based upon the Port's effective Link width, relative to the effective Link widths of the other Half Station's Ports. Settings can reduce or increase a Port's effective rate, down to x1 or up to x8, respectively. (*That is*, regardless of the actual Link width, a Link can only be reduced to a x1 effective rate, or increased to a x8 effective rate.) The effective Link Width Request weight is calculated, by multiplying the Port's negotiated Link width (not strapped width) by the *Congested Port Weight* field Setting.

The Half Station's internal credit allocation logic decides how to allocate the Common Pool credits, as they become available in a congested scenario. Regardless of the Common Pool credit availability, each Port maintains ownership of the ingress credits that were initially allocated to it. In a congested state, those dedicated credits are replenished to their assigned Port, after an ACK is received from the final destination.

The effective rate Setting applies to both the Common Header and Common Payload/Completion pools, for the selected Half Station, Port, and VC. Although the effective rate Setting is in the **INCH Threshold Port x VC0 Posted** and **INCH Threshold Port x VC1 Posted** registers, the value applies to credit updates for all three possible traffic types (Posted, Non-Posted, and Completion).

Note: *The offsets for these registers are listed on the previous page.*

Table 9-7. INCH Threshold Port x VC0 Posted and INCH Threshold Port x VC1 Posted Register *Congested Port Weight* fields (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, field [22:20]) Values

***Congested Port Weight* Setting (Bits [22:20])**	**Description**
000b = eff_rate	Request is weighted, based upon the Port's Link width relative to the effective Link widths of the other Half Station's Ports.
001b = 2x eff_rate	Increases the weight of a Request by 2 (*for example*, a x4 Link Width Request weight increases to a x8 Link Width Request weight).
010b = 4x eff_rate	Increases the weight of a Request by 4 (*for example*, a x1 Link Width Request weight increases to a x4 Link Width Request weight).
011b = 8x eff_rate	Increases the weight of a Request by 8 (*that is*, a x1 Link Width Request weight increases to a x8 Link Width Request weight).
100b = 0	Port receives no credit from the common pool, until a decongested state is reached.
101b = eff_rate/2	Decreases the weight of a Request by 2 (*for example*, a x8 Link Width Request weight decreases to a x4 Link Width Request weight).
110b = eff_rate/4	Decreases the weight of a Request by 4 (*for example*, a x8 Link Width Request weight decreases to a x2 Link Width Request weight).
111b = eff_rate/8	Decreases the weight of a Request by 8 (*that is*, a x8 Link Width Request weight decreases to a x1 Link Width Request weight).

9.3.6 INCH Port Pool Registers (Offsets 940h and 944h)

The **INCH Port Pool** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) are registers whose original intent was to provide another level of reservation for Common Pool credits. The registers are named as follows, and are located at:

- **INCH Port Pool for Ports 0, 1**, offset 940h
- **INCH Port Pool for Ports 4, 5**, offset 944h

These registers are essentially redundant to what is accomplished by changing the values of the **INCH Threshold** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets A00h through A8Ch).

Consider the INCH Port Pool registers to be *reserved* and only change the credit Settings, using the INCH Threshold registers. Do not change the INCH Port Pool registers from their default values, unless directed otherwise by PLX Technical Support.

The **INCH Port Pool** registers initial values are provided in sets of two for each Port – Payload pool and Header pool. Table 9-8 lists the bit decode for each Port.

The initial values of the **INCH Port Pool** registers are all Cleared which means that, by default, there is no additional level of reservation. Additionally, the **INCH Threshold** registers default values evenly allocate all available credit, across all enabled Ports.

Table 9-8. INCH Port Pool Settings (Offsets 940h and 944h)

Ports	Payload Pool Bit(s)[a]	Header Pool Bit(s)[a]
0, 4	2:0	6:4
1, 5	10:8	14:12

a. The hyperlinks provided to the bits listed are to register offset 940h.

9.3.7 Wait for ACK – Avoiding Congestion

Once a TLP arrives, it remains on the PEX 8604 until it is no longer required. The TLP can quickly egress the PEX 8604. However, until an ACK is received, indicating that the TLP was correctly received, each TLP must remain on the PEX 8604 and be ready to be re-sent multiple times. While on the PEX 8604, the TLP continues to use Half-Station common pool resources.

The *PCI Express Base r2.0* recommends sending an ACK within the approximate time it takes to send 1.5 to 3 MPS TLPs. It does not, however, suggest that smaller TLPs obtain faster ACKs. This data book describes the way in which the PEX 8604 sends an ACK. However, the PEX 8604, has no way of knowing its Link partner's ACK policy.

To minimize the amount of TLPs stored on the PEX 8604 while waiting for an ACK, follow these guidelines:

- Avoid traffic patterns where a great deal of back-to-back TLP bytes travel from a wide Link to a single narrow Link, because the narrow Link can only forward TLPs at a fraction of the ingress rate. *For example*, if a 4-KB MRd is transmitted upstream from a x1 Port and the upstream Port is x2, the upstream Port transmits a 4-KB CPLD to the Requester, two times faster than the Requester can receive the data. If the Requester transmits many of these MRd Requests, large amounts of CPLD data that require storage on the PEX 8604 will quickly accumulate.
- If there are many small TLPs, determine whether the PEX 8604's ACK response time can be reduced, as per the *PCI Express Base r2.0* guidelines.
- Evenly space the TLP pattern, rather than use a burst of many back-to-back TLPs followed by a long stall, to even the distribution and accommodate a fixed ACK Transmission Latency Timer.

9.4 Latency

Latency is the length of time it takes to proceed from one event to another. Latency can be measured in several different ways, but perhaps the most common measurement for a switch is *Start TLP-to-Start TLP (STP-to-STP) latency*. Figure 9-3 and Table 9-9 illustrate an STP-to-STP Latency Measurement. When the Egress Start TLP symbol is transmitted out of a switch before the Ingress Port End symbol arrives, the transfer is termed *Cut-Thru*. If an Egress Port queue is not already established, the PEX 8604 always cuts the packet through. The PEX 8604 has the same latency, regardless of whether the traffic is upstream or peer-to-peer.

As expected with the PEX 8604 Cut-Thru architecture, STP-to-STP latency is basically constant for all Payload sizes. A faster Link can receive the Header for decode faster, with a slightly lower latency. There will generally be a constant latency for any ingress width to the same egress width, or any ingress width to a smaller egress width, operating at the same Link speed. This is indicated by the shaded-green entries in Table 9-9.

For cases in which the egress Port has a higher bandwidth than the ingress Port, then a fraction of the packet, given by the following formula:

$$F = (E-I) / E$$

must be buffered (to prevent under-run in the middle of the TLP), before the TLP can be forwarded to the egress Link.

where

- *F* is the fraction sum
- *E* is egress bandwidth
- *I* is ingress bandwidth

Figure 9-3. Start TLP-to-Start TLP Latency Measurement

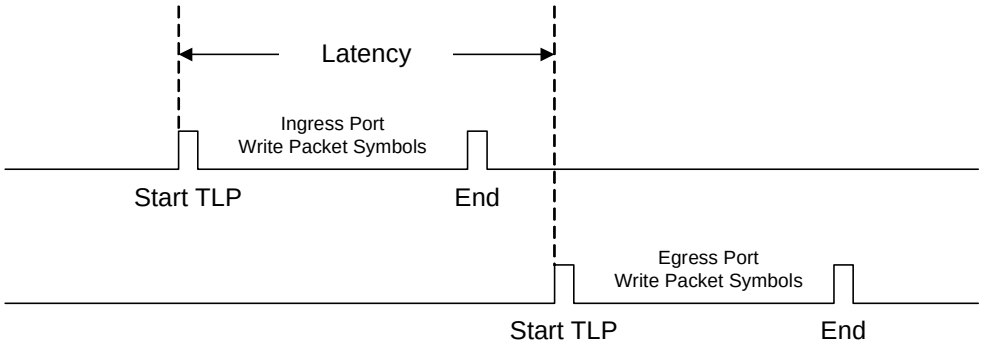


Table 9-9. Sample STP-to-STP Latency

Latency for TLP with a Data Payload of 4/64/256 Bytes (in ns)		
	From Ingress	
	x2 Gen 2	x1 Gen 2
To Egress	164/214/314	184/310/614
x2 Gen 2	174/180/180	200/296/488
x1 Gen 2	188/188/188	180/180/188

9.4.1 Host-Centric Latency

Host-centric traffic flows only to or from the Host. Host-centric latency depends upon the quantity of active streams. If there is only one active stream, or if the total Host bandwidth is greater than or equal to the sum of all traffic streams, the traffic is well-balanced and the latency measurements provided in Table 9-9 apply.

If there is more traffic than an upstream Host can sink, congestion occurs when all the TLPs concurrently attempt to use the limited Host bandwidth. The latencies in that case depend upon the level of traffic congestion. In this case, Host bandwidth is at 100%, but the total downstream bandwidth is more than the Host bandwidth, and latencies continue to increase until the congestion eases.

Another case of increased latency is if the Host serially sends large amounts of Read Completion data to one downstream Port and then another downstream Port. *For example*, if the upstream Port is x2 and the two downstream Ports are both x1, it appears that there should not be a latency build-up, because the bandwidth matches. However, if the Host cannot interleave the destinations, one destination must wait until the Host completes transmitting traffic to the other destination, before it can receive any Read Completion data. In this case, the round-trip Read latency can significantly increase.

For example, suppose that one downstream Port transmits 16, 4-KB MRd Requests upstream. Those Read Requests represent 64 KB of data. If the upstream Port is x2 and the downstream Port is x1, the Read Completions back up into the PEX 8604, perhaps all the way to the Root Complex. Suppose another downstream Port transmits only one, 1-KB MRd Request upstream, shortly after the 16, 4-KB MRds were received by the Root Complex. For many Root Complexes, this one, 1-KB Read Request from the second device must wait for the 16, 4-KB MRd Requests from the first device to complete before being serviced. The PEX 8604 buffer is approximately 10 KB; therefore, the second downstream device must wait for (64-10) 54 KB of Completion data to transmit across a x1 Link before it begins to receive its Read Completions. On a x1 Link, 54 KB takes about 48 µs, which significantly increases the second device's latency. The PEX 8604 contains Read Pacing logic that prevents this type of latency increase that occurs when multiple devices concurrently read data from the Root Complex. (Refer to Section 9.6.)

9.4.2 Peer-to-Peer Latency

If an Egress Port queue is not established (*such as* multiple streams to the same destination Port), peer-to-peer latencies match the best-case values listed in Table 9-9. The PEX 8604 has the same latency, regardless of whether the traffic is Host-centric or peer-to-peer. Latency is constant in the non-congested case, no matter the source Port nor destination Port, if the Source Port has the same or greater bandwidth than the destination Port.

The discussion for Host-centric traffic applies to all Ports for peer-to-peer traffic. It is recommended that there be a method outside the scope of this data book, however, for balancing traffic flow for peer-to-peer applications.

9.4.3 Other Latency Measurements

In addition to STP-to-STP latency, there are other latencies to consider. Table 9-10 lists various best-case latencies for several Link widths and speeds. Transmitted DLLPs can be required to wait for a TLP. DLLP policies can prevent sending a DLLP for a time period longer than the best case.

Table 9-10. Miscellaneous Best Case Link Latencies (in ns)

Latency[a]	x2 Gen 2	x1 Gen 2
STP in to UpdateFC SDP[b]	144	180
TLP's END in to ACK SDP	72	72
UpdateFC SDP in to STP	120	140

a. Gen 1 latency values are expected to be the same as, or very close to, Gen 2 latency values.

b. SDP is "Start DLLP".

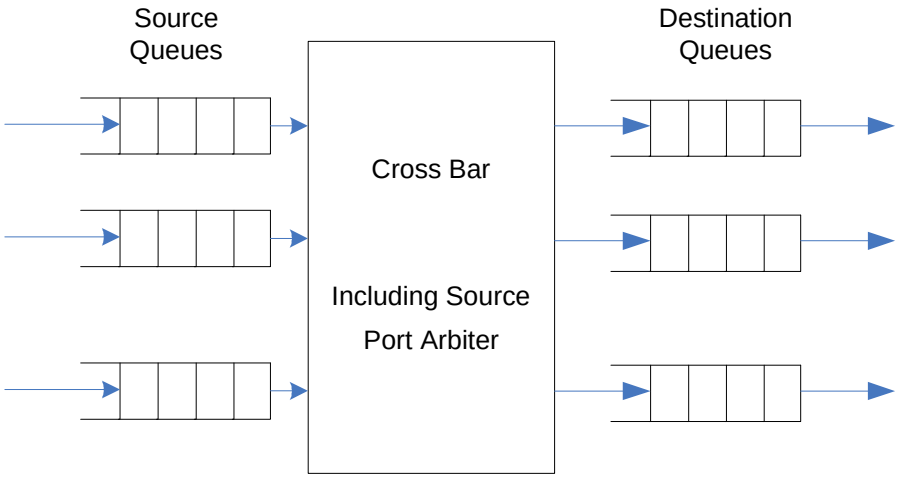
9.5 Queuing Options

On-chip queuing does not exist in balanced bandwidth scenarios, where the total ingress bandwidth is less than or equal to the egress bandwidth. In the common case, where the total ingress bandwidth is greater than the egress bandwidth, queues develop on the PEX 8604. The PEX 8604 provides two alternatives, as to where to locate such queuing (refer to Figure 9-4):

- **Destination queue** – Associated with a single Destination Port. All the TLPs in a Destination queue will egress out the same Port.
- **Source queue** – Associated with a single ingress Port. All the TLPs in a Source queue come from the same Port.

Each queue is discussed in the sections that follow.

Figure 9-4. On-Chip Queuing



9.5.1 Destination Queuing

Note: *For the queuing examples provided in this section, "Port 1" indicates "first Port," not the Port physically identified as Port 1.*

The default behavior is for all queues to develop at the Destination Port. If TLPs are arriving from four sources to a common Destination Port, the TLPs are scheduled according to First-In, First-Out (FIFO). The crossbar can forward a TLP every 4 ns, to each Destination queue; therefore, it is unlikely that a Source queue can develop or last very long.

A Destination queue develops whenever the *ingress rate* – the sum of all ingress Ports targeting a Destination Port – exceeds the egress rate. A Destination queue might also develop in a credit-starved situation, where there is no credit available to forward TLPs.

For example, if TLPs arriving from four sources all go to a common Destination Port, the TLPs are scheduled, based upon the order in which they arrive at the Destination queue FIFO[a]. If all four flows are equally active, the TLPs naturally interleave as 1,2,3,4,1,2,3,4. If three of the Ports, however, have a head start before the fourth Port turns On, the output can be 1,2,3,1,2,3,1,2,3,1,2,3,1,2,3,4,1,2,3,4. In this case, all the new Port (Port 4) TLPs must wait for the earlier Port 1,2,3 traffic to be transferred before the Port 4 TLPs can be transferred. Therefore, the latency for Port 4 traffic to travel through the PEX 8604 can widely vary, based upon the traffic passing through the switch.

a. Conventional PCI Strong Ordering rules can override the FIFO. Conventional PCI requires Posted TLPs to be able to pass Non-Posted and Completion TLPs, to avoid deadlock.

9.5.2 Source Queuing

Caution: ***Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.***

Note: *For the queuing examples provided in this section, "Port 1" indicates "first Port," not the Port physically identified as Port 1.*

Source queuing can be enabled for applications that require deterministic bounded latency for a few Ports, while the latency for other Ports is not as important.

Source queuing limits the Destination queue depth. When the Destination queue reaches the maximum depth, any subsequent TLPs targeting that Port are not forwarded, but are queued up in a per-Source Port-based queue. The Source Port queue does not forward TLPs until the Destination queue drops to a programmed threshold, upon which TLP forwarding is re-enabled.

Note: *A Source Port queue that cannot forward to a Destination queue blocks all subsequent TLPs arriving on that same Source Port, although the target Port is a different destination.*

The **Port Egress TLP Threshold** register (offset F10h) controls the minimum and maximum queue depths. Table 9-11 summarizes the register bit Settings. The Port Lower TLP Counter is the quantity of TLPs that the Destination queue must reach after becoming saturated, before re-enabling TLP forwarding. The Port Upper TLP Counter is the quantity of TLPs that can be queued in the Destination queue.

In the Destination queue example provided in Section 9.5.1, the early arriving Port 1,2,3 TLPs stalled Port 4's TLP for an indeterminate length of time. By programming, with source queuing enabled and a Destination Port Lower TLP Counter programmed to 1 and Port Upper TLP Counter programmed to 3 (TLPs), the worst case is that Port 4 must wait for three TLPs (1,2,3) before getting its first turn. With these Settings, the example TLP output would be 1,2,3,4,1,2,3,4,1,2,3,4. The *turn to be forwarded* refers to a Port Arbitration wait, described in Section 9.5.3.

To avoid unnecessary idles on the destination Link, program a Port Lower TLP Counter of 1, and a Port Upper TLP Counter of 2.

Table 9-11. Port Egress TLP Threshold Register Port Lower and Upper TLP Counters (Offset F10h)

Bit(s)[a]	Name	Description
10:0	**Port Lower TLP Counter**	When Source Scheduling is disabled due to the Port Upper TLP Counter (threshold) being exceeded, Source Scheduling is re-enabled when the Port TLP Counter goes below the Port Lower TLP Counter (this threshold). Because the default Setting of this field is 7FFh (2,047), which is greater than the maximum amount of TLPs that can be queued in the PEX 8604, the Source Scheduler is disabled, by default.
26:16	**Port Upper TLP Counter**	When the Port TLP Counter is greater than or equal to this value, the Source Scheduler disables TLP Scheduling to this egress Port. Because the default Setting of this field is 7FFh (2,047), which is greater than the maximum amount of TLPs that can be queued in the PEX 8604, the Source Scheduler is disabled, by default.

*a. Bits not identified in Table 9-11 are **reserved**.*

9.5.3 Port Arbitration

In the crossbar that connects the Source queues to the Destination queues, there is a Port Arbiter for each Destination Port. The Port Arbiter ensures that each Source Port receives a deterministic bandwidth connecting to a Destination Port. The Port Arbiter ensures that each Source Port receives a deterministic bandwidth connecting to a Destination Port. Every Port has two default fixed Round-Robin Port Arbiters, one for each VC.

In addition to the default fixed Round-Robin Port Arbiter, there is one Device-Specific Weighted Round-Robin (WRR) Port arbitration hardware resource that can enabled by system software. The Device-Specific WRR arbitration is also Round-Robin, but with programmable weighting for a particular Port or Ports. When WRR is enabled, the Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3; if the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0.

System software discovers the Port Arbitration Capability, as reflected in the **VC0 Resource Capability** register (offset 158h[1:0]). If the system software needs to make use of an advertised WRR arbitration with 32-phase capability for a Port, it programs the Port's **VC0 Resource Control** register *Port Arbitration Select* field (offset 15Ch[19:17]) to 001b.

The WRR Source Port Arbiter has a 32-phase Port Arbitration Table, as outlined in the *PCI Express Base r2.0*, and documented in the **Port Arbitration Table Phase *x*** registers (When WRR is enabled, Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3; if the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0, offsets 1A8h through 1B4h). (Refer to the *PCI Express Base r2.0*, as well as Section 13.13.1, "WRR Port Arbitration Table Registers (Offsets 1A8h – 1BCh)," for further details.)

Once one or more Phase registers are written, the software writes the Port's **VC0 Resource Control** register *Load Port Arbitration Table* bit (offset 15Ch[16]). When written, the register values are transferred to the WRR arbitration logic, and immediately take effect.

Port arbitration makes decisions on a per-TLP basis. A Port with more short TLPs will appear to receive less bandwidth, compared to a Port with fewer long TLPs, if both Ports have the same weight and both target a congested Port.

9.5.4 Port Bandwidth Allocation

For applications that need to allocate a fixed bandwidth to each Port, the PEX 8604 can help enforce the relative bandwidth ratio between Ports in a congested scenario.

By combining source queuing, Port Arbitration, and initial credit, as well as some knowledge of average Payload size, many combinations of Port bandwidth allocation are possible.

9.6 Read Pacing

Caution: ***Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.***

The Read Pacing feature is supported on all Ports. The Read Pacing Configuration registers, however, are implemented only on the upstream Port.

PCI Express has a weakness concerning the quantity of outstanding bytes requested by Reads. It is possible that a single device can overwhelm the system with a reasonable quantity of large Read Requests, thereby impacting the performance of other connected devices, by filling the ingress transaction queue in the Root Complex.

The Root Complex must handle the transactions in the order in which they are posted. Transactions posted from less aggressive reading devices, which may be more sensitive to latency, suffer performance reductions due to the unfairly weighted path (head of line blocking) in the transaction queue that the large reads represent.

Read Pacing attempts to apply some rules to Memory Read Requests, so that no one Port can overwhelm a system. There are two aspects to the PEX 8604's Read Pacing capability:

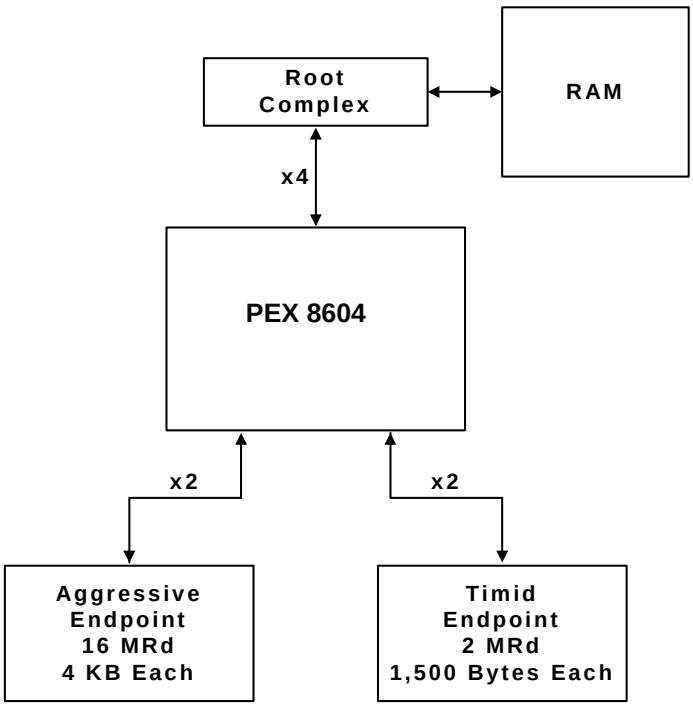
- Read spacing
- Read threshold

The following sections provide examples and further information regarding Read Pacing.

9.6.1 Read Pacing Example

Figure 9-5 illustrates an example of a system that benefits from Read Pacing.

Figure 9-5. Read Pacing Example



In a typical Host-centric application, endpoints have Direct Memory Access (DMA) engines that write to and read from Main memory. A performance bottleneck can occur during the Read to Main memory, through the Root Complex. For the example illustrated in Figure 9-5, the aggressive endpoint sends many large (16, 4-KB) Memory Read Requests, while another endpoint, or Timid Endpoint (TEP), sends only two 1,500-byte Memory Read Requests. The TEP then waits for a response before sending additional Read Requests[a].

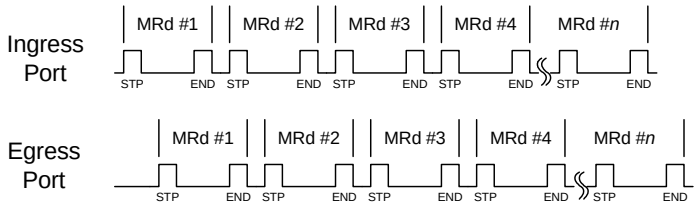
If either endpoint is running by itself, neither sees a problem. However, if both endpoints are concurrently active, the aggressive endpoint dominates the Root Complex Memory Controller. In addition, due to the bandwidth mismatch, Completions can queue up in the PEX 8604, creating too many Completions for the switch to store at one time. As a result, the PEX 8604 backpressures the Root Complex for Completions. The Root Complex can only forward Completions to the PEX 8604 at the aggressive endpoint's rate, which is significantly less than the Root Complex could otherwise handle.

The net impact is not to the aggressive endpoint, because there are a sufficient quantity of Completions queued up in the PEX 8604 to keep it busy. In fact, the aggressive endpoint experiences better performance with a switch, than connected directly to the Root Complex[b]. Rather, the TEP experiences lower performance results. Its Memory Read Requests wait in line behind multiple aggressive endpoint Requests, and the Root Complex can drain Requests only at the same rate of the PEX 8604, not at the upstream Link's capacity.

Figure 9-6 illustrates how a PCI Express switch, without Read Pacing, forwards Memory Read Requests (MRds).

Read Pacing solves the performance loss seen by the TEP, while improving the aggressive endpoint's performance. The following sections provide examples of the way in which the PEX 8604 functions when Read Pacing is enabled, and Read Spreading is enabled or disabled.

Figure 9-6. Read Pacing Off (Disabled)



a. This is based upon an actual setup in a third-party lab. Fibre Channel endpoints can easily send 16, 4-KB MRd at a time, while Gigabit Ethernet endpoints might send only one or two 1,500-byte endpoints at a time.

b. Without a switch, when the Root Complex has something else to do, the aggressive endpoint loses its data stream. With a switch, the buffering of multiple Completions hides the fact that the Root Complex is multitasking.

9.6.2 Read Spacing (Spreading) Logic

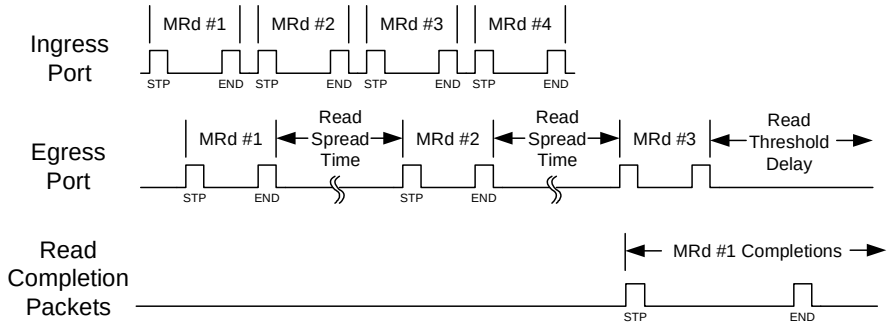
Read Spacing (also referred to as *Read Spreading*) spreads out Read Requests. The PEX 8604 Read Spacing logic looks at the Read Request size and the endpoint's bandwidth, to determine how often to forward subsequent Read Requests. *For example*, Read Requests arriving on a x1 Link can only sink data at a x1 rate. If a x1 endpoint submits multiple Read Requests to a x2 Link, the Read Spacing logic does not forward the subsequent Read Requests until the endpoint has sufficient time to sink a portion of the Completion data from the previous Read Requests.

Initially, a queue of Completions must build up to hide the time that it takes for the data to return. As a result, Reads are forwarded at 2x the endpoint's bandwidth. This 2x rate is maintained until a threshold of outstanding Read data is reached, at which time Reads are forwarded at 1x the endpoint's bandwidth.

Read Pacing must be enabled for Read Spreading to be enabled. *That is*, for a Port to have Read Spreading enabled, the Port's **Read Pacing Control** register *Port x Read Pacing Disable* and **Read Spreading Control** register *Port x Memory Read Spreading Disable* bits (offsets 544h[5, 4, 1, 0] and 548h[5, 4, 1, 0], respectively) must both be Cleared.

Figure 9-7 illustrates the way in which the PEX 8604 forwards Read Requests when the Read Pacing and Read Spreading-related bits are enabled. (Refer to Section 9.6.5 for additional register/bit information.) The PEX 8604 continues to spread and forward the Read Requests, until the amount of Completion data for which it is waiting exceeds the value programmed in the **Read Pacing Threshold *x*** register(s) for that Link width (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port, offsets 54Ch and 550h, respectively).

Figure 9-7. Read Pacing On (Enabled) and Read Spreading On (Enabled)

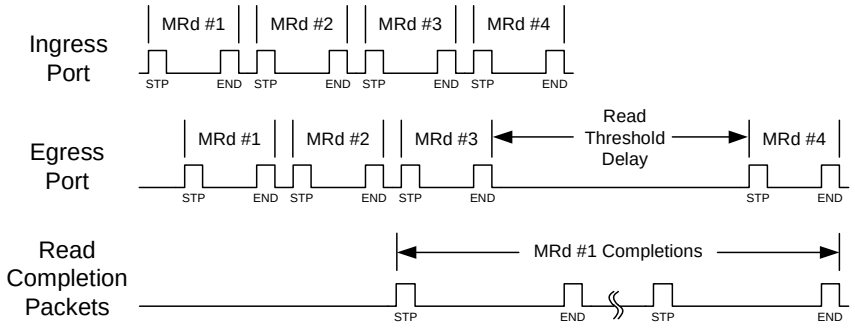


9.6.3 Read Threshold

The Read threshold is the maximum quantity of outstanding DWords (1 DWord = 4 bytes) that the endpoint Port requested to be read, but were not yet returned as Completion data. The threshold is related to the PEX 8604's buffering capacity – all outstanding Read data ought to be able to be buffered in the switch, to remain out of the way of other Completions for other endpoint's Read Requests.

After a Port reaches its Read threshold, subsequent Read Requests from that Port queue up in the PEX 8604, waiting for Completion data to reduce the outstanding count to below the threshold. If an overabundant quantity of Read Requests queue in the PEX 8604, no additional Read credit is allocated, which backpressures the Read Requester. Figure 9-8 illustrates the way in which the PEX 8604 forwards Read Requests when its Read Spacing logic is enabled and Read Spreading logic is disabled.

Figure 9-8. Read Pacing On (Enabled) and Read Spreading Off (Disabled)



9.6.4 Read Pacing Benefits

When Read Pacing logic is enabled, the PEX 8604 provides the follow benefits:

- Maximum Read latency that an endpoint may experience can be dramatically reduced.

  By reducing the amount of queued Read Requests, and therefore pending Read Completion data at the Root Complex, new Read Requests from Ports that do not have pending Read Requests can be serviced with a predictable and/or reasonable amount of latency.

- Timid endpoint bandwidth is dramatically increased in busy applications.

  Because queues of pending Read Requests in the Root Complex are limited, and congestion caused by a large amount of Completion data intended for a high-bandwidth, needy Port (or Ports) is avoided, the bandwidth needs of endpoints with smaller bandwidth requirements are met (*that is*, the endpoints are not starved).

- PEX 8604's Read Pacing Threshold logic allows all busy Ports to be equally serviced in congested scenarios, regardless of their individual Read requesting behavior.

  For example, all Ports might simultaneously request data, some aggressively and some timidly. While unable to quickly drain their queued Completions, the Ports' Read Pacing Threshold logic forwards the additional Read Requests to the Root Complex, equally and fairly, while ensuring Completion data is available for each Port, when the Port is ready to accept it.

9.6.5 Enabling Read Pacing and Read Spreading

Caution: ***Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.***

Read Pacing is disabled, by default. To enable Read Pacing, the Port's **Read Pacing Control** register *Port x Read Pacing Disable* bit (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port, offset 544h[5, 4, 1, 0]) must be Cleared. A bit value of 0 enables Read Pacing, whereas a value of 1 (default) disables Read Pacing.

The Port's **Read Spreading Control** register *Port x Memory Read Spreading Disable* bit (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port, offset 548h[5, 4, 1, 0]) is used to enable or disable Read Spreading. A value of 1 disables Read Spreading for the corresponding Port. Read Spreading is enabled, by default (value of 0); however, it is overridden by the Port's *Port x Read Pacing Disable* bit, by default.

Both sets of Read Spreading and Pacing Control register bits are represented in Table 9-12. (For complete details, refer to the register offset 54Ch and 550h description provided in Section 13.16.2, "Device-Specific Registers – Read Pacing (Offsets 544h – 554h).") Figure 9-6 through Figure 9-8 illustrate what occurs when the bits are enabled or disabled.

The Read Pacing thresholds are Set, based upon the Source Port's programmed Link width. The **Read Pacing Threshold 0** register controls the threshold values for x2 Link widths, and the **Read Pacing Threshold 1** register controls the threshold values for x1 Link widths (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port, offsets 54Ch and 550h, respectively). The thresholds are in DWords. Narrower Link widths have lower thresholds, because they must buffer smaller quantities.

Table 9-12. Read Pacing and Memory Read Spreading Control Register Disable Bits

Register Offset	Bit(s)[a]	Description	Default
544h	5, 4, 1, 0	**Port *x* Read Pacing Disable** Bits [5, 4, 1, 0] correspond to the Read Pacing Disable for Ports 5, 4, 1, and 0, respectively. 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	Fh
548h	5, 4, 1, 0	**Port *x* Memory Read Spreading Disable** Bits [5, 4, 1, 0] correspond to the Memory Read Spreading Disable for Ports 5, 4, 1, and 0, respectively. 0 = Memory Read Spreading is enabled for this Port 1 = Memory Read Spreading is disabled for this Port	0h

*a. Bits not identified in Table 9-12 are **Reserved** or **Factory Test Only**.*

9.7 Dual Cast

9.7.1 Introduction

This section describes the functions and programming of the PEX 8604's Dual Cast feature. A typical system configuration and register programming example is also provided.

Dual Cast allows programs to concurrently write the same data to two different destinations. Whenever Posted Memory Write TLPs entering the PEX 8604 through a designated Port (referred to as the *Dual Cast Source Port*) are addressed to designated memory regions (referred to as *Dual Cast BARs*), the switch automatically generates a copy of the original TLP (referred to as the *Dual Cast Copy TLP*), replacing the original TLP's address with one that is mapped to an egress Port designated as the *Dual Cast Destination Port*.

When an incoming TLP is copied in this manner, both the original TLP and Dual Cast copy TLP are concurrently queued at their respective egress Ports, effectively doubling the PEX 8604's egress rate for the same ingress rate.

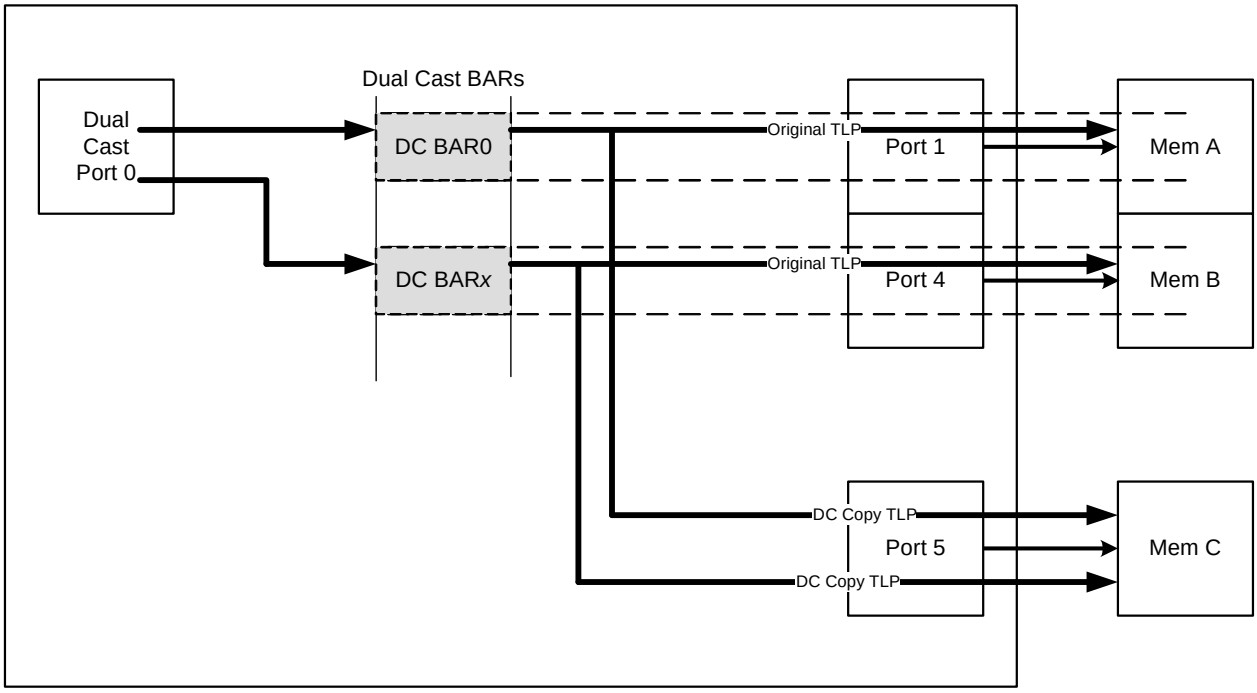
9.7.2 Dual Cast System Model

Figure 9-9 illustrates Dual Cast functions. In this figure, the designated Dual Cast Source Port is Port 0. Only Memory Write TLPs that enter the PEX 8604 through this Port (or alternately, any Port) are subject to Dual Casting. Dual Cast Control registers allow the programmer to define up to eight separate Dual Cast BARs, over which Dual Casting will be applied. If a Memory Write TLP enters the PEX 8604 through the designated Dual Cast Source Port, **and** its Header address falls within an active Dual Cast BAR, then the switch automatically generates a Dual Cast Copy TLP, replacing the original TLP's Header address with a new address mapped to the designated Dual Cast Destination Port.

Dual Cast BARs can be mapped to any egress Port of the PEX 8604. In other words, original Memory Write TLPs that are being copied can exit the PEX 8604 on any egress Port, as they would normally. However, Dual Cast Copy TLPs, regardless of which Dual Cast BAR generates them, must all exit the PEX 8604 through the designated Dual Cast Destination Port.

The Dual Cast Destination Port can also be configured as NT. Refer to Section 9.7.5 for additional programming requirements.

Figure 9-9. Typical Dual-Cast System Model



9.7.3 Dual Cast Control Registers

This section describes each of the Dual Cast Control registers. Eight sets of identical registers describe each of the eight Dual Cast BARs. An additional register specifies the Dual Cast Source and Destination Ports. These registers are described, in detail, in the following subsections. For a complete listing of the registers, refer to Section 13.14.10, "Device-Specific Registers – Vendor-Specific Dual Cast Extended Capability (Offsets 448h – 51Ch)." The Dual Cast registers are located in Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port.

9.7.3.1 Dual Cast Low BAR[0-7], Dual Cast High BAR[0-7]

The 32-bit **Dual Cast Low** and **High BAR*x*** registers in Port 0 (refer to Table 9-13) are used to define the 64-bit physical Base address of each of the Dual Cast BAR address windows, numbered 0 through 7.

Dual Cast Low BAR*x* contains the lower 32-bits of the Base address of Dual Cast BAR window *n*. Only the upper 12 bits [31:20] of this register are used to specify address. Bits [19:0] of this register are not de-coded, and are hardwired with the value 0_000Ch. Thus, Dual Cast BARs are naturally aligned on 1-MB boundaries. Because the 1-MB boundary is also a 4-KB boundary, any Memory Write TLP that falls within the Dual Cast BAR's Address range will be guaranteed never to exceed the top of the Dual Cast BAR*x* range.

Dual Cast High BAR*x* contains the upper 32 bits of the Base address for Dual Cast BAR window *n*. For Base addresses in the lower 4 GB or for all 32-bit systems, this register should be Cleared (default).

Table 9-13. Dual Cast High/Low BAR*x* Register Locations

Base Address Register	Port 0 Register Offset	
	Dual Cast Low[31:0] (Lower 32 Bits)	Dual Cast High[31:0] (Upper 32 Bits)
BAR0	450h	454h
BAR1	468h	46Ch
BAR2	480h	484h
BAR3	498h	49Ch
BAR4	4B0h	4B4h
BAR5	4C8h	4CCh
BAR6	4E0h	4E4h
BAR7	4F8h	4FCh

9.7.3.2 Dual Cast Low BAR[0-7] Translation, Dual Cast High BAR[0-7] Translation

The 32-bit **Dual Cast Low** and **High BAR*x* Translation** registers in Port 0 (refer to Table 9-14) specify the destination address of the Dual Cast Copy TLP for their corresponding Dual Cast BARs. When a Dual Cast Copy TLP is formed, the original TLP's Header Address bits are replaced with corresponding Address bits from these registers.

Restrictions

- Dual Cast BAR Translation addresses must be mapped to the Dual Cast Destination Port, as specified in the **Dual Cast Source Destination Port** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 510h). (Refer to Section 9.7.3.4.) While the original TLPs that are copied can be mapped to any PEX 8604 Port, copied TLPs from all Dual Cast BARs must be mapped to the Dual Cast Destination Port.
- Dual Cast BAR Translation address plus the Dual Cast BAR window size must never exceed the Address range mapped to the Dual Cast Destination Port.

Table 9-14. Dual Cast High/Low BAR*x* Translation Register Locations

Base Address Register	Port 0 Register Offset	
	Dual Cast Low Translation[31:0] (Lower 32 Bits)	Dual Cast High Translation[31:0] (Upper 32 Bits)
BAR0	458h	45Ch
BAR1	470h	474h
BAR2	488h	48Ch
BAR3	4A0h	4A4h
BAR4	4B8h	4BCh
BAR5	4D0h	4D4h
BAR6	4E8h	4ECh
BAR7	500h	504h

9.7.3.3 Dual Cast Low BAR[0-7] Setup, Dual Cast High BAR[0-7] Setup

The 32-bit **Dual Cast Low** and **High BAR*x* Setup** registers in Port 0 (refer to Table 9-15) form a 64-bit value used to define the Dual Cast BAR window size, which increases in powers of 2 in size, starting from 1 MB.

The Dual Cast BAR window size increases in powers of 2, starting from 1 MB. The address window size is determined by the quantity of Set bits, starting from bit 63 down to bit 20. For each bit that is a value of 1, the Copy TLP's Header Address bit is replaced by the corresponding Address bit in the **Dual Cast Low/High BAR*x* Translation** registers, as illustrated in Figure 9-10.

If bits [63:20] are all Set, the source window size is 1 MB. If bits [63:21] are all Set, and bit 20 is Cleared, the window size is 2 MB. When **Dual Cast High BAR*x* Setup**[31] is Cleared, the corresponding Dual Cast BAR is disabled. Table 9-16 lists example **Dual Cast Low/High BAR*x* Setup** register values and the corresponding Dual Cast BAR Address window sizes.

Table 9-15. Dual Cast High/Low BAR*x* Setup Register Locations

Base Address Register	Port 0 Register Offset	
	Dual Cast Low Setup[31:0] (Lower 32 Bits)	Dual Cast High Setup[31:0] (Upper 32 Bits)
BAR0	460h	464h
BAR1	478h	47Ch
BAR2	490h	494h
BAR3	4A8h	4ACh
BAR4	4C0h	4C4h
BAR5	4D8h	4DCh
BAR6	4F0h	4F4h
BAR7	508h	50Ch

Figure 9-10. Dual Cast High/Low BAR*x* Setup Register Example

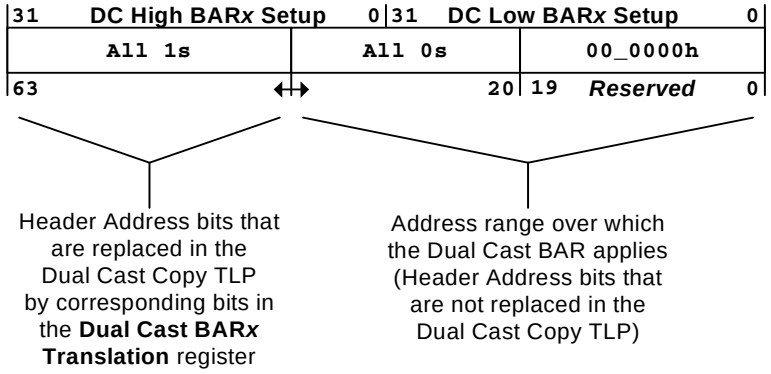


Table 9-16. Dual Cast BAR*x* Setup Register Address Window Sizing Examples

Dual Cast High BAR*x* Setup[31:0]	Dual Cast Low BAR*x* Setup[31:20]	Dual Cast BAR*x* Window Size
0000_0000h	XXXh	Disabled (default)
FFFF_FFFFh	FFFh	1 MB
FFFF_FFFFh	FFEh	2 MB
FFFF_FFFFh	000h	4 GB
FFFF_FFFEh	000h	8 GB

Restrictions

- Dual Cast BAR Address windows must not overlap one another.
- Dual Cast Source Address windows 0 through 7 can be mapped to any Port (including the upstream Port and NT Port); however, only Write TLPs that enter the PEX 8604 through the designated Dual Cast Source Port are subject to Dual Casting. (Refer to Section 9.7.3.4.)
- Both the original forwarded TLP **and** Dual Cast Copy TLP must be acknowledged on their respective egress Ports, before the original incoming TLP can be retired.
- Dual Cast BAR regions can be coded only as 64-bit BARs. For regions under 4 GB, Dual Cast High **BAR*x*** = 0000_0000h.

9.7.3.4 Dual Cast Source Destination Port

The **Dual Cast Source Destination Port** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port; ***Reserved*** (RsvdP) for Dual Cast BAR Limit Lower register, offset 510h) is used to specify the Dual Cast Source and Destination Ports. Table 9-17 lists the bit definitions for this register. Bits not listed are ***reserved*** (zero).

Table 9-17. Dual Cast Source Destination Port Register Definition (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port; *Reserved* (RsvdP) for Dual Cast BAR Limit Lower register, offset 510h)

Bit(s)	Function
3:0	**Dual Cast Source Port #** Valid only when bit 8 (*Dual Cast Source Port Enable*) is Set. Specifies the source (ingress) Port Number upon which Dual Cast BARs are applied. Encodings not listed are reserved. Refer to register offset 510h[3:0] for the associated Port Number values.
7:4	**Dual Cast Destination Port #** Specifies the destination (egress) Port Number to which Dual Cast BAR Translation addresses are mapped, and to which Dual Cast Copy TLPs will be queued. Encodings not listed are reserved. Refer to register offset 510h[7:4] for the associated Port Number values.
8	**Dual Cast Source Port Enable** 0 = Dual Cast applies to Write TLPs entering any Port on the Dual Cast Source Port. In that case, the field [3:0] (*Dual Cast Source Port #*) value is “Don’t Care.” 1 = Dual Cast applies only to Write TLPs entering the PEX 8604, by way of the Dual Cast Source Port Number specified in field [3:0].

9.7.4 Dual Cast Programming Example

In this example, we consider a PEX 8604 configured as x2, x1, x1, with Port 0 being the upstream Port (connected to Root Complex), and Ports 1 and 5 configured as Transparent downstream Ports. Port 1 maps to a block of physical memory at Base address AAA0_0000h (32-bit addressing). Port 5 maps to a block of memory at Base address BBB0_0000h.

For this example, the switch must be programmed such that Write TLPs entering Port 0 and addressed to Port 1 (in the range AAA0_0000h to AAAF_FFFFh) are Dual Cast (copied) to the memory that is mapped to Port 5, starting at address BBB0_0000h.

9.7.4.1 Register Programming Steps

1. Program the **Dual Cast BAR0** registers with the Base address of the memory on Port 1.
   Dual Cast Low BAR0[31:0]=AAA0_000Ch ***(Note:** [19:0] are hardwired to 0_0000h.)*
   Dual Cast High BAR0[31:0]=0000_0000h
2. Program the **Dual Cast BAR0 Setup** registers to specify the Dual Cast BAR window size (1 MB).
   Dual Cast Low BAR0 Setup[31:0]=FFF0_0000h ***(Note:** [19:0] are hardwired to 0_0000h.)*
   Dual Cast High BAR0 Setup[31:0]=FFFF_FFFFh
3. Program the **Dual Cast BAR0 Translation** registers with the address of the memory on Port 5.
   Dual Cast Low BAR0 Translation[31:0]=BBB0_0000h ***(Note:** [19:0] are hardwired to 0_0000h.)*
   Dual Cast High BAR0 Translation[31:0]=0000_0000h
4. Program the **Dual Cast Source Destination Port** register bits, as follows:
   Dual Cast Source Destination Port[3:0]=0h (Dual Cast Source Port 0)
   Dual Cast Source Destination Port[7:4]=5h (Dual Cast Destination Port 5)
   Dual Cast Source Destination Port[8]=1 (Dual Cast on Port 0 only)

At this point, all Write TLPs entering the PEX 8604 by way of Port 0, having addresses in the range AAA0_0000h to AAAF_FFFFh, will be copied to memory at Base address BBB0_0000h. To verify that Dual Cast is enabled, try Clearing memory at address BBB0_0000h, then write a non-zero pattern to memory at address AAA0_0000h. A read of memory at BBB0_0000h should now show what was written at address AAA0_0000h.

9.7.5 Dual Cast to a Non-Transparent Destination Port

When the Dual Cast Destination Port is configured as Non-Transparent (NT), the Dual Cast Copy TLPs do not use the same Address Translation mechanism as original unicast TLPs that are routed to that Port. Where a unicast TLP uses the Address Translation mechanism in the NT Port (NT BAR), Dual Cast Copy TLPs are sent directly to the NT Port's Egress queue. Therefore, in applications where the Dual Cast Destination Port is the NT Port, the **Dual Cast Low/High BAR*x* Translation** registers must be loaded with the physical Base address of the destination memory in the NT address domain.

9.7.6 Error Reporting of Failed Dual Cast Cycles

If either the PCI address-routed destination device or the device connected to the Dual Cast Destination Port fails to return an ACK for the Dual Casted Memory Write, the standard PCI Express Correctable Errors (Replay Timer Timeout on first transmission attempt, Replay Rollover Status after four failed attempts) are reported.

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Chapter 10 Interrupts

10.1 Interrupt Support

The PEX 8604 supports the PCI Express interrupt model, which uses two mechanisms:

- INT*x* Interrupt Message-type emulation (compatible with the *PCI r3.0*-defined Interrupt signals)
- Message Signaled Interrupt (MSI), when enabled

For Conventional PCI compatibility, the PCI INT*x* emulation mechanism is used to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software, provides the same level of service as the corresponding PCI interrupt signaling mechanism, and is independent of System Interrupt Controller specifics. The PCI INT*x* emulation mechanism virtualizes PCI physical Interrupt signals, by using an in-band signaling mechanism, for the assertion and de-assertion of INT*x* interrupt signals.

In addition to PCI INT*x*-compatible interrupt emulation, the PEX 8604 supports the MSI mechanism. The PCI Express MSI mechanism is compatible with the MSI Capability defined in the *PCI r3.0*.

INT*x* and MSIs are mutually exclusive, on a per-Port basis; either can be enabled in a system (depending upon which interrupt type the system software supports, for assertion and de-assertion of interrupt signals), but never concurrently within the same domain. (Refer to the **PCI Command** register *Interrupt Disable* bit, offset 04h[10], and **MSI Capability** register, offset 48h, respectively.) The PEX 8604 does not convert received INT*x* Messages to MSI Messages.

The PEX 8604's external Interrupt output, PEX_INTA#, indicates the assertion and/or de-assertion of the internally generated INT*x* signal:

- **Non-Hot Plug-triggered interrupts** – PEX_INTA# assertion is controlled by the following **ECC Error Check Disable** register bits:
  - **NT mode only** – *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port, offset 1C8h[7])
  - *Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts* (offset 1C8h[6])
  - *Enable PEX_INTA# Interrupt Output(s) for Device-Specific Error-Triggered Interrupts* (offset 1C8h[5])

  When any of these bits are Set, Device-Specific errors trigger PEX_INTA# assertion; however, PEX_INTA# assertion and INT*x* Message generation are mutually exclusive, on a per-Port basis.
- **Hot Plug or Link State-triggered INT*x* events** – PEX_INTA# assertion is controlled by the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for Hot Plug or Link State Event-Triggered Interrupts* bit (offset 1C8h[4]). When this bit is Set, Hot Plug or Link State events trigger PEX_INTA# assertion; however, an INT*x* Message is not generated in this case. PEX_INTA# assertion and INT*x* Message generation for Hot Plug or Link State cases are mutually exclusive, on a per-Port basis.

The NT Port Virtual and Link Interfaces can each independently support the interrupt mechanism (INT*x* or MSI) used in their respective domains. (Refer to Section 14.7, "NT Port Interrupts," for details.)

10.1.1 Interrupt Sources or Events

The PEX 8604 internally generated interrupt/Message sources include:

- Hot Plug or Link State events:
  - Presence Detect Changed (logical OR of PRSNT# (I/O Expander PRSNT# input), and SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Attention Button Pressed
  - Power Fault Detected
  - MRL Sensor Changed
  - Command Completed
  - Link Bandwidth Management Status
  - Link Autonomous Bandwidth Status
- PCI Express Hot Plug events:
  - Presence Detect Changed (SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Data Link Layer State Changed
- Device-Specific errors (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, unless noted otherwise):
  - Payload Link List RAM 1-Bit ECC error (offset 1C0h[1:0])
  - Payload Link List RAM 2-Bit ECC error (offset 1C0h[3:2])
  - Ingress Link List RAM 1-Bit ECC error (offset 1C0h[6, 4])
  - Ingress Link List RAM 2-Bit ECC error (offset 1C0h[7, 5])
  - Packet RAM 0 1-Bit ECC error (offset 1C0h[12, 11, 9, 8])
  - Packet RAM 0 2-Bit ECC error (offset 1C0h[18, 17, 15, 14])
  - Packet RAM 1 1-Bit ECC error (offset 1C0h[24, 23, 21, 20])
  - Packet RAM 1 2-Bit ECC error (offset 1C0h[30, 29, 27, 26])
  - Egress Completion FIFO Overflow (All Ports, offset 1CCh[0])
  - Destination Queue Linked List RAM 2-Bit ECC error (offset 1CCh[4])
  - Destination Queue Linked List RAM 1-Bit ECC error (offset 1CCh[6])
  - Source Queue Linked List RAM 1-Bit ECC error (offset 1CCh[9:8])
  - Source Queue Linked List RAM 2-Bit ECC error (offset 1CCh[11:10])
  - Retry Buffer 1-Bit ECC error (offset 1CCh[12])
  - Retry Buffer 2-Bit ECC error (offset 1CCh[13])

*a. The SerDes Receiver Detect mechanism is comprised of the **Even/Odd Port Receiver Detect Status** register Receiver Detected on Lane x bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 200h[25:24], and Odd Ports, offset 204h[25:24]) or Hot Plug PRSNT# (from external I^2C I/O Expander) input for the Port.*

  - Header (TLP ID) RAM 2-Bit ECC error (offset 1CCh[21:20])
  - Header (TLP ID) RAM 1-Bit ECC error (offset 1CCh[25:24])
  - PCI Express Correctable/Uncorrectable Link errors
  - *DL_Active* state change on the NT Port Link Interface (refer to Section 14.7, "NT Port Interrupts")
- General-Purpose Input/Output (GPIO) events (upstream Port only)
- Non-Transparent (NT) Doorbell events (refer to Section 14.7, "NT Port Interrupts")

The PEX 8604 externally generated interrupt/Message sources include INT*x* Messages from downstream devices.

Table 10-1 lists the interrupt sources.

Table 10-1. Interrupt Sources

Event/Error	Description
Hot Plug or Link State events	**Slot Status** register (Downstream Ports, offset 80h): • *Presence Detect Changed* (bit 19 is Set) • *Data Link Layer State Changed* (bit 24 is Set)
PCI Express Hot Plug events	The master control of Hot Plug interrupt is the **Slot Control** register *Hot Plug Interrupt Enable* bit (Transparent Downstream Ports, offset 80h[5]). There are six sources of Hot Plug interrupt. Each Hot Plug source has its own *Enable* bit in the **Slot Control** register: • *Attention Button Pressed Enable* (bit 0) • *Power Fault Detector Enable* (bit 1) • *MRL Sensor Changed Enable* (bit 2) • *Presence Detect Changed Enable* (bit 3) • *Command Completed Interrupt Enable* (bit 4) • *Data Link Layer State Changed Enable* (bit 12) The interrupt status of each Hot Plug source is provided by the Port's **Slot Status** register (Transparent Downstream Ports, offset 80h). ***Note:*** *Presence (Presence Detect State, offset 80h[22], in each Transparent downstream Port) is determined by the logical OR of:* • *SerDes Receiver Detect (**Even/Odd Port Receiver Detect Status** register Receiver Detected on Lane x bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 200h[25:24], and Odd Ports, offset 204h[25:24])), and* • *Hot Plug PRSNT# (from external I^2C I/O Expander) input for the Port*
General-Purpose Input Interrupt events	External interrupt from any of the GPIO[30, 29, 16:0] signals that are configured as an Interrupt input in the **GPIO 0_15 Direction Control** and **GPIO 16, 29, 30 Direction Control** register *GPIOx Direction Control* bit(s) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 62Ch and 630h, respectively).

Table 10-1. Interrupt Sources *(Cont.)*

Event/Error	Description
Device-Specific errors	• Device-Specific errors indicated by the **Device-Specific Error Status for Egress ECC Error** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1C0h[31:0]), if not masked in the **Device-Specific Error Mask for Egress ECC Error** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1C4h[31:0]) • Egress Completion FIFO Overflow error indicated by the Port's **Error Handler 32-Bit Error Status** register *Completion FIFO Overflow Status* bit (offset 1CCh[0]), if not masked by the Port's **Error Handler 32-Bit Error Mask** register *Completion FIFO Overflow Mask* bit (offset 1D0h[0]) • Device-Specific errors indicated by the **Error Handler 32-Bit Error Status** register bit(s) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1CCh[26:4])), if not masked in their corresponding **Error Handler 32-Bit Error Mask** register bit(s) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1D0h[26:4]) • NT Port Link Interface Correctable errors reported by the NT Port Virtual Interface (to the Host of the upstream Port domain), collectively flagged in the **Link Error Status Virtual** register *Link Side Correctable Error Status* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h[0]), with specific errors indicated in the **Correctable Error Status** register (NT Port Link Interface, offset FC4h), if not masked both globally in the **Link Error Mask Virtual** register *Link Side Correctable Error Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[0]), nor individually in the **Correctable Error Mask** register (NT Port Link Interface, offset FC8h). • NT Port Link Interface Uncorrectable errors reported by the NT Port Virtual Interface (to the Host of the upstream Port domain), collectively flagged in the **Link Error Status Virtual** register *Link Side Uncorrectable Error Status* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h[1]), with specific errors indicated in the **Uncorrectable Error Status** register (NT Port Link Interface, offset FB8h), if not masked both globally in the **Link Error Mask Virtual** register *Link Side Uncorrectable Error Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[1]), nor individually in the **Uncorrectable Error Mask** register (NT Port Link Interface, offset FBCh). • NT Port Link Interface State change – Interrupt to the NT Port Virtual Interface Host, if enabled (not masked) by the **Link Error Mask Virtual** register *Link Side DL Active Change Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[2]). • Link Side Uncorrectable Error Message Drop interrupt to the NT Port Virtual Interface Host, if enabled (not masked) by the **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[3]). This feature supports applications using back-to-back NT Ports, where an Uncorrectable Error Message received (and properly dropped) by the NT Port Link Interface can trigger an interrupt to the NT Port Virtual Interface Host.

Table 10-1. Interrupt Sources *(Cont.)*

Event/Error	Description
NT Mode Only	
Device-Specific NT Port Link Interface errors and events	• NT Port Link Interface Correctable errors reported by the NT Port Virtual Interface (to the Host of the upstream Port domain), collectively flagged in the **Link Error Status Virtual** register *Link Side Correctable Error Status* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h[0]), with specific errors indicated in the **Correctable Error Status** register (NT Port Link Interface, offset FC4h), if not masked both globally in the **Link Error Mask Virtual** register *Link Side Correctable Error Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[0]), nor individually in the **Correctable Error Mask** register (NT Port Link Interface, offset FC8h). • NT Port Link Interface Uncorrectable errors reported by the NT Port Virtual Interface (to the Host of the upstream Port domain), collectively flagged in the **Link Error Status Virtual** register *Link Side Uncorrectable Error Status* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h[1]), with specific errors indicated in the **Uncorrectable Error Status** register NT Port Link Interface, offset FB8h), if not masked both globally in the **Link Error Mask Virtual** register *Link Side Uncorrectable Error Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[1]), nor individually in the **Uncorrectable Error Mask** register (NT Port Link Interface, offset FBCh). • NT Port Link Interface State change – Interrupt to the NT Port Virtual Interface Host, if enabled (not masked) by the **Link Error Mask Virtual** register *Link Side DL Active Change Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[2]). • Link Side Uncorrectable Error Message Drop interrupt to the NT Port Virtual Interface Host, if enabled (not masked) by the **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[3]). This feature supports applications using back-to-back NT Ports, where an Uncorrectable Error Message received (and properly dropped) by the NT Port Link Interface can trigger an interrupt to the NT Port Virtual Interface Host.
NT-Virtual Doorbell events	**NT Port Virtual Interface IRQ Set/Clear** register (offsets C4Ch[15:0] and/or C50h[15:0]) bit is Set while the corresponding **NT Port Virtual Interface IRQ Set/Clear** register (offsets C54h[15:0] and/or C58h[15:0]) bit is Cleared.
NT-Link Doorbell events	**NT Link Interface IRQ Set/Clear** register (offsets C5Ch[15:0] and/or C60h[15:0]) bit is Set while the corresponding **NT Link Interface IRQ Set/Clear** register (offsets C64h[15:0] and/or C68h[15:0]) bit is Cleared.

10.1.2 Interrupt Handling

The PEX 8604 provides an Interrupt Generation module with each Port. The module reads the Request for interrupts from different sources and generates an MSI or PCI-compatible Assert_INT*x*/ Deassert_INT*x* Interrupt Message. MSIs support a PCI Express edge-triggered interrupt, whereas Assert_INT*x* and Deassert_INT*x* Message transactions emulate PCI level-triggered interrupt signaling. The System Interrupt Controller functions include:

- Sensing Interrupt events
- Signaling the interrupt, by way of the INT*x* mechanism, and Setting the Interrupt Status bit
- Signaling the interrupt, by way of the MSI mechanism
- Handling INT*x*-type Interrupt Messages from downstream devices

10.2 INT*x* Emulation Support

The PEX 8604 supports PCI INT*x* emulation, to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software. PCI INT*x* emulation virtualizes PCI physical Interrupt signals, by using the in-band signaling mechanism.

PCI **Interrupt** registers (defined in the *PCI r3.0*) are supported. The *PCI r3.0* **PCI Command** register *Interrupt Disable* and **PCI Status** register *Interrupt Status* bits are also supported (offset 04h[10 and 19], respectively).

Although the *PCI Express Base r2.0* provides INTA#, INTB#, INTC#, and INTD# for INT*x* signaling, the PEX 8604 uses only INTA# for internal Interrupt Message generation, because it is a single-function device. However, incoming Messages from downstream devices can be of INTA#, INTB#, INTC#, or INTD# type. Internally generated INTA# Messages from the downstream Port are also re-mapped and collapsed at the upstream Port, according to the downstream Port's Device Number, with its own Device Number and Received Device Number from the downstream device.

When an interrupt is requested, the **PCI Status** register *Interrupt Status* bit is Set. If INT*x* interrupts are enabled (**PCI Command** register *Interrupt Disable* and **MSI Control** register *MSI Enable* bits, offsets 04h[10] and 48h[16], respectively, are Cleared), an Assert_INT*x* Message is generated and transmitted upstream to indicate the Port interrupt status. For each interrupt event, there is a corresponding *Interrupt Mask* bit; an Interrupt Message can be generated only when the corresponding *Interrupt Mask* bit is Cleared. Software reads and Clears the event and *Interrupt Status* bit after servicing the interrupt.

A Port de-asserts INT*x* or PEX_INTA# interrupts, in response to one or more of the following conditions:

- Port's **PCI Command** register *Interrupt Disable* bit (offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- Upstream Port Link goes down (DL_Down condition), or receives a Hot Reset (unless Hot Reset/DL_Down Reset is disabled, by Setting the **Debug Control** register *Upstream Port and NT-Link DL_Down Reset Propagation Disable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[20]))
- Software Clears the corresponding *Interrupt Status* bit

10.2.1 INT*x*-Type Interrupt Message Re-Mapping and Collapsing

The upstream Port re-maps and collapses the INT*x virtual wires* received at the downstream Port, based upon the downstream Port's Device Number and Received INT*x* Message Requester ID Device Number, and generates a new Interrupt Message, according to the mapping defined in Table 10-2.

Each virtual PCI-to-PCI bridge of a downstream Port specifies the Port Number associated with the INT*x* (Interrupt) Messages received or generated, and forwards the Interrupt Messages upstream.

A downstream Port transmits an Assert_INTA/Deassert_INTA Message to the upstream Port, due to a Hot Plug and/or PCI Express Hot Plug, Link State, GPIO, NT Port Doorbell interrupt, and/or Device-Specific error/event.

Internally generated INT*x* Messages always originate as type INTA Messages, because the PEX 8604 is a single-function device. Internally generated Interrupt INTA Messages from downstream Ports are re-mapped at the upstream Port to INTA, INTB, INTC, or INTD Messages, according to the mapping defined in Table 10-2.

INT*x* Messages from downstream devices and from internally generated Interrupt Messages are ORed together to generate INTA, INTB, INTC, or INTD level-sensitive signals, and edge-detection circuitry in the upstream Port generates the Assert_INT*x* and Deassert_INT*x* Messages. The upstream Port then forwards the new Messages upstream, by way of its Link.

Table 10-2. Downstream/Upstream Port INT*x* Interrupt Message Mapping

Device Number	At Downstream Port	By Upstream Port
0, 4	INTA	INTA
	INTB	INTB
	INTC	INTC
	INTD	INTD
1, 5	INTA	INTB
	INTB	INTC
	INTC	INTD
	INTD	INTA

10.2.1.1 Interrupt Re-Mapping and Collapsing – NT PCI-to-PCI Bridge Mode

In NT PCI-to-PCI Bridge mode, an NT Port Virtual Interface-generated interrupt is treated like an external event to the PCI-to-PCI bridge immediately upstream, for tracking purposes. In this mode, when the upstream Port receives an INT*x* Message from the NT Virtual Interface, the upstream Port re-mapping-collapsing logic performs double Swizzling, one based upon the NT Port Virtual Interface's Captured Device Number, and another based upon the virtual downstream Port (PCI-to-PCI) Device Number.

If software asserts a Secondary Bus Reset to this PCI-to-PCI bridge, the PCI-to-PCI bridge de-asserts the NT Port Virtual Interface interrupt.

10.3 MSI Support

One of the interrupt schemes supported by the PEX 8604 is the MSI mechanism, which is required for PCI Express devices. The MSI method uses Memory Write transactions to deliver interrupts. MSIs are edge-triggered interrupts.

Note: *MSIs and INTx are mutually exclusive, on a per-Port basis. The mechanisms that generate these types of interrupts* ***cannot*** *be simultaneously enabled.*

10.3.1 MSI Operation

At configuration time, system software traverses the function Capability list. If a Capability ID of 05h is found, the function implements MSIs. System software reads the **MSI Capability** structure registers, to determine function capabilities.

The **MSI Control** register *Multiple Message Capable* field (offset 48h[19:17]) default value is 010b, which indicates that the PEX 8604 requests up to four MSI Vectors (Address and Data). When the register's *Multiple Message Enable* field (offset 48h[22:20]) is Cleared (default), only one Vector is allocated, and therefore, the PEX 8604 can generate only one Vector for all errors or events. When system software writes a non-zero value to the *Multiple Message Enable* field, multiple-Vector support is enabled (the quantity of Vectors supported is dependent upon the value). Table 10-3 lists the supported MSI Vector types.

Table 10-3. Supported MSI Vector Types

Vector Type	Transparent Mode	NT Mode	
		Virtual Interface	Link Interface
Power Management, or Hot Plug or Link State events	✔	✔	
Device-Specific errors	✔	✔	✔
GPIO interrupts	✔	✔	
NT Doorbell interrupts		✔	✔

System software initializes the MSI Address registers (offsets 4Ch and 50h) and **MSI Data** register (offset 54h), with a system-specified Vector. After system software enables the MSI function (by Setting the **MSI Control** register *MSI Enable* bit, offset 48h[16]), when an Interrupt event occurs, the Interrupt Generation module generates a DWord Memory Write to the address specified by the **MSI Address** (lower 32 bits of the *Message Address* field) and **MSI Upper Address** (upper 32 bits of the *Message Address* field) register contents (offsets 4Ch and 50h, respectively). The single DWord Payload includes zero (0) for the upper two bytes, and the lower two bytes are taken from the **MSI Data** register. The **MSI Control** register *Multiple Message Enable* field (offset 48h[22:20]) can be programmed to any value of 000b through 111b. When programmed to 010b through 111b, the lower three bits of Message data are changed to indicate the general type of interrupt event that occurred. (Refer to Table 10-3.)

The quantity of MSI Vectors generated is dependent upon the quantity enabled, as follows:

- If **one** MSI Vector is enabled (default), all interrupt categories generate the same MSI Vector
- If **two** MSI Vectors are enabled, Device-Specific errors generate their own MSI Vector, while all other categories are combined and generate the same Vector
- If **four** MSI Vectors are enabled, each interrupt category generates its own MSI Vector

If a non-masked Interrupt event occurs before system software Sets the *MSI Enable* bit, normally (but unlike Conventional PCI interrupts, which are level-triggered), an MSI packet is sent immediately after software Sets the *MSI Enable* bit, to notify the system of the prior event. Alternatively, MSIs for prior events can be disabled, on a per-Port basis, by Setting the **ECC Error Check Disable** register *Disable Sending MSI if MSI Is Enabled after Interrupt Status Set* bit (offset 1C8h[8]).

When the error or event that caused the interrupt is serviced, the PEX 8604 can generate a new MSI Memory Write as a result of new events. Because MSIs are edge-triggered events, four bits are provided for masking the errors (**MSI Mask** register *Interrupt Mask* bits, offset 58h[3:0]). A new MSI can be generated only after the *Interrupt Mask* bits are serviced. System software should mask these bits when the MSI event is being processed.

The **MSI Control** register *MSI 64-Bit Address Capable* bit is enabled (offset 48h[23], is Set), by default. If the serial EEPROM and/or I^2C/SMBus Clears the bit, the **MSI Capability** structure is reduced by 1 DWord (*that is*, register offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively).

10.3.1.1 NT PCI-to-PCI Bridge Mode MSIs – NT PCI-to-PCI Bridge Mode

In NT PCI-to-PCI Bridge mode, MSI TLPs are not generated if the **PCI Command** register *Bus Master Enable* bit (offset 04h[2]) is Cleared in the upstream Port, NT Port Virtual Interface, and Virtual Downstream PCI-to-PCI bridge.

10.3.2 MSI Capability Registers

For details, refer to Section 13.8, "MSI Capability Registers (Offsets 48h – 64h)."

10.4 PEX_INTA# Interrupts

PEX_INTA# Interrupt output is enabled when the following conditions exist:

- INT*x* Messages are enabled (**PCI Command** register *Interrupt Disable* bit, offset 04h[10], is Set) and MSIs are disabled (**MSI Control** register *MSI Enable* bit, offset 48h[16], is Cleared)
- PEX_INTA# outputs are enabled for the following interrupts, when the **ECC Error Check Disable** register bit associated with that interrupt is Set:
  - **NT mode only** – *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port, offset 1C8h[7])
  - *Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts* bit (offset 1C8h[6])
  - *Enable PEX_INTA# Interrupt Output(s) for Device-Specific Error-Triggered Interrupts* bit (offset 1C8h[5])
  - *Enable PEX_INTA# Interrupt Output(s) for Hot Plug or Link State Event-Triggered Interrupts* bit (offset 1C8h[4])

The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources:

- Conventional PCI INT*x* Message generation
- Native MSI transaction generation
- Device-Specific PEX_INTA# assertion

PEX_INTA# assertion (Low) indicates that the PEX 8604 detected one or more of the events and/or errors (if not masked) listed in Table 10-1.

Note: *PEX_INTA# assertion and INTx messaging are mutually exclusive for a given interrupt event. When MSIs are enabled (offset 48h[16], is Set), both PEX_INTA# and INTx are disabled for PEX 8604 internally generated interrupts. The forwarding of external INTx Messages received from a downstream Port to the upstream Port is always enabled.*

10.5 General-Purpose Input/Output

The PEX 8604 contains 19 GPIO balls and associated registers, that can be programmed to function as GPIO and/or Interrupt inputs. Default functionality is GPIO inputs; however, serial EEPROM, I^2C/SMBus, and/or software can program the GPIO registers to define functionality for each I/O, to be used as GPIO, Interrupt inputs, or Serial Hot Plug PERST# outputs.

Table 10-4 lists the registers used for GPIO functionality.

Table 10-4. Registers Used for GPIO Functionality

Register Offset[a]	Register Name
62Ch	**GPIO 0_15 Direction Control**
630h	**GPIO 16, 29, 30 Direction Control**
638h	**GPIO 0_16, 29, 30 Input De-Bounce**
63Ch	**GPIO 0_15 Input Data**
640h	**GPIO 16, 29, 30 Input Data**
644h	**GPIO 0_15 Output Data**
648h	**GPIO 16, 29, 30 Output Data**
64Ch	**GPIO 0_16, 29, 30 Interrupt Polarity**
650h	**GPIO 0_16, 29, 30 Interrupt Status**
654h	**GPIO 0_16, 29, 30 Interrupt Mask**

a. All registers listed in this table are located in Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port.

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Chapter 11 Hot Plug Support

11.1 Introduction

Hot Plug capability allows board insertion and removal from a running system, without adversely affecting the system. Boards are typically inserted or removed to repair faulty boards or re-configure the system without system down time. Hot Plug capability allows systems to isolate faulty boards in the event of a failure.

11.2 Hot Plug Features

The following are the PEX 8604 Hot Plug features:

- Hot insertion and removal
- All Ports are Hot Plug-capable, through I^2C (Serial Hot Plug Controller on every Port)
- Serial Hot Plug Controller with I^2C I/O Expander on three Transparent downstream Ports
- Insertion and removal of PCI Express boards, without removing system power
- Generates Power Management Event (PME) on a Hot Plug event in a sleeping system
- Electromechanical Interlock Control feature available on Serial Hot Plug-capable Ports

11.3 Hot Plug Signals

The on-chip signals for Serial Hot Plug Controller support are defined in Section 3.4.2, "Serial Hot Plug Signals." In addition to the set of on-chip Serial Hot Plug signals, the PEX 8604 supports Serial Hot Plug signals to and from the I^2C I/O Expander, which are used with Serial Hot Plug-capable Transparent downstream Ports. (Refer to Section 11.6.2.)

11.4 Hot Plug Registers

All Transparent downstream Ports include identical sets of Hot Plug registers.

The PCI Express Hot Plug Configuration, Capability, Command, Status, and Event registers are described in Section 13.9, "PCI Express Capability Registers (Offsets 68h – A0h)."

Device-Specific Hot Plug configuration features are programmable in register offset 1E0h of each Transparent downstream Port.

11.5 Hot Plug Interrupts

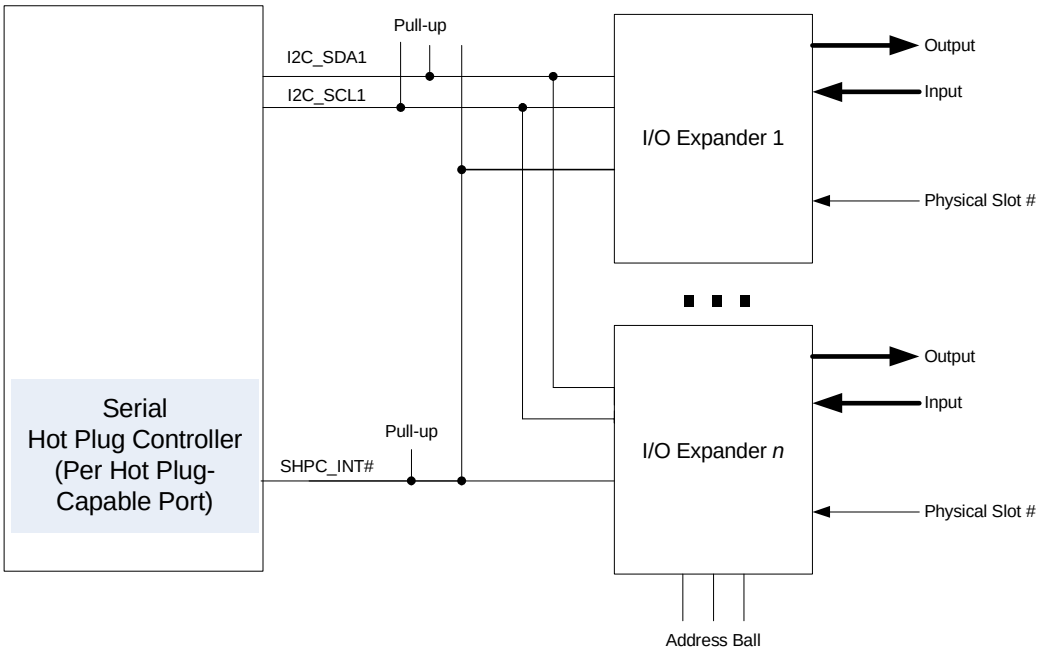
Refer to Chapter 10, "Interrupts," for details.

11.6 Serial Hot Plug Controller

Note: *The I^2C Master interface is described in this section. The Master capabilities are limited to the Serial Hot Plug Controller.*

Using I/O Expander ICs sitting on an I^2C Bus, the PEX 8604 has the option of Hot Plug capability on all its Transparent downstream Ports. Figure 11-1 illustrates the internal Serial Hot Plug Controller interface. The Serial Hot Plug Controller controls the output Ports on the I/O Expanders and retrieves the Port status, *such as* device connect status, Power Fault, and MRL Sensor position, from all I/O Expanders. When there is an input change to an I/O Expander, an INT*x* interrupt from an I/O Expander goes Low and the PEX 8604 reads the I/O Expander. When an I/O Expander output Port requires updating with a new value, the PEX 8604 writes to the I/O Expander through the I^2C Bus.

Figure 11-1. Serial Hot Plug Interface Diagram



11.6.1 Hot Plug Operations by way of I2C I/O Expander

When software issues a Slot Power On command, the Serial Hot Plug Controller issues an I2C Write to the I/O Expander, to assert the PWREN output on the I/O Expander, and thereby turn On the power. After the Write is complete and the T_{pepv} time has elapsed, the Serial Hot Plug Controller issues another Write to the I/O Expander, to assert its RECLKEN# output, and thereby turn On the Reference Clock (REFCLK) at the slot.

After the RECLKEN# output is asserted, the Serial Hot Plug Controller issues another Write, to de-assert the I/O Expander PERST# output to the slot. If there are commands, *such as* Attention or Power LED changes along with the Power Control command, the Serial Hot Plug Controller includes the LED output value change, along with these Writes, to change the LED status. The same procedure applies to other commands, *such as* Port Power Off. After the Serial Hot Plug Controller completes all Write operations, it Sets the *Command Completed* bit. When another command is issued before the current command completes, the results are undefined. With a 100-kHz I2C clock, the time required to complete one Write operation to an I/O Expander is approximately 1 ms.

11.6.2 I2C I/O Expander Parts Selection and Pin Definition

Two types of I2C I/O Expanders can be used for Serial Hot Plug:

- **16-bit device** – For the 16-bit device, the 7-bit I2C address must be 0100_XXXb; a Maxim MAX7311, NXP PCA9555, or TI PCA9555 is recommended. I/O Expander addresses must begin with the lowest address, and increment sequentially (corresponding to increasing PEX 8604 Port Numbers), for each device. For MAX7311 (which supports more addresses than the other 16-bit devices), the 7-bit I2C addresses can be in two ranges, 0100_XXXb and 1010_XXXb. All 16 I/O pins of the devices are used for one Port. A 16-bit device supports one Serial Hot Plug Port. (Refer to Figure 11-2.)

  For further details, refer to the manufacturer's data sheets for the Maxim MAX7311, NXP PCA9555, or TI PCA9555.

- **40-bit device** – For the 40-bit device, the 7-bit I2C address must be within two ranges, 0100_XXXb and 1010_XXXb; an NXP PCA9698 is recommended. I/O Expander addresses must begin with the lowest address, and increment sequentially (corresponding to increasing PEX 8604 Port Numbers), for each device. The lower 32 I/O pins are used for two Ports. A 40-bit device can support two sets of Serial Hot Plug pins. The two sets are indicated with suffix PX and PY, in Figure 11-3.

  For further details, refer to the manufacturer's data sheet for the NXP PCA9698.

The PEX 8604 can support multiple 16- or 40-bit I/O Expanders, but not both types concurrently, to provide Hot Plug services on all Transparent downstream Ports. (Refer to the **Power Management Hot Plug User Configuration** register *40-Pin I/O Expander Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1E0h[17])). Each I/O Expander has a 3-bit address, and thus one PEX 8604 can support up to three external I/O Expanders.

Table 11-1 defines the external I2C I/O Expander pins, in location order.

Table 11-1. External I²C I/O Expander Pin Definitions, by Location

Signal Name	Direction	Description	Location	
			16-Bit Device[a]	40-Bit Device[b]
PWRLED#	O	**Hot Plug Power LED Output**	IO0_0 or P00	IO0_0 IO2_0
ATNLED#	O	**Hot Plug Attention LED Output**	IO0_1 or P01	IO0_1 IO2_1
PWREN	O	**Hot Plug Power Enable Output**	IO0_2 or P02	IO0_2 IO2_2
RECLKEN#	O	**Hot Plug Reference Clock Enable Output**	IO0_3 or P03	IO0_3 IO2_3
PERST#	O	**Hot Plug Reset Output**	IO0_4 or P04	IO0_4 IO2_4
INTERLOCK	O	**Electromechanical Interlock Output Control** Used to physically lock the adapter or Manually operated Retention Latch (MRL) in place until software releases it. The signal default is 0. The current state of the Electromechanical Interlock is reflected in the **Slot Status** register *Electromechanical Interlock Status* bit (offset 80h[23]). This output can be toggled by writing 1 to the **Slot Control** register *Electromechanical Interlock Control* bit (offset 80h[11]). A Write of 0 has no effect. INTERLOCK is enabled when the **Slot Capability** register *Electromechanical Interlock Present* bit (offset 7Ch[17]) is Set (default for Serial Hot Plug-capable Transparent downstream Ports).	IO0_5 or P05	IO0_5 IO2_5
GPIO	I/O	**General-Purpose Input/Output (GPIO)** Configured as input (default) or output by the *HPC GPIO Config* bit (offset 1E0h[18]), with the pin value in the *HPC GPIO Input/Output Value* bit (offset 1E0h[19]).	IO0_6 or P06	IO0_6 IO2_6
SLOT NUMBER[3:0]	I	**Physical Slot Number Bits 7Ch[26:23]** Slot Number value from I/O Expander inputs, which map to the **Slot Capability** register *Physical Slot Number* bits (offset 7Ch[26:23]). The value of the lowest four bits of the Physical Slot Number (offset 7Ch[22:19]) are automatically programmed to the same value as the Port Number.	{IO1_2:0, IO0_7} or {P1[2:0], P07}	{IO1_2:0, IO0_7} {IO3_2:0, IO2_7}
PRSNT#	I	**Hot Plug PRSNT2# Input**	IO1_3 or P13	IO1_3 IO3_3
MRL#	I	**Hot Plug Manually Operated Retention Latch Sensor Input**	IO1_4 or P14	IO1_4 IO3_4
BUTTON#	I	**Hot Plug Attention Button Input**	IO1_5 or P15	IO1_5 IO3_5
PWRFLT#	I	**Hot Plug Power Fault Input**	IO1_6 or P16	IO1_6 IO3_6
PWRGOOD	I	**Hot Plug Power Good Input**	IO1_7 or P17	IO1_7 IO3_7

a. Refer to Figure 11-2 for pinout.

b. Refer to Figure 11-3 for pinout.

Figure 11-2. 16-Bit I2C I/O Expander Pinout

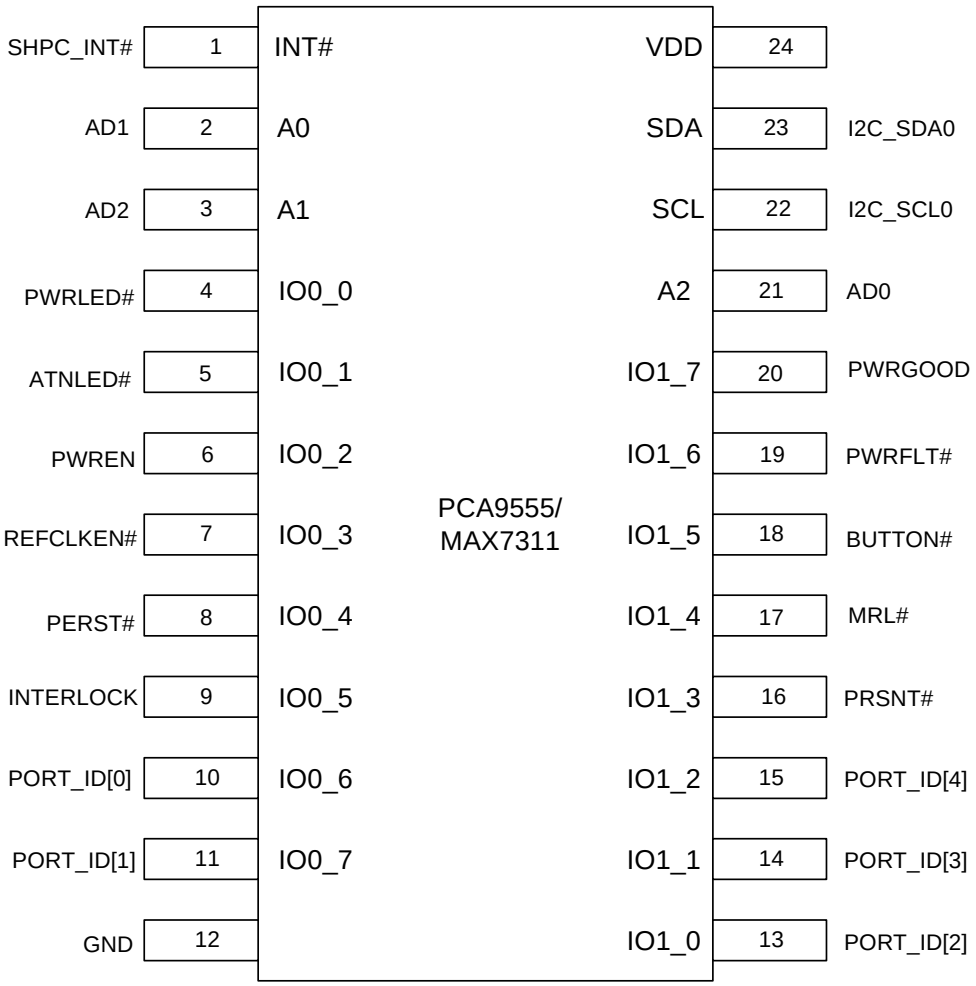
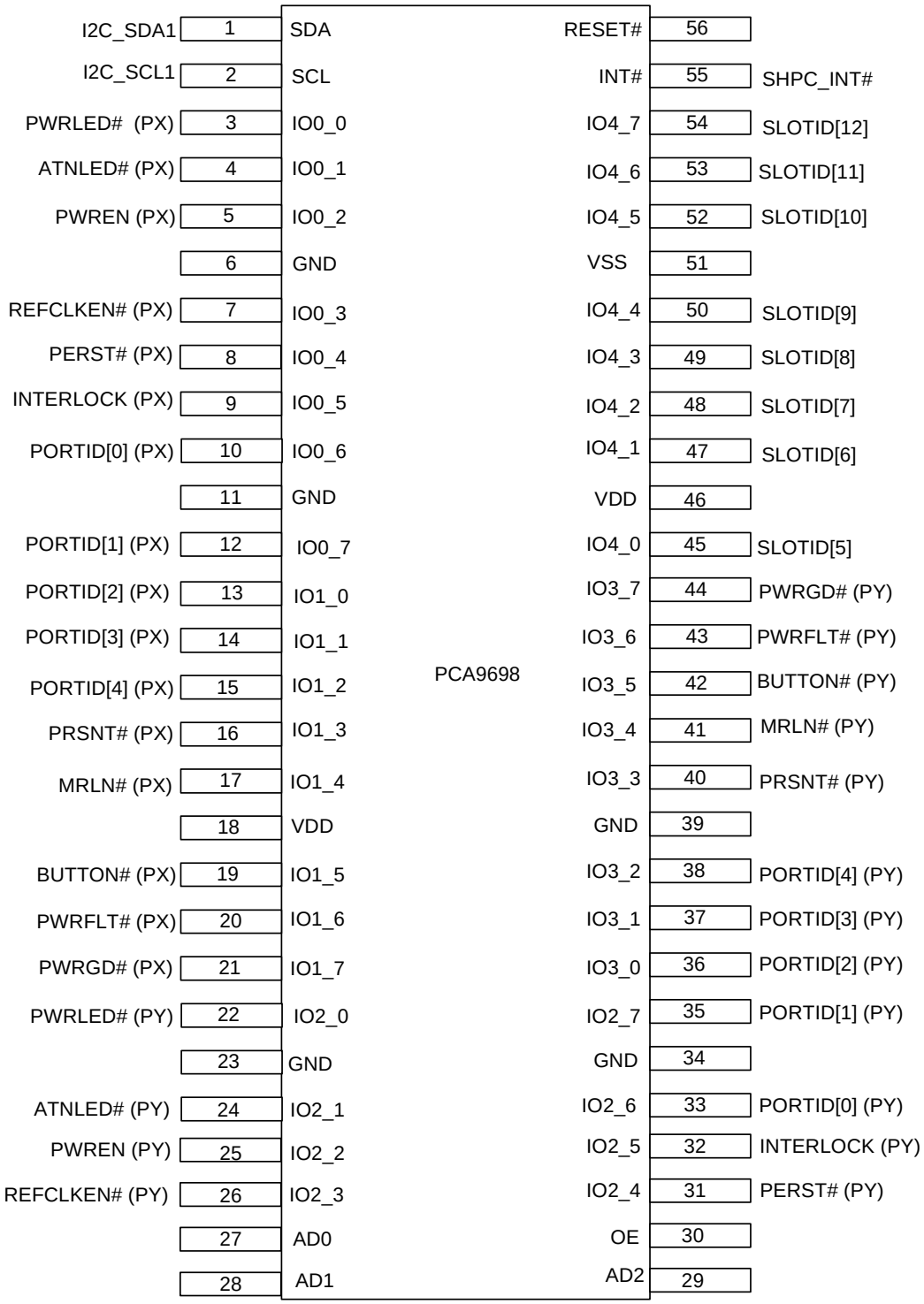


Figure 11-3. 40-Bit I²C I/O Expander Pinout



11.6.3 Serial Hot Plug Port Enumeration and Assignment

Each I/O Expander has a 7-bit address; the PEX 8604 scans for sequential I^2C addresses, starting with address 40h.

After PEX_PERST# de-asserts and the serial EEPROM (if present) load completes, the Serial Hot Plug Controller accesses all I^2C addresses to perform the I/O Expander hunt, to determine the presence of external I/O Expander devices. If the Controller receives an Acknowledge Control Packet (ACK) from the I/O Expander, it remembers the presence of an external I/O Expander device, which is assigned to one of the Transparent downstream Ports.

Note: *The PEX 8604 can support up to three downstream Ports. Every Transparent downstream Port can support Hot Plug.*

To simplify the Serial Hot Plug Port enumeration and assignment, the virtual Serial Hot Plug Port definition is provided as follows, and the mapping between virtual Serial Hot Plug Port and PEX 8604 Ports is provided later.

Table 11-2 defines the virtual Serial Hot Plug Port for a 16-bit device, *such as* a Maxim MAX7311, NXP PCA9555, or TI PCA9555. Table 11-3 defines the virtual Serial Hot Plug Port for a 40-bit device, *such as* an NXP PCA9698.

The following three types of Ports are not Serial Hot Plug-capable, and therefore are not assigned a virtual Serial Hot Plug Port Number:

- Disabled Ports, due to Port configuration
- Upstream Port
- NT Port

Table 11-2. Virtual Serial Hot Plug Port Definition for 16-Bit Device

I^2C Slave Address[2:0]	000b	001b	010b	011b
Virtual Serial Hot Plug Port #	0	1	2	3

Table 11-3. Virtual Serial Hot Plug Port Definition for 40-Bit Device

I^2C Slave Address[2:0]	000b	000b	001b	001b
I/O Pin Range	0-15	16-31	0-15	16-31
Virtual Serial Hot Plug Port #	0	1	2	3

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Chapter 12 Power Management

12.1 Overview

The PEX 8604 Power Management (PM) features provide the following services:

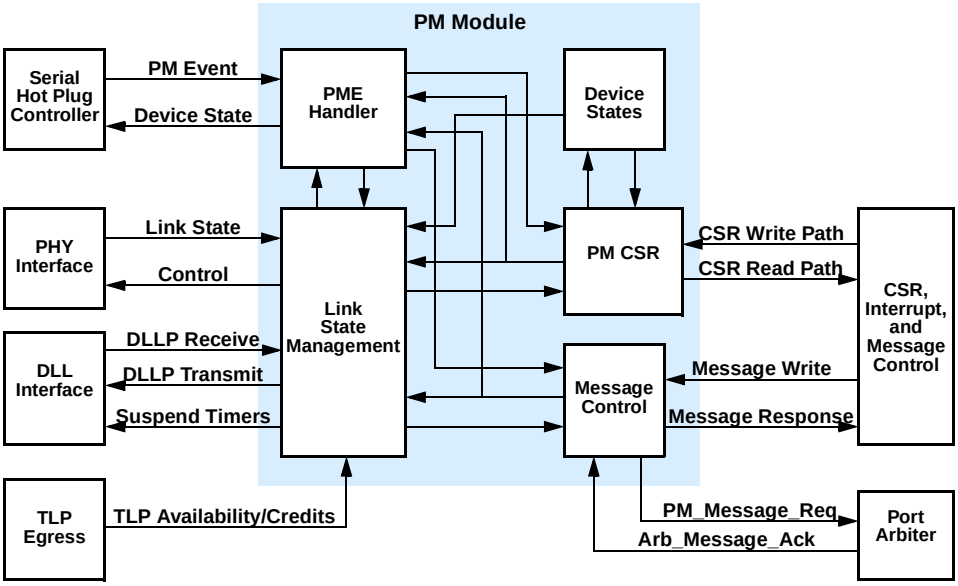
- Mechanisms to identify PM capabilities
- Ability to transition into certain PM states
- Notification of the current PM state of each Port
- Support for the option to wakeup the system upon a specific event

The PEX 8604 supports hardware-autonomous PM and software-driven D-State PM. The switch also supports the L0s and L1 Link PM states in hardware-autonomous Active State Power Management (ASPM), as well as the L1, L2/L3 Ready, and L3 Link PM states in Conventional PCI-compatible PM. D0, D3hot, and D3cold Device PM states are supported in Conventional PCI-compatible PM. Because the PEX 8604 does not support Vaux, Power Management Event (PME) generation from the D3cold Device PM state is ***not supported***.

The PM module interfaces with a Physical Layer (PHY) electrical sub-block, to transition the Link state into a low-power state, when the module receives a Power State Change Request from a downstream component, or an internal event forces the Link state entry into low-power states in hardware-autonomous ASPM mode. PCI Express Link states are not directly visible to Conventional PCI Bus driver software; however, they are derived from the PM state of the components residing on those Links.

Figure 12-1 provides a functional block diagram of the PEX 8604 PM module.

Figure 12-1. PM Module Functional Block Diagram



12.2 Power Management Features

- *PCI Express Base r2.0*-compliant
- *PCI Power Mgmt. r1.2*-compliant
- Link Power Management States (*L-States*; also referred to as *Link PM states*)
  - PCI Bus Power Management – L1, L2/L3 Ready, and L3 (Vaux is ***not supported***)
  - Active State Power Management (ASPM) – L0s and L1
- Device Power Management State (*D-States*; also referred to as *Device PM states*)
  - D0 (D0uninitialized and D0active) and D3 (D3hot and D3cold) support
- Power Management Event (PME) support from D3hot
- PME due to Hot Plug and/or PCI Express Hot Plug events
- Forwards PME_Turn_Off broadcast messages
- Supports Clock Power Management using CLK_REQ#
- Implements Gen 2-specific Control and Status registers, and associated interrupts
- Supports ASPM L0s, ASPM L1, PCI PM L1, and L2/L3 Ready Link PM states in NT mode

12.3 Power Management Capability

12.3.1 Device Power Management States

The PEX 8604 supports the PCI Express PCI-PM D0 and D3hot Device PM states. The D1 and D2 Device PM states, which are optional in the *PCI Express Base r2.0*, are ***not supported*** by the PEX 8604.

The D3hot Device PM state can be entered from the D0 Device PM state, when system software programs the Port's **PCI Power Management Status and Control** register *Power State* field (offset 44h[1:0]) to 11b. The D0uninitialized Device PM state can be entered from the D3hot Device PM state when system software Clears the Port's *Power State* field.

12.3.1.1 D0 Device Power Management State

The D0 Device PM state is divided into two distinct sub-states – *uninitialized* and *active*. When power is initially applied to a PCI Express component, it defaults to the D0uninitialized Device PM state. The component remains in the D0uninitialized Device PM state until the serial EEPROM load and initial Link training completes.

A device enters the D0active Device PM state when system software Sets any combination of the **PCI Command** register *Bus Master Enable*, *Memory Access Enable*, and/or *I/O Access Enable* bits (offset 04h[2, 1, and/or 0], respectively).

12.3.1.2 D3hot Device Power Management State

Once in the D3hot Device PM state, the PEX 8604 can later be transitioned into the D3cold Device PM state, by removing power from its Host component. Functions that are in the D3hot Device PM state can be transitioned, by software, to the D0uninitialized Device PM state. When in the D3hot Device PM state, Hot Plug or Link State operations cause a PME in the PEX 8604.

Only Type 0 Configuration accesses are allowed in the D3hot Device PM state. Memory and I/O transactions result in an Unsupported Request (UR). Completions flowing in either direction are not affected.

Type 1 transactions flowing toward a PEX 8604 Port in the D3hot Device PM state are terminated as URs. Type 0 Configuration transactions complete successfully. When the PEX 8604 upstream Port is programmed to the D3hot Device PM state, the Port initiates Conventional PCI-PM L1 Link PM state entry.

12.3.2 Link Power Management States

PEX 8604 components hold their upstream Link and downstream Links in the L0 Link PM state when they are in the standard operational state (Conventional PCI-PM state is in the D0active Device PM state). ASPM defines a mechanism for components in the D0 Device PM state, to reduce Link power by placing their Links into a low-power state and instructing the other end of the Link to do likewise. This allows hardware-autonomous, dynamic Link power reduction beyond what is achievable by software-only-controlled PM. Table 12-1 defines the relationship between a component's Power state and its upstream Link. Table 12-2 defines the relationship between Link PM states and power-saving actions.

Conventional PCI PM, and the L1 and L2/L3 Ready Link PM states are controlled by system software programming the PEX 8604 into the D3hot Device PM state, and subsequently causing the Root Complex to broadcast the PME_Turn_Off Message to the downstream hierarchy.

Table 12-1. Relationship between Component Power State and Upstream Link

Downstream Component Device PM State	Permissible Upstream Component Device PM State	Permissible Interconnect Link PM State
D0	D0	L0, L0s, L1 (optional) – ASPM.
D3hot	D0 to D3hot	L1, L2/L3 Ready.
D3cold (no Vaux)	D0 to D3cold	L3 (off). Zero power.

Table 12-2. Relationship between Link PM States and Power-Saving Actions

Link PM State	Power-Saving Actions
Tx L0s	PHY Tx Lanes are in a high-impedance state.
Rx L0s	PHY Rx Lanes in a low-power state.
L1	PHY Tx and Rx Lanes are in a low-power state. FC timers are suspended.
L2/L3 Ready	PHY Tx and Rx Lanes are in a low-power state. FC timers are suspended.
L3 (D3cold)	Component is fully powered Off.

12.3.3 PCI Express Power Management Support

The PEX 8604 supports PM features required in the *PCI Express Base r2.0*. Table 12-3 lists supported and non-supported features and the register bits/fields used for configuration or activation.

Table 12-3. Supported PCI Express PM Capabilities

Register		Description	Supported	
Offset	Bit(s)		Yes	No
40h	PCI Power Management Capability (All Ports)			
	7:0	**Capability ID** Program to 01h, to indicate that the Capability structure is the PCI Power Management Capability structure.	✔	
	15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	✔	
	18:16	**Version** Default 011b indicates compliance with the *PCI Power Mgmt. r1.2*.	✔	
	19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.		✔
	21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	✔	
	24:22	**AUX Current** The PEX 8604 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.		✔
	25	**D1 Support** Default value of 0 indicates that the PEX 8604 does ***not support*** the D1 Device PM state.		✔
	26	**D2 Support** Default value of 0 indicates that the PEX 8604 does ***not support*** the D2 Device PM state.		✔
	31:27	**PME Support** Bits [31, 30, and 27] must be Set, to indicate that the PEX 8604 will forward PME Messages, as required by the *PCI Express Base r2.0*.	✔	

Table 12-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
	PCI Power Management Status and Control (All Ports)			
	1:0	**Power State** Used to determine the current Device PM state of the Port, and to program the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	✔	
	3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	✔	
	8	**PME Enable** 0 = Disables PME generation by the corresponding PEX 8604 Port[a] 1 = Enables PME generation by the corresponding PEX 8604 Port	✔	
44h	12:9	**Data Select** Initially writable by serial EEPROM and/or I^2C only[b]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I^2C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	✔	
	14:13	**Data Scale** Writable by serial EEPROM and/or I^2C only[b]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h, and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h.	✔	
	15	**PME Status** 0 = PME is not generated by the corresponding PEX 8604 Port[a] 1 = PME is being generated by the corresponding PEX 8604 Port	✔	

a. Because the PEX 8604 does not consume auxiliary power, this bit is not sticky, and is always Cleared at power-on reset.

*b. With no serial EEPROM nor previous I^2C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

Table 12-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
44h		**PCI Power Management Control/Status Bridge Extensions (All Ports)**		
	22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.		✔
	23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.		✔
		PCI Power Management Data (All Ports)		
	31:24	**Data** Writable by serial EEPROM and/or I^2C only[b]. There are four supported *Data Select* values (0h, 3h, 4h, and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	✔	
6Ch		**Device Capability (All Ports)**		
	8:6	**Endpoint L0s Acceptable Latency** Because the PEX 8604 is a switch and not an endpoint, the PEX 8604 does ***not support*** this feature. 000b = Disables the capability		✔
	11:9	**Endpoint L1 Acceptable Latency** Because the PEX 8604 is a switch and not an endpoint, the PEX 8604 does ***not support*** this feature. 000b = Disables the capability		✔
	25:18	**Captured Slot Power Limit Value (Upstream Port and NT Port)** For the PEX 8604 upstream Port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*). Do not change for downstream Ports.	✔	
	27:26	**Captured Slot Power Limit Scale (Upstream Port and NT Port)** For the PEX 8604 upstream Port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001 Do not change for downstream Ports.	✔	

a. Because the PEX 8604 does not consume auxiliary power, this bit is not sticky, and is always Cleared at power-on reset.

*b. With no serial EEPROM nor previous I^2C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

Table 12-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
70h		**Device Control (All Ports)**		
	10	**AUX Power PM Enable**		✔
		Device Status (All Ports)		
	20	**AUX Power Detected**		✔
74h		**Link Capability (All Ports)**		
	11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.	✔	
	14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the **Common Physical Layer Command/Status** register *N_FTS Value* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 238h[15:8]) value and Link speed. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *N_FTS Value* x 4 (4 symbol time in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *N_FTS Value* x 4 (4 symbol time in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = Corresponding PEX 8604 Port L0s Link PM state Exit Latency is 512 ns to less than 1 µs at 5.0 GT/s 101b = Corresponding PEX 8604 Port L0s Link PM state Exit Latency is 1 µs to less than 2 µs at 2.5 GT/s All other encodings are ***reserved***.	✔	
	17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = Corresponding PEX 8604 Port L1 Link PM state Exit Latency is 1 µs to less than 2 µs at 5.0 GT/s 010b = Corresponding PEX 8604 Port L1 Link PM state Exit Latency is 2 µs to less than 4 µs at 2.5 GT/s All other encodings are ***reserved***.	✔	
	18	**Clock Power Management Capable**	✔	

Table 12-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
78h		**Link Control (All Ports)**		
	1:0	**Active State Power Management (ASPM)** 00b = Disable[c] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries	✔	
	8	**Clock Power Management Enable** The PEX 8604 does ***not support*** removal of the Reference Clock in the L1 and L2/L3 Ready Link PM states.		✔
7Ch		**Slot Capability (Downstream Ports; Upstream Port Always Reads 0)**		
	0	**Attention Button Present** ***Reserved*** for the upstream Port and NT Port. 0 = Attention Button is not implemented 1 = Attention Button is implemented on the slot chassis of the corresponding PEX 8604 Transparent downstream Port with an I^2C I/O Expander	✔	
	1	**Power Controller Present** ***Reserved*** for the upstream Port and NT Port. 0 = Power Controller is not implemented. The Hot Plug Controller is disabled for that slot and a power-up sequence is not executed. The slot remains in the disabled state. 1 = Power Controller is implemented for the slot of the corresponding PEX 8604 Transparent downstream Port with an I^2C I/O Expander. The Controller powers up the slot when the Manually operated Retention Latch (MRL) is closed and the **Slot Control** register *Power Controller Control* bit (offset 80h[10]) is Cleared. Otherwise, if bit 2 (*MRL Sensor Present*) is disabled (Cleared), the MRL's position has no effect on powering up the slot.	✔	
	2	**MRL Sensor Present** ***Reserved*** for the upstream Port and NT Port. 0 = MRL Sensor is not implemented. MRL position is "Don't Care" for that slot. 1 = MRL Sensor is implemented on the slot chassis of the corresponding PEX 8604 Transparent downstream Port with an I^2C I/O Expander. The PEX 8604 senses whether the MRL is open or closed for a slot. MRL should be Low for power-on for that slot.	✔	
	3	**Attention Indicator Present** ***Reserved*** for the upstream Port and NT Port. 0 = Attention Indicator is not implemented 1 = Attention Indicator is implemented on the slot chassis of the corresponding PEX 8604 Transparent downstream Port with an I^2C I/O Expander	✔	

c. The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.

Table 12-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
	Slot Capability (Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*			
	4	**Power Indicator Present** ***Reserved*** for the upstream Port and NT Port. 0 = Power Indicator is not implemented 1 = Power Indicator is implemented on the slot chassis of the corresponding PEX 8604 Transparent downstream Port with an I^2C I/O Expander	✔	
	5	**Hot Plug Surprise** ***Reserved*** for the upstream Port and NT Port. 0 = No device in the corresponding PEX 8604 downstream Port (with an I^2C I/O Expander) slot is removed from the system without prior notification 1 = Device in the corresponding PEX 8604 downstream Port slot can be removed from the system without prior notification	✔	
	6	**Hot Plug Capable** ***Reserved*** for the upstream Port and NT Port. 0 = Corresponding PEX 8604 downstream Port slot is not capable of supporting Hot Plug operations 1 = Corresponding PEX 8604 Transparent downstream Port (with an I^2C I/O Expander) slot is capable of supporting Hot Plug operations	✔	
7Ch	14:7	**Slot Power Limit Value** ***Reserved*** for the upstream Port. The maximum power supplied by the corresponding PEX 8604 downstream slot is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the *Slot Power Limit Scale* field value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I^2C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.	✔	
	16:15	**Slot Power Limit Scale** ***Reserved*** for the upstream Port. The maximum power supplied by the corresponding PEX 8604 downstream slot is determined by multiplying the value in this field by the *Slot Power Limit Value* field value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I^2C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	

Table 12-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
80h		**Slot Control (Transparent Downstream Serial Hot Plug-Enabled Ports; Upstream Port Always Reads 0)**		
	1	**Power Fault Detector Enable** ***Reserved*** for the upstream Port and NT Port. 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), for a Power Fault Detected event on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port	✔	
	9:8	**Power Indicator Control** ***Reserved*** for the upstream Port and NT Port. Controls the Power Indicator on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port slot. Reads return the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port Power Indicator's current state. Writing a non-zero value triggers a Command Completed event (even if the value written is the same as the existing value). Writing 00b preserves the current value and does not trigger a Command Completed event. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator	✔	
	10	**Power Controller Control** ***Reserved*** for the upstream Port and NT Port. Controls the Power Controller on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port slot. 0 = Turns On the Power Controller; requires some delay to be effective 1 = Turns Off the Power Controller	✔	
		Slot Status (Transparent Downstream Serial Hot Plug-Enabled Ports; Upstream Port Always Reads 0)		
	17	**Power Fault Detected** ***Reserved*** for the upstream Port and NT Port. 1 = Power Controller of the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port slot detected a Power Fault at the slot	✔	

Table 12-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
138h	**Power Budget Extended Capability Header (Upstream Port, and also the NT Port Link Interface)**			
	15:0	**PCI Express Extended Capability ID** Program to 0004h, as required by the *PCI Express Base r2.0*.	✔	
	19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.	✔	
	31:20	**Next Capability Offset** Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	✔	
13Ch	**Data Select (Upstream Port, and also the NT Port Link Interface)**			
	7:0	**Data Select** Indexes the Power Budget data reported, by way of eight upstream Port/NT Port Link Interface **Power Budget Data** registers, per Port, and selects the DWord of Power Budget data that appears in each **Power Budget Data** register. Index values start at 0, to select the first DWord of Power Budget data; subsequent DWords of Power Budget data are selected by increasing index values 1 to 7.	✔	

Table 12-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
140h	Power Budget Data (Upstream Port, and also the NT Port Link Interface)			
	7:0	**Base Power** Eight registers per upstream Port/NT Port Link Interface. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the field [9:8] (*Data Scale*) contents, to produce the actual power consumption value.	✔	
	9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The device power consumption is determined by multiplying the field [7:0] (*Base Power*) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	
	12:10	**PM Sub-State** 000b = Power Management sub-state of the operating condition being described	✔	
	14:13	**PM State** Power Management state of the operating condition being described. 00b = D0 Device PM state 11b = D3 Device PM state All other encodings are ***reserved***.	✔	
	17:15	**Type** Type of operating condition being described. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are ***reserved***.	✔	
	20:18	**Power Rail** Power Rail of the operating condition being described. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other encodings are ***reserved***.	✔	
	Note: *Eight registers, per upstream Port/NT Port Link Interface, can be programmed through the serial EEPROM, I^2C, and/or SMBus. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the* ***Data Select*** *register Data Select field (Upstream Port, and also the NT Port Link Interface, offset 13Ch[7:0]).*			

Table 12-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
144h		**Power Budget Capability (Upstream Port, and also the NT Port Link Interface)**		
	0	**System Allocated** 1 = Power budget for the device is included within the system power budget	✔	
1E0h		**Power Management Hot Plug User Configuration (All Ports)**		
	0	**L0s Entry Idle Counter** Traffic idle time to meet to enter the L0s Link PM state. 0 = Idle condition must last 1 µs 1 = Idle condition must last 4 µs	✔	
	2	**HPC PME Turn-Off Enable** Functionality associated with this bit is enabled only on the downstream Ports. 1 = PME Turn-Off Message is transmitted before the Port is turned Off on a downstream Port	✔	
	10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met	✔	

12.4 Power Management Tracking

Note: *NT Port Link Interface entry and exit to ASPM and Conventional PCI PM-compatible power states do not depend upon the Transparent upstream nor downstream Port power states or traffic. They are solely dependent upon the NT Port Link Interface's traffic conditions.*

Upstream Port logic tracks the Link status of each downstream and upstream Port Link, to derive the following conditions:

- Upstream Port enters the L0s Link PM state when all enabled downstream Receivers are in the L0s Link PM state or deeper, or in a Link Down state.
- Upstream Port enters the active L1 Link PM state, only when all downstream Ports are in the active L1 Link PM state or deeper, or the Link is down.
- When a downstream Port is in the active L1 Link PM state and an ASPM L1 Link PM state exit is occurring in the downstream Port, the upstream Port exits the L1 Link PM state.
- When the upstream Port is in the active L1 Link PM state and an active L1 Link PM state exit is occurring, due to Receiver Electrical Idle exit, the downstream Port exits the L1 Link PM state.
- When a PME_TO_Ack Message is received only on all active (not in Link Down) downstream Ports, a PME_TO_Ack Message is issued toward the upstream Port. The NT Port Virtual Interface is marked as being in the *DL_Down* state.
- When all downstream Ports are in the L2/L3 Ready Link PM or Link Down state, the upstream Port transmits PM_ENTER_L23 DLLPs toward the Root Complex.

12.5 Power Management Event Handler

PM_PME Messages are Posted Transaction Layer Packets (TLPs) that inform the PM software which agent within the PCI Express hierarchy has requested a PM-state change. PM_PME Messages are always routed toward the Root Complex.

PCI Express components are permitted to wake the system from any supported PM state, through the request of a PME.

When a PEX 8604 Transparent downstream Port is in the D3hot Device PM state, the following Hot Plug and/or PCI Express Hot Plug events cause the **PCI Power Management Status and Control** register *PME Status* bit (offset 44h[15]) to be Set:

- For Hot Plug-capable Transparent downstream Ports
  - Presence Detect Changed (logical OR of PRSNT# (I/O Expander PRSNT# input), and SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Attention Button Pressed
  - Power Fault Detected
  - MRL Sensor Changed
  - Command Completed
  - Link Bandwidth Management Status
  - Link Autonomous Bandwidth Status
- For non-Hot Plug-capable Transparent downstream Ports
  - Presence Detect Changed (SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Data Link Layer State Changed

This causes the downstream Port to generate a PM_PME Message, if the **PCI Power Management Status and Control** register *PME Enable* bit (offset 44h[8]) is Set.

*a. The SerDes Receiver Detect mechanism is comprised of the **Even/Odd Port Receiver Detect Status** register Receiver Detected on Lane x bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 200h[25:24], and Odd Ports, offset 204h[25:24]) or Hot Plug PRSNT# (from external I^2C I/O Expander) input for the Port.*

Chapter 13 Transparent Port Registers

13.1 Introduction

This chapter defines the PEX 8604 Transparent Port registers. Each PEX 8604 Port has its own Configuration, Capability, Control, and Status register space. The register mapping is the same for each Port. (Refer to Table 13-1.) This chapter also presents the PEX 8604 programmable registers and the order in which they appear in the register map. Register descriptions, when applicable, include details regarding their use and meaning in the upstream Port and downstream Ports. (Refer to Table 13-4.) Other registers are defined in:

- Chapter 15, "NT Port Virtual Interface Registers – NT Mode Only"
- Chapter 16, "NT Port Link Interface Registers – NT Mode Only"

Note: *For Chip-specific registers (those that exist only in Port 0), if Port 0 is a Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.*

All PEX 8604 registers can be accessed by Configuration or Memory Requests.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI-to-PCI Bridge r1.2*
- *PCI Express Base r2.0*
- *I^2C Bus v2.1*

13.2 Type 1 Port Register Map

Table 13-1 defines the Transparent mode Type 1 Port register mapping.

Table 13-1. Type 1 Port Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)			00h … 3Ch
		Capability Pointer (40h)	34h
	Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Capability Registers (Offsets 40h – 44h)			44h
	Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Capability Registers (Offsets 48h – 64h)			… 64h
	Next Capability Pointer (A4h)	Capability ID (10h)	68h
PCI Express Capability Registers (Offsets 68h – A0h)			… A0h
	Next Capability Pointer (00h)	SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)			… FCh
Next Capability Offset (FB4h)	1h	PCI Express Extended Capability ID (0003h)	100h
Device Serial Number Extended Capability Registers (Offsets 100h – 134h)			… 134h
Next Capability Offset (148h)	1h	PCI Express Extended Capability ID (0004h)	138h
Power Budget Extended Capability Registers (Offsets 138h – 144h)			… 144h
Next Capability Offset (448h, 950h, or 520h)	1h	PCI Express Extended Capability ID (0002h)	148h
Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)			… 1BCh

Table 13-1. Type 1 Port Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers (Offsets 1C0h – 51Ch)		1C0h … 51Ch
Next Capability Offset (950h or 520h)	1h / PCI Express Extended Capability ID (000Bh)	448h
Device-Specific Registers (Offsets 1C0h – 51Ch)		… 51Ch
Next Capability Offset (950h)	1h / PCI Express Extended Capability ID (000Dh)	520h
ACS Extended Capability Registers (Offsets 520h – 52Ch)		… 52Ch
Device-Specific Registers (Offsets 530h – F8Ch)		530h …
Next Capability Offset 2 (000h)	1h / PCI Express Extended Capability ID 2 (000Bh)	950h
Device-Specific Registers (Offsets 530h – F8Ch)		… F8Ch
Factory Test Only/Reserved		F90h – FB0h
Next Capability Offset (138h or 148h)	1h / PCI Express Extended Capability ID (0001h)	FB4h
Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)		… FDCh
Reserved		FE0h – FFCh

13.3 Port Register Configuration and Map

The PEX 8604 Port registers are configured similarly – not all the same. Port 0 includes more Device-Specific registers than the other Ports. Port 0 also contains registers that are used to set up and control the PEX 8604, as well as a serial EEPROM interface, I^2C Slave interface, and SMBus Slave interface logic and control. The Port registers contain setup and control information specific to each Port.

Table 13-2 defines the Port register configuration and map.

Table 13-2. Port Register Configuration and Map

Register Types	Port 0	Ports 1, 4, and 5
PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)	00h – 3Ch	00h – 3Ch
PCI Power Management Capability Registers (Offsets 40h – 44h)	40h – 44h	40h – 44h
MSI Capability Registers (Offsets 48h – 64h)	48h – 64h	48h – 64h
PCI Express Capability Registers (Offsets 68h – A0h)	68h – A0h	68h – A0h
Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)	A4h – FCh	A4h – FCh
Device Serial Number Extended Capability Registers (Offsets 100h – 134h)	100h – 134h	100h – 134h
Power Budget Extended Capability Registers (Offsets 138h – 144h)	Upstream Port 138h – 144h	
Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)	148h – 1BCh	148h – 1BCh
WRR Port Arbitration Table Registers (Offsets 1A8h – 1BCh)	When Weighted Round Robin (WRR) is enabled, the Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3; if the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0 1A8h – 1BCh	
Device-Specific Registers (Offsets 1C0h – 51Ch)		
Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)	1C0h – 1FCh	1E0h – 1ECh, 1F8h, 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)	200h – 25Ch	
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)	260h – 26Ch	
Device-Specific Registers – Miscellaneous Control (Offset 28Ch)	28Ch	
Device-Specific Registers – I^2C Slave Interface (Offsets 290h – 2C4h)	290h – 2C4h	
Device-Specific Registers – Bus Number CAM (Offsets 2C8h – 304h)	2C8h – 304h	
Device-Specific Registers – I/O CAM (Offsets 308h – 340h)	308h – 340h	
Device-Specific Registers – SMBus Slave Interface (Offset 344h)	344h	
Device-Specific Registers – Address-Mapping CAM (Offsets 348h – 444h)	348h – 444h	
Device-Specific Registers – Vendor-Specific Dual Cast Extended Capability (Offsets 448h – 51Ch)	448h – 51Ch	
ACS Extended Capability Registers (Offsets 520h – 52Ch)	520h – 52Ch	520h – 52Ch
Device-Specific Registers (Offsets 530h – F8Ch)		
Device-Specific Registers – Virtual Channel Weighted Round Robin Arbitration (Offsets 530h – 540h)	Upstream Port 530h – 540h	
Device-Specific Registers – Read Pacing (Offsets 544h – 554h)	Upstream Port 544h – 554h	

Table 13-2. Port Register Configuration and Map *(Cont.)*

Register Types	Port 0	Ports 1, 4, and 5
Device-Specific Registers – Port Configuration (Offsets 574h – 628h)	574h – 628h	
Device-Specific Registers – General-Purpose Input/Output (Offsets 62Ch – 65Ch)	62Ch – 65Ch	
Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)	660h – 67Ch	
Device-Specific Registers – IOCAM Base and Limit Upper 16 Bits (Offsets 680h – 6BCh)	680h – 6BCh	
Device-Specific Registers – Base Address Shadow (Offsets 6C0h – 73Ch)	6C0h – 73Ch	
Device-Specific Registers – Virtual Channel Resource Control Shadow (Offsets 740h – 83Ch)	740h – 83Ch	
Device-Specific Registers – Ingress Credit Handler Port Pool (Offsets 940h – 94Ch)	940h – 94Ch	
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)	950h – 95Ch	950h – 95Ch
Device-Specific Registers – ACS Extended Capability (Offsets 980h – 9FCh)	980h – 9FCh	
Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch)	A00h – B7Ch	
Device-Specific Registers – Physical Layer (Offsets B80h – C30h)	B80h – C30h	
Device-Specific Registers – Port Configuration Header (Offsets E00h – E3Ch)	E00h – E3Ch	
Device-Specific Registers – Physical Layer (Offsets E40h – EFCh)	E40h – EFCh	
Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F3Ch)	F00h – F3Ch	F10h
Device-Specific Registers – Error Reporting (Offsets F40h – F4Ch)	F40h – F4Ch	
Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)	F50h – F8Ch	
Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)	FB4h – FDCh	FB4h – FDCh

Table 13-3 lists registers that are generally individual registers that support all Ports (changing the register value in one Port changes the same register in all Ports), except for the NT Port Link Interface, which has its own copy (not duplicated in other Ports). Additional exceptions are also listed.

Table 13-3. Singular Registers Shared by Multiple Ports

Register Offset	Register Name	Comment
00h	Vendor ID and Device ID	
08h	PCI Class Code and Revision ID	NT Port Virtual Interface has its own register.
34h	Capability Pointer	
A4h	Subsystem Capability	NT Port Virtual Interface has its own register.
A8h	Subsystem Vendor ID and Subsystem ID	
100h	Device Serial Number Extended Capability Header	
104h	Serial Number (Lower DW)	
108h	Serial Number (Upper DW)	
520h	ACS Extended Capability Header	
950h	Vendor-Specific Extended Capability 2	NT Port Virtual Interface has its own register.
954h	Vendor-Specific Header 2	
958h	Hardwired Vendor ID and Hardwired Device ID	Shared by all Ports including the NT Port Link Interface.
95Ch	Hardwired Revision ID	Shared by all Ports including the NT Port Link Interface.

13.4 Register Access

Each PEX 8604 Port implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) comprise the PCI-compatible Configuration Space, and the upper 960 Dwords (offsets 100h through FFFh) comprise the PCI Express Extended Configuration Space. The PEX 8604 supports six mechanisms for accessing the Transparent Mode registers:

- PCI r3.0-Compatible Configuration Mechanism
- PCI Express Enhanced Configuration Access Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- I^2C Slave Interface (refer to Section 7.2, "I^2C Slave Interface")
- SMBus Slave Interface (refer to Section 7.3, "SMBus Slave Interface")
- Serial Peripheral Interface (SPI) Bus (refer to Chapter 6, "Serial EEPROM Controller")

The sideband register access mechanisms (serial EEPROM, I^2C, and/or SMBus) can modify Read-Only (RO) register values.

Each Port captures the Bus Number and Device Number on every Type 0 Configuration Write, as required by the *PCI r3.0*. Therefore, following a Fundamental Reset, software must initially perform a Configuration Write to each Port (using either the PCI r3.0-Compatible Configuration Mechanism or PCI Express Enhanced Configuration Access Mechanism), to allow each Port to capture its designated Bus Number and Device Number. The initial access to each Port, *for example*, could be a Configuration Write Request to a RO register, such as the **Device ID** / **Vendor ID** register (offset 00h).

13.4.1 *PCI r3.0*-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PEX 8604 Ports' first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration Space. The mechanism uses PCI Type 0 and Type 1 Configuration transactions to access the PEX 8604 Configuration registers. Each Port can convert a Type 1 Configuration Request (destined to a downstream Port or device) to a Type 0 Configuration Request (targeting the next downstream Port or device), as described below.

The PEX 8604 decodes all Type 1 Configuration accesses received on its upstream Port, when any of the following conditions exist:

- If the Bus Number in the Configuration access is not within the upstream Port's Secondary Bus Number and Subordinate Bus Number range, the PEX 8604 upstream Port responds with an Unsupported Request (UR).
- Specified Bus Number in the Configuration access is the PEX 8604 internal virtual PCI Bus Number, the PEX 8604 automatically converts the Type 1 Configuration access into the appropriate Type 0 Configuration access for the specified device.
  - If the specified device corresponds to the PCI-to-PCI bridge in one of the PEX 8604 downstream Ports, the PEX 8604 processes the Read or Write Request to the specified downstream Port register specified in the original Type 1 Configuration access.
  - If the specified Device Number does not correspond to any of the PEX 8604 downstream Port Device Numbers, the PEX 8604 responds with a UR.
- If the specified Bus Number in the Type 1 Configuration access is not the PEX 8604 internal virtual PCI Bus Number, but is the Bus Number of one of the PEX 8604 downstream Port secondary/subordinate buses, the PEX 8604 passes the Configuration access on to the PCI Express Link attached to that PEX 8604 downstream Port.
- If the specified Bus Number is the downstream Port Secondary Bus Number, and the specified Device Number is 0, the PEX 8604 converts the Type 1 Configuration access to a Type 0 Configuration access before passing it on.
  - If the specified Device Number is not 0, the downstream Port drops the Transaction Layer Packet (TLP) and generates a UR.
- If the specified Bus Number is not the downstream Port Secondary Bus Number, the PEX 8604 passes along the Type 1 Configuration access, without change.

Because the mechanism is limited to the first 256 bytes of the PCI Express Configuration Space of the PEX 8604 Ports, the PCI Express Enhanced Configuration Access Mechanism or Device-Specific Memory-Mapped Configuration Mechanism must be used to access beyond Byte FFh. The PCI Express Enhanced Configuration Access mechanism can access the registers in the PCI-compatible region, as well as those in the PCI Express Extended Configuration Space.

13.4.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism is implemented on all PCI Express PCs and on systems that do not implement a processor-specific firmware interface to the Configuration Space. The mechanism provides a Memory-Mapped Address space in the Root Complex, through which the Root Complex translates a Memory access into one or more Configuration Requests. Device drivers normally use an application programming interface (API) provided by the Operating System (OS), to use this mechanism.

The mechanism can be used to access all PEX 8604 registers.

13.4.3 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the Configuration registers of all Ports in a single 128-KB Memory map, as listed in Table 13-4. The registers of each Port are contained within a 4-KB range. The PEX 8604 supports a total of two to four simultaneously active Ports.

This mechanism follows the *PCI Express Base r2.0* Configuration Request Routing rules, which do not allow the propagation of Configuration Requests from downstream-to-upstream, nor peer-to-peer. By default, if any PEX 8604 downstream Port receives a Memory Request from a downstream device targeting the PEX 8604 Configuration registers, the Port:

- Responds to a Memory Read Request with a UR
- By default:
  - Silently discards a Memory Write Request (in compliance with the *PCI Express Base r2.0*)
    –or–
  - If the Port's **ECC Error Check Disable** register *Software Force Non-Posted Request* bit (offset 1C8h[3]) is Set, the Port responds with a UR

In Memory Requests that target PEX 8604 registers, the Payload Length indicated within the Memory Request Header must be 1 DWord. Lengths greater than 1 DWord result in a Completer Abort error.

To use this mechanism, program the upstream Port Type 1 Configuration Space **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively), which are typically enumerated at boot time by BIOS and/or the OS software. After the PEX 8604 upstream Port BARs are enumerated, Port 0 registers can be accessed with Memory Reads from and Writes to the first 4 KB (0000h to 0FFFh), Port 1 registers can be accessed with Memory Reads from and Writes to the second 4 KB (1000h to 1FFFh), and so forth. (Refer to Table 13-4.) Within each of these 4-KB windows, individual registers are located at the DWord offsets indicated in Table 13-1.

Upstream Port **BAR0** and **BAR1** are typically enumerated at boot time, by BIOS and/or the OS software. When upstream Port **BAR0** and **BAR1** are written (by serial EEPROM, I^2C Slave interface, and/or software), the PEX 8604 automatically copies the values into the Port 0 **BAR0** and **BAR1 Shadow** registers. (Refer to Table 13-38 for register mapping.) The particular registers used within this block depend upon which Port is the upstream Port.

If upstream Port **BAR0** and **BAR1** are enumerated by serial EEPROM, rather than by BIOS/OS, the serial EEPROM must be programmed to also load the same values to the corresponding **BAR0** and **BAR1 Shadow** registers.

Table 13-4. Register Offsets from Upstream Port BAR0/1 Base Address

Port Number	Internal Register 4-KB Memory Space Range	Location Range
Port 0	0000h to 0FFFh	0 to 4 KB
Port 1	1000h to 1FFFh	4 to 8 KB
Port 4	4000h to 4FFFh	16 to 20 KB
Port 5	5000h to 5FFFh	20 to 24 KB

13.5 Register Descriptions

The remainder of this chapter details the PEX 8604 registers, including:

- Bit/field names
- Description of register functions for the PEX 8604 upstream Port and downstream Ports
- Type (*such as* RW or HwInit; refer to Table 13-5 for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8604 serial EEPROM and/or I^2C/SMBus Initialization feature
- Default power-on/reset value

Table 13-5. Register Types, Grouped by User Accessibility

Type	Description
HwInit	**Hardware-Initialized** Refers to the PEX 8604 Hardware-Initialization mechanism or PEX 8604 Serial EEPROM or I^2C register Initialization features. RO after initialization and can only be reset with a Fundamental Reset. HwInit register bits are not modified by a Soft Reset.
RO	**Read-Only** Read-Only and cannot be altered by software. Permitted to be initialized by the PEX 8604 Hardware-Initialization mechanism or PEX 8604 serial EEPROM and/or I^2C register Initialization features.
ROS	**Read-Only, Sticky** Same as RO, except that bits are neither initialized nor modified by a Soft Reset.
RsvdP	***Reserved* and Preserved** ***Reserved*** for future RW implementations. Registers are RO and must return 0 when read. Software must preserve value read for Writes to bits.
RsvdZ	***Reserved* and Zero** ***Reserved*** for future RW1C implementations. Registers are RO and must return 0 when read. Software must use 0 for Writes to bits.
RW	**Read-Write** Read/Write and permitted to be Set or Cleared by software to the needed state.
RW1C	**Write 1 to Clear Status (Transparent mode)** Indicates status when read. A status bit Set by the system (to indicate status) is Cleared by writing 1 to that bit. Writing 0 has no effect. **Read-Write, Clear Interrupt (NT mode, Doorbell interrupts)** Indicates that a value of 1 Clears the interrupt.
RW1CS	**Write 1 to Clear, Sticky** Same as RW1C, except that bits are neither initialized nor modified by a Soft Reset.
RW1S	**Read-Write, Set Interrupt (NT mode, Doorbell interrupts)** Indicates that a value of 1 Sets the interrupt.
RWS	**Read-Write, Sticky** Same as RW, except that bits are Set or Cleared by software to the needed state. Bits are neither initialized nor modified by a Soft Reset.
RZ	**Software Read Zero** Software Read always returns 0; however, software is allowed to write this register.

13.6 PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the PCI-Compatible Type 1 Configuration Header registers. Table 13-6 defines the register map.

Table 13-6. PCI-Compatible Type 1 Configuration Header Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
PCI Class Code			PCI Revision ID	08h
PCI BIST ***(Not Supported)***	PCI Header Type	Master Latency Timer ***(Not Supported)***	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Secondary Latency Timer ***(Not Supported)***	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status	***Not Supported/Reserved***	I/O Limit	I/O Base	1Ch
Memory Limit		Memory Base		20h
Prefetchable Memory Limit		Prefetchable Memory Base		24h
Prefetchable Memory Upper Base Address				28h
Prefetchable Memory Upper Limit Address				2Ch
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		30h
Reserved			Capability Pointer (40h)	34h
Expansion ROM Base Address ***(Reserved)***				38h
Not Supported/Reserved	Bridge Control	PCI Interrupt Pin	PCI Interrupt Line	3Ch

Register 13-1. 00h PCI Configuration ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8604, if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	8604h

Register 13-2. 04h PCI Command/Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Command			
0	**I/O Access Enable** 0 = PEX 8604 ignores I/O Space accesses on the corresponding Port's primary interface 1 = PEX 8604 responds to I/O Space accesses on the corresponding Port's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8604 ignores Memory Space accesses on the corresponding Port's primary interface 1 = PEX 8604 responds to Memory Space accesses on the corresponding Port's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8604 Memory and I/O Request forwarding upstream. Neither affect Message (including INT*x* Interrupt Messages) forwarding nor Completions traveling upstream or downstream. 0 = PEX 8604 handles Memory and I/O Requests received on the corresponding Port downstream/secondary interface as Unsupported Requests (URs); for Non-Posted Requests, the PEX 8604 returns a Completion with UR Completion status. Because MSI Messages are in-band Memory Writes, disables MSI Messages as well. 1 = PEX 8604 forwards Memory and I/O Requests upstream.	RW	Yes	0
3	**Special Cycle Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
4	**Memory Write and Invalidate Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
5	**VGA Palette Snoop** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
6	**Parity Error Response Enable** Controls bit 24 (*Master Data Parity Error Detected*).	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0

Register 13-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**SERR# Enable** Controls bit 30 (*Signaled System Error*). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex, and, enables primary interface forwarding of ERR_FATAL and ERR_NONFATAL Messages from downstream Ports and devices when the Port's **Bridge Control** register *SERR# Enable* bit (offset 3Ch[17]) is Set	RW	Yes	0
9	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
10	**Interrupt Disable** 0 = Corresponding PEX 8604 Port is enabled to generate INT*x* Interrupt Messages and assert PEX_INTA# output 1 = Corresponding PEX 8604 Port is prevented from generating INT*x* Interrupt Messages and asserting PEX_INTA# output	RW	Yes	0
15:11	***Reserved***	RsvdP	No	0-0h

Register 13-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	PCI Status			
18:16	***Reserved***	RsvdP	No	000b
19	**Interrupt Status** 0 = No INT*x* Interrupt Message is pending 1 = INT*x* Interrupt Message is pending internally to the corresponding PEX 8604 Port –or– PEX_INTA# (if enabled) is asserted	RO	No	0
20	**Capability List** Capability function is supported. Set, as required by the *PCI Express Base r2.0*.	RO	Yes	1
21	**66 MHz Capable** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
24	**Master Data Parity Error Detected** If bit 6 (*Parity Error Response Enable*) is Set, the corresponding PEX 8604 Port Sets this bit when the Port: • Forwards the poisoned Transaction Layer Packet (TLP) Write Request from the secondary to the primary interface, –or– • Receives a Completion marked as poisoned on the primary interface If the *Parity Error Response Enable* bit is Cleared, the PEX 8604 never Sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	00b
27	**Signaled Target Abort** The upstream Port Sets this bit if one of the following conditions exist: • Upstream Port receives a Memory Request targeting a PEX 8604 register, and the Payload Length (indicated within the Memory Request Header) is greater than 1 DWord • Upstream Port receives a Memory Request targeting a PEX 8604 register address within a non-existent Port • Transparent downstream Port Sets this bit if it detects an Access Control Services (ACS) violation This error is reported by the **Uncorrectable Error Status** register *Completer Abort Status* bit (offset FB8h[15]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 13-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
28	**Received Target Abort** ***Reserved***	RsvdP	No	0
29	**Received Master Abort** ***Reserved***	RsvdP	No	0
30	**Signaled System Error** If bit 8 (*SERR# Enable*) is Set, the corresponding PEX 8604 Port Sets this bit when it transmits or forwards an ERR_FATAL or ERR_NONFATAL Message upstream. This error is natively reported by the **Device Status** register *Fatal Error Detected* and *Non-Fatal Error Detected* bits (offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	**Detected Parity Error** This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility. 1 = Corresponding Port received a Poisoned TLP on its primary side, regardless of the bit 6 (*Parity Error Response Enable*) state	RW1C	Yes	0

Register 13-3. 08h PCI Class Code and Revision ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Revision ID				
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the Silicon Revision (BAh), the PLX-assigned Revision ID for this version of the PEX 8604. The PEX 8604 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	BAh
PCI Class Code				**060400h**
15:8	**Register-Level Programming Interface** The PEX 8604 Ports support the *PCI-to-PCI Bridge r1.2* requirements, but not subtractive decoding, on their upstream interface.	RO	Yes	00h
23:16	**Sub-Class Code** PCI-to-PCI bridge.	RO	Yes	04h
31:24	**Base Class Code** Bridge device.	RO	Yes	06h

Register 13-4. 0Ch Miscellaneous Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Cache Line Size				
7:0	**Cache Line Size** System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8604 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	**Master Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00h
PCI Header Type				
22:16	**Configuration Layout Type** The corresponding PEX 8604 Port Configuration Space Header adheres to the Type 1 PCI-to-PCI Bridge Configuration Space layout defined by the *PCI-to-PCI Bridge r1.2*.	RO	No	01h
23	**Multi-Function Device** 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	No	0
PCI BIST				
31:24	**PCI BIST** ***Not supported*** Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

Register 13-5. 10h Base Address 0 (Upstream Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**Memory Space Indicator** 0 = Base Address register maps the PEX 8604 Configuration registers into Memory space ***Note:*** *The upstream Port is hardwired to 0.*	Upstream	RO	No	0
	Reserved	Downstream	RsvdP	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	Upstream	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
3	**Prefetchable** 0 = Base Address register maps the PEX 8604 Configuration registers into Non-Prefetchable Memory space ***Note:*** *The upstream Port is hardwired to 0.*	Upstream	RO	Yes	0
	Reserved	Downstream	RsvdP	No	0
16:4	***Reserved***		RsvdP	No	0-0h
31:17	**Base Address 0** Base Address (**BAR0**) for the Device-Specific Memory-Mapped Configuration mechanism.	Upstream	RW	Yes	0-0h
	Reserved	Downstream	RsvdP	No	0-0h

Register 13-6. 14h Base Address 1 (Upstream Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1** RO when the **Base Address 0** (**BAR0**) register is not enabled as a 64-bit BAR (*Memory Map Type* field (offset 10h[2:1]) is not programmed to 10b).	Upstream	RO	Yes	0000_0000h
	For 64-bit addressing (**BAR0/1**), Base Address 1 (**BAR1**) extends Base Address 0 (**BAR0**) to provide the upper 32 Address bits when the **Base Address 0** register *Memory Map Type* field (offset 10h[2:1]) is programmed to 10b.	Downstream	RW	Yes	0000_0000h

Register 13-7. 18h Bus Number (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Primary Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the PCI Bus segment to which the primary interface of this Port is connected. Set by Configuration software.	RW	Yes	00h
15:8	**Secondary Bus Number** Secondary Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the PCI Bus segment that is the secondary interface of this Port. Set by Configuration software.	RW	Yes	00h
23:16	**Subordinate Bus Number** Subordinate Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the highest numbered PCI Bus segment that is subordinate to this Port. Set by Configuration software.	RW	Yes	00h
31:24	**Secondary Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	00h

Register 13-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *If ISA Addressing mode is enabled (**PCI Command** register I/O Access Enable bit, offset 04h[0], is Set), the PEX 8604 Port forwards I/O transactions from its primary interface to its secondary interface (downstream) if an I/O address is within the range defined by the **I/O Base** and **I/O Limit** registers when the Base is less than or equal to the Limit.* *Conversely, the PEX 8604 Port forwards I/O transactions from its secondary interface to its primary interface (upstream) if an I/O address is outside this Address range. If the PEX 8604 Port does not implement an I/O Address range, the Port forwards all I/O transactions on its secondary interface upstream, to its primary interface.*				
I/O Base				
3:0	**I/O Base Addressing Capability** 1h = 32-bit I/O Address decoding is supported All other encodings are ***reserved***.	RO	Yes	1h
7:4	**I/O_BAR[15:12]** I/O Base Address[15:12]. The PEX 8604 Ports use their **I/O Base** and **I/O Limit** registers to determine the address range of I/O transactions to forward from one interface to the other. I/O Base Address[15:12] bits specify the corresponding PEX 8604 Port I/O Base Address[15:12]. The PEX 8604 assumes I/O Base Address[11:0]=000h. For 16-bit I/O addressing, the PEX 8604 assumes Address[31:16]=0000h. For 32-bit addressing, the PEX 8604 decodes Address[31:0], and uses the **I/O Upper Base and Limit Address** register *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits* fields (offset 30h[15:0 and 31:16], respectively).	RW	Yes	Fh
I/O Limit				
11:8	**I/O Limit Addressing Capability** 1h = 32-bit I/O Address decoding is supported All other encodings are ***reserved***.	RO	Yes	1h
15:12	**I/O_Limit[15:12]** I/O Limit Address[15:12]. The PEX 8604 Ports use their **I/O Base** and **I/O Limit** registers to determine the Address range of I/O transactions to forward from one interface to the other. I/O Limit Address[15:12] bits specify the corresponding PEX 8604 Port I/O Limit Address[15:12]. The PEX 8604 assumes Address bits [11:0] of the I/O Limit Address are FFFh. For 16-bit I/O addressing, the PEX 8604 decodes Address bits [15:0] and assumes Address bits [31:16] of the I/O Limit Address are 0000h. For 32-bit addressing, the PEX 8604 decodes Address bits [31:0], and uses the **I/O Upper Base and Limit Address** register *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits* fields (offset 30h[15:0 and 31:16], respectively). If the I/O Limit Address is less than the I/O Base Address, the PEX 8604 does not forward I/O transactions from the corresponding Port primary/upstream bus to its secondary/downstream bus. However, the PEX 8604 forwards all I/O transactions from the secondary bus of the corresponding Port to its primary bus.	RW	Yes	0h

Register 13-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Secondary Status			
20:16	***Reserved***	RsvdP	No	0-0h
21	**66 MHz Capable** ***Not supported*** 0 = Not enabled, because PCI Express does ***not support*** 66 MHz	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Reserved*** Not enabled, because PCI Express does ***not support*** this function.	RsvdP	No	0
24	**Master Data Parity Error** If the **Bridge Control** register *Parity Error Response Enable* bit (offset 3Ch[16]) is Set, the corresponding PEX 8604 Port Sets this bit when transmitting or receiving a TLP on its downstream side, and when either of the following two conditions occur: • Port receives Completion marked poisoned • Port forwards poisoned TLP Write Request If the *Parity Error Response Enable* bit is Cleared, the PEX 8604 never Sets this bit. These errors are reported by the Port's **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), and mirrored to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00b
27	**Signaled Target Abort** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
28	**Received Target Abort** Cleared, as required by the *PCI Express Base r2.0*, because the PEX 8604 never initiates a Request itself.	RsvdP	No	0
29	**Received Master Abort** Cleared, as required by the *PCI Express Base r2.0*, because the PEX 8604 never initiates a Request itself.	RsvdP	No	0
30	**Received System Error** 1 = Downstream Port received an ERR_FATAL or ERR_NONFATAL Message on its secondary interface from a downstream device	RW1C	Yes	0
31	**Detected Parity Error** 1 = Downstream Port received a poisoned TLP from a downstream device, regardless of the **Bridge Control** register *Parity Error Response Enable* bit (offset 3Ch[16]) state	RW1C	Yes	0

Register 13-9. 20h Memory Base and Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The PEX 8604 Port forwards Memory transactions from its primary interface to its secondary interface (downstream) if a Memory address is within the range defined by the* ***Memory Base*** *and* ***Memory Limit*** *registers (when the Base is less than or equal to the Limit).* *Conversely, the PEX 8604 Port forwards Memory transactions from its secondary interface to its primary interface (upstream) if a Memory address is outside this Address range (provided that the address is not within the range defined by the* ***Prefetchable Memory Base*** *(offsets 28h + 24h[15:0]) and* ***Prefetchable Memory Limit*** *(offsets 2Ch + 24h[31:16]) registers).*			
Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**MEM_BAR[31:20]** Memory Base Address[31:20]. Specifies the corresponding PEX 8604 Port Non-Prefetchable Memory Base Address[31:20]. The PEX 8604 assumes Memory Base Address[19:0]=0_0000h.	RW	Yes	FFFh
Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**MEM_Limit[31:20]** Memory Limit Address[31:20]. Specifies the corresponding PEX 8604 Port Non-Prefetchable Memory Limit Address[31:20]. The PEX 8604 assumes Memory Limit Address[19:0]=F_FFFFh.	RW	Yes	000h

Register 13-10. 24h Prefetchable Memory Base and Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *The PEX 8604 Port forwards Memory transactions from its primary interface to its secondary interface (downstream) if a Memory address is within the range defined by the* ***Prefetchable Memory Base*** *(offsets 28h + 24h[15:0]) and* ***Prefetchable Memory Limit*** *(offsets 2Ch + 24h[31:16]) registers (when the Base is less than or equal to the Limit).* *Conversely, the PEX 8604 Port forwards Memory transactions from its secondary interface to its primary interface (upstream) if a Memory address is outside this Address range (provided that the address is not within the range defined by the* ***Memory Base*** *and* ***Memory Limit*** *registers (offset 20h)).*				
Prefetchable Memory Base				
0	**Prefetchable Memory Base Capability** 0 = Corresponding PEX 8604 Port supports 32-bit Prefetchable Memory Addressing 1 = Corresponding PEX 8604 Port defaults to 64-bit Prefetchable Memory Addressing support, as required by the *PCI Express Base r2.0* ***Note:*** *If the application needs 32-bit only Prefetchable space, the serial EEPROM and/or I^2C must Clear both this bit and bit 16 (Prefetchable Memory Limit Capability).*	RO	Yes	1
3:1	***Reserved***	RsvdP	No	000b
15:4	**PMEM_BAR[31:20]** Prefetchable Memory Base Address[31:20]. Specifies the corresponding PEX 8604 Port Prefetchable Memory Base Address[31:20]. The PEX 8604 assumes Prefetchable Memory Base Address[19:0]=0_0000h.	RW	Yes	FFFh
Prefetchable Memory Limit				
16	**Prefetchable Memory Limit Capability** 0 = Corresponding PEX 8604 Port supports 32-bit Prefetchable Memory Addressing 1 = Corresponding PEX 8604 Port defaults to 64-bit Prefetchable Memory Addressing support, as required by the *PCI Express Base r2.0*	RO	Yes	1
19:17	***Reserved***	RsvdP	No	000b
31:20	**PMEM_Limit[31:20]** Prefetchable Memory Limit Address[31:20]. Specifies the corresponding PEX 8604 Port Prefetchable Memory Limit Address[31:20]. The PEX 8604 assumes Prefetchable Memory Limit Address[19:0]=F_FFFFh.	RW	Yes	000h

Register 13-11. 28h Prefetchable Memory Upper Base Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
31:0	**PBUP[63:32]** Prefetchable Memory Base Address[63:32]. The PEX 8604 uses this register for Prefetchable Memory Upper Base Address[63:32]. When the **Prefetchable Memory Base** register *Prefetchable Memory Base Capability* field indicates 32-bit addressing, this register is RO and returns 0000_0000h.	Offset 24h[0]=1	RW	Yes	0000_0000h
		Offset 24h[0]=0	RO	No	0000_0000h

Register 13-12. 2Ch Prefetchable Memory Upper Limit Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
31:0	**PLIMUP[63:32]** Prefetchable Memory Limit Address[63:32]. The PEX 8604 uses this register for Prefetchable Memory Upper Limit Address[63:32]. When the **Prefetchable Memory Limit** register *Prefetchable Memory Limit Capability* field indicates 32-bit addressing, this register is RO and returns 0000_0000h. ***Note:*** *The serial EEPROM must not write a non-zero value into this register when the RO attribute is Set for this register.*	Offset 24h[16]=1	RW	Yes	0000_0000h
		Offset 24h[16]=0	RO	No	0000_0000h

Register 13-13. 30h I/O Upper Base and Limit Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
15:0	**I/O Base Upper 16 Bits** The PEX 8604 uses this register for I/O Base Address[31:16]. When the **I/O Base** register *I/O Base Addressing Capability* field indicates 16-bit addressing, this register is RO and returns 0000h.	Offset 1Ch[3:0]=1h	RW	Yes	0000h
		Offset 1Ch[3:0]=0h	RO	No	0000h
31:16	**I/O Limit Upper 16 Bits** The PEX 8604 uses this register for I/O Limit Address[31:16]. When the **I/O Limit** register *I/O Limit Addressing Capability* field indicates 16-bit addressing, this register is RO and returns 0000h. ***Note:*** *The serial EEPROM must not write a non-zero value into this register when the RO attribute is Set for this register.*	Offset 1Ch[11:8]=1h	RW	Yes	0000h
		Offset 1Ch[11:8]=0h	RO	No	0000h

Register 13-14. 34h Capability Pointer (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability Pointer** Default 40h points to the **PCI Power Management Capability** structure.	RO	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-15. 38h Expansion ROM Base Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Expansion ROM Base Address** ***Reserved***	RsvdP	No	0000_0000h

Register 13-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Interrupt Line				
7:0	**Interrupt Line Routing Value** The PEX 8604 does ***not*** use this register; however, the register is included for operating system and device driver use.	RW	Yes	00h
PCI Interrupt Pin				
15:8	**Interrupt Pin** Identifies the Conventional PCI Interrupt Message(s) that the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8604. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
Bridge Control				
16	**Parity Error Response Enable** Controls the response to Poisoned TLPs. 0 = Disables the **Secondary Status** register *Master Data Parity Error* bit (offset 1Ch[24]) 1 = Enables the **Secondary Status** register *Master Data Parity Error* bit (offset 1Ch[24])	RW	Yes	0
17	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command** register *SERR# Enable* bit (offset 04h[8]) is Set, enables the **PCI Status** register *Signaled System Error* bit (offset 04h[30]).	RW	Yes	0
18	**ISA Enable** Modifies the PEX 8604's response to ISA I/O addresses enabled by the **I/O Base** and **I/O Limit** registers (offset 1Ch[7:0 and 15:8], respectively) and located in the first 64 KB of the PCI I/O Address space (0000_0000h to 0000_FFFFh). The default state of this bit after reset is 0. 0 = If ISA Addressing mode is enabled (**PCI Command** register *I/O Access Enable* bit, offset 04h[0], is Set), the PEX 8604 Port forwards I/O Requests within the Address range defined by the **I/O Base** and **I/O Limit** registers. 1 = PEX 8604 blocks forwarding from the primary to secondary interface, of I/O transactions addressing the last 768 bytes in each 1-KB block of the Port's I/O Address range. In the opposite direction (secondary to primary), if I/O Addressing mode is enabled, the PEX 8604 Port forwards I/O transactions that address the last 768 bytes in each 1-KB block of the Port's I/O Address range. ***Note:*** *Refer also to the **Ingress Control** register Disable VGA BIOS Memory Access Decoding bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 660h[28]).*	RW	Yes	0

Register 13-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
19	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 18 (*ISA Enable*) Setting VGA address forwarding is qualified by the **PCI Command** register *Memory Access Enable* and *I/O Access Enable* bits (offset 04h[1:0], respectively). The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *Memory Access Enable* and *I/O Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit ***Notes:*** *When Set in an egress Port, the Port is configured as a non-Cut-Thru path. (Refer to Section 2.1.3.2, "Cut-Thru," for further details.)* *Refer also to the **Ingress Control** register Disable VGA BIOS Memory Access Decoding bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 660h[28]).* ***Conventional PCI VGA support** – To avoid potential I/O address conflicts, if the VGA Enable bit is Set in the upstream Port and a downstream Port, Set the **PCI Command** register I/O Access Enable bit (offset 04h[0]) in the remaining downstream Ports, unless those downstream Ports are configured to use default 32-bit address decoding and their I/O Address range is Set above 1_0000h.*	RW	Yes	0

Register 13-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20	**VGA 16-Bit Decode Enable** Used only when bit 19 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses ***Note:*** *Refer also to the* ***Ingress Control*** *register Disable VGA BIOS Memory Access Decoding bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 660h[28]).*	RW	Yes	0
21	**Master Abort Mode** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
22	**Secondary Bus Reset** 1 = Causes a Hot Reset on the corresponding PEX 8604 Port downstream Link	RW	Yes	0
23	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
24	**Primary Discard Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
25	**Secondary Discard Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
26	**Discard Timer Status** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
27	**Discard Timer SERR# Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
31:28	***Reserved***	RsvdP	No	0h

13.7 PCI Power Management Capability Registers (Offsets 40h – 44h)

This section details the PCI Power Management Capability registers. Table 13-7 defines the register map.

Table 13-7. PCI Power Management Capability Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions ***(Reserved)***	PCI Power Management Status and Control		44h

Register 13-17. 40h PCI Power Management Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability ID** Program to 01h, to indicate that the Capability structure is the **PCI Power Management Capability** structure.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	RO	Yes	48h
18:16	**Version** Default 011b indicates compliance with the *PCI Power Mgmt. r1.2.*	RO	Yes	011b
19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.	RsvdP	No	0
20	***Reserved***	RsvdP	No	0
21	**Device-Specific Initialization** 0 = Device-Specific Initialization is ***not*** required	RO	Yes	0
24:22	**AUX Current** The PEX 8604 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.	RO	Yes	000b
25	**D1 Support** ***Not supported*** 0 = PEX 8604 does ***not support*** the D1 Device PM state	RsvdP	No	0
26	**D2 Support** ***Not supported*** 0 = PEX 8604 does ***not support*** the D2 Device PM state	RsvdP	No	0
31:27	**PME Support** Bits [31, 30, and 27] must be Set, to indicate that the PEX 8604 will forward PME Messages, as required by the *PCI Express Base r2.0*.	RO	Yes	19h

Register 13-18. 44h PCI Power Management Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Power Management Status and Control				
1:0	**Power State** Used to determine the current Device PM state of the Port, and to program the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	RO	Yes	1
7:4	***Reserved***	RsvdP	No	0h
8	**PME Enable** 0 = Disables PME generation by the corresponding PEX 8604 Port[a] 1 = Enables PME generation by the corresponding PEX 8604 Port	RWS	No	0
12:9	**Data Select** Initially writable by serial EEPROM and/or I²C only[b]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I²C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	RO	Yes	0h
14:13	**Data Scale** Writable by serial EEPROM and/or I²C only[b]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h, and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h.	RO	Yes	00b
15	**PME Status** 0 = PME is not generated by the corresponding PEX 8604 Port[a] 1 = PME is being generated by the corresponding PEX 8604 Port	RW1CS	No	0

Register 13-18. 44h PCI Power Management Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Power Management Control/Status Bridge Extensions				
21:16	***Reserved***	RsvdP	No	0-0h
22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
PCI Power Management Data				
31:24	**Data** Writable by serial EEPROM and/or I^2C only[b]. There are four supported *Data Select* values (0h, 3h, 4h, and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	RO	Yes	00h

a. Because the PEX 8604 does not consume auxiliary power, this bit is not sticky, and is always Cleared at power-on reset.

*b. With no serial EEPROM nor previous I^2C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

13.8 MSI Capability Registers (Offsets 48h – 64h)

This section details the Message Signaled Interrupt (MSI) Capability registers. Table 13-8 defines the register map.

Table 13-8. MSI Capability Register Map (All Ports)[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
MSI Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address				4Ch
MSI Upper Address				50h
Reserved		MSI Data		54h
MSI Mask				58h
MSI Status				5Ch
Reserved				60h – 64h

*a. Offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*

Register 13-19. 48h MSI Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
MSI Capability Header				
7:0	**Capability ID** Program to 05h, as required by the *PCI r3.0*.	RO	Yes	05h
15:8	**Next Capability Pointer** Program to 68h, to point to the **PCI Express Capability** structure.	RO	Yes	68h
MSI Control				
16	**MSI Enable** 0 = MSIs for the corresponding Port are disabled 1 = MSIs for the corresponding Port are enabled, and INT*x* Interrupt Messages and PEX_INTA# output assertion are disabled	RW	Yes	0
19:17	**Multiple Message Capable** 000b = PEX 8604 Port can request only one Vector 001b = PEX 8604 Port can request two Vectors 010b through 111b = PEX 8604 Port can request four Vectors	RO	Yes	010b
22:20	**Multiple Message Enable** 000b = PEX 8604 Port is allocated one Vector, by default 001b = PEX 8604 Port is allocated two Vectors 010b through 111b = PEX 8604 Port is allocated four Vectors ***Note:*** *This field should not be programmed with a value larger than that of field [19:17] (Multiple Message Capable). If the value of this field is larger than that of field [19:17], the Multiple Message Capable value takes effect.*	RW	Yes	000b
23	**MSI 64-Bit Address Capable** 0 = PEX 8604 is capable of generating MSI 32-bit addresses (**MSI Address** register, offset 4Ch, is the Message address) 1 = PEX 8604 is capable of generating MSI 64-bit addresses (**MSI Address** register, offset 4Ch, is the lower 32 bits of the Message address, and **MSI Upper Address** register, offset 50h, is the upper 32 bits of the Message address)	RO	Yes	1
24	**Per Vector Masking Capable** 0 = PEX 8604 does not have Per Vector Masking capability 1 = PEX 8604 has Per Vector Masking capability	RO	Yes	1
31:25	***Reserved***	RsvdP	No	0-0h

Register 13-20. 4Ch MSI Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
1:0	***Reserved***	RsvdP	No	00b
31:2	**Message Address** ***Note:*** *Refer to register offset 50h for MSI Upper Address, if offset 48h[23] is Set (default).*	RW	Yes	0-0h

Register 13-21. 50h MSI Upper Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**Message Upper Address** This register is valid/used only when the **MSI Control** register *MSI 64-Bit Address Capable* bit (offset 48h[23]) is Set. MSI Write transaction upper address[63:32]. ***Note:*** *Refer to register offset 4Ch for MSI Address.*	RW	Yes	0000_0000h

Register 13-22. 54h MSI Data (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
Note: *The offset for this register changes from 54h, to 50h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*				
15:0	**Message Data** MSI Write transaction TLP payload.	RW	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-23. 58h MSI Mask (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
The interrupt sources in a PEX 8604 Port are grouped into four categories – Power Management/Hot Plug or Link State events, Device-Specific errors, GPIO-generated interrupts, and NT-Virtual Doorbell-generated interrupts. The quantity of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the quantity of MSI Vectors that can be requested is: • **Four** – Each interrupt category generates its own MSI Vector • **Two** – Device-Specific errors generate their own MSI Vector, while all other categories are combined and generate the same Vector • **One** – All interrupt categories generate the same MSI Vector NT-Virtual Doorbell interrupts are generated only on the NT Port. The Type is the same, regardless of whether it is for a Transparent or NT Port. ***Notes:*** *The offset for this register changes from 58h, to 54h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be used to mask their respective **MSI Status** register bits (offset 5Ch).*					
0	**MSI Mask for Power Management, or Hot Plug or Link State, Events** MSI mask for Power Management event- or Hot Plug or Link State event-generated interrupts.	Offset 48h[22:20]≥010b	RW	Yes	0
	MSI Mask for Shared Interrupt Sources MSI mask for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	Offset 48h[22:20]≤001b	RW	Yes	0
1	**MSI Mask for Device-Specific Errors** MSI mask for Device-Specific error-generated interrupts.	Offset 48h[22:20]≥001b	RW	Yes	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0
2	**MSI Mask for GPIO-Generated Interrupts**	Offset 48h[22:20]≥010b	RW	Yes	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
3	**MSI Mask for NT-Virtual Doorbell-Generated Interrupts** ***This bit is valid only in NT mode.*** Refer to the NT Port registers located at offsets C4Ch through C58h.	Offset 48h[22:20]≥010b	RW	Yes	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
31:4	***Reserved***		RsvdP	No	0000_000h

Register 13-24. 5Ch MSI Status (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
The interrupt sources in a PEX 8604 Port are grouped into four categories – Power Management/Hot Plug or Link State events, Device-Specific errors, GPIO-generated interrupts, and NT-Virtual Doorbell-generated interrupts. The quantity of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the quantity of MSI Vectors that can be requested is: • **Four** – Each interrupt generates its own MSI Vector • **Two** – Device-Specific errors generate their own MSI Vector, while all other categories are combined and generate the same Vector • **One** – All interrupt categories generate the same MSI Vector NT-Virtual Doorbell interrupts are generated only on the NT Port. The Type is the same, regardless of whether it is for a Transparent or NT Port. ***Notes:*** *The offset for this register changes from 5Ch, to 58h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be masked by their respective **MSI Mask** register bits (offset 58h).*					
0	**MSI Pending Status for Power Management, or Hot Plug or Link State, Events** MSI pending status for Power Management event- or Hot Plug or Link State event-generated interrupts.	Offset 48h[22:20]≥010b	RO	Yes	0
	MSI Pending Status for Shared Interrupt Sources MSI pending status for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	Offset 48h[22:20]≤001b	RO	Yes	0
1	**MSI Pending Status for Device-Specific Errors** MSI pending status for Device-Specific error-generated interrupts.	Offset 48h[22:20]≥001b	RO	Yes	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0
2	**MSI Pending Status for GPIO-Generated Interrupts**	Offset 48h[22:20]≥010b	RO	Yes	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
3	**MSI Pending Status for NT-Virtual Doorbell-Generated Interrupts** ***This bit is valid only in NT mode.*** Refer to the NT Port registers located at offsets C4Ch through C58h.	Offset 48h[22:20]≥010b	RO	Yes	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
31:4	***Reserved***		RsvdP	No	0000_000h

13.9 PCI Express Capability Registers (Offsets 68h – A0h)

This section details the PCI Express Capability registers. Hot Plug Capability, Command, Status, and Events are included in these registers. Table 13-9 defines the register map.

Table 13-9. PCI Express Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capability		Next Capability Pointer (A4h)	Capability ID (10h)	68h
Device Capability				6Ch
Device Status		***Not Supported/Reserved***	Device Control	70h
Link Capability				74h
Link Status		Link Control		78h
Reserved (Upstream) Slot Capability (Downstream)				7Ch
Reserved (Upstream)				80h
Slot Status (Downstream)		Slot Control (Downstream)		
Reserved				84h – 88h
Device Capability 2				8Ch
Device Status 2 ***(Reserved)***		Device Control 2		90h
Reserved				94h
Link Status 2		Link Control 2		98h
Reserved				9Ch – A0h

Register 13-25. 68h PCI Express Capability List and Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
PCI Express Capability List					
7:0	**Capability ID** Program to 10h, as required by the *PCI Express Base r2.0.*		RO	Yes	10h
15:8	**Next Capability Pointer** Program to A4h, to point to the **Subsystem Capability** structure.		RO	Yes	A4h
PCI Express Capability					
19:16	**Capability Version** The PEX 8604 Ports program this field to 2h, as required by the *PCI Express Base r2.0.*		RO	Yes	2h
23:20	**Device/Port Type** Set at reset, as required by the *PCI Express Base r2.0.*	Upstream	RO	Yes	5h
		Downstream	RO	Yes	6h
24	**Slot Implemented** 0 = Disables or connects to the upstream Port	Upstream	RsvdP	No	0
	0 = Disables or connects to an integrated component 1 = Indicates that the downstream Port connects to a slot, as opposed to being connected to an integrated component or being disabled ***Note:*** *The PEX 8604 serial EEPROM register Initialization capability and/or and/or I^2C can be used to Clear this bit, indicating that the corresponding PEX 8604 downstream Port connects to an integrated component or is disabled.*	Downstream	RO	Yes	1
29:25	**Interrupt Message Number** The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.		RO	Yes	00_000b
31:30	***Reserved***		RsvdP	No	00b

Register 13-26. 6Ch Device Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
2:0	**Maximum Payload Size Supported** Maximum Payload Size Port limitations are as follows: Because there are x1 and x2 Ports in the Port configuration, the Maximum Payload Size for each Port is limited to 512 bytes. 000b = PEX 8604 Port supports a 128-byte maximum payload 001b = PEX 8604 Port supports a 256-byte maximum payload 010b = PEX 8604 Port supports a 512-byte maximum payload No other encodings are supported.		HwInit	Yes	010b
4:3	**Phantom Functions Supported** ***Not supported***		RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum *Tag* field is 5 bits 1 = Maximum *Tag* field is 8 bits		RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** ***Not supported*** Because the PEX 8604 is a switch and not an endpoint, the PEX 8604 does ***not support*** this feature. 000b = Disables the capability		RO	Yes	000b
11:9	**Endpoint L1 Acceptable Latency** ***Not supported*** Because the PEX 8604 is a switch and not an endpoint, the PEX 8604 does ***not support*** this feature. 000b = Disables the capability		RO	Yes	000b
14:12	***Reserved***, as required by the *PCI Express Base r2.0*.		RsvdP	No	000b
15	**Role-Based Error Reporting**		RO	Yes	1

Register 13-26. 6Ch Device Capability (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
17:16	***Reserved***		RsvdP	No	00b
25:18	**Captured Slot Power Limit Value** For the PEX 8604 upstream Port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	Upstream	RO	Yes	00h
	Not valid	Downstream	RsvdP	No	00h
27:26	**Captured Slot Power Limit Scale** For the PEX 8604 upstream Port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	Upstream	RO	Yes	00b
	Not valid	Downstream	RsvdP	No	00b
31:28	***Reserved***		RsvdP	No	0h

Register 13-27. 70h Device Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Device Control			
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8604 Port to report Correctable errors	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8604 Port to report Non-Fatal errors	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8604 Port to report Fatal errors	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8604 Port to report UR errors	RW	Yes	0
4	**Enable Relaxed Ordering** ***Not supported***	RsvdP	No	0
7:5	**Maximum Payload Size** Software can change this field to configure the PEX 8604 Ports to support other Payload Sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capability** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]). 000b = PEX 8604 Port supports a 128-byte maximum payload 001b = PEX 8604 Port supports a 256-byte maximum payload 010b = PEX 8604 Port supports a 512-byte maximum payload No other encodings are supported.	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported***	RsvdP	No	0
9	**Phantom Functions Enable** ***Not supported***	RsvdP	No	0
10	**AUX Power PM Enable** ***Not supported***	RsvdP	No	0
11	**Enable No Snoop** ***Not supported***	RsvdP	No	0
14:12	**Max Read Request Size** ***Not supported***	RsvdP	No	000b
15	***Reserved*** Hardwired to 0, as required by the *PCI Express Base r2.0*.	RsvdP	No	0

Register 13-27. 70h Device Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Device Status			
16	**Correctable Error Detected** Set when the corresponding Port detects a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable*) state. 0 = Corresponding PEX 8604 Port did not detect a Correctable error 1 = Corresponding PEX 8604 Port detected a Correctable error	RW1C	Yes	0
17	**Non-Fatal Error Detected** Set when the corresponding Port detects a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable*) state. 0 = Corresponding PEX 8604 Port did not detect a Non-Fatal error 1 = Corresponding PEX 8604 Port detected a Non-Fatal error	RW1C	Yes	0
18	**Fatal Error Detected** Set when the corresponding Port detects a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable*) state. 0 = Corresponding PEX 8604 Port did not detect a Fatal error 1 = Corresponding PEX 8604 Port detected a Fatal error	RW1C	Yes	0
19	**Unsupported Request Detected** Set when the corresponding Port detects a UR, regardless of the bit 3 (*Unsupported Request Reporting Enable*) state. 0 = Corresponding PEX 8604 Port did not detect a UR 1 = Corresponding PEX 8604 Port detected a UR	RW1C	Yes	0
20	**AUX Power Detected** ***Not supported***	RsvdP	No	0
21	**Transactions Pending** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 13-28. 74h Link Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
3:0	**Supported Link Speeds** Indicates the Port's supported Link speed. 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s and 2.5 GT/s Link speeds are supported All other encodings are ***reserved***.		RO	Yes	0010b (STRAP_RESERVED17#=H) 0001b (STRAP_RESERVED17#=L)
9:4	**Maximum Link Width** The PEX 8604 maximum Link width is x2 = 00_0010b. Valid widths are x1 or x2. Actual maximum Link width is Set by the STRAP_PORTCFG[1:0] inputs. 00_0000b = ***Reserved*** 00_0001b = x1 00_0010b = x2 All other encodings are ***not supported***.		ROS	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.		RO	Yes	11b

Register 13-28. 74h Link Capability (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the **Common Physical Layer Command/Status** register *N_FTS Value* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 238h[15:8]) value and Link speed. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = Corresponding PEX 8604 Port L0s Link PM state Exit Latency is 512 ns to less than 1 µs at 5.0 GT/s 101b = Corresponding PEX 8604 Port L0s Link PM state Exit Latency is 1 µs to less than 2 µs at 2.5 GT/s All other encodings are ***reserved***.		RO	No	100b (5.0 GT/s) 101b (2.5 GT/s)
17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = Corresponding PEX 8604 Port L1 Link PM state Exit Latency is 1 µs to less than 2 µs at 5.0 GT/s 010b = Corresponding PEX 8604 Port L1 Link PM state Exit Latency is 2 µs to less than 4 µs at 2.5 GT/s All other encodings are ***reserved***.		RO	Yes	001b (5.0 GT/s) 010b (2.5 GT/s)
18	**Clock Power Management Capable**		RO	Yes	0
19	***Reserved*** This bit must be hardwired to 0, for the upstream Port and components that do not support this optional capability.	Upstream	RsvdP	No	0
	Surprise Down Error Reporting Capable Must be Set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. If this bit is Cleared, the **Uncorrectable Error Status** register *Surprise Down Error Status* bit (offset FB8h[5]) is disabled. ***Note:*** *If this bit is Set and later Cleared at runtime (such as by I²C), it must be Cleared while the Link is up; otherwise, if the Link is down when this bit is Cleared, a subsequent Surprise Down error event is not masked.*	Downstream	RO	Yes	1

Register 13-28. 74h Link Capability (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	Data Link Layer Link Active Reporting Capable Valid for downstream Ports only.	Downstream	RO	Yes	1
21	***Reserved*** Hardwired to 0, as required by the *PCI Express Base r2.0*.	Upstream	RsvdP	No	0
	Link Bandwidth Notification Capability 1 = Indicates support for the Link Bandwidth Notification status and interrupt mechanisms	Downstream	RO	Yes	1
23:22	***Reserved***		RsvdP	No	00b
31:24	**Port Number** The Port Number is defined by the STRAP_PORTCFG[1:0] input Strapping options. (Refer to Table 13-10. Encodings not listed are ***reserved***.) Available Port Numbers are 0, 1, 4, and 5.		ROS	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])

Table 13-10. Port Configurations

STRAP_PORTCFG[1:0]	Port 0	Port 1	Port 4	Port 5
(default) 00b	**x1**	**x1**	**x1**	**x1**
01b	**x2**	**x1**		**x1**
10b	**x2**	**x2**		

Register 13-29. 78h Link Status and Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Link Control					
1:0	**Active State Power Management (ASPM)** 00b = Disable[a] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries		RW	Yes	00b
2	***Reserved***		RsvdP	No	0
3	**Read Request Return Parameter Control** Read Request Return Parameter "R" control. Read Completion Boundary (RCB). Cleared, as required by the *PCI Express Base r2.0.*		RO	Yes	0
4	***Not valid***	Upstream	RsvdP	No	0
	Link Disable 1 = Places the Link on the corresponding PEX 8604 downstream Port to the *Disabled* Link Training state	Downstream	RW	Yes	0
5	***Not valid*** Always read as 0.	Upstream	RsvdP	No	0
	Retrain Link For PEX 8604 Ports, always returns 0 when read; however, software is allowed to write this register. Writing 1 to this bit causes the corresponding PEX 8604 downstream Port to initiate retraining of its PCI Express Link.	Downstream	RZ	Yes	0
6	**Common Clock Configuration** 0 = Port and the device at the other end of the Port's PCI Express Link use an asynchronous Reference Clock source 1 = Port and the device at the other end of the Port's PCI Express Link use a common (synchronous) Reference Clock source (constant phase relationship)		RW	Yes	0
7	**Extended Sync** When Set, causes the Port to transmit: • 4,096 FTS Ordered-Sets in the L0s Link PM state, • Followed by a single SKIP Ordered-Set prior to entering the L0 Link PM state, • Finally, transmission of 1,024 TS1 Ordered-Sets in the *Recovery* state.		RW	Yes	0

Register 13-29. 78h Link Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
8	**Clock Power Management Enable** ***Reserved*** Read and Writable only when the **Link Capability** register *Clock Power Management Capable* bit is Set. The PEX 8604 does ***not support*** removal of the Reference Clock in the L1 and L2/L3 Ready Link PM states.		RsvdP	No	0
9	**Hardware-Autonomous Width Disable** ***Reserved***		RsvdP	No	0
10	***Reserved***	Upstream	RsvdP	No	0
	Link Bandwidth Management Interrupt Enable 0 = Disables interrupt generation 1 = Enables generation of an interrupt, to indicate that the **Link Status** register *Link Bandwidth Management Status* bit (offset 78h[30]) has been Set	Downstream	RW	Yes	0
11	***Reserved***	Upstream	RsvdP	No	0
	Link Autonomous Bandwidth Interrupt Enable 0 = Disables interrupt generation 1 = Enables generation of an interrupt, to indicate that the **Link Status** register *Link Autonomous Bandwidth Status* bit (offset 78h[31]) has been Set	Downstream	RW	Yes	0
15:12	***Reserved***		RsvdP	No	0h
	Link Status				
19:16	**Current Link Speed** Indicates the negotiated Link speed of the Port's PCI Express Link. 0001b = 2.5 GT/s Link speed 0010b = 5.0 GT/s Link speed All other encodings are ***reserved***. The value in this field is undefined when the Link is not up.		RO	No	0001b
25:20	**Negotiated Link Width** Dependent upon the physical Port configuration. Link width is determined by the negotiated value with the attached Lane/Port. 00_0000b = Link is down (default) 00_0001b = x1 or Port is in the *DL_Down* state 00_0010b = x2 All other encodings are ***not supported***.		RO	No	00_0000b
26	***Reserved***		RsvdP	No	0
27	***Reserved***	Upstream	RsvdP	No	0
	Link Training 1 = Indicates that the corresponding PEX 8604 downstream Port requested Link training, and the Link training is in-progress or about to start	Downstream	RO	No	0

Register 13-29. 78h Link Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
28	**Slot Clock Configuration** 0 = Indicates that the PEX 8604 uses an independent clock 1 = Indicates that the PEX 8604 uses the same physical Reference Clock that the platform provides on the connector		HwInit	Yes	0
29	***Reserved***	Upstream	RsvdP	No	0
	Data Link Layer Link Active When Set, and the **Link Capability** register *Data Link Layer Link Active Reporting Capable* bit (offset 74h[20]) is also Set, indicates the following: • Data Link Layer (DLL) is in the *DL_Active* state • Link is operational • Flow Control (FC) Initialization has successfully completed	Downstream	RO	Yes	0
30	***Reserved***	Upstream	RsvdP	No	0
	Link Bandwidth Management Status Set by hardware to indicate that either of the following has occurred, without the Port transitioning through DL_Down status: • Link retraining has completed following a Write of 1 to the **Link Control** register *Retrain Link* bit (offset 78h[5]) • Hardware has changed Link speed or width, to attempt to correct unreliable Link operation, either through an Link Training and Status State Machine (LTSSM) timeout or higher-level process	Downstream	RW1C	Yes	0
31	***Reserved***	Upstream	RsvdP	No	0
	Link Autonomous Bandwidth Status Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation.	Downstream	RW1C	Yes	0

a. The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.

Register 13-30. 7Ch Slot Capability (Downstream Ports; Upstream Port Always Reads 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Notes: For bits [6, 4:0], the default values are shown to be 1 for downstream Ports, which is true only if the Port is Parallel and/or Serial Hot Plug-capable; otherwise, the default value is 0. This also applies to bit 17 for Serial Hot Plug Ports. Serial Hot Plug-capable means that the PEX 8604 has detected that an external I^2C I/O Expander is present.					
	Reserved	Upstream	RsvdP	No	0
0	**Attention Button Present** 0 = Attention Button is not implemented 1 = Attention Button is implemented on the slot chassis of the corresponding PEX 8604 Transparent downstream Port with an I^2C I/O Expander	Downstream	RO	Yes	1
	Reserved	Upstream	RsvdP	No	0
1	**Power Controller Present** 0 = Power Controller is not implemented. The Hot Plug Controller is disabled for that slot and a power-up sequence is not executed. The slot remains in the disabled state. 1 = Power Controller is implemented for the slot of the corresponding PEX 8604 Transparent downstream Port with an I^2C I/O Expander. The Controller powers up the slot when the Manually operated Retention Latch (MRL) is closed and the **Slot Control** register *Power Controller Control* bit (offset 80h[10]) is Cleared. Otherwise, if bit 2 (*MRL Sensor Present*) is disabled (Cleared), the MRL's position has no effect on powering up the slot.	Downstream	RO	Yes	1
	Reserved	Upstream	RsvdP	No	0
2	**MRL Sensor Present** 0 = MRL Sensor is not implemented. MRL position is "Don't Care" for that slot. 1 = MRL Sensor is implemented on the slot chassis of the corresponding PEX 8604 Transparent downstream Port with an I^2C I/O Expander. The PEX 8604 senses whether the MRL is open or closed for a slot. MRL should be Low for power-on for that slot.	Downstream	RO	Yes	1
	Reserved	Upstream	RsvdP	No	0
3	**Attention Indicator Present** 0 = Attention Indicator is not implemented 1 = Attention Indicator is implemented on the slot chassis of the corresponding PEX 8604 Transparent downstream Port with an I^2C I/O Expander	Downstream	RO	Yes	1

Register 13-30. 7Ch Slot Capability
(Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
4	***Reserved***	Upstream	RsvdP	No	0
	Power Indicator Present 0 = Power Indicator is not implemented 1 = Power Indicator is implemented on the slot chassis of the corresponding PEX 8604 Transparent downstream Port with an I²C I/O Expander	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	Hot Plug Surprise 0 = No device in the corresponding PEX 8604 downstream Port (with an I²C I/O Expander) slot is removed from the system without prior notification 1 = Device in the corresponding PEX 8604 downstream Port slot can be removed from the system without prior notification	Downstream	RO	Yes	0
6	***Reserved***	Upstream	RsvdP	No	0
	Hot Plug Capable 0 = Corresponding PEX 8604 downstream Port slot is not capable of supporting Hot Plug operations 1 = Corresponding PEX 8604 Transparent downstream Port (with an I²C I/O Expander) slot is capable of supporting Hot Plug operations	Downstream	RO	Yes	1
14:7	***Reserved***	Upstream	RsvdP	No	00h
	Slot Power Limit Value The maximum power supplied by the corresponding PEX 8604 downstream slot is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the field [16:15] (*Slot Power Limit Scale*) value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I²C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.	Downstream	RO	Yes	19h

Register 13-30. 7Ch Slot Capability
(Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
16:15	***Reserved***	Upstream	RsvdP	No	00b
	Slot Power Limit Scale The maximum power supplied by the corresponding PEX 8604 downstream slot is determined by multiplying the value in this field by the field [14:7] (*Slot Power Limit Value*) value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I²C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	Downstream	RO	Yes	00b
17	***Reserved***	Upstream; Downstream non-Serial Hot Plug-enabled	RsvdP	No	0
	Electromechanical Interlock Present This bit is valid for Serial Hot Plug Ports that have an I/O Expander. 0 = Electromechanical Interlock is not implemented on the chassis for this slot 1 = Electromechanical Interlock is implemented on the chassis for this slot	Downstream Serial Hot Plug-enabled	RO	Yes	0
18	**No Command Completed Support** ***Reserved***		RsvdP	No	0
31:19	***Reserved***	Upstream	RsvdP	No	0-0h
	Physical Slot Number Indicates the physical Slot Number attached to this Port. If the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default), this field must be hardware-initialized to a value that assigns a Slot Number that is unique within the chassis, regardless of the form factor associated with the slot. Must be initialized to 0h for Ports connected to devices that are integrated on the system board.	Downstream	RO	Yes	0-0h

Bit(s)	Description/Function
22:19	Port Numbers 0, 1, 4, and 5
26:23	Loaded from I²C I/O Expander
31:27	***Reserved***

Register 13-31. 80h Slot Status and Control (Transparent Downstream Serial Hot Plug-Enabled Ports; Upstream Port Always Reads 0)

Bit(s)	Description		Ports	Type	Serial EEPROM and I^2C	Default
Slot Control						
Note: *To change the values of the MRL Sensor Changed Enable (bit 2), Power Fault Detector Enable (bit 1), and/or Attention Button Pressed Enable (bit 0) bits, the corresponding bit(s) in the **Slot Capability** register (offset 7Ch[2:0], respectively) must be Set first.*						
0	***Reserved***		Upstream	RsvdP	No	0
	Attention Button Pressed Enable 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0]. are both Set), for an Attention Button Pressed event on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port	Offset 7Ch[0]=0	Downstream	RO	No	0
		Offset 7Ch[0]=1	Downstream	RW	Yes	0
1	***Reserved***		Upstream	RsvdP	No	0
	Power Fault Detector Enable 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), for a Power Fault Detected event on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port	Offset 7Ch[1]=0	Downstream	RO	No	0
		Offset 7Ch[1]=1	Downstream	RW	Yes	0

Register 13-31. 80h Slot Status and Control
(Transparent Downstream Serial Hot Plug-Enabled Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description		Ports	Type	Serial EEPROM and I^2C	Default
2	***Reserved***		Upstream	RsvdP	No	0
	MRL Sensor Changed Enable 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), for an MRL Sensor Changed event on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port	Offset 7Ch[2]=0	Downstream	RO	No	0
		Offset 7Ch[2]=1	Downstream	RW	Yes	0
3	***Not valid***		Upstream	RsvdP	No	0
	Presence Detect Changed Enable A Presence Detect Changed event is triggered by either the SerDes Receiver Detect (**Even/Odd Port Receiver Detect Status** register *Receiver Detected on Lane x* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 200h[25:24], and Odd Ports, offset 204h[25:24])) or Hot Plug PRSNT# input (from external I^2C I/O Expander) on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port. 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), for a Presence Detect Changed event on the corresponding PEX 8604 downstream Port		Downstream	RW	Yes	0

Register 13-31. 80h Slot Status and Control
(Transparent Downstream Serial Hot Plug-Enabled Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
4	***Reserved***	Upstream	RsvdP	No	0
	Command Completed Interrupt Enable 0 = Function is disabled 1 = Enables software notification with an interrupt when a command is completed by the Serial Hot Plug Controller on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port	Downstream	RW	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Hot Plug Interrupt Enable 0 = Function is disabled 1 = Enables an interrupt on enabled Hot Plug/Link State events for the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port	Downstream	RW	Yes	0
7:6	***Reserved***	Upstream	RsvdP	No	00b
	Attention Indicator Control Controls the Attention Indicator on the corresponding PEX 8604 downstream Port slot. Reads return the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port Attention Indicator's current state. Writing a non-zero value triggers a Command Completed event (even if the value written is the same as the existing value). Writing 00b preserves the current value and does not trigger a Command Completed event. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator	Downstream	RW	Yes	11b

Register 13-31. 80h Slot Status and Control (Transparent Downstream Serial Hot Plug-Enabled Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
	Reserved	Upstream	RsvdP	No	00b
9:8	**Power Indicator Control** Controls the Power Indicator on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port slot. Reads return the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port Power Indicator's current state. Writing a non-zero value triggers a Command Completed event (even if the value written is the same as the existing value). Writing 00b preserves the current value and does not trigger a Command Completed event. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator	Downstream	RW	Yes	11b (MRL open) 01b (MRL closed)
	Reserved	Upstream	RsvdP	No	0
10	**Power Controller Control** Controls the Power Controller on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port slot. 0 = Turns On the Power Controller; requires some delay to be effective 1 = Turns Off the Power Controller	Downstream	RW	Yes	1 (MRL open) 0 (MRL closed)
	Reserved	Upstream; Downstream non-Serial Hot Plug-enabled	RsvdP	No	0
11	**Electromechanical Interlock Control** This bit is valid for Serial Hot Plug Ports that have an I/O Expander. If an Electromechanical Interlock is implemented, writing 1 to this bit causes the state of the interlock to toggle. A Write of 0 to this bit has no effect. A Read of this bit always returns 0.	Downstream Serial Hot Plug-enabled	RW	Yes	0
	Not valid	Upstream	RsvdP	No	0
12	**Data Link Layer State Changed Enable** Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), when the **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]) is changed.	Downstream	RW	Yes	0
15:13	***Reserved***		RsvdP	No	000b

Register 13-31. 80h Slot Status and Control
(Transparent Downstream Serial Hot Plug-Enabled Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Slot Status					
16	***Reserved***	Upstream	RsvdP	No	0
	Attention Button Pressed 1 = Attention Button of the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port slot was pressed	Downstream	RW1C	Yes	0
17	***Reserved***	Upstream	RsvdP	No	0
	Power Fault Detected 1 = Power Controller of the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port slot detected a Power Fault at the slot	Downstream	RW1C	Yes	0
18	***Reserved***	Upstream	RsvdP	No	0
	MRL Sensor Changed 1 = MRL Sensor state change was detected on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port slot	Downstream	RW1C	Yes	0
19	***Reserved***	Upstream	RsvdP	No	0
	Presence Detect Changed A Presence Detect Changed event is triggered by either the SerDes Receiver Detect (**Even/Odd Port Receiver Detect Status** register *Receiver Detected on Lane x* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 200h[25:24], and Odd Ports, offset 204h[25:24])) or Hot Plug PRSNT# input (from external I^2C I/O Expander) on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port. Write 1 to Clear. 1 = Value reported in bit 22 (*Presence Detect State*) changed	Downstream	RW1C	Yes	0

Register 13-31. 80h Slot Status and Control (Transparent Downstream Serial Hot Plug-Enabled Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	Command Completed 1 = Serial Hot Plug Controller on the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port slot completed an issued command to: • *Attention Indicator Control* (field [7:6]) • *Power Indicator Control* (field [9:8]) • *Power Controller Control* (bit 10) • *Electromechanical Interlock Control* (bit 11) (Serial Hot Plug-enabled Ports only)	Downstream	RW1C	Yes	0
21	***Reserved***	Upstream; Downstream non-Serial Hot Plug-enabled	RsvdP	No	0
	MRL Sensor State Reveals the corresponding PEX 8604 Serial Hot Plug-capable Transparent downstream Port MRL Sensor's current state. 0 = MRL Sensor is closed 1 = MRL Sensor is open	Downstream Serial Hot Plug-enabled	RO	No	0
22	***Not valid***	Upstream	RsvdP	No	0
	Presence Detect State For downstream Ports that implement slots, indicates the presence of an adapter in the slot, reflected by the logical OR of the corresponding downstream Port's SerDes Receiver Detect (**Even/Odd Port Receiver Detect Status** register *Receiver Detected on Lane x* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 200h[25:24], and Odd Ports, offset 204h[25:24])), and, if present, the PRSNT# input on the external I/O Expander for the Serial Hot Plug-enabled Port. Hardwired to 1 when the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) value is 0. 0 = Slot is empty, or device is not present 1 = Slot is occupied, or device is present	Downstream, Offset 68h[24]=1	RO	No	0
		Downstream, Offset 68h[24]=0	RO	No	1
23	***Reserved***	Upstream; Downstream non-Serial Hot Plug-enabled	RsvdP	No	0
	Electromechanical Interlock Status This bit is valid for Serial Hot Plug Ports that have an I/O Expander. When an Electromechanical Interlock is implemented, indicates the Electromechanical Interlock's current status. 0 = Electromechanical Interlock is disengaged 1 = Electromechanical Interlock is engaged	Downstream Serial Hot Plug-enabled	RW1C	Yes	0

Register 13-31. 80h Slot Status and Control (Transparent Downstream Serial Hot Plug-Enabled Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
24	***Not valid***	Upstream	RsvdP	No	0
	Data Link Layer State Changed In response to a Data Link Layer State Changed event, software must read the **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]), to determine whether the Link is active before initiating Configuration Requests to the device. 1 = Value reported in the **Link Status** register *Data Link Layer Link Active* bit changed	Downstream	RW1C	Yes	0
31:25	***Reserved***		RsvdZ	No	0-0h

Register 13-32. 8Ch Device Capability 2 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
4:0	***Reserved***		RsvdP	No	0-0h
5	***Reserved***	Upstream	RsvdP	No	0
	ARI Forwarding Supported 0 = Alternative Routing-ID Interpretation (ARI) forwarding is not supported 1 = ARI forwarding is supported	Downstream	RO	Yes	1
31:6	***Reserved***		RsvdP	No	0-0h

Register 13-33. 90h Device Status and Control 2 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Device Control 2					
4:0	***Reserved***		RsvdP	No	0-0h
5	***Reserved***	Upstream	RsvdP	No	0
	ARI Forwarding Enable 0 = Disabled 1 = Enabled; Downstream Port disables its traditional Device Number field from being forced to 0 when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to extended functions in an ARI device immediately below the Port	Downstream	RW	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Status 2					
31:16	***Reserved***		RsvdP	No	0-0h

Register 13-34. 98h Link Status and Control 2 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Link Control 2					
3:0	**Target Link Speed** 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s Link speed is supported All other encodings are ***reserved***.		RWS	Yes	0010b
4	**Enter Compliance**		RWS	Yes	0
5	**Hardware Autonomous Speed Disable** ***Reserved*** Initial transition to the highest supported common Link speed is not blocked by this bit.		RsvdP	No	0
6	***Not valid***	Upstream	RsvdP	Yes	0
	Selectable De-Emphasis Selects the standard de-emphasis level when the Link is operating at 5.0 GT/s. When the Link is operating at 2.5 GT/s, the Setting of this bit has no effect (de-emphasis at 2.5 GT/s is -3.5 dB). 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB (Link is operating at 2.5 GT/s)	Downstream	HwInit	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
9:7	**Transmit Margin** Intended for debug and compliance testing only.	Upstream	RWS	Yes	000b
	Reserved	Downstream	RsvdP	Yes	0
10	**Enter Modified Compliance** Intended for debug and compliance testing only. Valid only for Function 0 of the upstream Port.	Upstream	RWS	Yes	0
	Reserved	Downstream	RsvdP	Yes	0
11	**Compliance SOS** 1 = LTSSM must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern	Upstream	RWS	Yes	0
	Reserved	Downstream	RsvdP	Yes	0
12	**Compliance De-Emphasis** Sets the de-emphasis level in the *Polling.Compliance* state, if the entry occurred due to bit 4 (*Enter Compliance*) being Set.	Upstream	RWS	Yes	0
	Reserved	Downstream	RsvdP	Yes	0
15:13	***Reserved***		RsvdP	No	000b

Register 13-34. 98h Link Status and Control 2 (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Link Status 2					
16	**Current De-Emphasis Level** Reflects the de-emphasis level. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB (Link is operating at 2.5 GT/s)		RO	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
31:17	***Reserved***		RsvdP	No	0-0h

13.10 Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)

This section details the Subsystem ID and Subsystem Vendor ID Capability registers. Table 13-11 defines the register map.

Table 13-11. Subsystem ID and Subsystem Vendor ID Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Reserved	Next Capability Pointer (00h)	SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID	Subsystem Vendor ID		A8h
Reserved			ACh – FCh

Register 13-35. A4h Subsystem Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**SSID/SSVID Capability ID** Detects the SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the *PCI-to-PCI Bridge r1.2*.	RO	Yes	0Dh
15:8	**Next Capability Pointer** 00h = This capability is the last capability in the PEX 8604 Port's Capabilities list The PEX 8604 Extended Capabilities list starts at offset 100h.	RO	Yes	00h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-36. A8h Subsystem ID and Subsystem Vendor ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**Subsystem Vendor ID** The Vendor ID (offset 00h[15:0]) identifies the manufacturer of the PEX 8604, and the Subsystem Vendor ID optionally identifies the board or system vendor. As with the Vendor ID value, the Subsystem Vendor ID value must be a valid PCI-SIG-assigned Vendor ID. The value of this field is usually identical for all PEX 8604 Ports.	RO	Yes	10B5h
31:16	**Subsystem ID** The Device ID (offset 00h[31:16]) identifies the PEX 8604, and optionally the Subsystem ID in combination with the Subsystem Vendor ID, uniquely identifies the board or system. The value of this field is usually identical for all PEX 8604 Ports, and is chosen or assigned only by the "owner" of the valid Vendor ID value used for the Subsystem Vendor ID. If the board or system vendor is not a PCI-SIG member, PLX can assign, free of charge, a unique Subsystem ID value, in which case the Subsystem Vendor ID remains the PLX default value, 10B5h.	RO	Yes	8604h

13.11 Device Serial Number Extended Capability Registers (Offsets 100h – 134h)

This section details the Device Serial Number Extended Capability registers. Table 13-12 defines the register map.

Table 13-12. Device Serial Number Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h)	Capability Version (1h) / PCI Express Extended Capability ID (0003h)	100h
Serial Number (Lower DW)		104h
Serial Number (Upper DW)		108h
Reserved		10Ch – 134h

Register 13-37. 100h Device Serial Number Extended Capability Header (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID** Program to 0003h, as required by the *PCI Express Base r2.0*.	RO	Yes	0003h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.	RO	Yes	1h
31:20	**Next Capability Offset** Program to FB4h, which addresses the **Advanced Error Reporting Extended Capability** structure.	RO	Yes	FB4h

Register 13-38. 104h Serial Number (Lower DW) (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**PCI Express Device Serial Number (1st DW)** Lower half of a 64-bit register. Value programmed by Serial EEPROM register initialization. Per the *PCI Express Base r2.0*, all switch PEX 8604 Ports must contain the same value; therefore, one physical register is shared by all PEX 8604 Ports. (Refer to Table 13-3.) The Serial Number registers contain the IEEE-defined 64-bit Extended Unique Identifier (EUI-64™). The lower 24 bits are the Company ID value assigned by the IEEE registration authority, and the upper 40 bits are the Extension ID assigned by the identified Company.	RO	Yes	B5DF_0E00h

Register 13-39. 108h Serial Number (Upper DW) (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**PCI Express Device Serial Number (2nd DW)** Upper half of a 64-bit register. Value programmed by Serial EEPROM register initialization. Per the *PCI Express Base r2.0*, all switch Ports must contain the same value; therefore, one physical register is shared by all PEX 8604 Ports. (Refer to Table 13-3.) The Serial Number registers contain the IEEE-defined 64-bit Extended Unique Identifier (EUI-64™). The lower 24 bits are the Company ID value assigned by the IEEE registration authority, and the upper 40 bits are the Extension ID assigned by the identified Company.	RO	Yes	BA_8601_10h

13.12 Power Budget Extended Capability Registers (Offsets 138h – 144h)

This section details the Power Budget Extended Capability registers. These registers work differently than the others, especially with respect to serial EEPROM Reads and Writes. *For example*, when writing to Index 5 of the upstream Port/NT Port Link Interface **Power Budget Data** register (offset 140h), write 5 into the upstream Port/NT Port Link Interface **Data Select** register *Data Select* field (offset 13Ch[7:0]), then write the value into the upstream Port/NT Port Link Interface **Power Budget Data** register. Table 13-13 defines the register map.

Table 13-13. Power Budget Extended Capability Register Map (Upstream Port, and also the NT Port Link Interface)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Next Capability Offset (148h)	Capability Version (1h)	PCI Express Extended Capability ID (0004h)		138h
Reserved			Data Select	13Ch
Power Budget Data				140h
Power Budget Capability				144h

Register 13-40. 138h Power Budget Extended Capability Header (Upstream Port, and also the NT Port Link Interface)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID** Program to 0004h, as required by the *PCI Express Base r2.0*.	Upstream	RO	Yes	0004h
	Reserved	Downstream	RsvdP	No	0000h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.	Upstream	RO	Yes	1h
	Reserved	Downstream	RsvdP	No	0h
31:20	**Next Capability Offset** Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	Upstream	RO	Yes	148h
	Reserved	Downstream	RsvdP	No	000h

Register 13-41. 13Ch Data Select (Upstream Port, and also the NT Port Link Interface)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
7:0	**Data Select** Indexes the Power Budget data reported, by way of eight upstream Port/NT Port Link Interface **Power Budget Data** registers, per Port, and selects the DWord of Power Budget data that appears in each **Power Budget Data** register. Index values start at 0, to select the first DWord of Power Budget data; subsequent DWords of Power Budget data are selected by increasing index values 1 to 7.	Upstream	RW	Yes	00h
	Reserved	Downstream	RsvdP	No	00h
31:8	***Reserved***		RsvdP	No	0000_00h

Register 13-42. 140h Power Budget Data (Upstream Port, and also the NT Port Link Interface)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *Eight registers per upstream Port/NT Port Link Interface can be programmed, through the serial EEPROM, I²C, and/or SMBus. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the **Data Select** register Data Select field (Upstream Port, and also the NT Port Link Interface, offset 13Ch[7:0]).*					
7:0	**Base Power** Eight registers per upstream Port/NT Port Link Interface. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the field [9:8] (*Data Scale*) contents, to produce the actual power consumption value.	Upstream	RO	Yes	00h
	Reserved	Downstream	RsvdP	No	00h
9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The device power consumption is determined by multiplying the field [7:0] (*Base Power*) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	Upstream	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
12:10	**PM Sub-State** 000b = Power Management sub-state of the operating condition being described	Upstream	RO	Yes	000b
	Reserved	Downstream	RsvdP	No	000b

Register 13-42. 140h Power Budget Data (Upstream Port, and also the NT Port Link Interface) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
14:13	**PM State** Power Management state of the operating condition being described. 00b = D0 Device PM state 11b = D3 Device PM state All other encodings are ***reserved***.	Upstream	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
17:15	**Type** Type of operating condition being described. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are ***reserved***.	Upstream	RO	Yes	000b
	Reserved	Downstream	RsvdP	No	000b
20:18	**Power Rail** Power Rail of the operating condition being described. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other encodings are ***reserved***.	Upstream	RO	Yes	000b
	Reserved	Downstream	RsvdP	No	000b
31:21	***Reserved***		RsvdP	No	0-0h

Register 13-43. 144h Power Budget Capability (Upstream Port, and also the NT Port Link Interface)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**System Allocated** 1 = Power budget for the device is included within the system power budget	Upstream	HwInit	Yes	1
	Reserved	Downstream	RsvdP	No	0
31:1	***Reserved***		RsvdP	No	0-0h

13.13 Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)

This section details the Virtual Channel Extended Capability registers, which are duplicated for each Port. Table 13-14 defines the register map for one Port.

Table 13-14. Virtual Channel Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (448h, 950h, or 520h) / Capability Version (1h)	PCI Express Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2		150h
Port VC Status ***(Reserved)***	Port VC Control	154h
VC0 Resource Capability		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
VC1 Resource Capability		164h
VC1 Resource Control		168h
VC1 Resource Status	***Reserved***	16Ch
Reserved	170h –	1A4h
WRR Port Arbitration Table Registers (Offsets 1A8h – 1BCh)		1A8h … 1BCh

Register 13-44. 148h Virtual Channel Extended Capability Header (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID** Program to 0002h, as required by the *PCI Express Base r2.0*.		RO	No	0002h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.		RO	No	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability** structure, offset 448h.	Port 0 is the upstream Port	RO	No	448h
	Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset 950h.	Port 0 is the NT Port	RO	No	950h
	Next extended capability is the **ACS Extended Capability** structure, offset 520h.	Otherwise	RO	No	520h

Register 13-45. 14Ch Port VC Capability 1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
2:0	**Extended VC Counter** 000b = PEX 8604 Port supports only the default Virtual Channel (VC0) 001b = PEX 8604 Port supports **one** extended Virtual Channel (VC1) All other encodings are ***reserved***.	RO	Yes	001b
3	***Reserved***	RsvdP	No	0
6:4	**Low-Priority Extended VC Counter** For Strict Priority arbitration, indicates the quantity of extended Virtual Channels (VCs) (those in addition to the default, VC0) that belong to the Low-Priority VC group for this PEX 8604 Port. Both VC0 and VC1 are assigned to the Low-Priority Virtual Channel group, by default. 000b = For this PEX 8604 Port, only the default VC, VC0, belongs to the Low-Priority Virtual Channel group. VC1 has higher priority than VC0. 001b = For this PEX 8604 Port, both VC0 and VC1 belong to the Low-Priority Virtual Channel group. All other encodings are ***reserved***.	RO	Yes	001b
7	***Reserved***	RsvdP	No	0
9:8	**Reference Clock** ***Reserved***	RsvdP	No	00b
11:10	**Port Arbitration Table Entry Size** 10b = Port Arbitration Table entry size is 4 bits	RO	Yes	10b
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-46. 150h Port VC Capability 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**VC Arbitration Capability** Indicates the type of VC arbitration supported by the device for the LPVC (Low-Priority Extended VC) group. 0 = Indicates that the Round-Robin (Hardware-Fixed) Arbitration scheme is not supported 1 = Indicates that the Round-Robin (Hardware-Fixed) Arbitration scheme is supported	RO	Yes	1
31:1	***Reserved***	RsvdP	No	0-0h

Register 13-47. 154h Port VC Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Port VC Control			
0	**Load VC Arbitration Table** ***Not supported*** Writing 1 updates the Port's VC Arbitration Table. Reads always return 0.	RsvdP	No	0
3:1	**VC Arbitration Select** Selects the Port's VC arbitration type, as per the supported arbitration type indicated by the **Port VC Capability 2** register *VC Arbitration Capability* bit (offset 150h[0]) value. 000b = Bit 0; Round-Robin (Hardware-Fixed) arbitration scheme All other encodings are ***reserved***.	RW	Yes	000b
15:4	***Reserved***	RsvdP	No	000h
	Port VC Status			
16	**VC Arbitration Table Status** ***Reserved***	RsvdP	No	0
31:17	***Reserved***	RsvdP	No	0-0h

Register 13-48. 158h VC0 Resource Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	**Port Arbitration Capability** When WRR is enabled, the Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3; if the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. Bit 0 = 1 – Non-configurable Round-Robin (Hardware-Fixed) Arbitration Bit 1 = 1 – Weighted Round-Robin (WRR) arbitration with 32 Phases	RO RO	No No	10b 01b
14:2	***Reserved***	RsvdP	No	0-0h
15	**Reject Snoop Transactions** Not a PCI Express switch feature; therefore, this bit is Cleared.	RsvdP	No	0
22:16	**Maximum Time Slots** ***Reserved***	RsvdP	No	000_0000b
23	***Reserved***	RsvdP	No	0
31:24	**Port Arbitration Table Offset** Offset of the Port Arbitration Table, as the quantity of DQWords from the Base address of the **Virtual Channel Extended Capability** structure. (Refer to Section 13.13.1 for further details.) When WRR is enabled, the Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3; if the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. 00h = Non-configurable Round-Robin (Hardware-Fixed) Arbitration 06h = Weighted Round-Robin (WRR) arbitration with 32 Phases	RO RO	No No	06h 00h

Register 13-49. 15Ch VC0 Resource Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**TC/VC0 Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.	RO	No	1
7:1		RW	Yes	7Fh
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.	RW1S	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for the corresponding PEX 8604 Port. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. When WRR is enabled, the Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3; if the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = WRR with 32 Phases	RW	Yes	001b
		RW	Yes	000b
23:20	***Reserved***	RsvdP	No	0h
26:24	**VC0 ID** Defines the Port's VC0 ID code. This bit is Cleared, because VC0 is the default VC.	RO	No	000b
30:27	***Reserved***	RsvdP	No	0h
31	**VC0 Enable** 0 = Not allowed 1 = Enables the Port's default VC, VC0	RO	No	1

Register 13-50. 160h VC0 Resource Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	***Reserved***	RsvdP	No	0000h
16	**Port Arbitration Table Status** 0 = Hardware has finished loading values stored in the Port Arbitration Table, after software Sets the **VC0 Resource Control** register *Load Port Arbitration Table* bit (offset 15Ch[16]) 1 = Port Arbitration Table entry was written to by software	RO	No	0
17	**VC0 Negotiation Pending** 0 = Port's VC0 negotiation is complete 1 = Port's VC0 initialization is not complete	RO	Yes	1
31:18	***Reserved***	RsvdP	No	0-0h

Register 13-51. 164h VC1 Resource Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Port Arbitration Capability** VC1 Requests use the Port arbitration method defined by the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) for VC0. 01h = Non-configurable Hardware-Fixed Port arbitration – the only value supported	RO	No	01h
14:8	***Reserved***	RsvdP	No	0-0h
15	**Reject Snoop Transactions** Not a PCI Express switch feature; therefore, this bit is Cleared.	RsvdP	No	0
22:16	**Maximum Time Slots** ***Reserved***	RsvdP	No	000_0000b
23	***Reserved***	RsvdP	No	0
31:24	**Port Arbitration Table Offset** ***Not used*** VC1 Requests use the Port arbitration method defined by the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) for VC0.	RsvdP	No	00h

Register 13-52. 168h VC1 Resource Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**TC/VC1 Map** Defines Traffic Classes [7:1], respectively, and indicates which TCs are mapped into VC1. Traffic Class 0 must be mapped to VC0. Traffic Classes [7:1] can be mapped to VC1.	RO	No	00h
7:1		RW	Yes	
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table** ***Not supported*** Hardware writable and software readable.	RsvdP	No	0
19:17	**Port Arbitration Select** ***Not supported***	RW	Yes	000b
23:20	***Reserved***	RsvdP	No	0h
26:24	**VC1 ID** Defines the Port's VC1 ID code.	RW	Yes	001b
30:27	***Reserved***	RsvdP	No	0h
31	**VC1 Enable** 0 = Disables the Port's VC1 1 = Enables the Port's VC1	RW	Yes	0

Register 13-53. 16Ch VC1 Resource Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	***Reserved***	RsvdP	No	0000h
16	**Port Arbitration Table Status** ***Not supported***	RO	No	0
17	**VC1 Negotiation Pending** 0 = Port's VC1 negotiation is complete 1 = Port's VC1 initialization or disabling is pending	RO	Yes	1
31:18	***Reserved***	RsvdP	No	0-0h

13.13.1 WRR Port Arbitration Table Registers (Offsets 1A8h – 1BCh)

This section details the WRR Port Arbitration Table registers. Port Arbitration Table phases are used to determine Port weighting during "Weighted Round-Robin with 32 Phases" Port arbitration.

Table 13-15 defines the register map. The numbers along the top of the table indicate the 4-bit fields of each 32-bit register. There are 32 phases, and any active Port Number can go into each Port *x*, Phase *x* box.

Note: ***The Port Arbitration Table is used only when Weighted Round-Robin (WRR) with 32-phase Port Arbitration is selected.*** *The Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3. Moreover, the fields within this register are valid only on the upstream Port.If the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. Furthermore, the fields within this register are valid only on Port 0 and* ***reserved*** *on all other Ports.*

Table 13-15. WRR Port Arbitration Table Register Map (When WRR is enabled)

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	
Port *x*, Phase 7	Port *x*, Phase 6	Port *x*, Phase 5	Port *x*, Phase 4	Port *x*, Phase 3	Port *x*, Phase 2	Port *x*, Phase 1	Port *x*, Phase 0	1A8h
Port *x*, Phase 15	Port *x*, Phase 14	Port *x*, Phase 13	Port *x*, Phase 12	Port *x*, Phase 11	Port *x*, Phase 10	Port *x*, Phase 9	Port *x*, Phase 8	1ACh
Port *x*, Phase 23	Port *x*, Phase 22	Port *x*, Phase 21	Port *x*, Phase 20	Port *x*, Phase 19	Port *x*, Phase 18	Port *x*, Phase 17	Port *x*, Phase 16	1B0h
Port *x*, Phase 31	Port *x*, Phase 30	Port *x*, Phase 29	Port *x*, Phase 28,	Port *x*, Phase 27	Port *x*, Phase 26	Port *x*, Phase 25	Port *x*, Phase 24	1B4h
Reserved								1B8h – 1BCh

Register 13-54. 1A8h WRR Port Arbitration Table Phases 0 to 7 (When WRR is enabled)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3. Moreover, the fields within this register are valid only on the upstream Port. If the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. Furthermore, the fields within this register are valid only on Port 0 and ***reserved*** on all other Ports.				
3:0	**Port Arbitration Table Phase 0**	RW	Yes	0h
7:4	**Port Arbitration Table Phase 1**	RW	Yes	1h
11:8	**Port Arbitration Table Phase 2**	RW	Yes	2h
15:12	**Port Arbitration Table Phase 3**	RW	Yes	3h
19:16	**Port Arbitration Table Phase 4**	RW	Yes	4h
23:20	**Port Arbitration Table Phase 5**	RW	Yes	5h
27:24	**Port Arbitration Table Phase 6**	RW	Yes	6h
31:28	**Port Arbitration Table Phase 7**	RW	Yes	7h

Register 13-55. 1ACh WRR Port Arbitration Table Phases 8 to 15 (When WRR is enabled)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3. Moreover, the fields within this register are valid only on the upstream Port. If the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. Furthermore, the fields within this register are valid only on Port 0 and ***reserved*** on all other Ports.				
3:0	**Port Arbitration Table Phase 8**	RW	Yes	8h
7:4	**Port Arbitration Table Phase 9**	RW	Yes	9h
11:8	**Port Arbitration Table Phase 10**	RW	Yes	Ah
15:12	**Port Arbitration Table Phase 11**	RW	Yes	Bh
19:16	**Port Arbitration Table Phase 12**	RW	Yes	Ch
23:20	**Port Arbitration Table Phase 13**	RW	Yes	Dh
27:24	**Port Arbitration Table Phase 14**	RW	Yes	Eh
31:28	**Port Arbitration Table Phase 15**	RW	Yes	Fh

Register 13-56. 1B0h WRR Port Arbitration Table Phases 16 to 23 (When WRR is enabled)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3. Moreover, the fields within this register are valid only on the upstream Port. If the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. Furthermore, the fields within this register are valid only on Port 0 and ***reserved*** on all other Ports.				
3:0	**Port Arbitration Table Phase 16**	RW	Yes	0h
7:4	**Port Arbitration Table Phase 17**	RW	Yes	1h
11:8	**Port Arbitration Table Phase 18**	RW	Yes	2h
15:12	**Port Arbitration Table Phase 19**	RW	Yes	3h
19:16	**Port Arbitration Table Phase 20**	RW	Yes	4h
23:20	**Port Arbitration Table Phase 21**	RW	Yes	5h
27:24	**Port Arbitration Table Phase 22**	RW	Yes	6h
31:28	**Port Arbitration Table Phase 23**	RW	Yes	7h

Register 13-57. 1B4h WRR Port Arbitration Table Phases 24 to 31 (When WRR is enabled)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3. Moreover, the fields within this register are valid only on the upstream Port. If the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. Furthermore, the fields within this register are valid only on Port 0 and ***reserved*** on all other Ports.				
3:0	**Port Arbitration Table Phase 24**	RW	Yes	8h
7:4	**Port Arbitration Table Phase 25**	RW	Yes	9h
11:8	**Port Arbitration Table Phase 26**	RW	Yes	Ah
15:12	**Port Arbitration Table Phase 27**	RW	Yes	Bh
19:16	**Port Arbitration Table Phase 28**	RW	Yes	Ch
23:20	**Port Arbitration Table Phase 29**	RW	Yes	Dh
27:24	**Port Arbitration Table Phase 30**	RW	Yes	Eh
31:28	**Port Arbitration Table Phase 31**	RW	Yes	Fh

13.14 Device-Specific Registers (Offsets 1C0h – 51Ch)

This section details the Device-Specific registers located at offsets 1C0h through 51Ch. Device-Specific registers are unique to the PEX 8604 and not referenced in the *PCI Express Base r2.0*. Table 13-16 defines the register map.

Other Device-Specific registers are detailed in Section 13.16, "Device-Specific Registers (Offsets 530h – F8Ch)."

Note: It is recommended that these registers not be changed from their default values.

Table 13-16. Device-Specific Register Map (Offsets 1C0h – 51Ch)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)		1C0h … 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)		200h … 25Ch
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)		260h … 26Ch
Factory Test Only/Reserved		270h – 288h
Device-Specific Registers – Miscellaneous Control (Offset 28Ch)		28Ch
Device-Specific Registers – I^2C Slave Interface (Offsets 290h – 2C4h)		290h … 2C4h
Device-Specific Registers – Bus Number CAM (Offsets 2C8h – 304h)		2C8h … 304h
Device-Specific Registers – I/O CAM (Offsets 308h – 340h)		308h … 340h
Device-Specific Registers – SMBus Slave Interface (Offset 344h)		344h
Device-Specific Registers – Address-Mapping CAM (Offsets 348h – 444h)		348h … 444h
Next Capability Offset (950h or 520h)	1h / PCI Express Extended Capability ID (000Bh)	448h
Device-Specific Registers – Vendor-Specific Dual Cast Extended Capability (Offsets 448h – 51Ch)		… 51Ch

13.14.1 Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)

This section details the Device-Specific Error Checking and Debug registers. Table 13-17 defines the register map.

Table 13-17. Device-Specific Error Checking and Debug Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device-Specific Error Status for Egress ECC Error				1C0h
Device-Specific Error Mask for Egress ECC Error				1C4h
ECC Error Check Disable				1C8h
Error Handler 32-Bit Error Status				1CCh
Error Handler 32-Bit Error Mask				1D0h
Factory Test Only				1D4h
Reserved		Clock Enable		1D8h
Debug Control				1DCh
Power Management Hot Plug User Configuration				1E0h
Egress Control and Status				1E4h
Bad TLP Counter				1E8h
Bad DLLP Counter				1ECh
Reserved				1F0h
Reserved		Software Lane Status		1F4h
ACK Transmission Latency Limit				1F8h
Factory Test Only				1FCh

Register 13-58. 1C0h Device-Specific Error Status for Egress ECC Error (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
ECC is checked by the egress Port, and any ECC error is reported by the egress Half Station (containing the egress Port), when that Port reads the Packet data from the ingress Half-Station RAM. *For example*, when Port 4 receives a packet, the data is stored in Half-Station 1 RAM; then, if the egress Port is in Half-Station 0 and an ECC error is detected when the Port reads the Half-Station 1 RAM, the error is flagged in the Port 0 register bit that reflects Half-Station 1 error status. ***Note:*** *The bits in this register can be masked by their respective* ***Device-Specific Error Mask for Egress ECC Error*** *register bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1C4h).*				
0	**Payload Link List RAM Instance 0 1-Bit Soft Error Status for Ports 0 and 4** 0 = No overflow is detected 1 = 1-bit Soft error is detected	RW1CS	Yes	0
1	**Payload Link List RAM Instance 0 1-Bit Soft Error Status for Ports 1 and 5** 0 = No overflow is detected 1 = 1-bit Soft error is detected	RW1CS	Yes	0
2	**Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Status for Ports 0 and 4** 0 = No overflow is detected 1 = Read detected a 2-bit Soft error	RW1CS	Yes	0
3	**Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Status for Ports 1 and 5** 0 = No overflow is detected 1 = Read detected a 2-bit Soft error	RW1CS	Yes	0
4	**Ingress Link List RAM Read Detected 1-Bit ECC Error Status for Ports 0 and 4** 0 = No error is detected 1 = Read detected a 1-Bit ECC error	RW1CS	Yes	0
5	**Ingress Link List RAM Read Detected 2-Bit ECC Error Status for Ports 0 and 4** 0 = No error is detected 1 = Read detected a 2-Bit ECC error	RW1CS	Yes	0
6	**Ingress Link List RAM Read Detected 1-Bit ECC Error Status for Ports 1 and 5** 0 = No error is detected 1 = Read detected a 1-Bit ECC error	RW1CS	Yes	0
7	**Ingress Link List RAM Read Detected 2-Bit ECC Error Status for Ports 1 and 5** 0 = No error is detected 1 = Read detected a 2-Bit ECC error	RW1CS	Yes	0

Register 13-58. 1C0h Device-Specific Error Status for Egress ECC Error (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 0 and 4** 0 = No error is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
9	**Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 1 and 5** 0 = No error is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
10	***Factory Test Only***	RO	No	0
11	**Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 0 and 4** 0 = No error is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
12	**Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 1 and 5** 0 = No error is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
13	***Factory Test Only***	RO	No	0
14	**Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Status for Ports 0 and 4** 0 = No error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
15	**Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Status for Ports 1 and 5** 0 = No error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0

Register 13-58. 1C0h Device-Specific Error Status for Egress ECC Error (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	***Factory Test Only***	RO	No	0
17	**Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Status for Ports 0 and 4** 0 = No error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
18	**Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Status for Ports 1 and 5** 0 = No error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
19	***Factory Test Only***	RO	No	0
20	**Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 0 and 4** 0 = No error is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
21	**Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 1 and 5** 0 = No error is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
22	***Factory Test Only***	RO	No	0
23	**Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 0 and 4** 0 = No error is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0

Register 13-58. 1C0h Device-Specific Error Status for Egress ECC Error (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
24	**Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 1 and 5** 0 = No error is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
25	***Factory Test Only***	RO	No	0
26	**Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Status for Ports 0 and 4** ***Reserved*** 0 = No error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
27	**Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Status for Ports 1 and 5** ***Reserved*** 0 = No error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
28	***Factory Test Only***	RO	No	0
29	**Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Status for Ports 0 and 4** ***Reserved*** 0 = No error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
30	**Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Status for Ports 1 and 5** ***Reserved*** 0 = No error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
31	***Factory Test Only***	RO	No	0

Register 13-59. 1C4h Device-Specific Error Mask for Egress ECC Error (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *The bits in this register can be used to mask their respective* ***Device-Specific Error Status for Egress ECC Error*** *register bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1C0h).*				
0	**Payload Link List RAM Instance 0 1-Bit Soft Error Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Payload Link List RAM Instance 0 1-Bit Soft Error Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
1	**Payload Link List RAM Instance 0 1-Bit Soft Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Payload Link List RAM Instance 0 1-Bit Soft Error Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1
2	**Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
3	**Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1
4	**Ingress Link List RAM Read Detected 1-Bit ECC Error Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Ingress Link List RAM Read Detected 1-Bit ECC Error Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
5	**Ingress Link List RAM Read Detected 2-Bit ECC Error Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Ingress Link List RAM Read Detected 2-Bit ECC Error Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
6	**Ingress Link List RAM Read Detected 1-Bit ECC Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Ingress Link List RAM Read Detected 1-Bit ECC Error Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1
7	**Ingress Link List RAM Read Detected 2-Bit ECC Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Ingress Link List RAM Read Detected 2-Bit ECC Error Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1

Register 13-59. 1C4h Device-Specific Error Mask for Egress ECC Error (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
9	**Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1
10	***Factory Test Only***	RWS	Yes	1
11	**Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
12	**Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1
13	***Factory Test Only***	RWS	Yes	1
14	**Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
15	**Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1

Register 13-59. 1C4h Device-Specific Error Mask for Egress ECC Error (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	***Factory Test Only***	RWS	Yes	1
17	**Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
18	**Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1
19	***Factory Test Only***	RWS	Yes	1
20	**Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
21	**Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1
22	***Factory Test Only***	RWS	Yes	1
23	**Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1

Register 13-59. 1C4h Device-Specific Error Mask for Egress ECC Error (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1
25	***Factory Test Only***	RWS	Yes	1
26	**Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
27	**Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1
28	***Factory Test Only***	RWS	Yes	1
29	**Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Status for Ports 0 and 4* bit is masked/disabled	RWS	Yes	1
30	**Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Status for Ports 1 and 5* bit is masked/disabled	RWS	Yes	1
31	***Factory Test Only***	RWS	Yes	1

Register 13-60. 1C8h ECC Error Check Disable (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**ECC 1-Bit Error Check Disable** 0 = RAM 1-Bit Soft Error Check enabled 1 = Disables RAM 1-Bit Soft Error Check	0	RWS	Yes	0
1	**ECC 2-Bit Error Check Disable** 0 = RAM 2-Bit Soft Error Check enabled 1 = Disables RAM 2-Bit Soft Error Check	0	RWS	Yes	0
2	**Software Force Error Enable** 1 = **Correctable Error Status** and **Uncorrectable Error Status** registers (offsets FC4h and FB8h, respectively) change from RW1CS to RW		RWS	Yes	0
3	**Software Force Non-Posted Request** Used to select software-forced errors to be associated with Posted or Non-Posted TLPs, because some errors are handled differently, depending upon the TLP type (Posted or Non-Posted). 0 = Handle software-forced errors as if the errors are associated with Posted TLPs 1 = Enables handling of errors associated with Posted TLPs as if those errors are associated with Non-Posted TLPs		RWS	Yes	0

Register 13-60. 1C8h ECC Error Check Disable (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
4	**Enable PEX_INTA# Interrupt Output(s) for Hot Plug or Link State Event-Triggered Interrupts** 0 = Hot Plug or Link State Event Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = Hot Plug or Link State Event Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)		RWS	Yes	0
5	**Enable PEX_INTA# Interrupt Output(s) for Device-Specific Error-Triggered Interrupts** 0 = Device-Specific Error Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = Device-Specific Error Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)		RWS	Yes	0
6	**Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts** 0 = General-Purpose Input/Output (GPIO) Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = GPIO Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)		RWS	Yes	0
7	**Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts** ***This bit is valid only in NT mode.*** Enables either PEX_INTA# or INT*x* Messages for NT-Virtual Doorbell interrupts (NT Port Virtual Interface, offsets C4Ch through C58h). 0 = NT-Virtual Doorbell Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = NT-Virtual Doorbell Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port	RWS	Yes	0
8	**Disable Sending MSI if MSI Is Enabled after Interrupt Status Set** 0 = Does not disable sending an MSI, if MSIs are enabled after an *Interrupt Status* bit is Set 1 = Disables sending an MSI, if MSIs are enabled after an *Interrupt Status* bit is Set ***Note:*** *This bit must remain Cleared, for compliance to specifications governing the MSI Capability.*		RWS	Yes	0
31:9	***Reserved***		RsvdP	No	0-0h

Register 13-61. 1CCh Error Handler 32-Bit Error Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Notes: *All errors in this register generate MSI/INTx interrupts, if enabled.* *The bits in this register can be masked by their respective* ***Error Handler 32-Bit Error Mask*** *register bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1D0h, with the exception of bit 0, which is in all Ports).*					
0	**Completion FIFO Overflow Status** 0 = No overflow is detected 1 = Completion FIFO Overflow is detected when a 4-deep Completion FIFO for ingress, or a 1-deep Completion FIFO for egress, overflows	All	RW1CS	Yes	0
1	***Reserved***		RsvdP	No	0
2	***Factory Test Only***		RW1CS	No	0
3	***Reserved***		RsvdP	No	0
4	**Destination Queue Link List RAM 2-Bit Error** 0 = No error is detected 1 = Destination Queue Link List RAM 2-bit error is detected		RW1CS	Yes	0
5	***Reserved***		RsvdP	No	0
6	**Destination Queue Link List RAM 1-Bit Error Counter Overflow** 0 = No error is detected 1 = Destination Queue Link List RAM 1-bit error is detected		RW1CS	Yes	0
7	***Reserved***		RsvdP	No	0
8	**Source Queue Link List RAM 1-Bit Error Counter Overflow for Ports 0 and 4** 0 = No error is detected 1 = Source Queue Link List RAM 1-bit error is detected		RW1CS	Yes	0
9	**Source Queue Link List RAM 1-Bit Error Counter Overflow for Ports 1 and 5** 0 = No error is detected 1 = Source Queue Link List RAM 1-bit error is detected		RW1CS	Yes	0
10	**Source Queue Link List RAM 2-Bit Error for Ports 0 and 4** 0 = No error is detected 1 = Source Queue Link List RAM 2-bit error is detected		RW1CS	Yes	0
11	**Source Queue Link List RAM 2-Bit Error for Ports 1 and 5** 0 = No error is detected 1 = Source Queue Link List RAM 2-bit error is detected		RW1CS	Yes	0
12	**Retry Buffer 1-Bit Error Counter Overflow** 0 = No error is detected 1 = Retry Buffer 1-bit error is detected		RW1CS	Yes	0
13	**Retry Buffer 2-Bit ECC Error** 0 = No error is detected 1 = Retry Buffer 2-bit error is detected		RW1CS	Yes	0
19:14	***Reserved***		RsvdP	No	0-0h

Register 13-61. 1CCh Error Handler 32-Bit Error Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
20	**TLP ID RAM 2-Bit ECC Error for Ports 0 and 4** 0 = No error is detected 1 = TLP ID RAM 2-bit ECC error is detected		RW1CS	Yes	0
21	**TLP ID RAM 2-Bit ECC Error for Ports 1 and 5** 0 = No error is detected 1 = TLP ID RAM 2-bit ECC error is detected		RW1CS	Yes	0
23:22	***Reserved***		RsvdP	No	00b
24	**TLP ID RAM 1-Bit ECC Error Counter Overflow for Ports 0 and 4** 0 = No error is detected 1 = TLP ID RAM 1-bit ECC Error Counter overflow is detected		RW1CS	Yes	0
25	**TLP ID RAM 1-Bit ECC Error Counter Overflow for Ports 1 and 5** 0 = No error is detected 1 = TLP ID RAM 1-bit ECC Error Counter overflow is detected		RW1CS	Yes	0
31:26	***Reserved***		RsvdP	No	0-0h

Register 13-62. 1D0h Error Handler 32-Bit Error Mask (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Notes: *Error logging is enabled in this register, by default.* *The bits in this register can be used to mask their respective* ***Error Handler 32-Bit Error Status*** *register bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1CCh, with the exception of bit 0, which is in all Ports).*					
0	**Completion FIFO Overflow Mask** 0 = If enabled, error generates MSI/INT*x* interrupt 1 = *Completion FIFO Overflow Status* bit is masked/disabled	All	RWS	Yes	1
1	***Reserved***		RsvdP	No	0
2	***Factory Test Only***		RWS	Yes	1
3	***Reserved***		RsvdP	No	0
4	**Destination Queue Link List RAM 2-Bit Error Mask** 0 = No effect on reporting activity 1 = *Destination Queue Link List RAM 2-Bit Error* bit is masked/disabled		RWS	Yes	1
5	***Reserved***		RsvdP	No	0
6	**Destination Queue Link List RAM 1-Bit Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Destination Queue Link List RAM 1-Bit Error Counter Overflow* bit is masked/disabled		RWS	Yes	1
7	***Reserved***		RsvdP	No	0

Register 13-62. 1D0h Error Handler 32-Bit Error Mask (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
8	**Source Queue Link List RAM 1-Bit Error Counter Overflow Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Source Queue Link List RAM 1-Bit Error Counter Overflow for Ports 0 and 4* bit is masked/disabled		RWS	Yes	1
9	**Source Queue Link List RAM 1-Bit Error Counter Overflow Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Source Queue Link List RAM 1-Bit Error Counter Overflow for Ports 1 and 5* bit is masked/disabled		RWS	Yes	1
10	**Source Queue Link List RAM 2-Bit Error Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *Source Queue Link List RAM 2-Bit Error for Ports 0 and 4* bit is masked/disabled		RWS	Yes	1
11	**Source Queue Link List RAM 2-Bit Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *Source Queue Link List RAM 2-Bit Error for Ports 1 and 5* bit is masked/disabled		RWS	Yes	1
12	**Retry Buffer 1-Bit Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Retry Buffer 1-Bit Error Counter Overflow* bit is masked/disabled		RWS	Yes	1
13	**Retry Buffer 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Retry Buffer 2-Bit ECC Error* bit is masked/disabled		RWS	Yes	1
19:14	***Reserved***		RsvdP	No	0-0h
20	**TLP ID RAM 2-Bit ECC Error Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *TLP ID RAM 2-Bit ECC Error for Ports 0 and 4* bit is masked/disabled		RWS	Yes	1
21	**TLP ID RAM 2-Bit ECC Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *TLP ID RAM 2-Bit ECC Error for Ports 1 and 5* bit is masked/disabled		RWS	Yes	1
23:22	***Reserved***		RsvdP	No	00b
24	**TLP ID RAM 1-Bit ECC Error Counter Overflow Mask for Ports 0 and 4** 0 = No effect on reporting activity 1 = *TLP ID RAM 1-Bit ECC Error Counter Overflow for Ports 0 and 4* bit is masked/disabled		RWS	Yes	1
25	**TLP ID RAM 2-Bit ECC Error Mask for Ports 1 and 5** 0 = No effect on reporting activity 1 = *TLP ID RAM 1-Bit ECC Error Counter Overflow for Ports 1 and 5* bit is masked/disabled		RWS	Yes	1
31:26	***Reserved***		RsvdP	No	0-0h

Register 13-63. 1D8h Clock Enable (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Ports are automatically enabled, according to the Port configuration defined by the STRAP_PORTCFG[1:0] inputs, which can be overridden by programming the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0]). An enabled Port can be selectively disabled, however, by Clearing the Port's *Port x Clock Enable* bit in this register. Port 0 must always remain enabled. ***Note:*** *It is not possible to enable more Ports than the maximum specified for the device.*				
0	**Port 0 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	1
1	**Port 1 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
5	**Port 5 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
15:6	***Factory Test Only***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-64. 1DCh Debug Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
Notes: *The first Configuration register programmed by the serial EEPROM* ***must*** *be the* ***Debug Control*** *register (Port 0, offset 1DCh), serial EEPROM locations 4h through 9h, as listed in Table 6-1, "Serial EEPROM Data."* *If Port 0 is a Legacy NT Port, this register is loaded from the NT Port Virtual Interface register offset 1DCh location in the serial EEPROM.*					
3:0	***Factory Test Only***	RO	No	Fh	
4	**UPCFG Timer Enable** Reflects the STRAP_UPCFG_TIMER_EN# input state. 0 = Upconfigure Timer is disabled 1 = Upconfigure Timer is enabled	RWS	Yes	0 (STRAP_UPCFG_TIMER_EN#=H) 1 (STRAP_UPCFG_TIMER_EN#=L)	
5	**SMBus Enable** Reflects the STRAP_SMBUS_EN# input state. 0 = SMBus Slave interface is disabled for device configuration (I²C mode is enabled) 1 = SMBus Slave interface is enabled for device configuration (SMBus mode is enabled)	RWS	Yes	0 (STRAP_SMBUS_EN#=H) 1 (STRAP_SMBUS_EN#=L)	
6	**NT P2P Enable** Reflects the STRAP_NT_P2P_EN# input state. This bit and its corresponding input must ***not*** be toggled at runtime. 0 = NT PCI-to-PCI bridge mode is disabled (STRAP_NT_P2P_EN#=H) (Legacy NT mode is enabled) 1 = NT PCI-to-PCI bridge mode is enabled (STRAP_NT_P2P_EN#=L)	RWS	Yes	0 (STRAP_NT_P2P_EN#=H) 1 (STRAP_NT_P2P_EN#=L)	
7	***Factory Test Only***	RWS	Yes	0	
11:8	**Upstream Port ID** Upstream Port Number – Reads the external Strap value on the STRAP_UPSTRM_PORTSEL[3:0] inputs, at Reset de-assertion. When bit 15 (*Hardware/Software Configuration Mode Control*) is Cleared, software is not allowed to change this value.	RO	Yes	Set by STRAP_UPSTRM_PORTSEL[3:0] input levels, serial EEPROM, or I²C followed by a Soft Reset	
	When bit 15 (*Hardware/Software Configuration Mode Control*) is Set, Upstream Port Number can be Set by software, using the values defined below. All other encodings are ***reserved***. ***Note:*** *Port 0 is recommended for the upstream Port designation.* 0h = Port 0 1h = Port 1 4h = Port 4 5h = Port 5	RW[a]	Yes		

Register 13-64. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
13:12	**Interrupt Fencing Mode Select** ***Note:*** *A Fundamental Reset is needed to recover from Fencing errors.* **Mode 1 (Default)** **1.** When the PEX 8604 receives a packet with a Fatal error (Malformed, DLL Protocol error) from an external device, or the device detects a Credit Overflow, Receiver Overflow, or Surprise Link Down, the switch logs the Header on the corresponding Port, sends a Fatal Error Message to the Host, then asserts FATAL_ERR#. **2.** When the PEX 8604 detects an internal Fatal error (ECC failure), the switch sends a Fatal Interrupt Message to the Host and asserts FATAL_ERR#. In certain situations, delivery of the interrupt is not guaranteed; however, the signal is always asserted upon a Fatal event. **Mode 2 (Generate Internal Reset)** Upon Fatal error (internal or external) detection, an internal Chip Level reset is asserted (equivalent to an In-Band Reset from the upstream Port). No error Messages are generated, and no attempt is made to block packets in transit. **Mode 3 (Block All Packet Transmission)** Upon Fatal error (internal or external) detection, the Port logs the error in the **Uncorrectable Error Status** register (offset FB8h), then asserts FATAL_ERR#. This Fatal error detection blocks all Ports from sending out TLPs. No error Messages are generated. If a packet is already in transmission, an EDB is inserted to cancel the packet **Mode 4 (Block All Packet Transmission and Create Surprise Down)** In addition to all the Mode 3 actions, the PEX 8604 forces the upstream Link to go down, thus causing a Surprise Down event on the Link, so that the Host is notified. 00b = Mode 1 (default) 01b = Mode 2 – Generate Internal Reset 10b = Mode 3 – Block All Packet Transmission 11b = Mode 4 – Block All Packet Transmission and Create Surprise Down	RWS	Yes	00b	

Register 13-64. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
14	***Factory Test Only***	RWS	Yes	0	
15	**Hardware/Software Configuration Mode Control** Allows software to configure which Port is the upstream Port, as well as which Port is a Legacy NT Port. 0 = Upstream Port and NT Port selection by the STRAP_UPSTRM_PORTSEL[3:0] and STRAP_NT_UPSTRM_PORTSEL[3:0] inputs, respectively, which can be overridden by the serial EEPROM and/or I^2C configuration mechanism. Cannot be changed by in-band software during runtime. 1 = In-band software can change which Port is configured to be the upstream Port and NT Port, by writing new values to fields [11:8 and 27:24] (*Upstream Port ID* and *NT Port Number*, respectively), followed by issuance of a Hot Reset to the upstream Port. Bit 20 (*Upstream Port and NT-Link DL_Down Reset Propagation Disable*) must be Cleared.	RWS	Yes	0	

Register 13-64. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
16	**Upstream Hot Reset Control** 0 = Reset all logic, except Sticky bits and Device-Specific registers 1 = Reset only the Configuration Space registers of all Ports defined by the *PCI Express Base r2.0* ***Note:*** *Only a Fundamental Reset serial EEPROM load affects this bit.*	RWS	Yes	0	1
17	**Disable Serial EEPROM Load on Hot Reset** 0 = Enables serial EEPROM load upon upstream Port or NT Port Link Interface Hot Reset or *DL_Down* state 1 = Disables serial EEPROM load upon upstream Port or NT Port Link Interface Hot Reset or *DL_Down* state	RWS	Yes	0	
18	**NT Mode Enable** ***Used only in NT mode.*** NT mode (Intelligent Adapter) is enabled by the STRAP_NT_ENABLE# input, which is overridden by the value of this bit if this register is programmed by the serial EEPROM upon Fundamental Reset. Software, serial EEPROM load upon upstream Port or NT Port Link Interface Hot Reset or *DL_Down* state, and/or I^2C are not allowed to change this value. 0 = NT mode is disabled (STRAP_NT_ENABLE#=H) 1 = NT mode is enabled (STRAP_NT_ENABLE#=L)	HwInit	Yes (Serial EEPROM only)	Set by STRAP_NT_ENABLE# input level or by serial EEPROM	
19	**NT Port DL_Down Reset Propagation Disable** ***Used only in NT mode.*** Setting this bit: • Enables the NT-Link Port to ignore a Hot Reset training sequence • Blocks the NT-Link Port from manifesting an internal reset due to an NT-Link DL_Down event	RWS	Yes	0	

Register 13-64. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
20	**Upstream Port and NT-Link DL_Down Reset Propagation Disable** Setting this bit: • Enables the upstream Port to ignore a Hot Reset training sequence, • Blocks the PEX 8604 from manifesting an internal reset due to a DL_Down event, and • Prevents the downstream Ports from issuing a Hot Reset to downstream devices when a Hot Reset or DL_Down event occurs on the upstream Link If NT mode is enabled, Setting this bit additionally: • Enables the NT-Link Port to ignore a Hot Reset training sequence, and • Blocks the PEX 8604 NT Port Link Interface from manifesting an internal reset due to a DL_Down event on the NT Port Link	RWS	Yes	0	
21	**Cut-Thru Enable** 0 = Disables Cut-Thru support 1 = Enables Cut-Thru support	RWS	Yes	1	
22	**NT Security Mode Enable** Setting this bit blocks Memory-Mapped access from the NT-Link side to all PEX 8604 registers, except the NT Port Link Interface registers. For Memory Requests that target NT-Link **BAR0** offsets other than 1_1XXXh (68 to 72 KB) within the 128-KB range, Reads return the data value 0h, and Write data is ignored.	RWS	Yes	0	
23	***Factory Test Only***	RWS	Yes	0	

Register 13-64. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
27:24	**NT Port Number** ***Used only in NT mode.*** When bit 18 (*NT Mode Enable*) is Set, and bit 15 (*Hardware/Software Configuration Mode Control*) is Cleared, the NT Port Number is Set by the STRAP_NT_UPSTRM_PORTSEL[3:0] inputs. This field is "Don't Care" for Transparent mode. Software is not allowed to change this value.	HwInit	Yes	0h	Set by STRAP_NT_UPSTRM_PORTSEL[3:0] input levels, serial EEPROM, or I^2C followed by a Soft Reset
	Used only in NT mode. When bits 18 (*NT Mode Enable*) and 15 (*Hardware/Software Configuration Mode Control*) are both Set, the NT Port Number selected by this field is Set by software, using the values defined below. All other encodings are ***reserved***. 0h = Port 0 1h = Port 1 4h = Port 4 5h = Port 5	R/W[a]	Yes		
28	**Virtual Interface Access Enable** ***Used only in NT mode.*** When the serial EEPROM is not present, the default value is 1; otherwise, the default value is 0. 0 = Retries Type 0 Configuration TLP received on the NT Port Virtual Interface 1 = Accepts Type 0 Configuration TLP on the NT Port Virtual Interface ***Notes:*** *This bit does not affect the PEX 8604 in Transparent mode, nor does it affect other transaction types.* *Set this bit to enable Configuration access to the NT Port Virtual Interface.*	RW	Yes	1	
29	**Link Interface Access Enable** ***Used only in NT mode.*** 0 = Retries Type 0 Configuration Request received on the NT Port Link Interface 1 = Accepts Type 0 Configuration Request received on the NT Port Link Interface ***Notes:*** *This bit does not affect the PEX 8604 in Transparent mode.* *Set this bit to enable Configuration access to the NT Port Link Interface.*	RW	Yes	0	

Register 13-64. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
30	**Inhibit EEPROM NT-Link Load on Hot Reset** ***Used only in NT mode.*** Inhibits serial EEPROM load of NT Port Link Interface registers when any one of the following conditions exist: • **Upstream Port Hot Reset** – Bits [17:16] (*Disable Serial EEPROM Load on Hot Reset* and *Upstream Hot Reset Control*, respectively) are Cleared • **Upstream Port *DL_Down* state** – Bits [20, 17:16] (*Upstream Port and NT-Link DL_Down Reset Propagation Disable*, *Disable Serial EEPROM Load on Hot Reset*, and *Upstream Hot Reset Control*, respectively) are Cleared • **NT Port Link Interface Hot Reset or *DL_Down* state** – Bit 17 (*Disable Serial EEPROM Load on Hot Reset*) is Cleared	RW	Yes	0	1
31	**Load Only EEPROM NT-Link on Hot Reset** ***Used only in NT mode.*** Load only serial EEPROM NT Port Link Interface register entries when any one of the following conditions exist: • **Upstream Port Hot Reset** – Bits [17:16] (*Disable Serial EEPROM Load on Hot Reset* and *Upstream Hot Reset Control*, respectively) are Cleared • **Upstream Port *DL_Down* state** – Bits [20, 17:16] (*Upstream Port and NT-Link DL_Down Reset Propagation Disable*, *Disable Serial EEPROM Load on Hot Reset*, and *Upstream Hot Reset Control*, respectively) are Cleared • **NT Port Link Interface Hot Reset or *DL_Down* state** – Bit 17 (*Disable Serial EEPROM Load on Hot Reset*) is Cleared	RW	Yes	0	1

a. Although these bits are RW, do not change by software.

Register 13-65. 1E0h Power Management Hot Plug User Configuration (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**L0s Entry Idle Counter** Traffic idle time to meet to enter the L0s Link PM state. 0 = Idle condition must last 1 µs 1 = Idle condition must last 4 µs		RW	Yes	0
1	**ASPM L1 Disable**		RW	Yes	0
2	***Not enabled*** Functionality associated with this bit is enabled only on the downstream Ports.	Upstream	RW	Yes	0
	HPC PME Turn-Off Enable 1 = PME Turn-Off Message is transmitted before the Port is turned Off on a downstream Port	Downstream	RW	Yes	0
4:3	***Reserved***		RsvdP	No	00b
5	***Factory Test Only***		RW	Yes	0
6	***Reserved***		RsvdP	No	0
7	**Disable PCI PM L1 Entry**		RW	Yes	0
8	**DLLP Timeout Link Retrain Disable** Disable Link retraining when no Data Link Layer Packets (DLLPs) are received for more than 256 µs. 0 = Enables Link retraining when no DLLPs are received for more than 256 µs (default) 1 = DLLP Timeout is disabled		RW	Yes	0
9	***Factory Test Only***		RW	Yes	0
10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met		RW	Yes	0
11	***Factory Test Only***		RW	Yes	0
12	**NT Hot Plug Enable** Can be programmed only by serial EEPROM and/or I^2C.		RO	Yes	0
14:13	**HP Parallel Port** ***Not supported*** No functionality, because Parallel Hot Plug is ***not supported***.		RO	Yes	00b
15	**HPC GPIO Write in Progress** Indicates that the last Write operation to an I/O Expander **GPIO *x* Output Data** register (offsets 644h and 648h) is still in progress.		RO	No	0

Register 13-65. 1E0h Power Management Hot Plug User Configuration (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
16	**HPC Serial Expansion Controller Disable** Valid only for Port 0. All other Ports' values are unused. 0 = Enables Serial Hot Plug capability on all Ports 1 = Disables Serial Hot Plug capability on all Ports	0	RW	Yes	0
17	**40-Pin I/O Expander Enable** 0 = Enables 16-pin I/O Expanders for all downstream Ports that implement Serial Hot Plug 1 = Enables 40-pin I/O Expanders for all downstream Ports that implement Serial Hot Plug ***Note:*** *Value of 1 can be enabled only by serial EEPROM (that is, neither software nor I^2C can be used to enable the 40-Pin I/O Expander).*	0	RW	Yes (See Note)	0
18	**HPC GPIO Config** Programs the GPIO direction for one GPIO. 0 = Input 1 = Output; register is RW		RW	Yes	0
19	**HPC GPIO Input/Output Value** If the external I^2C I/O Expander GPIO pin is programmed as input (*HPC GPIO Config*, bit 18, is Cleared), this bit reflects the logic value of the voltage on that Input pin. If the external I^2C I/O Expander GPIO pin is programmed as output (*HPC GPIO Config*, bit 18, is Set), the value written to this bit is written to the external GPIO pin, through the I^2C Slave interface.		RW	Yes	0
20	**HPC I/O Reload** 1 = Serial Hot Plug Controller (I^2C I/O Expander) Output pin values are re-loaded from field [26:21] (*HPC Output Reload Value*). After the action is complete, this bit is self-Clearing.		RW	Yes	0
26:21	**HPC Output Reload Value** When bit 20 (*HPC I/O Reload*) is Set, values from this field are re-loaded to the Hot Plug Controller outputs associated with the Port. Bit 21 = I/O Expander PWRLED# Bit 22 = I/O Expander ATNLED# Bit 23 = I/O Expander PWREN Bit 24 = I/O Expander RECLKEN# Bit 25 = I/O Expander PERST# Bit 26 = I/O Expander INTERLOCK		RW	Yes	0-0h
31:27	***Factory Test Only***		RW	Yes	0-0h

Register 13-66. 1E4h Egress Control and Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
1:0	***Reserved***	RW	Yes	00b
2	***Factory Test Only***	RW	Yes	1
7:3	***Factory Test Only***	RW	Yes	0-0h
8	**Reader Header Prefetch Disable** 0 = Enables Reader Header Prefetch capability 1 = Disables Reader Header Prefetch capability	RW	Yes	0
9	**Vendor-Specific Type 0 UR** 0 = Do not generate UR Vendor-Defined Type 0 Broadcast TLP in *DL_Down* state 1 = Generate UR Vendor-Defined Type 0 Broadcast TLP in *DL_Down* state	RW	Yes	0
10	**Egress Credit Timeout Enable** 0 = Egress Credit Timeout mechanism is disabled. 1 = Egress Credit Timeout mechanism is enabled. The timeout period is selected in bit 11 (*Egress Credit Timeout Value*). Status is reflected in bits [19 and 16] (*VC1 EGR Credit Timeout Status* and *VC0 EGR Credit Timeout Status*, respectively). If the Egress Credit Timer is enabled and expires (due to lack of Flow Control credits from the connected device), the Port brings down its Link. This event generates a Surprise Down Uncorrectable error, for Transparent downstream Ports. For upstream Port Egress Credit Timeout, the connected upstream device detects the Surprise Down event.	RW	Yes	0
11	**Egress Credit Timeout Value** 0 = 384 to 512 ms 1 = 896 to 1,024 ms	RW	Yes	0
15:12	***Reserved***	RsvdP	No	0h

Register 13-66. 1E4h Egress Control and Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**VC0 EGR Credit Timeout Status** 0 = No timeout 1 = Timeout	RW1C	No	0
18:17	**VC0 EGR Credit Timeout Type** 00b = Posted 01b = Non-Posted 10b = Completion 11b = ***Reserved***	RO	Yes	00b
19	**VC1 EGR Credit Timeout Status** 0 = No timeout 1 = Timeout	RW1C	No	0
21:20	**VC1 EGR Credit Timeout Type** 00b = Posted 01b = Non-Posted 10b = Completion 11b = ***Reserved***	RO	Yes	00b
22	***Factory Test Only***	RW	Yes	1
23	***Factory Test Only***	RW	Yes	0
31:24	***Factory Test Only***	RW	Yes	AAh

Register 13-67. 1E8h Bad TLP Counter (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Bad TLP Counter** Counts the quantity of TLPs received with bad Link Cyclic Redundancy Check (LCRC), or quantity of TLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 13-68. 1ECh Bad DLLP Counter (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Bad DLLP Counter** Counts the quantity of DLLPs received with bad LCRC, or quantity of DLLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 13-69. 1F4h Software Lane Status
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Lane 0 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
1	**Lane 1 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
7:2	***Factory Test Only***	RsvdP	No	0-0h
8	**Lane 4 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
9	**Lane 5 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
15:10	***Factory Test Only***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-70. 1F8h ACK Transmission Latency Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The value of this register should be valid after Link negotiation.				
11:0	**ACK Transmission Latency Limit** Acknowledge Control Packet (ACK) Transmission Latency Limit. The value of this field changes based upon Negotiated Link Width (offset 78h[25:20]) encoding, after the Link is up. x1 Link width = 255d x2 Link width = 217d	RWS	Yes	Set by STRAP_PORTCFG[1:0] input levels
15:12	***Reserved***	RsvdP	No	0h
23:16	**Upper 8 Bits of the Replay Timer Limit** If the serial EEPROM is not present, the value of this register changes based upon the negotiated Link width after the Link is up. The value in this register is a multiplier of the default internal timer values that are compliant to the *PCI Express Base r2.0*. These bits should normally remain the default value, 00h.	RWS	Yes	00h
30:24	***Reserved***	RsvdP	No	00h
31	**ACK Transmission Latency Timer Status** Indicates the written status of field [11:0] (*ACK Transmission Latency Limit*). After the register is written, either by software and/or serial EEPROM, this bit is Set, and Cleared only by a Fundamental Reset.	RO	No	0

13.14.2 Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)

This section details the Device-Specific Physical Layer (PHY) registers located at offsets 200h through 25Ch. Table 13-18 defines the register map.

Other Device-Specific PHY registers are detailed in:

- Section 13.16.13, "Device-Specific Registers – Physical Layer (Offsets B80h – C30h)"
- Section 13.16.15, "Device-Specific Registers – Physical Layer (Offsets E40h – EFCh)"

Table 13-18. Device-Specific PHY Register Map (Offsets 200h – 25Ch) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Even Port Lanes – Electrical Idle for Compliance Mask, and Receiver Detect Mask and Status		200h
Odd Port Lanes – Electrical Idle for Compliance Mask, and Receiver Detect Mask and Status		204h
Factory Test Only		208h – 20Ch
Physical Layer User Test Pattern, Bytes 0 through 3		210h
Physical Layer User Test Pattern, Bytes 4 through 7		214h
Physical Layer User Test Pattern, Bytes 8 through 11		218h
Physical Layer User Test Pattern, Bytes 12 through 15		21Ch
Even Ports – Physical Layer Command/Status		220h
Odd Ports – Physical Layer Command/Status		224h
Even Ports – Physical Layer Test		228h
Odd Ports – Physical Layer Test		22Ch
Reserved	Even Ports – Disable/Quiet/Test Pattern Rate	230h
Reserved	Odd Ports – Disable/Quiet/Test Pattern Rate	234h
Common Physical Layer Command/Status		238h
Reserved	Common Physical Layer Safety and Test	23Ch
Even Ports – SerDes Quad 0 Diagnostic Data		240h
Odd Ports – SerDes Quad 2 Diagnostic Data		244h
Reserved		248h – 24Ch
Even Ports – Physical Layer Safety and Test		250h
Odd Ports – Physical Layer Safety and Test		254h
Even Ports – User Test Pattern Delay		258h
Odd Ports – User Test Pattern Delay		25Ch

Notes: *In this section, the term "SerDes quad" or "quad" refers to assembling SerDes modules into groups of Lanes for testing purposes.*

Table 13-19 defines the PEX 8604 Port and Lane configurations. Ports that are not configured nor enabled are invisible to software.

Table 13-19. Port Configurations

STRAP_PORTCFG[1:0]	Port 0	Port 1	Port 4	Port 5
(default) 00b	x1	x1	x1	x1
01b	x2	x1		x1
10b	x2	x2		

Register 13-71. 200h Even Port Lanes – Electrical Idle for Compliance Mask, and Receiver Detect Mask and Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register is used for specifying the pre-determined quantity of Lanes that detected a Receiver during a LTSSM *Detect* state, but never detected an exit from Electrical Idle. Because the PEX 8604 has multiple Port configurations, a Mask register is used, rather than specifying a number. multiple bits are Set, and they correspond to Lanes that belong to the same Port, any of those specified Lanes can cause entry into the LTSSM *Polling.Compliance* state. ***Note:*** *Masking Electrical Idle detect does not affect the inferred Electrical Idle detection.* ***Use the SerDes x Mask Electrical Idle Detect bits with caution.***				
0	**Electrical Idle on SerDes 0 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
1	**Electrical Idle on SerDes 1 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
7:2	***Factory Test Only***	RsvdP	No	0-0h
8	**SerDes 0 Mask Electrical Idle Detect** 0 = Analog Electrical Idle detection is enabled for this SerDes. 1 = Analog Electrical Idle detection is disabled for this SerDes. Electrical Idle entrance inference, however, can be enabled by one or more available methods only if this bit is Set, and the Port's **SerDes Control** register (offset C28h) *Port x Electrical Idle Inference Disable* bit associated with this SerDes is Cleared.	RWS	Yes	0
9	**SerDes 1 Mask Electrical Idle Detect** 0 = Analog Electrical Idle detection is enabled for this SerDes. 1 = Analog Electrical Idle detection is disabled for this SerDes. Electrical Idle entrance inference, however, can be enabled by one or more available methods only if this bit is Set, and the Port's **SerDes Control** register (offset C28h) *Port x Electrical Idle Inference Disable* bit associated with this SerDes is Cleared.	RWS	Yes	0
15:10	***Factory Test Only***	RsvdP	No	0-0h
16	**SerDes 0 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes. The corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
17	**SerDes 1 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes. The corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
23:18	***Factory Test Only***	RsvdP	No	0-0h

Register 13-71. 200h Even Port Lanes – Electrical Idle for Compliance Mask, and Receiver Detect Mask and Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
24	**Receiver Detected on Lane 0** Returns the Receiver's LTSSM *Detect* state status, and reads back as 1 when a Receiver is detected on Lane 0.	RO	No	Set by SerDes
25	**Receiver Detected on Lane 1** Returns the Receiver's LTSSM *Detect* state status, and reads back as 1 when a Receiver is detected on Lane 1.	RO	No	Set by SerDes
31:26	***Factory Test Only***	RsvdP	No	0-0h

Register 13-72. 204h Odd Port Lanes – Electrical Idle for Compliance Mask, and Receiver Detect Mask and Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register is used for specifying the pre-determined quantity of Lanes that detected a Receiver during a LTSSM *Detect* state, but never detected an exit from Electrical Idle. Because the PEX 8604 has multiple Port configurations, a Mask register is used, rather than specifying a number. multiple bits are Set, and they correspond to Lanes that belong to the same Port, any of those specified Lanes can cause entry into the LTSSM *Polling.Compliance* state. ***Note:*** *Masking Electrical Idle detect does not affect the inferred Electrical Idle detection.* ***Use the SerDes x Mask Electrical Idle Detect bits with caution.***				
0	**Electrical Idle on SerDes 4 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
1	**Electrical Idle on SerDes 5 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
7:2	***Factory Test Only***	RsvdP	No	0-0h
8	**SerDes 4 Mask Electrical Idle Detect** 0 = Analog Electrical Idle detection is enabled for this SerDes. 1 = Analog Electrical Idle detection is disabled for this SerDes. Electrical Idle entrance inference, however, can be enabled by one or more available methods only if this bit is Set, and the Port's **SerDes Control** register (offset C28h) *Port x Electrical Idle Inference Disable* bit associated with this SerDes is Cleared.	RWS	Yes	0
9	**SerDes 5 Mask Electrical Idle Detect** 0 = Analog Electrical Idle detection is enabled for this SerDes. 1 = Analog Electrical Idle detection is disabled for this SerDes. Electrical Idle entrance inference, however, can be enabled by one or more available methods only if this bit is Set, and the Port's **SerDes Control** register (offset C28h) *Port x Electrical Idle Inference Disable* bit associated with this SerDes is Cleared.	RWS	Yes	0
15:10	***Factory Test Only***	RsvdP	No	0-0h
16	**SerDes 4 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes. The corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
17	**SerDes 5 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes. The corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
23:18	***Factory Test Only***	RsvdP	No	0-0h

Register 13-72. 204h Odd Port Lanes – Electrical Idle for Compliance Mask, and Receiver Detect Mask and Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
24	**Receiver Detected on Lane 4** Returns the Receiver's LTSSM *Detect* state status, and reads back as 1 when a Receiver is detected on Lane 4.	RO	No	Set by SerDes
25	**Receiver Detected on Lane 5** Returns the Receiver's LTSSM *Detect* state status, and reads back as 1 when a Receiver is detected on Lane 5.	RO	No	Set by SerDes
31:26	***Factory Test Only***	RsvdP	No	0-0h

Register 13-73. 210h Physical Layer User Test Pattern, Bytes 0 through 3 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 18.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 0 of the UTP. This is the first byte transferred.	RW	Yes	00h
15:8	Byte 1 of the UTP.	RW	Yes	00h
23:16	Byte 2 of the UTP.	RW	Yes	00h
31:24	Byte 3 of the UTP.	RW	Yes	00h

Register 13-74. 214h Physical Layer User Test Pattern, Bytes 4 through 7 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 18.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 4 of the UTP. This is the fifth byte transferred.	RW	Yes	00h
15:8	Byte 5 of the UTP.	RW	Yes	00h
23:16	Byte 6 of the UTP.	RW	Yes	00h
31:24	Byte 7 of the UTP.	RW	Yes	00h

Register 13-75. 218h Physical Layer User Test Pattern, Bytes 8 through 11 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 18.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 8 of the UTP. This is the ninth byte transferred.	RW	Yes	00h
15:8	Byte 9 of the UTP.	RW	Yes	00h
23:16	Byte 10 of the UTP.	RW	Yes	00h
31:24	Byte 11 of the UTP.	RW	Yes	00h

Register 13-76. 21Ch Physical Layer User Test Pattern, Bytes 12 through 15 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 18.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 12 of the UTP. This is the thirteenth byte transferred.	RW	Yes	00h
15:8	Byte 13 of the UTP.	RW	Yes	00h
23:16	Byte 14 of the UTP.	RW	Yes	00h
31:24	Byte 15 of the UTP.	RW	Yes	00h

Register 13-77. 220h Even Ports – Physical Layer Command/Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides the Loopback, Scrambler Disable, and Compliance Receive commands, and Ready as Loopback Master status, for each even-numbered Port.				
0	**Port 0 Loopback Command** 0 = Port is not enabled to go to the *Loopback* Master state. 1 = Port attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RW	Yes	0
1	**Port 0 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on the Port's Lane(s), and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Port's scrambler is enabled 1 = Port's scrambler is disabled	RW	Yes	0
2	**Port 0 Compliance Receive Command** 0 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* state 1 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* state	RW	Yes	0
3	**Port 0 Ready as Loopback Master** Link Training and Status State Machine (LTSSM) established Loopback as a Master for the Port. 0 = Port is not in Loopback Master mode. 1 = Indicates that the Port has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 0 (*Port 0 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8604 exits the *Loopback.Active* state.	RO	No	0
7:4	***Factory Test Only***	RsvdP	No	0h

Register 13-77. 220h Even Ports – Physical Layer Command/Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**Port 4 Loopback Command** 0 = Port is not enabled to go to the *Loopback* Master state. 1 = Port attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RW	Yes	0
9	**Port 4 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on the Port's Lane, and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Port's scrambler is enabled 1 = Port's scrambler is disabled	RW	Yes	0
10	**Port 4 Compliance Receive Command** 0 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* state 1 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* state	RW	Yes	0
11	**Port 4 Ready as Loopback Master** LTSSM established Loopback as a Master for the Port. 0 = Port is not in Loopback Master mode. 1 = Indicates that the Port has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 8 (*Port 4 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8604 exits the *Loopback.Active* state.	RO	No	0
31:12	***Factory Test Only***	RsvdP	No	0000_0h

Register 13-78. 224h Odd Ports – Physical Layer Command/Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides the Loopback, Scrambler Disable, and Compliance Receive commands, and Ready as Loopback Master status, for each odd-numbered Port.				
0	**Port 1 Loopback Command** 0 = Port is not enabled to go to the *Loopback* Master state. 1 = Port attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RW	Yes	0
1	**Port 1 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on the Port's Lane(s), and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Port's scrambler is enabled 1 = Port's scrambler is disabled	RW	Yes	0
2	**Port 1 Compliance Receive Command** 0 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* state 1 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* state	RW	Yes	0
3	**Port 1 Ready as Loopback Master** LTSSM established Loopback as a Master for the Port. 0 = Port is not in Loopback Master mode. 1 = Indicates that the Port has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 0 (*Port 1 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8604 exits the *Loopback.Active* state.	RO	No	0
7:4	***Factory Test Only***	RsvdP	No	0h

Register 13-78. 224h Odd Ports – Physical Layer Command/Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**Port 5 Loopback Command** 0 = Port is not enabled to go to the *Loopback* Master state. 1 = Port attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RW	Yes	0
9	**Port 5 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on the Port's Lane, and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Port's scrambler is enabled 1 = Port's scrambler is disabled	RW	Yes	0
10	**Port 5 Compliance Receive Command** 0 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* state 1 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* state	RW	Yes	0
11	**Port 5 Ready as Loopback Master** LTSSM established Loopback as a Master for the Port. 0 = Port is not in Loopback Master mode. 1 = Indicates that the Port has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 8 (*Port 5 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8604 exits the *Loopback.Active* state.	RO	No	0
31:12	***Factory Test Only***	RsvdP	No	0000_0h

Register 13-79. 228h Even Ports – Physical Layer Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register provides controls to enable various PHY test modes, for the Even Ports.				
0	**Port 0 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port's LTSSM are reduced to microsecond scale	RW	Yes	0
1	***Factory Test Only***	RsvdP	No	0
2	**Port 4 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port's LTSSM are reduced to microsecond scale	RW	Yes	0
7:3	***Factory Test Only/Reserved***	RsvdP	No	0-0h
10:8	***Factory Test Only***	RW	Yes	000b
15, 11	**Detect.Quiet Wait Time Select Code[1:0]** Selects the amount of time to wait during the *Detect.Quiet* state, before starting the Receiver Detect operation, when a break from Electrical Idle is detected. If Electrical Idle is detected on all Lanes, the wait time is 12 ms. 00b = 0 ms 01b = 4 ms 10b = 8 ms 11b = 12 ms	RWS	Yes	00b
14:12	***Factory Test Only***	RW	Yes	000b
16	**Lane 0 Serial Loopback Path Enable** 1 = Lane enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
17	**Lane 1 Serial Loopback Path Enable** 1 = Lane enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
23:18	***Factory Test Only***	RsvdP	No	0-0h

Register 13-79. 228h Even Ports – Physical Layer Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**Lane 0 Parallel Loopback Path Enable** The **Common Physical Layer Safety and Test** register *Analog Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[21]) overrides this control, and ***must be Cleared*** when using Parallel "Digital" *Loopback*. It is recommended that the Port associated with this Lane be placed into a *Port Disable* state, by Setting the Port's **Even/Odd Port Disable** register *Disable Port x* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[2, 0], and Odd Ports, offset 234h[2, 0]), followed by a *Port Quiet* state, by Setting the Port's *Hold Port x Quiet* bit (Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]), before Setting this bit. 0 = Parallel "Digital" *Loopback* (Slave) path is disabled for this Lane 1 = Lane manually enables the Parallel "Digital" *Loopback* (Slave) path, regardless of the LTSSM state ***Note:*** *This path is automatically enabled when the LTSSM enters the Loopback.Active state, as a Loopback Slave.*	RW	Yes	0
25	**Lane 1 Parallel Loopback Path Enable** The **Common Physical Layer Safety and Test** register *Analog Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[21]) overrides this control, and ***must be Cleared*** when using Parallel "Digital" *Loopback*. It is recommended that the Port associated with this Lane be placed into a *Port Disable* state, by Setting the Port's **Even/Odd Port Disable** register *Disable Port x* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[2, 0], and Odd Ports, offset 234h[2, 0]), followed by a *Port Quiet* state, by Setting the Port's *Hold Port x Quiet* bit (Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]), before Setting this bit. 0 = Parallel "Digital" *Loopback* (Slave) path is disabled for this Lane 1 = Lane manually enables the Parallel "Digital" *Loopback* (Slave) path, regardless of the LTSSM state ***Note:*** *This path is automatically enabled when the LTSSM enters the Loopback.Active state, as a Loopback Slave.*	RW	Yes	0
31:26	***Factory Test Only***	RsvdP	No	0-0h

Register 13-80. 22Ch Odd Ports – Physical Layer Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides controls to enable various PHY test modes, for the Odd Ports.				
0	**Port 1 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port's LTSSM are reduced to microsecond scale	RW	Yes	0
1	***Factory Test Only***	RsvdP	No	0
2	**Port 5 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port's LTSSM are reduced to microsecond scale	RW	Yes	0
7:3	***Factory Test Only***	RsvdP	No	0-0h
10:8	***Factory Test Only***	RW	Yes	000b
15, 11	**Detect.Quiet Wait Time Select Code[1:0]** Selects the amount of time to wait during the *Detect.Quiet* state, before starting the Receiver Detect operation, when a break from Electrical Idle is detected. If Electrical Idle is detected on all Lanes, the wait time is 12 ms. 00b = 0 ms 01b = 4 ms 10b = 8 ms 11b = 12 ms	RWS	Yes	00b
14:12	***Factory Test Only***	RW	Yes	000b
16	**Lane 4 Serial Loopback Path Enable** 1 = Lane enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
17	**Lane 5 Serial Loopback Path Enable** 1 = Lane enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
23:18	***Factory Test Only***	RsvdP	No	0-0h

Register 13-80. 22Ch Odd Ports – Physical Layer Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**Lane 4 Parallel Loopback Path Enable** The **Common Physical Layer Safety and Test** register *Analog Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[21]) overrides this control, and ***must be Cleared*** when using Parallel "Digital" *Loopback*. It is recommended that the Port associated with this Lane be placed into a *Port Disable* state, by Setting the Port's **Even/Odd Port Disable** register *Disable Port x* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[2, 0], and Odd Ports, offset 234h[2, 0]), followed by a *Port Quiet* state, by Setting the Port's *Hold Port x Quiet* bit (Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]), before Setting this bit. 0 = Parallel "Digital" *Loopback* (Slave) path is disabled for this Lane 1 = Lane manually enables the Parallel "Digital" *Loopback* (Slave) path, regardless of the LTSSM state ***Note:*** *This path is automatically enabled when the LTSSM enters the Loopback.Active state, as a Loopback Slave.*	RW	Yes	0
25	**Lane 5 Parallel Loopback Path Enable** The **Common Physical Layer Safety and Test** register *Analog Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[21]) overrides this control, and ***must be Cleared*** when using Parallel "Digital" *Loopback*. It is recommended that the Port associated with this Lane be placed into a *Port Disable* state, by Setting the Port's **Even/Odd Port Disable** register *Disable Port x* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[2, 0], and Odd Ports, offset 234h[2, 0]), followed by a *Port Quiet* state, by Setting the Port's *Hold Port x Quiet* bit (Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]), before Setting this bit. 0 = Parallel "Digital" *Loopback* (Slave) path is disabled for this Lane 1 = Lane manually enables the Parallel "Digital" *Loopback* (Slave) path, regardless of the LTSSM state ***Note:*** *This path is automatically enabled when the LTSSM enters the Loopback.Active state, as a Loopback Slave.*	RW	Yes	0
31:26	***Factory Test Only***	RsvdP	No	0-0h

Register 13-81. 230h Even Ports – Disable/Quiet/Test Pattern Rate (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register is used to disable or enable the LTSSM within individual Even Ports. The bits are intended to be used in lieu of placing the Port into the *Loopback.Active* state as a Loopback Master. These bits enable the test patterns to be transmitted, with or without a device attached at the far end. The recommended usage is as follows: **1.** Set the Port's *Disable Port x* and *Port x Quiet* bits. • Setting the Port's *Disable Port x* bit forces the Port into the *Detect.Quiet* state. If no device is attached, it is not necessary to Set the Port's *Disable Port x* bit. • If 5.0 GT/s is needed, also Set the Port's *Test Pattern x Rate* bit. **2.** If Set, Clear the Port's *Disable Port x* bit. **3.** Load the UTP registers and enable UTP transmission, or just enable PRBS transmission.				
0	**Disable Port 0** While Port 0 is disabled, Receiver termination is disabled and the SerDes that belong to the Port are placed into the L1 Link PM state. 0 = Enables Link Training operation on Port 0. 1 = LTSSM remains in the *Detect.Quiet* state on Port 0, if it is currently in, or returns to, that state. Unconditionally disables Port 0. This is different from the Link Training and Status State Machine (LTSSM) *Disabled* state, in that Port 0 does not attempt to enter this state. If Port 0 is idle, it ceases attempting to detect a Receiver. If Port 0 is up, it immediately returns to the *Detect.Quiet* state and remains there. No Electrical Idle Ordered-Set (EIOS) is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. Port 0 remains disabled until this bit is Cleared.	RWS	Yes	0
1	***Factory Test Only***	RsvdP	No	0
2	**Disable Port 4** While Port 4 is disabled, Receiver termination is disabled and the SerDes that belong to the Port are placed into the L1 Link PM state. 0 = Enables Link Training operation on Port 4. 1 = LTSSM remains in the *Detect.Quiet* state on Port 4, if it is currently in, or returns to, that state. Unconditionally disables Port 4. This is different from the LTSSM *Disabled* state, in that Port 4 does not attempt to enter this state. If Port 4 is idle, it ceases attempting to detect a Receiver. If Port 4 is up, it immediately returns to the *Detect.Quiet* state and remains there. No EIOS is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. Port 4 remains disabled until this bit is Cleared.	RWS	Yes	0
7:3	***Factory Test Only***	RsvdP	No	0-0h

Register 13-81. 230h Even Ports – Disable/Quiet/Test Pattern Rate (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**Hold Port 0 Quiet** Unlike bit 0 (*Disable Port 0*), this bit does not force the LTSSM into the *Detect.Quiet* state. Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed into the L0 Link PM state. Port 0 can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state. 0 = LTSSM is allowed to exit the *Detect.Quiet* state in a normal manner (no effect on the LTSSM) 1 = LTSSM remains in the *Detect.Quiet* state on Port 0 if it is currently in, or returns to, that state ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active state as a Loopback Master.*	RWS	Yes	0
9	***Factory Test Only***	RsvdP	No	0
10	**Hold Port 4 Quiet** Unlike bit 2 (*Disable Port 4*), this bit does not force the LTSSM into the *Detect.Quiet* state. Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed into the L0 Link PM state. Port 4 can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state. 0 = LTSSM is allowed to exit the *Detect.Quiet* state in a normal manner (no effect on the LTSSM) 1 = LTSSM remains in the *Detect.Quiet* state on Port 4 if it is currently in, or returns to, that state ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active state as a Loopback Master.*	RWS	Yes	0
15:11	***Factory Test Only***	RsvdP	No	0-0h
16	**Port 0 Test Pattern *x* Rate** Port transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if bit 8 (*Hold Port 0 Quiet*) is also Set (manual rate selection is enabled only when the *Hold Port 0 Quiet* bit is Set). 0 = UTP is transmitted at 2.5 GT/s 1 = UTP is transmitted at 5.0 GT/s	RWS	Yes	0
17	***Factory Test Only***	RsvdP	No	0
18	**Port 4 Test Pattern *x* Rate** Port transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if bit 10 (*Hold Port 4 Quiet*) is also Set (manual rate selection is enabled only when the *Hold Port 4 Quiet* bit is Set). 0 = UTP is transmitted at 2.5 GT/s 1 = UTP is transmitted at 5.0 GT/s	RWS	Yes	0
23:18	***Factory Test Only***	RsvdP	No	0-0h
31:24	***Reserved***	RsvdP	No	00h

Register 13-82. 234h Odd Ports – Disable/Quiet/Test Pattern Rate (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register is used to disable or enable the LTSSM within individual Odd Ports. The bits are intended to be used in lieu of placing the Port into the *Loopback.Active* state as a Loopback Master. These bits enable the test patterns to be transmitted, with or without a device attached at the far end. The recommended usage is as follows: **1.** Set the Port's *Disable Port x* and *Port x Quiet* bits. • Setting the Port's *Disable Port x* bit forces the Port into the *Detect.Quiet* state. If no device is attached, it is not necessary to Set the Port's *Disable Port x* bit. • If 5.0 GT/s is needed, also Set the Port's *Test Pattern x Rate* bit. **2.** If Set, Clear the Port's *Disable Port x* bit. **3.** Load the UTP registers and enable UTP transmission, or just enable PRBS transmission.				
0	**Disable Port 1** While Port 1 is disabled, Receiver termination is disabled and the SerDes that belong to the Port are placed into the L1 Link PM state. 0 = Enables Link Training operation on Port 1. 1 = LTSSM remains in the *Detect.Quiet* state on Port 1, if it is currently in, or returns to, that state. Unconditionally disables Port 1. This is different from the LTSSM *Disabled* state, in that Port 1 does not attempt to enter this state. If Port 1 is idle, it ceases attempting to detect a Receiver. If Port 1 is up, it immediately returns to the *Detect.Quiet* state and remains there. No EIOS is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. Port 1 remains disabled until this bit is Cleared.	RWS	Yes	0
1	***Factory Test Only***	RsvdP	No	0
2	**Disable Port 5** While Port 5 is disabled, Receiver termination is disabled and the SerDes that belong to the Port are placed into the L1 Link PM state. 0 = Enables Link Training operation on Port 5. 1 = LTSSM remains in the *Detect.Quiet* state on Port 5, if it is currently in, or returns to, that state. Unconditionally disables Port 5. This is different from the LTSSM *Disabled* state, in that Port 5 does not attempt to enter this state. If Port 5 is idle, it ceases attempting to detect a Receiver. If Port 5 is up, it immediately returns to the *Detect.Quiet* state and remains there. No EIOS is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. Port 5 remains disabled until this bit is Cleared.	RWS	Yes	0
7:3	***Factory Test Only/Reserved***	RsvdP	No	0-0h

Register 13-82. 234h Odd Ports – Disable/Quiet/Test Pattern Rate (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**Hold Port 1 Quiet** Unlike bit 0 (*Disable Port 1*), this bit does not force the LTSSM into the *Detect.Quiet* state. Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed into the L0 Link PM state. Port 1 can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state. 0 = LTSSM is allowed to exit the *Detect.Quiet* state in a normal manner (no effect on the LTSSM) 1 = LTSSM remains in the *Detect.Quiet* state on Port 1 if it is currently in, or returns to, that state ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active state as a Loopback Master.*	RWS	Yes	0
9	***Factory Test Only***	RsvdP	No	0
10	**Hold Port 5 Quiet** Unlike bit 2 (*Disable Port 5*), this bit does not force the LTSSM into the *Detect.Quiet* state. Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed into the L0 Link PM state. Port 5 can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state. 0 = LTSSM is allowed to exit the *Detect.Quiet* state in a normal manner (no effect on the LTSSM) 1 = LTSSM remains in the *Detect.Quiet* state on Port 5 if it is currently in, or returns to, that state ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active state as a Loopback Master.*	RWS	Yes	0
15:11	***Factory Test Only/Reserved***	RsvdP	No	0-0h
16	**Port 1 Test Pattern *x* Rate** Port transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if bit 8 (*Hold Port 1 Quiet*) is also Set (manual rate selection is enabled only when the *Hold Port 1 Quiet* bit is Set). 0 = UTP is transmitted at 2.5 GT/s 1 = UTP is transmitted at 5.0 GT/s	RWS	Yes	0
17	***Factory Test Only***	RsvdP	No	0
18	**Port 5 Test Pattern *x* Rate** Port transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if bit 10 (*Hold Port 5 Quiet*) is also Set (manual rate selection is enabled only when the *Hold Port 5 Quiet* bit is Set). 0 = UTP is transmitted at 2.5 GT/s 1 = UTP is transmitted at 5.0 GT/s	RWS	Yes	0
23:19	***Factory Test Only***	RsvdP	No	0-0h
31:24	***Reserved***	RsvdP	No	00h

Register 13-83. 238h Common Physical Layer Command/Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4:0	**Number of Ports Available** Returns the quantity of enabled Ports, based upon the selected Port configuration.	RO	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
5	**Upstream Cross-Link Enable** 0 = Disables upstream cross-link, upstream Port cannot be connected to another upstream Port 1 = Enables upstream cross-link, upstream Port can be connected to another upstream Port	RWS	Yes	1
6	**Downstream Cross-Link Enable** 0 = Disables downstream cross-link, downstream Ports cannot be connected to other downstream Ports 1 = Enables downstream cross-link, downstream Ports can be connected to other downstream Ports	RWS	Yes	1
7	**Elastic Buffer Low-Latency Mode Disable** 0 = Enables Elastic Buffer Low-Latency mode 1 = Disables Elastic Buffer Low-Latency mode	RWS	Yes	0
15:8	**N_FTS Value** Number of Fast Training Sets (N_FTS) value to transmit (in Training Sets).	RWS	Yes	64h
31:16	**User Test Pattern K-Code Flag** The corresponding UTP byte is transmitted as a kcode. ***Caution: Use caution when turning on k-characters, because the transmit logic does not examine illegal codes for validity. Also, sequences of control codes that can be detected as legal SKIP Ordered-Sets in the middle of the data pattern can confuse the Receive data checking logic. Therefore, it is recommended to not turn on k-characters when testing with a UTP.***	RWS	Yes	0000h

Register 13-84. 23Ch Common Physical Layer Safety and Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register contains the PHY Safety and Test Control bits that are common to all PEX 8604 Ports and Lanes.				
0	**L0 to Recovery on Unexpected Electrical Idle Disable** 0 = LTSSM transitions from the L0 Link PM state to the *Recovery* state when an Electrical Idle is detected, without first receiving an Electrical Idle Ordered-Set 1 = LTSSM does not transition from the L0 Link PM state to the *Recovery* state when an Electrical Idle is detected, without first receiving an Electrical Idle Ordered-Set	RWS	Yes	0
1	**Framer Filter K28 Disable** Enabling the K28 Framer Filter increases robustness of the link by not retraining the Link upon detection of a single COM symbol. 0 = Four consecutive COM symbols must be detected within a packet, to cause the Link to be retrained 1 = If a COM symbol is detected within a packet, loss of symbol lock is assumed, and the Link is immediately retrained	RWS	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Retrain on Receive Error Burst** 1 = LTSSM enters the *Recovery* state, if 256 Receiver errors are detected within 1 ms	RWS	Yes	0
5	**Lane Reversal Disable** 0 = Enables Lane reversal support on all Ports 1 = Disables Lane reversal support on all Ports	RWS	Yes	0
6	**Upconfigure Capability Disable** 0 = Upconfigure capability is advertised on all Ports 1 = Upconfigure capability is not advertised on all Ports	RWS	Yes	0
7	***Reserved***	RsvdP	No	0
19:8	**SKIP Ordered-Set Interval** Specifies the SKIP Ordered-Set interval (in symbol times). When a value of 000h is written, SKIP Ordered-Set transmission is disabled. 000h = Disables SKIP Ordered-Set transmission 49Ch = Minimum interval (1,180 symbol times) 602h = Maximum interval (1,538 symbol times) ***Note:*** *A high value (such as FFFh) can cause the Link to fail.*	RWS	Yes	49Ch

Register 13-84. 23Ch Common Physical Layer Safety and Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	RsvdP	No	0
21	**Analog Loopback Enable** 0 = PEX 8604 enters Digital Loopback Slave mode if an external device sends at least two consecutive TS1 Ordered-Sets that have the *Loopback* bit exclusively Set in the TS1 Training Control symbol. The PEX 8604 then loops back data through the Elastic buffer, 8b/10b decoder, and 8b/10b encoder. 1 = Loopback point of all Ports is before the Elastic buffer. This means that data recovered from the Serial data in the recovered Receive Clock domain is re-serialized, then re-transmitted in that same recovered clock domain. This allows the Loopback Master to transmit and receive a user test pattern (UTP) in an asynchronous clocking system. It is also the **required** mode for re-transmitting a PRBS pattern back to the Loopback Master. Overrides the Lane's Parallel "Digital" Loopback Setting (**Even/Odd Port Physical Test** register *Lane x Parallel Loopback Path Enable* bits – Even Ports, offset 228h[26, 24], and Odd Ports, offset 22Ch[26, 24]). ***Note:*** *This bit must be Cleared when using Parallel "Digital" Loopback.*	RWS	Yes	0
22	***Reserved***	RsvdP	No	0
23	***Factory Test Only***	RW	Yes	0
31:24	***Reserved***	RsvdP	No	00h

Register 13-85. 240h Even Ports – SerDes Quad 0 Diagnostic Data (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
There are two **Even/Odd Port SerDes Quad *x* Diagnostic Data** (Diagnostic Data) registers, one for each SerDes quad, at offsets 240h and 244h, in Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port. The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' *SerDes Diagnostic Data Select* bits (field [25:24]). When field [25:24] is Cleared, the information in that Diagnostic Data register is for the first SerDes within that SerDes quad. When field [25:24] is programmed to 01b, the information in that Diagnostic Data register is for the second SerDes within that SerDes quad. Following this pattern, a value of 10b indicates the third SerDes within that SerDes quad, and a value of 11b indicates the fourth SerDes within that SerDes quad. If a SerDes module does not exist in that position, the bits are "***Factory Test Only***," ***reserved*** (RsvdP), and not serial EEPROM nor I^2C writable. This register is used to retrieve Diagnostic Test results for SerDes[0, 1].				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the quantity of errors detected by the UTP (bit 30 is Cleared) or PRBS (bit 30 is Set) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing one or more of the **Even/Odd Port User Test Pattern Delay** register *SerDes x User Test Pattern Enable* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[17:16], and Odd Ports, offset 25Ch[17:16]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing one or more of the **Even/Odd Port User Test Pattern Delay** register *SerDes x PRBS Enable* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[25:24], and Odd Ports, offset 25Ch[25:24]).	RO	No	00h

Register 13-85. 240h Even Ports – SerDes Quad 0 Diagnostic Data (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes (SerDes[0, 1]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [15:0] of this register. The binary code represents a status selection for one of the SerDes Quad 0 Lanes. The test results for physical device Lanes [0, 1] are selected with corresponding binary codes from 0-1. ***Note:*** *To obtain diagnostic data on all SerDes in the quad, run a test, then cycle these bits.*	RW	Yes	00b
29:26	**PRBS Error Injection** 1h = Causes the pattern generators for this SerDes quad's Lanes to insert an error into the transmitted pattern, once every 127 words	RW	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter	RO	No	0
31	***Reserved***	RsvdP	No	0

Register 13-86. 244h Odd Ports – SerDes Quad 2 Diagnostic Data (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
There are two **Even/Odd Port SerDes Quad *x* Diagnostic Data** (Diagnostic Data) registers, one for each SerDes quad, at offsets 240h and 244h, in Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port. The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' *SerDes Diagnostic Data Select* bits (field [25:24]). When field [25:24] is Cleared, the information in that Diagnostic Data register is for the first SerDes within that SerDes quad. When field [25:24] is programmed to 01b, the information in that Diagnostic Data register is for the second SerDes within that SerDes quad. Following this pattern, a value of 10b indicates the third SerDes within that SerDes quad, and a value of 11b indicates the fourth SerDes within that SerDes quad. If a SerDes module does not exist in that position, the bits are "***Factory Test Only***," ***reserved*** (RsvdP), and not serial EEPROM nor I^2C writable. This register is used to retrieve Diagnostic Test results for SerDes[4, 5].				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the quantity of errors detected by the UTP (bit 30 is Cleared) or PRBS (bit 30 is Set) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing one or more of the **Even/Odd Port User Test Pattern Delay** register *SerDes x User Test Pattern Enable* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[17:16], and Odd Ports, offset 25Ch[17:16]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing one or more of the **Even/Odd Port User Test Pattern Delay** register *SerDes x PRBS Enable* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[25:24], and Odd Ports, offset 25Ch[25:24]).	RO	No	00h

Register 13-86. 244h Odd Ports – SerDes Quad 2 Diagnostic Data (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes (SerDes[4, 5]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [15:0] of this register. The binary code represents a status selection for one of the SerDes Quad 2 Lanes. The test results for physical device Lanes [4, 5] are selected with corresponding binary codes from 0-1. ***Note:*** *To obtain diagnostic data on all SerDes in the quad, run a test, then cycle these bits.*	RW	Yes	00b
29:26	**PRBS Error Injection** 1h = Causes the pattern generators for this SerDes quad's Lanes to insert an error into the transmitted pattern, once every 127 words	RW	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter	RO	No	0
31	***Reserved***	RsvdP	No	0

Register 13-87. 250h Even Ports – Physical Layer Safety and Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register contains PHY Safety bits that are associated with the Even Ports. It also contains Controls and Status for Link width re-configuration on Ports that are x2 capable in the Even PHY partition. Link width fields in this register are provided, to enable software to direct Link width Up/Down configuration. The Link width fields are loaded with the Target Link width, which should not exceed the originally negotiated Link width, and afterward, the **Link Control** register *Retrain Link* bit (offset 78h[5]) is Set. If the Target Link width is not equal to the current Link width, the LTSSM transitions from *Recovery* to *Configuration*, then re-negotiates the Link width.				
0	**Port 0 Downtrain Disable** This bit supports Port 0, at up to x2 Link widths. 1 = Port 0 does not reduce its Link width during Link configuration, to eliminate faulty Lanes. Instead, the LTSSM returns to its *Detect* state and Retries Link training. This continues until the Link is able to train on all Lanes that detected a Receiver. ***Caution: This bit should be used with extreme caution, because its use could lead to an endless loop, in which the Link never reaches the L0 Link PM state.***	RWS	Yes	0
1	***Reserved***	RsvdP	No	0
2	**Auto_Speed Disable** 1 = Upstream Port does not initiate a speed change	RWS	Yes	0
3	**Enable x1 Even Port Skip Detect L0s Entry Mode** 1 = SKIP detection that is used for determining the end of L0s Link PM state Fast Training Sets on all Even Ports uses the Electrical Idle Inference SKIP Detector, instead of the standard detector located on the Deskew buffer output	RWS	Yes	1
7:4	**Downstream Port 0 Hot Reset 2 ms Minimum Enable** 1h = If Port 0 is a downstream Port, it remains in the Hot Reset state for a minimum of 2 ms	RWS	Yes	0h
11:8	***Reserved***	RsvdP	No	0h

Register 13-87. 250h Even Ports – Physical Layer Safety and Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
14:12	**Electrical Idle Inference Time Select[2:0]** For Even Ports, selects the amount of time to wait until no SKIP Ordered-Sets are detected, for Electrical Idle to be inferred. Does not affect Electrical Idle inference during the *Recovery.Speed* state. 000b = 4 µs 001b = 6 µs 010b = 8 µs 011b = 16 µs 100b = 32 µs 101b = 64 µs 110b = 128 µs (default) 111b = 256 µs	RWS	Yes	110b
15	**Enable SSC Mode PhyStatus** 1 = For Even Ports, if SSC mode is enabled STRAP_SSC_ISO_ENABLE#=L), the PhyStatus of each Port 0 Lane is sourced only from Lane 0. This is true for any Port 0 Link width.	RWS	Yes	1
19:16	**Port 0 Target Link Width** Provides the capability to allow software to cause Link retraining to a wider or narrower width than the current width, *such as* to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets. Written with the Target Link width for Port 0, to support Link Width Upconfiguration. The initial value of this field is the Port's Negotiated Link Width (offset 78h[25:20]).	RWS	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])

Register 13-87. 250h Even Ports – Physical Layer Safety and Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
20	**Port 0 Upconfigure Capability Received** Set during Link training, if the Port received an Upconfigure Capability notification from the connected device. 0 = Device connected to the Port does not indicate that it is capable of Link Width Upconfiguration. 1 = Device connected to the Port indicates that it is capable of Link Width Upconfiguration. Software can cause the Port to either upconfigure the Link to a previously negotiated Link width, or downconfigure the Link to a narrower width, by writing the needed Target Link Width value to this register, followed by Setting the Port's **Link Control** register *Retrain Link* bit (offset 78h[5]).	RO	No	0
22:21	**Recovery.Speed Electrical Idle Inference Time Divider Select[1:0]** For Even Ports, selects the amount of time that no TS1 nor TS2 Ordered-Sets are detected during the *Recovery.Speed* state, for Electrical Idle to be inferred. (Refer to the *PCI Express Base r2.0*, Section 4.2.4.3, for the specific Unit Interval (UI) values.) 00b = *PCI Express Base r2.0* UI 01b = *PCI Express Base r2.0* UI/2 10b = *PCI Express Base r2.0* UI/4 11b = *PCI Express Base r2.0* UI/8	RWS	Yes	00b
23	**Even Ports Enable Elastic Buffer Reset on Recovery Entrance** 1 = Elastic buffer(s) associated with any Even Port are synchronously reset upon entering the LTSSM *Recovery* state	RWS	Yes	0
26:24	***Reserved***	RsvdP	No	000b
27, 31:29	**Configuration Fail Counter[3:0]** For Even Ports, specifies the quantity of times that the *Configuration* state must fail, before a Port toggles its Gen 2 Feature Disable flag. Writing 0000b to this field disables this Gen 1 compatibility function. The initial value of this field is determined by the STRAP_UPCFG_TIMER_EN# input state. If the input is Low when reset de-asserts, the initial value of this field is 0001b; otherwise, the initial value is 0000b.	RWS	Yes	0000b (STRAP_UPCFG_TIMER_EN#=H) 0001b (STRAP_UPCFG_TIMER_EN#=L)
28	***Reserved***	RsvdP	No	0

Register 13-88. 254h Odd Ports – Physical Layer Safety and Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register contains PHY Safety bits that are associated with the Odd Ports. It also contains Controls and Status for Link width re-configuration on Ports that are x2 capable in the Odd PHY partition. Link width fields in this register are provided, to enable software to direct Link width Up/Down configuration. The Link width fields are loaded with the Target Link width, which should not exceed the originally negotiated Link width, and afterward, the **Link Control** register *Retrain Link* bit (offset 78h[5]) is Set. If the Target Link width is not equal to the current Link width, the LTSSM transitions from *Recovery* to *Configuration*, then re-negotiates the Link width.				
0	**Port 1 Downtrain Disable** This bit supports Port 1, at up to x2 Link widths. 1 = Port 1 does not reduce its Link width during Link configuration, to eliminate faulty Lanes. Instead, the LTSSM returns to its *Detect* state and Retries Link training. This continues until the Link is able to train on all Lanes that detected a Receiver. ***Caution: This bit should be used with extreme caution, because its use could lead to an endless loop, in which the Link never reaches the L0 Link PM state.***	RWS	Yes	0
1	***Reserved***	RsvdP	No	0
2	**Auto_Speed Disable** 1 = Upstream Port does not initiate a speed change	RWS	Yes	0
3	**Enable x1 Odd Port Skip Detect L0s Entry Mode** 1 = SKIP detection that is used for determining the end of L0s Link PM state Fast Training Sets on all Odd Ports uses the Electrical Idle Inference SKIP Detector, instead of the standard detector located on the Deskew buffer output	RWS	Yes	1
7:4	**Downstream Port 1 Hot Reset 2 ms Minimum Enable** 1h = If Port 1 is a downstream Port, it remains in the Hot Reset state for a minimum of 2 ms	RWS	Yes	0h
11:8	***Reserved***	RsvdP	No	0h
14:12	**Electrical Idle Inference Time Select[2:0]** For Odd Ports, selects the amount of time to wait until no SKIP Ordered-Sets are detected, for Electrical Idle to be inferred. Does not affect Electrical Idle inference during the *Recovery.Speed* state. 000b = 4 µs 001b = 6 µs 010b = 8 µs 011b = 16 µs 100b = 32 µs 101b = 64 µs 110b = 128 µs (default) 111b = 256 µs	RWS	Yes	110b
15	**Enable SSC Mode PhyStatus** This bit is ***not*** operational for Odd Ports. It is intended for use only by Even Port 0.	RWS	Yes	1

Register 13-88. 254h Odd Ports – Physical Layer Safety and Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:16	**Port 1 Target Link Width** Provides the capability to allow software to cause Link retraining to a wider or narrower width than the current width, *such as* to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets. Written with the Target Link width for Port 1, to support Link Width Upconfiguration. The initial value of this field is the Port's Negotiated Link Width (offset 78h[25:20]).	RWS	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
20	**Port 1 Upconfigure Capability Received** Set during Link training, if the Port received an Upconfigure Capability notification from the connected device. 0 = Device connected to the Port does not indicate that it is capable of Link Width Upconfiguration. 1 = Device connected to the Port indicates that it is capable of Link Width Upconfiguration. Software can cause the Port to either upconfigure the Link to a previously negotiated Link width, or downconfigure the Link to a narrower width, by writing the needed Target Link Width value to this register, followed by Setting the Port's **Link Control** register *Retrain Link* bit (offset 78h[5]).	RO	No	0
22:21	**Recovery.Speed Electrical Idle Inference Time Divider Select[1:0]** For Odd Ports, selects the amount of time that no TS1 nor TS2 Ordered-Sets are detected during the *Recovery.Speed* state, for Electrical Idle to be inferred. (Refer to the *PCI Express Base r2.0*, Section 4.2.4.3, for the specific Unit Interval (UI) values.) 00b = *PCI Express Base r2.0* UI 01b = *PCI Express Base r2.0* UI/2 10b = *PCI Express Base r2.0* UI/4 11b = *PCI Express Base r2.0* UI/8	RWS	Yes	00b
23	**Odd Ports Enable Elastic Buffer Reset on Recovery Entrance** 1 = Elastic buffer(s) associated with any Odd Port are synchronously reset upon entering the LTSSM *Recovery* state	RWS	No	0

Register 13-88. 254h Odd Ports – Physical Layer Safety and Test (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
26:24	***Reserved***	RsvdP	No	000b
27, 31:29	**Configuration Fail Counter[3:0]** For Odd Ports, specifies the quantity of times that the *Configuration* state must fail, before a Port toggles its Gen 2 Feature Disable flag. Writing 0000b to this field disables this Gen 1 compatibility function. The initial value of this field is determined by the STRAP_UPCFG_TIMER_EN# input state. If the input is Low when reset de-asserts, the initial value of this field is 0001b; otherwise, the initial value is 0000b.	RWS	Yes	0000b (STRAP_UPCFG_TIMER_EN#=H) 0001b (STRAP_UPCFG_TIMER_EN#=L)
28	***Reserved***	RsvdP	No	0

Register 13-89. 258h Even Ports – User Test Pattern Delay (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	**Lane 0 User Test Pattern Delay** Selects the delay (in symbol times) applied when transmitting the UTP on Lane 0. 00b = 0 01b = 1 10b = 4 11b = 8	RW	Yes	00b
3:2	**Lane 1 User Test Pattern Delay** Selects the delay (in symbol times) applied when transmitting the UTP on Lane 1. 00b = 0 01b = 1 10b = 4 11b = 8	RW	Yes	00b
15:4	***Factory Test Only***	RW	Yes	000h

Register 13-89. 258h Even Ports – User Test Pattern Delay (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
16	**SerDes 0 User Test Pattern Enable** 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 210h through 21Ch)) on SerDes 0 in Digital Far-End Loopback Master mode ***Notes: This bit and bit 24 (SerDes 0 PRBS Enable) are mutually exclusive functions and must not be enabled together for SerDes 0. The logical result of bit 24 ANDed with bit 16 must be 0.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the Port's Even/Odd Port Quiet register Hold Port x Quiet bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]) is Set.***	RW	Yes	0
17	**SerDes 1 User Test Pattern Enable** 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 210h through 21Ch)) on SerDes 1 in Digital Far-End Loopback Master mode ***Notes: This bit and bit 25 (SerDes 1 PRBS Enable) are mutually exclusive functions and must not be enabled together for SerDes 1. The logical result of bit 25 ANDed with bit 17 must be 0.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the Port's Even/Odd Port Quiet register Hold Port x Quiet bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]) is Set.***	RW	Yes	0
23:18	***Factory Test Only***	RW	Yes	00h

Register 13-89. 258h Even Ports – User Test Pattern Delay (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**SerDes 0 PRBS Enable** 0 = Disables PRBS sequence generation/checking on SerDes 0 1 = Enables PRBS sequence generation/checking on SerDes 0 ***Notes: This bit and bit 16 (SerDes 0 User Test Pattern Enable) are mutually exclusive functions and must not be enabled together for SerDes 0. The logical result of bit 16 ANDed with bit 24 must be 0.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the Port's Even/Odd Port Quiet register Hold Port x Quiet bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]) is Set.***	RW	Yes	0
25	**SerDes 1 PRBS Enable** 0 = Disables PRBS sequence generation/checking on SerDes 1 1 = Enables PRBS sequence generation/checking on SerDes 1 ***Notes: This bit and bit 17 (SerDes 1 User Test Pattern Enable) are mutually exclusive functions and must not be enabled together for SerDes 1. The logical result of bit 17 ANDed with bit 25 must be 0.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the Port's Even/Odd Port Quiet register Hold Port x Quiet bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]) is Set.***	RW	Yes	0
31:26	***Factory Test Only***	RW	Yes	00h

Register 13-90. 25Ch Odd Ports – User Test Pattern Delay (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
1:0	**Lane 4 User Test Pattern Delay** Selects the delay (in symbol times) applied when transmitting the UTP on Lane 4. 00b = 0 01b = 1 10b = 4 11b = 8	RW	Yes	00b
3:2	**Lane 5 User Test Pattern Delay** Selects the delay (in symbol times) applied when transmitting the UTP on Lane 5. 00b = 0 01b = 1 10b = 4 11b = 8	RW	Yes	00b
15:6	***Factory Test Only***	RW	Yes	0-0h

Register 13-90. 25Ch Odd Ports – User Test Pattern Delay (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**SerDes 4 User Test Pattern Enable** 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 210h through 21Ch)) on SerDes 4 in Digital Far-End Loopback Master mode ***Notes: This bit and bit 24 (SerDes 4 PRBS Enable) are mutually exclusive functions and must not be enabled together for SerDes 4. The logical result of bit 24 ANDed with bit 16 must be 0.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the Port's Even/Odd Port Quiet register Hold Port x Quiet bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]) is Set.***	RW	Yes	0
17	**SerDes 5 User Test Pattern Enable** 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 210h through 21Ch)) on SerDes 5 in Digital Far-End Loopback Master mode ***Notes: This bit and bit 25 (SerDes 5 PRBS Enable) are mutually exclusive functions and must not be enabled together for SerDes 5. The logical result of bit 25 ANDed with bit 17 must be 0.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the Port's Even/Odd Port Quiet register Hold Port x Quiet bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]) is Set.***	RW	Yes	0
23:18	***Factory Test Only***	RW	Yes	0-0h

Register 13-90. 25Ch Odd Ports – User Test Pattern Delay (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**SerDes 4 PRBS Enable** 0 = Disables PRBS sequence generation/checking on SerDes 4 1 = Enables PRBS sequence generation/checking on SerDes 4 ***Notes: This bit and bit 16 (SerDes 4 User Test Pattern Enable) are mutually exclusive functions and must not be enabled together for SerDes 4. The logical result of bit 16 ANDed with bit 24 must be 0.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the Port's Even/Odd Port Quiet register Hold Port x Quiet bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]) is Set.***	RW	Yes	0
25	**SerDes 5 PRBS Enable** 0 = Disables PRBS sequence generation/checking on SerDes 5 1 = Enables PRBS sequence generation/checking on SerDes 5 ***Notes: This bit and bit 17 (SerDes 5 User Test Pattern Enable) are mutually exclusive functions and must not be enabled together for SerDes 5. The logical result of bit 17 ANDed with bit 25 must be 0.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the Port's Even/Odd Port Quiet register Hold Port x Quiet bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]) is Set.***	RW	Yes	0
23:18	***Factory Test Only***	RW	Yes	0-0h

13.14.3 Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)

This section details the Device-Specific Serial EEPROM registers. Table 13-20 defines the register map.

Table 13-20. Device-Specific Serial EEPROM Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Status Data from Serial EEPROM	Serial EEPROM Status / Serial EEPROM Control	260h
Serial EEPROM Buffer		264h
Serial EEPROM Clock Frequency		268h
Expansion ROM Base Address	***Reserved*** / Serial EEPROM 3rd Address Byte	26Ch

Register 13-91. 260h Serial EEPROM Status and Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Serial EEPROM Control				
12:0	**EepBlkAddr** Serial EEPROM Block Address for 32 KB.	RW	Yes	000h
15:13	**EepCmd[2:0]** Commands to the Serial EEPROM Controller. 000b = ***Reserved*** 001b = Data from bits [31:24] (**Status Data from Serial EEPROM** register) is written to the serial EEPROM's internal **Status** register 010b = Write four bytes of data from the EepBuf into the memory location pointed to by field [12:0] (*EepBlkAddr*) 011b = Read four bytes of data from the memory location pointed to by field [12:0] (*EepBlkAddr*) into the EepBuf 100b = Reset Write Enable latch 101b = Data from the serial EEPROM's internal **Status** register is written to bits [31:24] (**Status Data from Serial EEPROM** register) 110b = Set Write Enable latch 111b = ***Reserved*** ***Note:*** *For value of 001b, only bits [31, 27:26] can be written into the serial EEPROM's internal **Status** register.*	RW	Yes	000b

Register 13-91. 260h Serial EEPROM Status and Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Serial EEPROM Status					
17:16	**EepPrsnt[1:0]** Serial EEPROM Present status. 00b = Not present 01b = Serial EEPROM is present – validation signature verified 10b = ***Reserved*** 11b = Serial EEPROM is present – validation signature not verified		RO	No	00b
18	**EepCmdStatus** Serial EEPROM Command status. 0 = Serial EEPROM Command is complete 1 = Serial EEPROM Command is not complete		RO	No	0
19	***Reserved***		RsvdP	No	0
20	**EepBlkAddr Upper Bit** Serial EEPROM Block Address upper bit 13. Extends the serial EEPROM to 64 KB.		RW	Yes	0
21	**EepAddrWidth Override** 0 = Field [23:22] (*EepAddrWidth*) is RO 1 = Field [23:22] (*EepAddrWidth*) is software-writable		RW	Yes	0
23:22	**EepAddrWidth** Serial EEPROM Address width. If the addressing width cannot be determined, 00b is returned. A non-zero value is reported only if the validation signature (5Ah) is successfully read from the first serial EEPROM location. This field is usually RO; however, it is RW if bit 21 (*EepAddrWidth Override*) is Set. 00b = Undetermined 01b = 1 byte 10b = 2 bytes 11b = 3 bytes	Bit 21 = 0	RO	No	00b
		Bit 21 = 1	RW	No	00b

Register 13-91. 260h Serial EEPROM Status and Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">Status Data from Serial EEPROM[a]</td></tr>
<tr><td>24</td><td>EepRdy
Serial EEPROM RDY#.
0 = Serial EEPROM is ready to transmit data
1 = Write cycle is in progress</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>25</td><td>EepWen
Serial EEPROM Write enable.
0 = Serial EEPROM Write is disabled
1 = Serial EEPROM Write is enabled</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>27:26</td><td>EepBp[1:0]
Serial EEPROM Block-Write Protect bits. Block Protection options protect the top ¼, top ½, or the entire serial EEPROM. PEX 8604 Configuration data is stored in the lower addresses; therefore, when using Block Protection, the entire serial EEPROM should be protected with BP[1:0]=11b.
<table>
<tr><th rowspan="2">BP[1:0]</th><th rowspan="2">Level</th><th colspan="4">Array Addresses Protected, by Device Size</th></tr>
<tr><th>8 KB</th><th>16 KB</th><th>32 KB</th><th>64-KB</th></tr>
<tr><td>00b</td><td>0</td><td>None</td><td>None</td><td>None</td><td>None</td></tr>
<tr><td>01b</td><td>1
(top ¼)</td><td>1800h – 1FFFh</td><td>3000h – 3FFFh</td><td>6000h – 7FFFh</td><td>–</td></tr>
<tr><td>10b</td><td>2
(top ½)</td><td>1000h – 1FFFh</td><td>2000h – 3FFFh</td><td>4000h – 7FFFh</td><td>–</td></tr>
<tr><td>11b</td><td>3
(All)</td><td>0000h – 1FFFh</td><td>0000h – 3FFFh</td><td>0000h – 7FFFh</td><td>–</td></tr>
</table></td><td>RW</td><td>Yes</td><td>00b</td></tr>
</table>

Register 13-91. 260h Serial EEPROM Status and Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
30:28	**EepWrStatus** Serial EEPROM Write status. Value is 000b when the serial EEPROM is not in an internal Write cycle. ***Note:*** *The definition of this field varies among serial EEPROM manufacturers. Reads of the serial EEPROM's internal* ***Status*** *register can return 000b or 111b, depending upon the serial EEPROM that is used.*	RO	No	000b
31	**EepWpen** Serial EEPROM Write Protect enable. Overrides the internal serial EEPROM Write Protect WP# input and enables/disables Writes to the **Serial EEPROM Status** register (bits [23:16] of this register): • When WP#=H or this bit is Cleared, and bit 25 (*EepWen*) is Set, the **Serial EEPROM Status** register is writable • When WP#=L and this bit is Set, or bit 25 (*EepWen*) is Cleared, the **Serial EEPROM Status** register is write-protected ***Notes:*** *If the internal serial EEPROM Write Protect WP# input is Low, after software Sets the EepWen bit to write-protect the* ***Serial EEPROM Status*** *register, the EepWen value cannot be Cleared, nor can the EepBp[1:0] field be Cleared to disable Block Protection, until the WP# input is High.* *This bit is* ***not*** *implemented in certain serial EEPROMs. Refer to the serial EEPROM manufacturer's data sheet.*	RW	Yes	0

a. Within the serial EEPROM's internal ***Status*** *register, only bits [31, 27:26] can be written.*

Register 13-92. 264h Serial EEPROM Buffer (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**EepBuf** Serial EEPROM RW buffer. Read/Write command to the **Serial EEPROM Control** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 260h) results in a 4-byte Read/Write to/from the serial EEPROM device.	RW	Yes	0000_0000h

Register 13-93. 268h Serial EEPROM Clock Frequency (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
2:0	**EepFreq[2:0]** Serial EEPROM clock (EE_SK) frequency control. 000b = 1 MHz (default) 001b = 1.98 MHz 010b = 5 MHz 011b = 9.62 MHz 100b = 12.5 MHz 101b = 15.6 MHz 110b = 17.86 MHz 111b = ***Reserved***	RW	Yes	000b
7:3	***Reserved***	RsvdP	No	0-0h
10:8	**EepCsStHld[2:0]** CS to SCLK setup and hold timing, provided as a quantity of ½ EE_SK Clock cycles. 000b = Use default timing for EE_CS# setup and EE_CS# hold timing to the serial EEPROM, for EE_CS# active to EE_SK active delay, and EE_SK inactive to EE_CS# inactive delay, respectively 001b = Non-zero value adds that quantity of ½ EE_SK clocks delay to the default setup and hold timing, between EE_CS# active and EE_SK active, and between EE_SK inactive and EE_CS# inactive	RW	Yes	000b
15:11	***Reserved***	RsvdP	No	0-0h
16	**Expansion ROM Size** 0 = 16 KB 1 = 32 KB	RW	Yes	0
31:17	***Reserved***	RsvdP	No	0-0h

Register 13-94. 26Ch Serial EEPROM 3rd Address Byte (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
7:0	**Serial EEPROM 3rd Address Byte**	RW	Yes	00h
15:8	***Reserved***	RsvdP	No	00h
31:16	**Expansion ROM Base Address** Indicates the NT Port Expansion ROM Base address within the serial EEPROM. The value is dependent upon the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 268h[16]) value. The lower six bits, [21:16], map to serial EEPROM byte Address bits [15:10] (aligned to a 256-DWord (1-KB) boundary). The NT Port Expansion ROM must not straddle a 64-KB boundary within the serial EEPROM. 0020h = Default Base address in serial EEPROM for a 16-KB NT Port Expansion ROM (*Expansion ROM Size* bit is Cleared) is 2000h (8 KB). The serial EEPROM size must be at least 32 KB. 0040h = Default Base address in serial EEPROM for a 32-KB NT Port Expansion ROM (*Expansion ROM Size* bit is Set) is 4000h (16 KB). The serial EEPROM size must be at least 64 KB.	RW	Yes	0020h

13.14.4 Device-Specific Registers – Miscellaneous Control (Offset 28Ch)

This section details the Device-Specific Miscellaneous Control register. Table 13-21 defines the register map.

Table 13-21. Device-Specific Miscellaneous Control Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	Miscellaneous Control	28Ch

Register 13-95. 28Ch Miscellaneous Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**VC1 (2nd VC) Disable** Use of VC1 is disabled, by default. To support its use, this bit must be Cleared. 0 = Enables VC1 to be used 1 = Disables VC1 from use	RWS	Yes	1
3:1	***Factory Test Only***	RWS	Yes	000b
7:4	***Reserved***	RsvdP	No	0h
15:8	***Factory Test Only***	RWS	Yes	00h
31:16	***Reserved***	RsvdP	No	0000h

13.14.5 Device-Specific Registers – I2C Slave Interface (Offsets 290h – 2C4h)

This section details the Device-Specific I2C Slave Interface register. Table 13-22 defines the register map.

The I2C Slave Interface is described, in detail, in Section 7.2, "I2C Slave Interface."

Table 13-22. Device-Specific I2C Slave Interface Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Factory Test Only		290h
I2C Configuration		294h
Factory Test Only		298h – 2A8h
Reserved		2ACh
Factory Test Only		2B0h
Reserved		2B4h – 2BCh
Factory Test Only		2C0h – 2C4h

Register 13-96. 294h I2C Configuration (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default	
2:0	**Slave Address** Bits [6:0] comprise the I2C/SMBus Slave address, 38h. The value is determined by bits [2:0] (which reflect the I2C_ADDR[2:0] input states, and default to 000b, by virtue of weak internal pull-up resistors), combined with the value of bits [6:3] (which default to 0111b). When I2C_ADDR2=H, Address Resolution Protocol (ARP) is disabled ***and*** bit 2 defaults to a value of 1. ***Note: The I2C/SMBus Slave address must not be changed by an I2C/SMBus Write command.***	HwInit	Yes	000b	38h
6:3		RW	Yes	0111b	
9:7	***Reserved***	RsvdP	No	000b	
10	***Factory Test Only***	RW	Yes	0	
31:11	***Reserved***	RW	Yes	0-0h	

13.14.6 Device-Specific Registers – Bus Number CAM (Offsets 2C8h – 304h)

This section details the Device-Specific Bus Number Content-Addressable Memory (BusNoCAM) registers, which are used to determine the Configuration TLP Completion routing. These registers contain mirror copies of the **Primary Bus Number**, **Secondary Bus Number**, and **Subordinate Bus Number** registers (offset 18h[23:16, 15:8, and 7:0], respectively), for each PEX 8604 Port. Table 13-23 defines the register map.

The BusNoCAM registers are automatically updated by hardware. ***Modifying these registers by writing to the addresses listed here is not recommended.***

Table 13-23. Device-Specific BusNoCAM Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved		BusNoCAM0		2C8h
Reserved		BusNoCAM1		2CCh
Factory Test Only				2D0h – 2D4h
Reserved		BusNoCAM4		2D8h
Reserved		BusNoCAM5		2DCh
Factory Test Only/Reserved				2E0h – 304h

Register 13-97. 2C8h BusNoCAM0
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Mirror copy of Port 0 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 0 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 0 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

Register 13-98. 2CCh BusNoCAM1
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Mirror copy of Port 1 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 1 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 1 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

Register 13-99. 2D8h BusNoCAM4
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Mirror copy of Port 4 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 4 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 4 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

Register 13-100. 2DCh BusNoCAM5
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Primary Bus Number** Mirror copy of Port 5 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 5 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 5 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

13.14.7 Device-Specific Registers – I/O CAM (Offsets 308h – 340h)

This section details the Device-Specific I/O Content-Addressable Memory (IOCAM) registers, which are used to determine I/O Request routing. These registers contain mirror copies of the **I/O Base** and **I/O Limit** registers (offset 1Ch[7:0 and 15:8], respectively), for each PEX 8604 Port. Table 13-24 defines the register map.

The IOCAM registers are automatically updated by hardware. ***Modifying these registers by writing to the addresses listed here is not recommended.***

Table 13-24. Device-Specific IOCAM Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
IOCAM1		IOCAM0		308h
Factory Test Only				30Ch
IOCAM5		IOCAM4		310h
Factory Test Only/Reserved				314h – 340h

Register 13-101. 308h IOCAM0
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 0 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 0 I/O Limit value.	RW	Yes	0h

Register 13-102. 30Ah IOCAM1
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 1 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 1 I/O Limit value.	RW	Yes	0h

Register 13-103. 310h IOCAM4
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 4 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 4 I/O Limit value.	RW	Yes	0h

Register 13-104. 312h IOCAM5
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 5 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 5 I/O Limit value.	RW	Yes	0h

13.14.8 Device-Specific Registers – SMBus Slave Interface (Offset 344h)

This section details the Device-Specific SMBus Slave Interface register. Table 13-22 defines the register map.

The SMBus Slave Interface is described, in detail, in Section 7.3, "SMBus Slave Interface."

Table 13-25. Device-Specific SMBus Slave Interface Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
SMBus Configuration		344h

Register 13-105. 344h SMBus Configuration (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**SMBus Enable** Initially loaded from the STRAP_SMBUS_EN# input state. Value can later be changed by serial EEPROM and/or Configuration Space register Read Write. 0 = Disables SMBus for device configuration (I^2C mode is enabled) 1 = Enables SMBus for device configuration (SMBus mode is enabled)	RW	Yes	0 (STRAP_SMBUS_EN#=H) 1 (STRAP_SMBUS_EN#=L)
7:1	**SMBus Device Address** Set by the Address Resolution Protocol (ARP), if ARP is enabled. If ARP is disabled (I2C_ADDR2=H), defaults to 38h, with Address bit [1:0] values loaded from the I2C_ADDR[1:0] input states.	RW	Yes	00h (I2C_ADDR2=L) 38h (I2C_ADDR2=H)
8	**ARP Disable** 0 = Device under test is able to respond to ARP commands 1 = Device under test is unable to respond to ARP commands	RW	Yes	0 (I2C_ADDR2=L) 1 (I2C_ADDR2=H)
9	**PEC Check Disable** 0 = Enable PEC checking on all packets 1 = Disables Packet Error Checks (PECs) checking on all packets; packets with the wrong PECs are accepted	RW	Yes	0
10	**AV Flag** Address Valid (AV) flag. Set, by default, when ARP is disabled (I2C_ADDR2=H).	RW	Yes	0 (I2C_ADDR2=L) 1 (I2C_ADDR2=H)
11	**AR Flag** Address Resolved (AR) flag.	RW	Yes	0

Register 13-105. 344h SMBus Configuration (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
13:12	**UDID Address Type** Unique Device Identifier (UDID) Address type. 00b = I2C_ADDR2=H (ARP is disabled) 10b = I2C_ADDR2=L (ARP is enabled) All other encodings are ***reserved***.	RW	Yes	00b (I2C_ADDR2=H) 10b (I2C_ADDR2=L)
14	**UDID PEC Support** 1 = Sets the *PEC Support* bit in the UDID	RW	Yes	1
15	**SMBus Parameter Reload** Set this bit if bits [10, 8, or 7:1] (*AV Flag*, *ARP Disable*, or *SMBus Device Address*, respectively) are changed after a serial EEPROM load. Effective only when bit 28 (*SMBus Command In-Progress*) is Cleared.	RO	No	0
23:16	**UDID Vendor-Specific ID** Sets the MSB of the UDID Vendor-Specific ID. Bits [23:20] of this field are programmed by the I2C_ADDR[1:0] inputs. The four combinations provide the following ID values: 00b = 7000_0000h 01b = B000_0000h 10b = D000_0000h 11b = E000_0000h	RW	Yes	Set by I2C_ADDR[1:0] input levels
26:24	**UDID Revision ID** Program to 001b for Silicon Revision BA.	RW	Yes	001b
27	***Factory Test Only***	RW	Yes	0
28	**SMBus Command In-Progress** 0 = SMBus state machine is idle 1 = SMBus state machine is active (not idle)	RO	No	0
29	**PEC Check Failed** 0 = PEC checking successfully completed when receiving a packet 1 = PEC checking failed when receiving a packet	RW1C	No	0
30	**Unsupported SMBus Command** 0 = Command received from SMBus is a supported command 1 = Command received from SMBus is an unsupported command	RW1C	No	0
31	***Factory Test Only***	RW1C	No	0

13.14.9 Device-Specific Registers – Address-Mapping CAM (Offsets 348h – 444h)

This section details the Device-Specific Address-Mapping Content-Addressable Memory (AMCAM) registers, which are used to used to determine Memory Request routing. These registers contain mirror copies of the **Memory Base and Limit**, **Prefetchable Memory Base and Limit**, **Prefetchable Memory Upper Base Address**, and **Prefetchable Memory Upper Limit Address** registers (offsets 20h, 24h, 28h, and 2Ch, respectively), for each PEX 8604 Port. Table 13-26 defines the register map.

The AMCAM registers are automatically updated by hardware. ***Modifying these registers by writing to the addresses listed here is not recommended.***

Table 13-26. Device-Specific AMCAM Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
AMCAM0 Memory Limit		AMCAM0 Memory Base		348h
AMCAM0 Prefetchable Memory Limit		AMCAM0 Prefetchable Memory Base		34Ch
AMCAM0 Prefetchable Memory Base Upper 32 Bits				350h
AMCAM0 Prefetchable Memory Limit Upper 32 Bits				354h
AMCAM1 Memory Limit		AMCAM1 Memory Base		358h
AMCAM1 Prefetchable Memory Limit		AMCAM1 Prefetchable Memory Base		35Ch
AMCAM1 Prefetchable Memory Base Upper 32 Bits				360h
AMCAM1 Prefetchable Memory Limit Upper 32 Bits				364h
Factory Test Only				368h – 384h
AMCAM4 Memory Limit		AMCAM4 Memory Base		388h
AMCAM4 Prefetchable Memory Limit		AMCAM4 Prefetchable Memory Base		38Ch
AMCAM4 Prefetchable Memory Base Upper 32 Bits				390h
AMCAM4 Prefetchable Memory Limit Upper 32 Bits				394h
AMCAM5 Memory Limit		AMCAM5 Memory Base		398h
AMCAM5 Prefetchable Memory Limit		AMCAM5 Prefetchable Memory Base		39Ch
AMCAM5 Prefetchable Memory Base Upper 32 Bits				3A0h
AMCAM5 Prefetchable Memory Limit Upper 32 Bits				3A4h
Factory Test Only				3A8h – 3E4h
Factory Test Only/Reserved				3E8h – 444h

Register 13-106. 348h AMCAM0 Memory Base and Limit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM0 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM0 Memory Base** Mirror copy of Port 0 Memory Base value.	RW	Yes	FFFh
AMCAM0 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM0 Memory Limit** Mirror copy of Port 0 Memory Limit value.	RW	Yes	000h

Register 13-107. 34Ch AMCAM0 Prefetchable Memory Base and Limit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM0 Prefetchable Memory Base				
3:0	**AMCAM0 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM0 Prefetchable Memory Base** AMCAM0 Port 0 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM0 Prefetchable Memory Limit				
19:16	**AMCAM0 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM0 Prefetchable Memory Limit** AMCAM0 Port 0 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 13-108. 350h AMCAM0 Prefetchable Memory Base Upper 32 Bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**AMCAM0 Prefetchable Memory Base Upper 32 Bits** AMCAM0 Port 0 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 13-109. 354h AMCAM0 Prefetchable Memory Limit Upper 32 Bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**AMCAM0 Prefetchable Memory Limit Upper 32 Bits** AMCAM0 Port 0 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

Register 13-110. 358h AMCAM1 Memory Base and Limit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM1 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM1 Memory Base** Mirror copy of Port 1 Memory Base value.	RW	Yes	FFFh
AMCAM1 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM1 Memory Limit** Mirror copy of Port 1 Memory Limit value.	RW	Yes	000h

Register 13-111. 35Ch AMCAM1 Prefetchable Memory Base and Limit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM1 Prefetchable Memory Base				
3:0	**AMCAM1 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM1 Prefetchable Memory Base** AMCAM1 Port 1 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM1 Prefetchable Memory Limit				
19:16	**AMCAM1 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM1 Prefetchable Memory Limit** AMCAM1 Port 1 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 13-112. 360h AMCAM1 Prefetchable Memory Base Upper 32 Bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**AMCAM1 Prefetchable Memory Base Upper 32 Bits** AMCAM1 Port 1 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 13-113. 364h AMCAM1 Prefetchable Memory Limit Upper 32 Bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**AMCAM1 Prefetchable Memory Limit Upper 32 Bits** AMCAM1 Port 1 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

Register 13-114. 388h AMCAM4 Memory Base and Limit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM4 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM4 Memory Base** Mirror copy of Port 4 Memory Base value.	RW	Yes	FFFh
AMCAM4 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM4 Memory Limit** Mirror copy of Port 4 Memory Limit value.	RW	Yes	000h

Register 13-115. 38Ch AMCAM4 Prefetchable Memory Base and Limit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM4 Prefetchable Memory Base				
3:0	**AMCAM4 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM4 Prefetchable Memory Base** AMCAM4 Port 4 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM4 Prefetchable Memory Limit				
19:16	**AMCAM4 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM4 Prefetchable Memory Limit** AMCAM4 Port 4 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 13-116. 390h AMCAM4 Prefetchable Memory Base Upper 32 Bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**AMCAM4 Prefetchable Memory Base Upper 32 Bits** AMCAM4 Port 4 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 13-117. 394h AMCAM4 Prefetchable Memory Limit Upper 32 Bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**AMCAM4 Prefetchable Memory Limit Upper 32 Bits** AMCAM4 Port 4 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

Register 13-118. 398h AMCAM5 Memory Base and Limit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM5 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM5 Memory Base** Mirror copy of Port 5 Memory Base value.	RW	Yes	FFFh
AMCAM5 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM5 Memory Limit** Mirror copy of Port 5 Memory Limit value.	RW	Yes	000h

Register 13-119. 39Ch AMCAM5 Prefetchable Memory Base and Limit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM5 Prefetchable Memory Base				
3:0	**AMCAM5 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM5 Prefetchable Memory Base** AMCAM5 Port 5 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM5 Prefetchable Memory Limit				
19:16	**AMCAM5 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM5 Prefetchable Memory Limit** AMCAM5 Port 5 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 13-120. 3A0h AMCAM5 Prefetchable Memory Base Upper 32 Bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**AMCAM5 Prefetchable Memory Base Upper 32 Bits** AMCAM5 Port 5 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 13-121. 3A4h AMCAM5 Prefetchable Memory Limit Upper 32 Bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**AMCAM5 Prefetchable Memory Limit Upper 32 Bits** AMCAM5 Port 5 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

13.14.10 Device-Specific Registers – Vendor-Specific Dual Cast Extended Capability (Offsets 448h – 51Ch)

This section details the Device-Specific, Vendor-Specific Dual Cast Extended Capability registers. Table 13-27 defines the register map.

Table 13-27. Device-Specific, Vendor-Specific Dual Cast Extended Capability Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (950h or 520h)	Capability Version (1h) / PCI Express Extended Capability ID (000Bh)	448h
Vendor-Specific Header 1		44Ch
Dual Cast Low BAR0		450h
Dual Cast High BAR0		454h
Dual Cast Low BAR0 Translation		458h
Dual Cast High BAR0 Translation		45Ch
Dual Cast Low BAR0 Setup		460h
Dual Cast High BAR0 Setup		464h
Dual Cast Low BAR1		468h
Dual Cast High BAR1		46Ch
Dual Cast Low BAR1 Translation		470h
Dual Cast High BAR1 Translation		474h
Dual Cast Low BAR1 Setup		478h
Dual Cast High BAR1 Setup		47Ch
Dual Cast Low BAR2		480h
Dual Cast High BAR2		484h
Dual Cast Low BAR2 Translation		488h
Dual Cast High BAR2 Translation		48Ch
Dual Cast Low BAR2 Setup		490h
Dual Cast High BAR2 Setup		494h
Dual Cast Low BAR3		498h
Dual Cast High BAR3		49Ch
Dual Cast Low BAR3 Translation		4A0h
Dual Cast High BAR3 Translation		4A4h
Dual Cast Low BAR3 Setup		4A8h
Dual Cast High BAR3 Setup		4ACh
Dual Cast Low BAR4		4B0h
Dual Cast High BAR4		4B4h
Dual Cast Low BAR4 Translation		4B8h
Dual Cast High BAR4 Translation		4BCh

Table 13-27. Device-Specific, Vendor-Specific Dual Cast Extended Capability Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Dual Cast Low BAR4 Setup		4C0h
Dual Cast High BAR4 Setup		4C4h
Dual Cast Low BAR5		4C8h
Dual Cast High BAR5		4CCh
Dual Cast Low BAR5 Translation		4D0h
Dual Cast High BAR5 Translation		4D4h
Dual Cast Low BAR5 Setup		4D8h
Dual Cast High BAR5 Setup		4DCh
Dual Cast Low BAR6		4E0h
Dual Cast High BAR6		4E4h
Dual Cast Low BAR6 Translation		4E8h
Dual Cast High BAR6 Translation		4ECh
Dual Cast Low BAR6 Setup		4F0h
Dual Cast High BAR6 Setup		4F4h
Dual Cast Low BAR7		4F8h
Dual Cast High BAR7		4FCh
Dual Cast Low BAR7 Translation		500h
Dual Cast High BAR7 Translation		504h
Dual Cast Low BAR7 Setup		508h
Dual Cast High BAR7 Setup		50Ch
Dual Cast Source Destination Port		510h
Reserved		514h – 51Ch

Register 13-122. 448h Vendor-Specific Extended Capability Header (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID** Program to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.		RO	Yes	000Bh
19:16	**Capability Version**		RO	Yes	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset 950h.	Upstream	RO	Yes	950h
	Next extended capability is the **ACS Extended Capability** structure, offset 520h.	Downstream	RO	No	520h

Register 13-123. 44Ch Vendor-Specific Header 1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Vendor-Specific ID** ID Number of this Extended Capability structure.	RO	Yes	0000h
19:16	**Vendor-Specific Rev** Version Number of this structure.	RO	Yes	0h
31:20	**Vendor-Specific Length** Quantity of bytes in the entire structure.	RO	Yes	0CCh

Register 13-124. 450h Dual Cast Low BAR0 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	**Prefetchable** Not used, but included for software compatibility with respect to Base Address Register (BAR) definition.	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 13-125. 454h Dual Cast High BAR0 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0-0h

Register 13-126. 458h Dual Cast Low BAR0 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 13-127. 45Ch Dual Cast High BAR0 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR0** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 450h[2:1]) is programmed to 10b.	RW	Yes	0-0h
	Reserved when the **Dual Cast Low BAR0** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 450h[2:1]) is Cleared.	RsvdP	No	0-0h

Register 13-128. 460h Dual Cast Low BAR0 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 13-129. 464h Dual Cast High BAR0 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR0** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 450h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0-0h
	Reserved when the **Dual Cast Low BAR0** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 450h[2:1]) is Cleared.	RsvdP	No	0-0h

Register 13-130. 468h Dual Cast Low BAR1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 13-131. 46Ch Dual Cast High BAR1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 13-132. 470h Dual Cast Low BAR1 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 13-133. 474h Dual Cast High BAR1 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR1** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 468h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR1** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 468h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-134. 478h Dual Cast Low BAR1 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 13-135. 47Ch Dual Cast High BAR1 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR1** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 468h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR1** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 468h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-136. 480h Dual Cast Low BAR2 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 13-137. 484h Dual Cast High BAR2 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 13-138. 488h Dual Cast Low BAR2 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 13-139. 48Ch Dual Cast High BAR2 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR2** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 480h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR2** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 480h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-140. 490h Dual Cast Low BAR2 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 13-141. 494h Dual Cast High BAR2 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR2** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 480h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR2** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 480h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-142. 498h Dual Cast Low BAR3 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 13-143. 49Ch Dual Cast High BAR3 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 13-144. 4A0h Dual Cast Low BAR3 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 13-145. 4A4h Dual Cast High BAR3 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR3** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 498h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR3** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 498h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-146. 4A8h Dual Cast Low BAR3 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 13-147. 4ACh Dual Cast High BAR3 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR3** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 498h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR3** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 498h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-148. 4B0h Dual Cast Low BAR4 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 13-149. 4B4h Dual Cast High BAR4 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 13-150. 4B8h Dual Cast Low BAR4 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 13-151. 4BCh Dual Cast High BAR4 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR4** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4B0h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR4** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4B0h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-152. 4C0h Dual Cast Low BAR4 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 13-153. 4C4h Dual Cast High BAR4 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR4** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4B0h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR4** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4B0h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-154. 4C8h Dual Cast Low BAR5 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 13-155. 4CCh Dual Cast High BAR5 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 13-156. 4D0h Dual Cast Low BAR5 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 13-157. 4D4h Dual Cast High BAR5 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR5** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4C8h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR5** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4C8h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-158. 4D8h Dual Cast Low BAR5 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 13-159. 4DCh Dual Cast High BAR5 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR5** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4C8h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR5** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4C8h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-160. 4E0h Dual Cast Low BAR6 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 13-161. 4E4h Dual Cast High BAR6 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 13-162. 4E8h Dual Cast Low BAR6 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 13-163. 4ECh Dual Cast High BAR6 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR6** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4E0h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR6** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4E0h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-164. 4F0h Dual Cast Low BAR6 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 13-165. 4F4h Dual Cast High BAR6 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR6** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4E0h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR6** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4E0h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-166. 4F8h Dual Cast Low BAR7 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 13-167. 4FCh Dual Cast High BAR7 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 13-168. 500h Dual Cast Low BAR7 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 13-169. 504h Dual Cast High BAR7 Translation (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR7** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4F8h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR7** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4F8h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-170. 508h Dual Cast Low BAR7 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 13-171. 50Ch Dual Cast High BAR7 Setup (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR7** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4F8h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR7** register *Memory Map Type* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 4F8h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 13-172. 510h Dual Cast Source Destination Port (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port; *Reserved* (RsvdP) for the Dual Cast BAR Limit Lower register)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
3:0	**Dual Cast Source Port #** Valid only when bit 8 (*Dual Cast Source Port Enable*) is Set. Specifies the source (ingress) Port Number upon which Dual Cast BARs are applied. Encodings not listed are ***reserved***. 0h = Port 0 1h = Port 1 4h = Port 4 5h = Port 5	RW	Yes	0h
7:4	**Dual Cast Destination Port #** Specifies the destination (egress) Port Number to which Dual Cast BAR Translation addresses are mapped, and to which Dual Cast Copy TLPs will be queued. Encodings not listed are ***reserved***. 0h = Port 0 1h = Port 1 4h = Port 4 5h = Port 5	RW	Yes	0h

Register 13-172. 510h Dual Cast Source Destination Port (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port; *Reserved* (RsvdP) for the Dual Cast BAR Limit Lower register) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**Dual Cast Source Port Enable** 0 = Dual Cast applies to Write TLPs entering any Port on the Dual Cast Source Port. In that case, the field [3:0] (*Dual Cast Source Port #*) value is "Don't Care." 1 = Dual Cast applies only to Write TLPs entering the PEX 8604, by way of the Dual Cast Source Port Number specified in field [3:0].	RW	Yes	0
31:9	***Reserved***	RsvdP	No	0-0h

13.15 ACS Extended Capability Registers (Offsets 520h – 52Ch)

This section details the ACS Extended Capability registers. Table 13-28 defines the register map.

Table 13-28. ACS Extended Capability Register Map (Downstream Ports)

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved (Upstream)			520h
Next Capability Offset (950h) (Downstream)	Capability Version (1h) (Downstream)	PCI Express Extended Capability ID (000Dh) (Downstream)	
Reserved (Upstream)			524h
ACS Control (Downstream)		ACS Capability (Downstream)	
Reserved (Upstream)			528h
Reserved (Downstream)		Egress Control Vector (Downstream)	
Reserved			52Ch

Register 13-173. 520h ACS Extended Capability Header (Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Note: *Because this register is implemented as one physical register common to all Ports, the upstream Port's register (which is **reserved**) has the same value as the downstream Ports' registers. However in the upstream Port, the ACS Extended Capability is excluded from the Linked List of PCI Express Extended Capabilities; therefore, the upstream Port's register is effectively hidden from system software, and the non-zero value has no significant consequence.*					
15:0	***Reserved***	Upstream	RsvdP	No	0000h
	PCI Express Extended Capability ID	Downstream	RO	Yes	000Dh
19:16	***Reserved***	Upstream	RsvdP	No	0h
	Capability Version	Downstream	RO	Yes	1h
31:20	***Reserved***	Upstream	RsvdP	No	000h
	Next Capability Offset Program to 950h, which addresses the **Vendor-Specific Extended Capability 2** structure.	Downstream	RO	Yes	950h

Register 13-174. 524h ACS Control and Capability (All Transparent Downstream Ports; *Reserved* (RsvdP) for the Upstream Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
12:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Encodings 01h through FFh directly indicate the number of each downstream Port's **Egress Control Vector** register *Peer-to-Peer Port x Control* bit (Downstream Ports, offset 528h[5, 4, 1, 0]). ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	HwInit	Yes	10h
15:13	***Reserved***		RsvdP	No	000b

Register 13-174. 524h ACS Control and Capability
(All Transparent Downstream Ports; *Reserved* (RsvdP) for the Upstream Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Control					
16	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
17	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
18	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect Enable Enables or disables ACS Peer-to-Peer Request redirect. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
19	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect Enable Enables or disables ACS Peer-to-Peer Completion redirect. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control Enable Enables or disables ACS Peer-to-Peer Egress control. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable Enables or disables ACS Direct Translated Peer-to-Peer. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 13-175. 528h Egress Control Vector (All Downstream Ports; *Reserved* (RsvdP) for the Upstream Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
*Note: The Peer-to-Peer Port x Control bits are valid when the **ACS Control** register ACS P2P Egress Control Enable bit (Downstream Ports, offset 524h[21]) is Set.*					
0	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 0 Control 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
1	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 1 Control 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
3:2	***Factory Test Only***		RsvdP	No	00b
4	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 4 Control 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 5 Control 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
15:6	***Factory Test Only***		RsvdP	No	0-0h
31:16	***Reserved***		RsvdP	No	0000h

13.16 Device-Specific Registers (Offsets 530h – F8Ch)

This section details the Device-Specific registers located at offsets 530h through F8Ch. Device-Specific registers are unique to the PEX 8604 and not referenced in the *PCI Express Base r2.0*. Table 13-29 defines the register map.

Other Device-Specific registers are detailed in Section 13.14, "Device-Specific Registers (Offsets 1C0h – 51Ch)."

Note: It is recommended that these registers not be changed from their default values.

Table 13-29. Device-Specific Register Map (Offsets 530h – F8Ch)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Virtual Channel Weighted Round Robin Arbitration (Offsets 530h – 540h)		530h … 540h
Device-Specific Registers – Read Pacing (Offsets 544h – 554h)		544h … 554h
Factory Test Only		558h – 570h
Device-Specific Registers – Port Configuration (Offsets 574h – 628h)		574h … 628h
Device-Specific Registers – General-Purpose Input/Output (Offsets 62Ch – 65Ch)		62Ch … 65Ch
Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)		660h … 67Ch
Device-Specific Registers – IOCAM Base and Limit Upper 16 Bits (Offsets 680h – 6BCh)		680h … 6BCh
Device-Specific Registers – Base Address Shadow (Offsets 6C0h – 73Ch)		6C0h … 73Ch

Table 13-29. Device-Specific Register Map (Offsets 530h – F8Ch) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Virtual Channel Resource Control Shadow (Offsets 740h – 83Ch)		740h … 83Ch
Reserved		840h – 93Ch
Device-Specific Registers – Ingress Credit Handler Port Pool (Offsets 940h – 94Ch)		940h … 94Ch
Next Capability Offset 2 (000h)	1h / PCI Express Extended Capability ID 2 (000Bh)	950h
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)		… 95Ch
Factory Test Only		960h – 974h
Reserved		978h – 97Ch
Device-Specific Registers – ACS Extended Capability (Offsets 980h – 9FCh)		980h … 9FCh
Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch)		A00h … B7Ch
Device-Specific Registers – Physical Layer (Offsets B80h – C30h)		B80h … C30h
Reserved		C34h – DFCh
Device-Specific Registers – Port Configuration Header (Offsets E00h – E3Ch)		E00h … E3Ch
Reserved		E40h – EECh
Device-Specific Registers – Physical Layer (Offsets E40h – EFCh)		E40h … EFCh
Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F3Ch)		F00h … F3Ch
Device-Specific Registers – Error Reporting (Offsets F40h – F4Ch)		F40h … F4Ch
Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)		F50h … F8Ch

13.16.1 Device-Specific Registers – Virtual Channel Weighted Round Robin Arbitration (Offsets 530h – 540h)

This section details the Device-Specific Virtual Channel (VC) Weighted Round-Robin (WRR) Arbitration registers. Table 13-30 defines the register map.

Table 13-30. Device-Specific VC WRR Arbitration Register Map (Upstream Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Factory Test Only		Port 1 Weighted Round Robin Select	Port 0 Weighted Round Robin Select	530h
Factory Test Only		Port 5 Weighted Round Robin Select	Port 4 Weighted Round Robin Select	534h
Factory Test Only				538h
Reserved				53Ch
VC Fixed Arbitration Select				540h

Register 13-176. 530h VC WRR 0 (Upstream Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
For each Port, there are eight time slices to be divided amongst VC0 and VC1. A value of 0 indicates that VC0 has the "right of way," and similarly, a value of 1 indicates that VC1 has the "right of way." The default value, AAh, represents Round-Robin arbitration (equal access to each Port) for VC0 and VC1.				
7:0	**Port 0 Weighted Round Robin Select** 0 = VC0 1 = VC1	RW	Yes	AAh
15:8	**Port 1 Weighted Round Robin Select** 0 = VC0 1 = VC1	RW	Yes	AAh
31:16	***Factory Test Only***	RsvdP	No	0000h

Register 13-177. 534h VC WRR 1 (Upstream Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
For each Port, there are eight time slices to be divided amongst VC0 and VC1. A value of 0 indicates that VC0 has the "right of way," and similarly, a value of 1 indicates that VC1 has the "right of way." The default value, AAh, represents Round-Robin arbitration (equal access to each Port) for VC0 and VC1.				
7:0	**Port 4 Weighted Round Robin Select** 0 = VC0 1 = VC1	RW	Yes	AAh
15:8	**Port 5 Weighted Round Robin Select** 0 = VC0 1 = VC1	RW	Yes	AAh
31:16	***Factory Test Only***	RsvdP	No	0000h

Register 13-178. 540h VC Fixed Arbitration Select (Upstream Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Port 0 VC0 High Priority** 0 = VC1 is given higher priority over VC0 when fixed VC priority is selected 1 = VC0 is given higher priority over VC1 when Fixed VC Priority is selected	RW	Yes	0
1	**Port 1 VC0 High Priority** 0 = VC1 is given higher priority over VC0 when fixed VC priority is selected 1 = VC0 is given higher priority over VC1 when Fixed VC Priority is selected	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 VC0 High Priority** 0 = VC1 is given higher priority over VC0 when fixed VC priority is selected 1 = VC0 is given higher priority over VC1 when Fixed VC Priority is selected	RW	Yes	0
5	**Port 5 VC0 High Priority** 0 = VC1 is given higher priority over VC0 when fixed VC priority is selected 1 = VC0 is given higher priority over VC1 when Fixed VC Priority is selected	RW	Yes	0
15:6	***Factory Test Only***	RsvdP	No	0-0h
17:16	***Reserved***	RsvdP	No	00b
18	**VC1 Shares VC0 Port Arbitration Table** 0 = VC1 uses the default Port Arbitration table 1 = VC1 on the upstream Port uses the same, possibly programmed, table that VC0 uses	RW	Yes	0
31:19	***Reserved***	RsvdP	No	0-0h

13.16.2 Device-Specific Registers – Read Pacing (Offsets 544h – 554h)

Caution: ***Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.***

This section details the Device-Specific Read Pacing registers. Although the Read Pacing feature is supported on all Ports, its registers are implemented only on the upstream Port; otherwise, these registers are ***reserved***. Table 13-31 defines the register map.

Read Pacing is described, in detail, in Section 9.6, "Read Pacing."

Table 13-31. Device-Specific Read Pacing Register Map (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved (Upstream)		Read Pacing Control (Upstream)		544h
Reserved (Downstream)				
Reserved (Upstream)		Read Spreading Control (Upstream)		548h
Reserved (Downstream)				
Read Pacing Threshold 0 (Upstream)		***Reserved*** (Upstream)		54Ch
Reserved (Downstream)				
Read Pacing Threshold 1 (Upstream)				550h
Reserved (Downstream)				
Reserved (Upstream)		Read Counter Clear (Upstream)		554h
Reserved (Downstream)				

Register 13-179. 544h Read Pacing Control (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Caution: *Read Pacing and Source Queuing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.*					
0	**Port 0 Read Pacing Disable** 0 = Read Pacing is enabled for Port 0 1 = Read Pacing is disabled for Port 0	Upstream	RW	Yes	1
	Reserved	Downstream	RsvdP	No	0
1	**Port 1 Read Pacing Disable** 0 = Read Pacing is enabled for Port 1 1 = Read Pacing is disabled for Port 1	Upstream	RW	Yes	1
	Reserved	Downstream	RsvdP	No	0
3:2	***Factory Test Only***		RsvdP	No	00b
4	**Port 4 Read Pacing Disable** 0 = Read Pacing is enabled for Port 4 1 = Read Pacing is disabled for Port 4	Upstream	RW	Yes	1
	Reserved	Downstream	RsvdP	No	0
5	**Port 5 Read Pacing Disable** 0 = Read Pacing is enabled for Port 5 1 = Read Pacing is disabled for Port 5	Upstream	RW	Yes	1
	Reserved	Downstream	RsvdP	No	0
15:6	***Factory Test Only***		RsvdP	No	0-0h
31:16	***Reserved***		RsvdP	No	0000h

Register 13-180. 548h Read Spreading Control (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Caution: ***Memory Read Spreading and Source Queuing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.*** ***Note:*** *Read Pacing (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port, offset 544h) must be enabled for Read Spreading to be enabled. (That is, for a Port to have Read Spreading enabled, the corresponding Port bits in offset 544h and this register must both be Cleared.)*					
0	**Port 0 Memory Read Spreading Disable** 0 = Memory Read Spreading is enabled for Port 0 1 = Memory Read Spreading is disabled for Port 0	Upstream	RW	Yes	0
	Reserved	Downstream	RsvdP	No	0
1	**Port 1 Memory Read Spreading Disable** 0 = Memory Read Spreading is enabled for Port 1 1 = Memory Read Spreading is disabled for Port 1	Upstream	RW	Yes	0
	Reserved	Downstream	RsvdP	No	0
3:2	***Factory Test Only***		RsvdP	No	00b
4	**Port 4 Memory Read Spreading Disable** 0 = Memory Read Spreading is enabled for Port 4 1 = Memory Read Spreading is disabled for Port 4	Upstream	RW	Yes	0
	Reserved	Downstream	RsvdP	No	0
5	**Port 5 Memory Read Spreading Disable** 0 = Memory Read Spreading is enabled for Port 5 1 = Memory Read Spreading is disabled for Port 5	Upstream	RW	Yes	0
	Reserved	Downstream	RsvdP	No	0
15:6	***Factory Test Only***		RsvdP	No	0-0h
31:16	***Reserved***		RsvdP	No	0000h

Register 13-181. 54Ch Read Pacing Threshold 0 (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
	Reserved		RsvdP	No	
28:16	**MRd_Size_Outstanding_Threshold for x2 Port** Memory Read size outstanding threshold for x2 Ports. This Counter specifies the maximum DWord of Memory Read Requests that can be outstanding for a x2 Port. Default value of 400h programs the threshold to 4 KB.	Upstream	RW	Yes	400h
	Reserved	Downstream	RsvdP	No	000h
31:29	***Reserved***		RsvdP	No	000b

Register 13-182. 550h Read Pacing Threshold 1 (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
12:0	**MRd_Size_Outstanding_Threshold for x1 Port** Memory Read size outstanding threshold for x1 Ports. This Counter specifies the maximum DWord of Memory Read Requests that can be outstanding for a x1 Port. Default value of 100h programs the threshold to 1 KB.	Upstream	RW	Yes	100h
	Reserved	Downstream	RsvdP	No	000h
31:13	***Reserved***		RsvdP	No	0-0h

Register 13-183. 554h Read Counter Clear (Upstream Port, and also the NT Port Virtual Interface if the NT Port is a Legacy NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**Port 0 Reset_Outstanding_MRd_Size_Counter** Reset Outstanding Memory Read Size Counter for Port 0. Writing 1 to this bit resets the Outstanding Memory Read Request Size Counter for Port 0.	Upstream	RW1C	Yes	0
	Reserved	Downstream	RsvdP	No	0
1	**Port 1 Reset_Outstanding_MRd_Size_Counter** Reset Outstanding Memory Read Size Counter for Port 1. Writing 1 to this bit resets the Outstanding Memory Read Request Size Counter for Port 1.	Upstream	RW1C	Yes	0
	Reserved	Downstream	RsvdP	No	0
3:2	***Factory Test Only***		RsvdP	No	00b
4	**Port 4 Reset_Outstanding_MRd_Size_Counter** Reset Outstanding Memory Read Size Counter for Port 4. Writing 1 to this bit resets the Outstanding Memory Read Request Size Counter for Port 4.	Upstream	RW1C	Yes	0
	Reserved	Downstream	RsvdP	No	0
5	**Port 5 Reset_Outstanding_MRd_Size_Counter** Reset Outstanding Memory Read Size Counter for Port 5. Writing 1 to this bit resets the Outstanding Memory Read Request Size Counter for Port 5.	Upstream	RW1C	Yes	0
	Reserved	Downstream	RsvdP	No	0
15:6	***Factory Test Only***		RsvdP	No	0-0h
31:16	***Reserved***		RsvdP	No	0000h

13.16.3 Device-Specific Registers – Port Configuration (Offsets 574h – 628h)

This section details the Device-Specific Port Configuration register. Table 13-32 defines the register map.

Table 13-32. Device-Specific Port Configuration Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved		Port Configuration		574h
Factory Test Only				578h – 628h

Register 13-184. 574h Port Configuration (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The configurations for each Port are provided in Table 13-33.*				
1:0	**Port Configuration** Port Configuration Link width, per Port. The serial EEPROM bit values always override the STRAP_PORTCFG[1:0] Strapping inputs (if the serial EEPROM values are loaded; refer to Table 13-33). This register is reset only by a Fundamental Reset (PEX_PERST# assertion). 00b = x1, x1, x1, x1 01b = x2, x1, x1 10b = x2, x2 11b = ***Reserved***	RO	Yes	Set by STRAP_PORTCFG[1:0] input levels
15:2	***Reserved***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

Table 13-33. Port Configurations

STRAP_PORTCFG[1:0]	Port 0	Port 1	Port 4	Port 5
(default) 00b	**x1**	**x1**	**x1**	**x1**
01b	**x2**	**x1**		**x1**
10b	**x2**	**x2**		

13.16.4 Device-Specific Registers – General-Purpose Input/Output (Offsets 62Ch – 65Ch)

This section details the Device-Specific General-Purpose Input/Output (GPIO) Configuration, Status, and Control registers. Table 13-34 defines the register map.

Table 13-34. Device-Specific GPIO Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
GPIO 0_15 Direction Control				62Ch
GPIO 16, 29, 30 Direction Control				630h
Reserved				634h
GPIO 0_16, 29, 30 Input De-Bounce				638h
Reserved		GPIO 0_15 Input Data		63Ch
GPIO 16, 29, 30 Input Data				640h
Reserved		GPIO 0_15 Output Data		644h
GPIO 16, 29, 30 Output Data				648h
GPIO 0_16, 29, 30 Interrupt Polarity				64Ch
GPIO 0_16, 29, 30 Interrupt Status				650h
GPIO 0_16, 29, 30 Interrupt Mask				654h
Factory Test Only				658h – 65Ch

Register 13-185. 62Ch GPIO 0_15 Direction Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**GPIO0 Source/Destination** **As Input:** 0 = To **GPIO0 Input Data** register (offset 63Ch[0]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO0 Output Data** register (offset 644h[0]) 1 = Serial Hot Plug PERST# output for Hot Plug Virtual Port 0	RWS	Yes	0
1	**GPIO0 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
2	**GPIO1 Source/Destination** **As Input:** 0 = To **GPIO1 Input Data** register (offset 63Ch[1]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO1 Output Data** register (offset 644h[1]) 1 = Serial Hot Plug PERST# output for Hot Plug Virtual Port 1	RWS	Yes	0
3	**GPIO1 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
4	**GPIO2 Source/Destination** **As Input:** 0 = To **GPIO2 Input Data** register (offset 63Ch[2]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO2 Output Data** register (offset 644h[2]) 1 = ***Reserved***	RWS	Yes	0
5	**GPIO2 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
6	**GPIO3 Source/Destination** **As Input:** 0 = To **GPIO3 Input Data** register (offset 63Ch[3]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO3 Output Data** register (offset 644h[3]) 1 = ***Reserved***	RWS	Yes	0
7	**GPIO3 Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 13-185. 62Ch GPIO 0_15 Direction Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**GPIO4 Source/Destination** **As Input:** 0 = To **GPIO4 Input Data** register (offset 63Ch[4]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO4 Output Data** register (offset 644h[4]) 1 = Serial Hot Plug PERST# output for Hot Plug Virtual Port 4	RWS	Yes	0
9	**GPIO4 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
10	**GPIO5 Source/Destination** **As Input:** 0 = To **GPIO5 Input Data** register (offset 63Ch[5]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO5 Output Data** register (offset 644h[5]) 1 = Serial Hot Plug PERST# output for Hot Plug Virtual Port 5	RWS	Yes	0
11	**GPIO5 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
12	**GPIO6 Source/Destination** **As Input:** 0 = To **GPIO6 Input Data** register (offset 63Ch[6]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO6 Output Data** register (offset 644h[6]) 1 = ***Reserved***	RWS	Yes	0
13	**GPIO6 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
14	**GPIO7 Source/Destination** **As Input:** 0 = To **GPIO7 Input Data** register (offset 63Ch[7]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO7 Output Data** register (offset 644h[7]) 1 = ***Reserved***	RWS	Yes	0
15	**GPIO7 Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 13-185. 62Ch GPIO 0_15 Direction Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**GPIO8 Source/Destination** **As Input:** 0 = To **GPIO8 Input Data** register (offset 63Ch[8]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO8 Output Data** register (offset 644h[8]) 1 = ***Reserved***	RWS	Yes	0
17	**GPIO8 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
18	**GPIO9 Source/Destination** **As Input:** 0 = To **GPIO9 Input Data** register (offset 63Ch[9]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO9 Output Data** register (offset 644h[9]) 1 = ***Reserved***	RWS	Yes	0
19	**GPIO9 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
20	**GPIO10 Source/Destination** **As Input:** 0 = To **GPIO10 Input Data** register (offset 63Ch[10]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO10 Output Data** register (offset 644h[10]) 1 = ***Reserved***	RWS	Yes	0
21	**GPIO10 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
22	**GPIO11 Source/Destination** **As Input:** 0 = To **GPIO11 Input Data** register (offset 63Ch[11]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO11 Output Data** register (offset 644h[11]) 1 = ***Reserved***	RWS	Yes	0
23	**GPIO11 Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 13-185. 62Ch GPIO 0_15 Direction Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
24	**GPIO12 Source/Destination** **As Input:** 0 = To **GPIO12 Input Data** register (offset 63Ch[12]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO12 Output Data** register (offset 644h[12]) 1 = ***Reserved***	RWS	Yes	0
25	**GPIO12 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
26	**GPIO13 Source/Destination** **As Input:** 0 = To **GPIO13 Input Data** register (offset 63Ch[13]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO13 Output Data** register (offset 644h[13]) 1 = ***Reserved***	RWS	Yes	0
27	**GPIO13 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
28	**GPIO14 Source/Destination** **As Input:** 0 = To **GPIO14 Input Data** register (offset 63Ch[14]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO14 Output Data** register (offset 644h[14]) 1 = ***Reserved***	RWS	Yes	0
29	**GPIO14 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
30	**GPIO15 Source/Destination** **As Input:** 0 = To **GPIO15 Input Data** register (offset 63Ch[15]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO15 Output Data** register (offset 644h[15]) 1 = ***Reserved***	RWS	Yes	0
31	**GPIO15 Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 13-186. 630h GPIO 16, 29, 30 Direction Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**GPIO16 Source/Destination** **As Input:** 0 = To **GPIO16 Input Data** register (offset 640h[0]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO16 Output Data** register (offset 648h[0]) 1 = ***Reserved***	RWS	Yes	0
1	**GPIO16 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
25:2	***Reserved***	RsvdP	No	0-0h
26	**GPIO29 Source/Destination** **As Input:** 0 = To **GPIO29 Input Data** register (offset 640h[13]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO29 Output Data** register (offset 648h[13]) 1 = ***Reserved***	RWS	Yes	0
27	**GPIO29 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
28	**GPIO30 Source/Destination** **As Input:** 0 = To **GPIO30 Input Data** register (offset 640h[14]) 1 = General interrupt (INT*x*, MSI, or PEX_INTA#) **As Output:** 0 = From **GPIO30 Output Data** register (offset 648h[14]) 1 = ***Reserved***	RWS	Yes	0
29	**GPIO30 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
31:30	***Reserved***	RsvdP	No	00b

Register 13-187. 638h GPIO 0_16, 29, 30 Input De-Bounce (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
30, 29, 16:0	**GPIO*x* Input De-Bounce Control** Controls de-bounce when the corresponding GPIO*x* signal is configured as an input (offset 62Ch[*x*], is Cleared, where *x* is the bit number associated with that GPIO*x* signal). Bits [30, 29, 16:0] correspond to GPIO[30, 29, 16:0], respectively. 0 = GPIO*x* input is not de-bounced 1 = GPIO*x* input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0-0h
31, 28:17	***Reserved***	RsvdP	No	0-0h

Register 13-188. 63Ch GPIO 0_15 Input Data (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**GPIO0 Input Data** If GPIO0 is configured as an output (offset 62Ch[1], is Set), Reads return 0. If GPIO0 is configured as an input (offset 62Ch[1], is Cleared), Reads return the logic value of the voltage on GPIO0.	RO	No	0
1	**GPIO1 Input Data** If GPIO1 is configured as an output (offset 62Ch[3], is Set), Reads return 0. If GPIO1 is configured as an input (offset 62Ch[3], is Cleared), Reads return the logic value of the voltage on GPIO1.	RO	No	0
2	**GPIO2 Input Data** If GPIO2 is configured as an output (offset 62Ch[5], is Set), Reads return 0. If GPIO2 is configured as an input (offset 62Ch[5], is Cleared), Reads return the logic value of the voltage on GPIO2.	RO	No	0
3	**GPIO3 Input Data** If GPIO3 is configured as an output (offset 62Ch[7], is Set), Reads return 0. If GPIO3 is configured as an input (offset 62Ch[7], is Cleared), Reads return the logic value of the voltage on GPIO3.	RO	No	0
4	**GPIO4 Input Data** If GPIO4 is configured as an output (offset 62Ch[9], is Set), Reads return 0. If GPIO4 is configured as an input (offset 62Ch[9], is Cleared), Reads return the logic value of the voltage on GPIO4.	RO	No	0
5	**GPIO5 Input Data** If GPIO5 is configured as an output (offset 62Ch[11], is Set), Reads return 0. If GPIO5 is configured as an input (offset 62Ch[11], is Cleared), Reads return the logic value of the voltage on GPIO5.	RO	No	0
6	**GPIO6 Input Data** If GPIO6 is configured as an output (offset 62Ch[13], is Set), Reads return 0. If GPIO6 is configured as an input (offset 62Ch[13], is Cleared), Reads return the logic value of the voltage on GPIO6.	RO	No	0
7	**GPIO7 Input Data** If GPIO7 is configured as an output (offset 62Ch[15], is Set), Reads return 0. If GPIO7 is configured as an input (offset 62Ch[15], is Cleared), Reads return the logic value of the voltage on GPIO7.	RO	No	0

Register 13-188. 63Ch GPIO 0_15 Input Data
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**GPIO8 Input Data** If GPIO8 is configured as an output (offset 62Ch[17], is Set), Reads return 0. If GPIO8 is configured as an input (offset 62Ch[17], is Cleared), Reads return the logic value of the voltage on GPIO8.	RO	No	0
9	**GPIO9 Input Data** If GPIO9 is configured as an output (offset 62Ch[19], is Set), Reads return 0. If GPIO9 is configured as an input (offset 62Ch[19], is Cleared), Reads return the logic value of the voltage on GPIO9.	RO	No	0
10	**GPIO10 Input Data** If GPIO10 is configured as an output (offset 62Ch[21], is Set), Reads return 0. If GPIO10 is configured as an input (offset 62Ch[21], is Cleared), Reads return the logic value of the voltage on GPIO10.	RO	No	0
11	**GPIO11 Input Data** If GPIO11 is configured as an output (offset 62Ch[23], is Set), Reads return 0. If GPIO11 is configured as an input (offset 62Ch[23], is Cleared), Reads return the logic value of the voltage on GPIO11.	RO	No	0
12	**GPIO12 Input Data** If GPIO12 is configured as an output (offset 62Ch[25], is Set), Reads return 0. If GPIO12 is configured as an input (offset 62Ch[25], is Cleared), Reads return the logic value of the voltage on GPIO12.	RO	No	0
13	**GPIO13 Input Data** If GPIO13 is configured as an output (offset 62Ch[27], is Set), Reads return 0. If GPIO13 is configured as an input (offset 62Ch[27], is Cleared), Reads return the logic value of the voltage on GPIO13.	RO	No	0
14	**GPIO14 Input Data** If GPIO14 is configured as an output (offset 62Ch[29], is Set), Reads return 0. If GPIO14 is configured as an input (offset 62Ch[29], is Cleared), Reads return the logic value of the voltage on GPIO14.	RO	No	0
15	**GPIO15 Input Data** If GPIO15 is configured as an output (offset 62Ch[31], is Set), Reads return 0. If GPIO15 is configured as an input (offset 62Ch[31], is Cleared), Reads return the logic value of the voltage on GPIO15.	RO	No	0
31:16	***Reserved***	RsvdP	No	0000h

Register 13-189. 640h GPIO 16, 29, 30 Input Data (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**GPIO16 Input Data** If GPIO16 is configured as an output (offset 630h[1], is Set), Reads return 0. If GPIO16 is configured as an input (offset 630h[1], is Cleared), Reads return the logic value of the voltage on GPIO16.	RO	No	0
12:1	***Reserved***	RsvdP	No	0-0h
13	**GPIO29 Input Data** If GPIO29 is configured as an output (offset 630h[27], is Set), Reads return 0. If GPIO29 is configured as an input (offset 630h[27], is Cleared), Reads return the logic value of the voltage on GPIO29.	RO	No	0
14	**GPIO30 Input Data** If GPIO30 is configured as an output (offset 630h[29], is Set), Reads return 0. If GPIO30 is configured as an input (offset 630h[29], is Cleared), Reads return the logic value of the voltage on GPIO30.	RO	No	0
31:15	***Reserved***	RsvdP	No	0-0h

Register 13-190. 644h GPIO 0_15 Output Data
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**GPIO0 Output Data** If GPIO0 is configured as an output (offset 62Ch[1], is Set), the value written to this bit is immediately driven to the GPIO0 output. Reads return the value written.	RWS	Yes	0
1	**GPIO1 Output Data** If GPIO1 is configured as an output (offset 62Ch[3], is Set), the value written to this bit is immediately driven to the GPIO1 output. Reads return the value written.	RWS	Yes	0
2	**GPIO2 Output Data** If GPIO2 is configured as an output (offset 62Ch[5], is Set), the value written to this bit is immediately driven to the GPIO2 output. Reads return the value written.	RWS	Yes	0
3	**GPIO3 Output Data** If GPIO3 is configured as an output (offset 62Ch[7], is Set), the value written to this bit is immediately driven to the GPIO3 output. Reads return the value written.	RWS	Yes	0
4	**GPIO4 Output Data** If GPIO4 is configured as an output (offset 62Ch[9], is Set), the value written to this bit is immediately driven to the GPIO4 output. Reads return the value written.	RWS	Yes	0
5	**GPIO5 Output Data** If GPIO5 is configured as an output (offset 62Ch[11], is Set), the value written to this bit is immediately driven to the GPIO5 output. Reads return the value written.	RWS	Yes	0
6	**GPIO6 Output Data** If GPIO6 is configured as an output (offset 62Ch[13], is Set), the value written to this bit is immediately driven to the GPIO6 output. Reads return the value written.	RWS	Yes	0
7	**GPIO7 Output Data** If GPIO7 is configured as an output (offset 62Ch[15], is Set), the value written to this bit is immediately driven to the GPIO7 output. Reads return the value written.	RWS	Yes	0

Register 13-190. 644h GPIO 0_15 Output Data
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**GPIO8 Output Data** If GPIO8 is configured as an output (offset 62Ch[17], is Set), the value written to this bit is immediately driven to the GPIO8 output. Reads return the value written.	RWS	Yes	0
9	**GPIO9 Output Data** If GPIO9 is configured as an output (offset 62Ch[19], is Set), the value written to this bit is immediately driven to the GPIO9 output. Reads return the value written.	RWS	Yes	0
10	**GPIO10 Output Data** If GPIO10 is configured as an output (offset 62Ch[21], is Set), the value written to this bit is immediately driven to the GPIO10 output. Reads return the value written.	RWS	Yes	0
11	**GPIO11 Output Data** If GPIO11 is configured as an output (offset 62Ch[23], is Set), the value written to this bit is immediately driven to the GPIO11 output. Reads return the value written.	RWS	Yes	0
12	**GPIO12 Output Data** If GPIO12 is configured as an output (offset 62Ch[25], is Set), the value written to this bit is immediately driven to the GPIO12 output. Reads return the value written.	RWS	Yes	0
13	**GPIO13 Output Data** If GPIO13 is configured as an output (offset 62Ch[27], is Set), the value written to this bit is immediately driven to the GPIO13 output. Reads return the value written.	RWS	Yes	0
14	**GPIO14 Output Data** If GPIO14 is configured as an output (offset 62Ch[29], is Set), the value written to this bit is immediately driven to the GPIO14 output. Reads return the value written.	RWS	Yes	0
15	**GPIO15 Output Data** If GPIO15 is configured as an output (offset 62Ch[31], is Set), the value written to this bit is immediately driven to the GPIO15 output. Reads return the value written.	RWS	Yes	0
31:16	***Reserved***	RsvdP	No	0000h

Register 13-191. 648h GPIO 16, 29, 30 Output Data (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**GPIO16 Output Data** If GPIO16 is configured as an output (offset 630h[1], is Set), the value written to this bit is immediately driven to the GPIO16 output. Reads return the value written.	RWS	Yes	0
12:1	***Reserved***	RsvdP	No	0-0h
13	**GPIO29 Output Data** If GPIO29 is configured as an output (offset 630h[27], is Set), the value written to this bit is immediately driven to the GPIO29 output. Reads return the value written.	RWS	Yes	0
14	**GPIO30 Output Data** If GPIO30 is configured as an output (offset 630h[29], is Set), the value written to this bit is immediately driven to the GPIO30 output. Reads return the value written.	RWS	Yes	0
31:15	***Reserved***	RsvdP	No	0-0h

Register 13-192. 64Ch GPIO 0_16, 29, 30 Interrupt Polarity (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
30, 29, 16:0	**GPIO Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the corresponding GPIO*x* signal. Bits [30, 29, 16:0] correspond to GPIO[30, 29, 16:0], respectively. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0-0h
31, 28:17	***Reserved***	RsvdP	No	0-0h

Register 13-193. 650h GPIO 0_16, 29, 30 Interrupt Status (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be masked by their respective bits in the* ***GPIO 0_16, 29, 30 Interrupt Mask*** *register (offset 654h).*				
30, 29, 16:0	**GPIO Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the corresponding GPIO*x* signal. Bits [30, 29, 16:0] correspond to GPIO[30, 29, 16:0], respectively. 0 = GPIO interrupt is inactive. 1 = GPIO interrupt is active. Interrupt status remains Set, as long the corresponding GPIO*x* signal is asserted, and Clears on its own when the corresponding GPIO*x* input de-asserts to the inactive state.	RO	No	0-0h
31, 28:17	***Reserved***	RsvdP	No	0-0h

Register 13-194. 654h GPIO 0_16, 29, 30 Interrupt Mask (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective bits in the* ***GPIO 0_16, 29, 30 Interrupt Status*** *register (offset 650h).*				
30, 29, 16:0	**GPIO Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked for the corresponding GPIO*x* signal. Bits [30, 29, 16:0] correspond to GPIO[30, 29, 16:0], respectively. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	7FFFFh
31, 28:17	***Reserved***	RsvdP	No	0-0h

13.16.5 Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)

This section details the Device-Specific Ingress Control and Port Enable registers, which also include the **Negotiated Link Width**, **Port Cut-Thru Enable Status**, and **Ingress PLL RAM ECC 1-Bit Counter** registers. Table 13-35 defines the register map.

Table 13-35. Device-Specific Ingress Control and Port Enable Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Ingress Control				660h
Ingress Control Shadow				664h
Reserved		Port Enable Status		668h
Factory Test Only	Negotiated Link Width for Ports 0, 4, 5			66Ch
Reserved				670h
Reserved		Port Cut-Thru Enable Status		674h
Reserved			Ingress PLL RAM ECC 1-Bit Counter	678h
Factory Test Only				67Ch

Register 13-195. 660h Ingress Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
22:0	***Factory Test Only***	RWS	Yes	0-0h
23	**Expansion ROM Virtual Side** 0 = Expansion ROM is located on the NT Port Link Interface 1 = Expansion ROM is located on the NT Port Virtual Interface	RWS	Yes	0
25:24	***Factory Test Only***	RWS	Yes	00b
26	**Disable Upstream Port BAR0 and BAR1** 0 = Enables the upstream Port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, Upstream Port, offsets 10h and 14h, respectively) 1 = Disables upstream Port **BAR0** and **BAR1**	RWS	Yes	0
27	***Not used***	RWS	Yes	0
28	**Disable VGA BIOS Memory Access Decoding** 0 = Enables the **Bridge Control** register *VGA 16-Bit Decode Enable*, *VGA Enable*, and *ISA Enable* bits (offset 3Ch[20:18], respectively), and enables decoding of the PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are blocked) 1 = Disables the **Bridge Control** register *VGA 16-Bit Decode Enable*, *VGA Enable*, and *ISA Enable* bits (offset 3Ch[20:18], respectively), and disables decoding of the PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are ***not*** blocked)	RWS	Yes	1
30:29	***Factory Test Only***	RWS	Yes	00b
31	***Not used***	RWS	Yes	0

Register 13-196. 664h Ingress Control Shadow (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RsvdP	No	0
1	**Use Serial EEPROM Values for Ingress Credit Initialization** Allow Configuration with a Device Number that is not 0, that is accessing downstream devices, to be forwarded. When the Device Number is 0, the Configuration terminates in a UR. 0 = Use default values for ingress credit initialization 1 = Use serial EEPROM values for ingress credit initialization	RWS	Yes	0
3:2	***Factory Test Only***	RWS	Yes	00b
4	**Drop EP TLPs** Drop Endpoint TLPs. 1 = Endpoint TLP was dropped	RWS	Yes	0
5	**No Special Treatment for Relaxed Ordering Traffic** The PEX 8604 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, then that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled by Setting this bit. 1 = Device-Specific Relaxed Ordering Completion will not be flagged to the egress block	RWS	Yes	0
7:6	***Factory Test Only***	RWS	Yes	00b
8	**Drop ECRC TLPs** Drop End-to-end Cyclic Redundancy Check (ECRC) TLPs. 1 = ECRC TLP was dropped	RWS	Yes	0
10:9	**ACK TLP Counter Timeout** Sets the quantity of ingress TLP Acknowledges (ACKs) pending, which causes a high-priority ACK to be sent. 00b = 16 TLPs 01b = 8 TLPs 10b = 4 TLPs 11b = Feature is disabled	RWS	Yes	00b
11	**NT Error Message Drop** 0 = If the NT Port Link Interface receives an Uncorrectable Error Message that is routed to the Root Complex, the NT Port Link Interface reports a Malformed TLP error. 1 = Do not malform a Fatal Error Message received on the NT Port Link Interface with routing equal to 0, and instead, drop the packet and log the error in the **Link Error Status Virtual** register *Link Side Uncorrectable Error Message Drop Status* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h[3]). If the corresponding **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[3]) is Set, the NT Port Virtual Interface signals an Interrupt (INT*x*, MSI, or PEX_INTA#) to the Local Host through the upstream Port, if interrupts are enabled.	RWS	Yes	0

Register 13-196. 664h Ingress Control Shadow
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
14:12	***Factory Test Only***	RWS	Yes	000b
15	**INCH Credit Reserve Flag** A transition from 0 to 1indicates that I^2C has finished with all CSR to INCH Initialization registers, and credit reservation can proceed.	RWS	Yes	0
19:16	***Factory Test Only***	RWS	Yes	0h
20	**Ingress MWr32 Counter Disable** 0 = Enables Ingress Memory Write 32-Bit Counter 1 = Disables Ingress Memory Write 32-Bit Counter	RWS	Yes	0
21	**Ingress MWr64 Counter Disable** 0 = Enables Ingress Memory Write 64-Bit Counter 1 = Disables Ingress Memory Write 64-Bit Counter	RWS	Yes	0
22	**Ingress MSG Counter Disable** 0 = Enables Ingress Message Counter 1 = Disables Ingress Message Counter	RWS	Yes	0
23	**Ingress MRd32 Counter Disable** 0 = Enables Ingress Memory Read 32-Bit Counter 1 = Disables Ingress Memory Read 32-Bit Counter	RWS	Yes	0
24	**Ingress MRd64 Counter Disable** 0 = Enables Ingress Memory Read 64-Bit Counter 1 = Disables Ingress Memory Read 64-Bit Counter	RWS	Yes	0
25	**Ingress Other Non-Posted Counter Disable** 0 = Enables Ingress Other Non-Posted Counter 1 = Disables Ingress Other Non-Posted Counter	RWS	Yes	0
26	**Ingress and Egress DLLP ACK Counter Disable** 0 = Enables Ingress and Egress DLLP ACK Counter 1 = Disables Ingress and Egress DLLP ACK Counter	RWS	Yes	0
27	**Ingress and Egress DLLP UpdateFC-P Counter Disable** 0 = Enables Ingress and Egress DLLP UpdateFC-Posted Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Posted Counter	RWS	Yes	0
28	**Ingress and Egress DLLP UpdateFC-NP Counter Disable** 0 = Enables Ingress and Egress DLLP UpdateFC-Non-Posted Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Non-Posted Counter	RWS	Yes	0
29	**Ingress and Egress DLLP UpdateFC-CPL Counter Disable** 0 = Enables Ingress and Egress DLLP UpdateFC-Completion Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Completion Counter	RWS	Yes	0
31:30	***Not used***	RWS	Yes	00b

Register 13-197. 668h Port Enable Status (Port 0, and also the NT Port if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The value of this register depends upon the Port configuration (refer to Table 13-36 for a sample mapping).*				
0	**Port 0 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
1	**Port 1 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
5	**Port 5 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
15:6	***Factory Test Only***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

Table 13-36. Port Configurations

STRAP_PORTCFG[1:0]	Port 0	Port 1	Port 4	Port 5	Port Enable Status Register Value (Port 0, and also the NT Port if Port 0 is a Legacy NT Port, Offset 668h)
(default) 00b	**x1**	**x1**	**x1**	**x1**	Program the upper 16 bits to FFFFh. To determine the value for the lower 16 bits, start with 0h and Set only those bit positions that correspond to the enabled Ports. Bits [15:6, 3, 2] must be Cleared.
01b	**x2**	**x1**		**x1**	
10b	**x2**	**x2**			

Register 13-198. 66Ch Negotiated Link Width for Ports 0, 4, 5 (Port 0, and also the NT Port if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
2:0	**Negotiated Link Width for Port 0** 000b = x1 001b = x2 All other encodings are ***reserved***.	RO	No	000b
3	**Link Speed for Port 0** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
6:4	**Negotiated Link Width for Port 1** 000b = x1 010b = x2 All other encodings are ***reserved***.	RO	No	000b
7	**Valid Negotiated Link Width for Port 1** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
15:8	***Factory Test Only***	RsvdP	No	0-0h
18:16	**Negotiated Link Width for Port 4** 000b = x1 All other encodings are ***reserved***.	RO	No	000b
19	**Link Speed for Port 4** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
22:20	**Negotiated Link Width for Port 5** 000b = x1 All other encodings are ***reserved***.	RO	No	000b
23	**Valid Negotiated Link Width for Port 5** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
31:24	***Factory Test Only***	RsvdP	No	0000h

Register 13-199. 674h Port Cut-Thru Enable Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Port 0 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
1	**Port 1 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
5	**Port 5 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
15:6	***Factory Test Only***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-200. 678h Ingress PLL RAM ECC 1-Bit Counter (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**1-Bit ECC Counter for PLL RAM Read from Ingress Block** A Write of 0 to bit 0 Clears the ECC Counter.	RO	No	00h
31:8	***Reserved***	RsvdP	No	0000_00h

13.16.6 Device-Specific Registers – IOCAM Base and Limit Upper 16 Bits (Offsets 680h – 6BCh)

This section details the Device-Specific IOCAM Base and Limit Upper 16-Bit registers. Table 13-37 defines the register map.

Table 13-37. Device-Specific IOCAM Base and Limit Upper 16 Bits Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
IOCAM UP 0				680h
IOCAM UP 1				684h
Factory Test Only				688h – 68Ch
IOCAM UP 4				690h
IOCAM UP 5				694h
Factory Test Only/Reserved				698h – 6BCh

Register 13-201. 680h IOCAM UP 0 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

Register 13-202. 684h IOCAM UP 1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

Register 13-203. 690h IOCAM UP 4
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

Register 13-204. 694h IOCAM UP 5
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

13.16.7 Device-Specific Registers – Base Address Shadow (Offsets 6C0h – 73Ch)

This section details the Device-Specific Base Address Shadow registers, which are a shadow copy of the two Type 1 Configuration Base Address registers (**BAR0** and **BAR1**) for each PEX 8604 Port. Table 13-38 defines the register map.

Table 13-38. Device-Specific BAR Shadow Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
BAR0 Shadow for Port 0	6C0h
BAR1 Shadow for Port 0	6C4h
BAR0 Shadow for Port 1	6C8h
BAR1 Shadow for Port 1	6CCh
Factory Test Only	6D0h – 6DCh
BAR0 Shadow for Port 4	6E0h
BAR1 Shadow for Port 4	6E4h
BAR0 Shadow for Port 5	6E8h
BAR1 Shadow for Port 5	6ECh
Factory Test Only	6F0h – 70Ch
Reserved	710h – 73Ch

Register 13-205. 6C0h BAR0 Shadow for Port 0 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 0. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 0 Base Address 0.	RW	Yes	0000h

Register 13-206. 6C4h BAR1 Shadow for Port 0 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 0** register *Memory Map Type* field (offset 6C0h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 0 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 0** register *Memory Map Type* field (offset 6C0h[2:1]) is not programmed to 10b.	RsvdP	Yes	0000_0000h

Register 13-207. 6C8h BAR0 Shadow for Port 1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 1. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 1 Base Address 0.	RW	Yes	0000h

Register 13-208. 6CCh BAR1 Shadow for Port 1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 1** register *Memory Map Type* field (offset 6C8h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 1 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 1** register *Memory Map Type* field (offset 6C8h[2:1]) is not programmed to 10b.	RsvdP	No	0000_0000h

Register 13-209. 6E0h BAR0 Shadow for Port 4 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 4. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 4 Base Address 0.	RW	Yes	0000h

Register 13-210. 6E4h BAR1 Shadow for Port 4 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 4** register *Memory Map Type* field (offset 6E0h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 4 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 4** register *Memory Map Type* field (offset 6E0h[2:1]) is not programmed to 10b.	RsvdP	No	0000_0000h

Register 13-211. 6E8h BAR0 Shadow for Port 5 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 5. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 5 Base Address 0.	RW	Yes	0000h

Register 13-212. 6ECh BAR1 Shadow for Port 5 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 5** register *Memory Map Type* field (offset 6E8h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 5 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 5** register *Memory Map Type* field (offset 6E8h[2:1]) is not programmed to 10b.	RsvdP	No	0000_0000h

13.16.8 Device-Specific Registers – Virtual Channel Resource Control Shadow (Offsets 740h – 83Ch)

This section details the Device-Specific Virtual Channel (VC) Resource Control Shadow registers, for each Port (which shadow the VC0 and VC1 registers at offsets 15Ch and 168h, respectively). Table 13-39 defines the register map.

Table 13-39. Device-Specific VC Resource Control Shadow Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Port 0 VC0 Resource Control		740h
Port 0 VC1 Resource Control		744h
Port 1 VC0 Resource Control		748h
Port 1 VC1 Resource Control		74Ch
Factory Test Only	750h –	75Ch
Port 4 VC0 Resource Control		760h
Port 4 VC1 Resource Control		764h
Port 5 VC0 Resource Control		768h
Port 5 VC1 Resource Control		76Ch
Factory Test Only	770h –	7BCh
Reserved	7C0h –	83Ch

Register 13-213. 740h Port 0 VC0 Resource Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**TC/VC0 Map for Port 0** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.	RO	No	1
7:1		RW	Yes	7Fh
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table for Port 0** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.	RW	Yes	0
19:17	**Port Arbitration Select for Port 0** Selects the Port Arbitration type for Port 0. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. When WRR is enabled, the Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3; if the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = WRR with 32 Phases	RW	Yes	001b
		RW	Yes	000b
23:20	***Reserved***	RsvdP	No	0h
26:24	**VC0 ID for Port 0** Defines the Port 0 VC0 ID code. This field is Cleared, because VC0 is the default VC.	RO	No	000b
30:27	***Reserved***	RsvdP	No	0h
31	**VC0 Enable for Port 0** 0 = Not allowed 1 = Enables the Port 0 default VC, VC0	RO	No	1

Register 13-214. 744h Port 0 VC1 Resource Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**TC/VC1 Map for Port 0** Defines Traffic Classes [7:1], respectively, and indicates which TCs are mapped into VC1. Traffic Class 0 must be mapped to VC0. Traffic Classes [7:1] can be mapped to VC1.	RO	No	00h
7:1		RW	Yes	
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table for Port 0** ***Not supported*** Hardware writable and software readable.	RW	Yes	0
19:17	**Port Arbitration Select for Port 0** ***Not supported***	RW	Yes	000b
23:20	***Reserved***	RsvdP	No	0h
26:24	**VC1 ID for Port 0** Defines the Port 0 VC1 ID code.	RW	Yes	001b
30:27	***Reserved***	RsvdP	No	0h
31	**VC1 Enable for Port 0** 0 = Disables Port 0 VC1 1 = Enables Port 0 VC1	RW	Yes	0

Register 13-215. 748h Port 1 VC0 Resource Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**TC/VC0 Map for Port 1** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.	RO	No	1
7:1		RW	Yes	7Fh
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table for Port 1** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.	RW	Yes	0
19:17	**Port Arbitration Select for Port 1** Selects the Port Arbitration type for Port 1. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. When WRR is enabled, the Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3; if the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = WRR with 32 Phases	RW	Yes	001b
		RW	Yes	000b
23:20	***Reserved***	RsvdP	No	0h
26:24	**VC0 ID for Port 1** Defines the Port 1 VC0 ID code. This field is Cleared, because VC0 is the default VC.	RO	No	000b
30:27	***Reserved***	RsvdP	No	0h
31	**VC0 Enable for Port 1** 0 = Not allowed 1 = Enables the Port 1 default VC, VC0	RO	No	1

Register 13-216. 74Ch Port 1 VC1 Resource Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**TC/VC1 Map for Port 1** Defines Traffic Classes [7:1], respectively, and indicates which TCs are mapped into VC1. Traffic Class 0 must be mapped to VC0. Traffic Classes [7:1] can be mapped to VC1.	RO	No	00h
7:1		RW	Yes	
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table for Port 1** ***Not supported*** Hardware writable and software readable.	RW	Yes	0
19:17	**Port Arbitration Select for Port 1** ***Not supported***	RW	Yes	000b
23:20	***Reserved***	RsvdP	No	0h
26:24	**VC1 ID for Port 1** Defines the Port 1 VC1 ID code.	RW	Yes	001b
30:27	***Reserved***	RsvdP	No	0h
31	**VC1 Enable for Port 1** 0 = Disables Port 1 VC1 1 = Enables Port 1 VC1	RW	Yes	0

Register 13-217. 760h Port 4 VC0 Resource Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**TC/VC0 Map for Port 4** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0.	RO	No	1
7:1	Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.	RW	Yes	7Fh
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table for Port 4** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.	RW	Yes	0
19:17	**Port Arbitration Select for Port 4** Selects the Port Arbitration type for Port 4. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. When WRR is enabled, the Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3; if the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = WRR with 32 Phases	RW RW	Yes Yes	001b 000b
23:20	***Reserved***	RsvdP	No	0h
26:24	**VC0 ID for Port 4** Defines the Port 4 VC0 ID code. This field is Cleared, because VC0 is the default VC.	RO	No	000b
30:27	***Reserved***	RsvdP	No	0h
31	**VC0 Enable for Port 4** 0 = Not allowed 1 = Enables the Port 4 default VC, VC0	RO	No	1

Register 13-218. 764h Port 4 VC1 Resource Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**TC/VC1 Map for Port 4** Defines Traffic Classes [7:1], respectively, and indicates which TCs are mapped into VC1. Traffic Class 0 must be mapped to VC0. Traffic Classes [7:1] can be mapped to VC1.	RO	No	00h
7:1		RW	Yes	
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table for Port 4** ***Not supported*** Hardware writable and software readable.	RW	Yes	0
19:17	**Port Arbitration Select for Port 4** ***Not supported***	RW	Yes	000b
23:20	***Reserved***	RsvdP	No	0h
26:24	**VC1 ID for Port 4** Defines the Port 4 VC1 ID code.	RW	Yes	001b
30:27	***Reserved***	RsvdP	No	0h
31	**VC1 Enable for Port 4** 0 = Disables Port 4 VC1 1 = Enables Port 4 VC1	RW	Yes	0

Register 13-219. 768h Port 5 VC0 Resource Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**TC/VC0 Map for Port 5** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0.	RO	No	1
7:1	Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.	RW	Yes	7Fh
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table for Port 5** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.	RW	Yes	0
19:17	**Port Arbitration Select for Port 5** Selects the Port Arbitration type for Port 5. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. When WRR is enabled, the Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3; if the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = WRR with 32 Phases	RW RW	Yes Yes	001b 000b
23:20	***Reserved***	RsvdP	No	0h
26:24	**VC0 ID for Port 5** Defines the Port 5 VC0 ID code. This field is Cleared, because VC0 is the default VC.	RO	No	000b
30:27	***Reserved***	RsvdP	No	0h
31	**VC0 Enable for Port 5** 0 = Not allowed 1 = Enables the Port 5 default VC, VC0	RO	No	1

Register 13-220. 76Ch Port 5 VC1 Resource Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**TC/VC1 Map for Port 5** Defines Traffic Classes [7:1], respectively, and indicates which TCs are mapped into VC1. Traffic Class 0 must be mapped to VC0. Traffic Classes [7:1] can be mapped to VC1.	RO	No	00h
7:1		RW	Yes	
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table for Port 5** ***Not supported*** Hardware writable and software readable.	RW	Yes	0
19:17	**Port Arbitration Select for Port 5** ***Not supported***	RW	Yes	000b
23:20	***Reserved***	RsvdP	No	0h
26:24	**VC1 ID for Port 5** Defines the Port 5 VC1 ID code.	RW	Yes	001b
30:27	***Reserved***	RsvdP	No	0h
31	**VC1 Enable for Port 5** 0 = Disables Port 5 VC1 1 = Enables Port 5 VC1	RW	Yes	0

13.16.9 Device-Specific Registers – Ingress Credit Handler Port Pool (Offsets 940h – 94Ch)

This section details the Device-Specific Ingress Credit Handler (INCH) Port Pool registers. Table 13-40 defines the register map.

The original intent for the INCH Port Pool registers was to provide another level of reservation of the Common Pool credits. These registers are essentially redundant to what is accomplished by changing the values of the **INCH Threshold** registers. (Refer to Section 13.16.12.)

Consider the INCH Port Pool registers to be *reserved* and only change the credit Settings, using the INCH Threshold registers. Do not change the INCH Port Pool registers from their default values, unless directed otherwise by PLX Technical Support.

Refer to Section 9.3, "Ingress Resources," and its subsections, for further details regarding credits and credit allocation.

Table 13-40. Device-Specific INCH Port Pool Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Factory Test Only		INCH Port Pool for Ports 0, 1		940h
Factory Test Only		INCH Port Pool for Ports 4, 5		944h
Factory Test Only				948h
Reserved				94Ch

Register 13-221. 940h INCH Port Pool for Ports 0, 1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: Consider the INCH Port Pool registers to be reserved and only change the credit Settings, using the Ingress Credit Handler (INCH) registers. Do not change the INCH Port Pool registers from their default values, unless directed otherwise by PLX Technical Support.				
2:0	**Port 0 Payload Pool** Payload credits (other than the initial credits) for Posted/Completion TLPs dedicated to Port 0. 000b = 0 001b = 8 010b = 16 011b = 24 100b = 32 101b = 64 110b, 111b = 128	RWS	Yes	000b
3	**Unused 0** Keep value at 0. Additional bit for Port 0 Payload Pool.	RWS	Yes	0
6:4	**Port 0 Header Pool** Combined Header credits (other than the initial credits) dedicated to Port 0. 000b = 0 TLP 001b = 4 TLPs 010b = 8 TLPs 011b = 16 TLPs 100b = 32 TLPs 101b = 48 TLPs 110b, 111b = 64 TLPs	RWS	Yes	000b
7	**Unused 1** Keep value at 0. Additional bit for Port 0 Header Pool.	RWS	Yes	0

Register 13-221. 940h INCH Port Pool for Ports 0, 1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
10:8	**Port 1 Payload Pool** Payload credits (other than the initial credits) for Posted/Completion TLPs dedicated to Port 1. 000b = 0 001b = 8 010b = 16 011b = 24 100b = 32 101b = 64 110b, 111b = 128	RWS	Yes	000b
11	**Unused 2** Keep value at 0. Additional bit for Port 1 Payload Pool.	RWS	Yes	0
14:12	**Port 1 Header Pool** Combined Header credits (other than the initial credits) dedicated to Port 1. 000b = 0 TLP 001b = 4 TLPs 010b = 8 TLPs 011b = 16 TLPs 100b = 32 TLPs 101b = 48 TLPs 110b, 111b = 64 TLPs	RWS	Yes	000b
15	**Unused 3** Keep value at 0. Additional bit for Port 1 Header Pool.	RWS	Yes	0
31:16	***Factory Test Only***	RsvdP	No	0000h

Register 13-222. 944h INCH Port Pool for Ports 4, 5 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: Consider the INCH Port Pool registers to be reserved and only change the credit Settings, using the Ingress Credit Handler (INCH) registers. Do not change the INCH Port Pool registers from their default values, unless directed otherwise by PLX Technical Support.				
2:0	**Port 4 Payload Pool** Payload credits (other than the initial credits) for Posted/Completion TLPs dedicated to Port 4. 000b = 0 001b = 8 010b = 16 011b = 24 100b = 32 101b = 64 110b, 111b = 128	RWS	Yes	000b
3	**Unused 0** Keep value at 0. Additional bit for Port 4 Payload Pool.	RWS	Yes	0
6:4	**Port 4 Header Pool** Combined Header credits (other than the initial credits) dedicated to Port 4. 000b = 0 TLP 001b = 4 TLPs 010b = 8 TLPs 011b = 16 TLPs 100b = 32 TLPs 101b = 48 TLPs 110b, 111b = 64 TLPs	RWS	Yes	000b
7	**Unused 1** Keep value at 0. Additional bit for Port 4 Header Pool.	RWS	Yes	0

Register 13-222. 944h INCH Port Pool for Ports 4, 5 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
10:8	**Port 5 Payload Pool** Payload credits (other than the initial credits) for Posted/Completion TLPs dedicated to Port 5. 000b = 0 001b = 8 010b = 16 011b = 24 100b = 32 101b = 64 110b, 111b = 128	RWS	Yes	000b
11	**Unused 2** Keep value at 0. Additional bit for Port 5 Payload Pool.	RWS	Yes	0
14:12	**Port 5 Header Pool** Combined Header credits (other than the initial credits) dedicated to Port 5. 000b = 0 TLP 001b = 4 TLPs 010b = 8 TLPs 011b = 16 TLPs 100b = 32 TLPs 101b = 48 TLPs 110b, 111b = 64 TLPs	RWS	Yes	000b
15	**Unused 3** Keep value at 0. Additional bit for Port 5 Header Pool.	RWS	Yes	0
31:16	***Factory Test Only***	RsvdP	No	0-0h

13.16.10 Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)

This section details the Device-Specific, Vendor-Specific Extended Capability 2 registers. Table 13-41 defines the register map.

Table 13-41. Device-Specific, Vendor-Specific Extended Capability 2 Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 2 (000h) / Capability Version 2 (1h)	PCI Express Extended Capability ID 2 (000Bh)	950h
Vendor-Specific Header 2		954h
Hardwired Device ID	Hardwired Vendor ID	958h
Reserved	Hardwired Revision ID	95Ch

Register 13-223. 950h Vendor-Specific Extended Capability 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID 2** Program to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 2**	RO	Yes	1h
31:20	**Next Capability Offset 2** 000h = This extended capability is the last capability in the PEX 8604 Extended Capabilities list	RO	Yes	000h

Register 13-224. 954h Vendor-Specific Header 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**Vendor-Specific ID 2** ID Number of this Extended Capability structure.	RO	Yes	0001h
19:16	**Vendor-Specific Rev 2** Version Number of this structure.	RO	Yes	0h
31:20	**Vendor-Specific Length 2** Quantity of bytes in the entire structure.	RO	Yes	010h

Register 13-225. 958h PLX Hardwired Configuration ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Hardwired Vendor ID** Always returns the PLX PCI-SIG-assigned Vendor ID value, 10B5h.	RO	No	10B5h
31:16	**Hardwired Device ID** Always returns the PEX 8604 default Device ID value, 8604h.	RO	No	8604h

Register 13-226. 95Ch PLX Hardwired Revision ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Hardwired Revision ID** Always returns the PEX 8604 default PCI Revision ID value, BAh.	RO	No	Current Rev # (BAh)
31:8	***Reserved***	RsvdP	No	0000_00h

13.16.11 Device-Specific Registers – ACS Extended Capability (Offsets 980h – 9FCh)

This section details the Device-Specific ACS Extended Capability registers. The registers in this structure are shadow copies of the Port 0 registers located at offsets 524h and 528h, for each Port. Table 13-42 defines the register map.

Table 13-42. Device-Specific ACS Extended Capability Register Map (Port 0)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
ACS Port 0 Control		ACS Port 0 Capability		980h
Reserved		ACS Port 0 Egress Control Vector		984h
ACS Port 1 Control		ACS Port 1 Capability		988h
Reserved		ACS Port 1 Egress Control Vector		98Ch
Factory Test Only				990h – 99Ch
ACS Port 4 Control		ACS Port 4 Capability		9A0h
Reserved		ACS Port 4 Egress Control Vector		9A4h
ACS Port 5 Control		ACS Port 5 Capability		9A8h
Reserved		ACS Port 5 Egress Control Vector		9ACh
Factory Test Only				9B0h – 9CCh
Reserved				9D0h – 9FCh

Register 13-227. 980h ACS Port 0 Control and Capability (Port 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 0 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
12:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	10h
15:13	***Reserved***		RsvdP	No	000b

Register 13-227. 980h ACS Port 0 Control and Capability (Port 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
ACS Port 0 Control					
	Reserved	Upstream	RsvdP	No	0
16	**ACS Source Validation Enable** RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
17	**ACS Translation Blocking Enable** RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
18	**ACS P2P Request Redirect Enable** RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
19	**ACS P2P Completion Redirect Enable** RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 13-227. 980h ACS Port 0 Control and Capability (Port 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 13-228. 984h ACS Port 0 Egress Control Vector (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The Peer-to-Peer Port x Control bits are valid when the* ***ACS Port 0 Control*** *register ACS Egress Control Enable bit (offset 980h[21]) is Set.*				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
15:6	***Factory Test Only***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-229. 988h ACS Port 1 Control and Capability (Port 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 1 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
12:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	10h
15:13	***Reserved***		RsvdP	No	000b

Register 13-229. 988h ACS Port 1 Control and Capability (Port 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 1 Control					
16	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation Enable RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
17	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking Enable RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
18	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect Enable RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
19	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect Enable RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 13-229. 988h ACS Port 1 Control and Capability (Port 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 13-230. 98Ch ACS Port 1 Egress Control Vector (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The Peer-to-Peer Port x Control bits are valid when the* ***ACS Port 1 Control*** *register ACS Egress Control Enable bit (offset 988h[21]) is Set.*				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
15:6	***Factory Test Only***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-231. 9A0h ACS Port 4 Control and Capability (Port 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 4 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
12:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	10h
15:13	***Reserved***		RsvdP	No	000b

Register 13-231. 9A0h ACS Port 4 Control and Capability (Port 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 4 Control					
16	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation Enable RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
17	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking Enable RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
18	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect Enable RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
19	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect Enable RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 13-231. 9A0h ACS Port 4 Control and Capability (Port 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 13-232. 9A4h ACS Port 4 Egress Control Vector (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The Peer-to-Peer Port x Control bits are valid when the* ***ACS Port 4 Control*** *register ACS Egress Control Enable bit (offset 9A0h[21]) is Set.*				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
15:6	***Factory Test Only***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-233. 9A8h ACS Port 5 Control and Capability (Port 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 5 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
12:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	10h
15:13	***Reserved***		RsvdP	No	000b

Register 13-233. 9A8h ACS Port 5 Control and Capability (Port 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
ACS Port 5 Control					
	Reserved	Upstream	RsvdP	No	0
16	**ACS Source Validation Enable** RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
17	**ACS Translation Blocking Enable** RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
18	**ACS P2P Request Redirect Enable** RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
19	**ACS P2P Completion Redirect Enable** RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 13-233. 9A8h ACS Port 5 Control and Capability (Port 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 13-234. 9ACh ACS Port 5 Egress Control Vector (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The Peer-to-Peer Port x Control bits are valid when the* ***ACS Port 5 Control*** *register ACS Egress Control Enable bit (offset 9A8h[21]) is Set.*				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
15:6	***Factory Test Only***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

13.16.12 Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch)

This section details the Device-Specific Ingress Credit Handler (INCH) Threshold registers. **Changing credit values from default register values must be done carefully; otherwise the PEX 8604 will not properly function.** Refer to Section 9.3, "Ingress Resources," and its subsections, for detailed information regarding rules associated with changing the **INCH Threshold** registers. Table 13-43 defines the register map.

Table 13-43. Device-Specific INCH Threshold Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
INCH Threshold Port 0 VC0 Posted	A00h
INCH Threshold Port 0 VC0 Non-Posted	A04h
INCH Threshold Port 0 VC0 Completion	A08h
INCH Threshold Port 0 VC1 Posted	A0Ch
INCH Threshold Port 0 VC1 Non-Posted	A10h
INCH Threshold Port 0 VC1 Completion	A14h
INCH Threshold Port 1 VC0 Posted	A18h
INCH Threshold Port 1 VC0 Non-Posted	A1Ch
INCH Threshold Port 1 VC0 Completion	A20h
INCH Threshold Port 1 VC1 Posted	A24h
INCH Threshold Port 1 VC1 Non-Posted	A28h
INCH Threshold Port 1 VC1 Completion	A2Ch
Factory Test Only	A30h – A5Ch
INCH Threshold Port 4 VC0 Posted	A60h
INCH Threshold Port 4 VC0 Non-Posted	A64h
INCH Threshold Port 4 VC0 Completion	A68h
INCH Threshold Port 4 VC1 Posted	A6Ch
INCH Threshold Port 4 VC1 Non-Posted	A70h
INCH Threshold Port 4 VC1 Completion	A74h
INCH Threshold Port 5 VC0 Posted	A78h
INCH Threshold Port 5 VC0 Non-Posted	A7Ch
INCH Threshold Port 5 VC0 Completion	A80h
INCH Threshold Port 5 VC1 Posted	A84h
INCH Threshold Port 5 VC1 Non-Posted	A88h
INCH Threshold Port 5 VC1 Completion	A8Ch
Factory Test Only	A90h – AECh
Reserved	AF0h – B7Ch

Register 13-235. A00h, A18h, A60h, A78h INCH Threshold Port *x* VC0 Posted (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Posted credits are used for VC0 Memory Write and Message transactions. Port *x* is Ports 0, 1, 4, and 5 for register offsets A00h, A18h, A60h, and A78h, respectively. (Refer to Table 13-43.)				
2:0	***Reserved***	RsvdP	No	000b
8:3	**Posted Payload Credit** Default advertised Posted Payload credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is in units of 8. Each increment provides 8 Posted Payload credits (*for example*, Ah = 80 Posted Payload credits). Each credit means that 16 bytes of storage are reserved for Posted TLP Payload data. x1 Port = 64 Payload Credits x2 Port = 256 Payload Credits	RWS	Yes	Refer to Description
15:9	**Posted Header Credit** Default advertised Posted Header credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is 1 for 1. Each increment provides 1 Posted Header credit (*for example*, Ah = 10 Posted Header credits). Each credit means that storage is reserved for the entire Header of a Posted TLP. x1 Port = 7 Header Credits x2 Port = 26 Header Credits	RWS	Yes	Refer to Description

Register 13-235. A00h, A18h, A60h, A78h INCH Threshold Port *x* VC0 Posted (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
17:16	**UpdateFC High-Priority Threshold for Posted Payload Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	**UpdateFC High-Priority Threshold for Posted Header Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	**Congested Port Weight** If the effective rate Setting times the negotiated Port Link width equates to less than x1 or greater than x8, the internal Credit Allocation logic rounds to x1 or x8, respectively. Refer to Section 9.3.5, "Credit Allocation When Common Pool Is Consumed," for further details. 000b = Request is weighted, based upon the Port's Link width relative to the effective Link widths of the other Half Station's Ports 001b = Increases the weight of a Request by 2x 010b = Increases the weight of a Request by 4x 011b = Increases the weight of a Request by 8x 100b = Port receives no credit out of the common pool, until a decongested state is reached 101b = Decreases the weight of a Request by 2x 110b = Decreases the weight of a Request by 4x 111b = Decreases the weight of a Request by 8x	RWS	Yes	000b
31:23	***Reserved***	RsvdP	No	0-0h

Register 13-236. A04h, A1Ch, A64h, A7Ch INCH Threshold Port *x* VC0 Non-Posted (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Non-Posted credits are used for VC0 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transactions. Port *x* is Ports 0, 1, 4, and 5 for register offsets A04h, A1Ch, A64h, and A7Ch, respectively. (Refer to Table 13-43.)				
8:0	**Non-Posted Payload Credit** The Non-Posted Payload is stored with the Non-Posted Header; therefore Non-Posted Payload credit is always available. Because of this, the PEX 8604 hardwires this field to 000h (infinite credits).	RsvdP	Yes	000h
15:9	**Non-Posted Header Credit** Default advertised Non-Posted Header credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is 1 for 1. Each increment provides 1 Non-Posted Header credit (*for example*, Ah = 10 Non-Posted Header credits). Each credit means that storage is reserved for the entire Header of a Non-Posted TLP. x1 Port = 7 Header Credits x2 Port = 26 Header Credits	RWS	Yes	Refer to Description
17:16	**UpdateFC High-Priority Threshold for Non-Posted Payload Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	**UpdateFC High-Priority Threshold for Non-Posted Header Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	***Not used***	RWS	Yes	000b
23	***Reserved***	RsvdP	No	0

Register 13-236. A04h, A1Ch, A64h, A7Ch INCH Threshold Port *x* VC0 Non-Posted (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
27:24	**BIST Port Control, Destination Port** Determines the Destination Half Station and Port, for TLPs received by a Port.	RWS	Yes	0h
28	**BIST Port Control, Start of Chain** Used to enable injection of a fixed Header and Payload in the corresponding Reader. 1 = Indicates that a Port is at the beginning of the test chain	RW	Yes	0
29	**BIST Port Control, End of Chain** Used to cause packets to be dropped in the corresponding ingress decoder. 1 = Indicates that a Port is at the end of the test chain	RW	Yes	0
30	**BIST Port Status, Port Header Error** 1 = Indicates that a Header (that is received by a Port) does not compare with the expected value. Writing a 1 Clears this bit.	RW1C	No	0
31	**BIST Port Status, Port Payload Error** 1 = Indicates that a Payload (that is received by a Port) does not compare with the expected value. Writing a 1 Clears this bit.	RW1C	No	0

Register 13-237. A08h, A20h, A68h, A80h INCH Threshold Port *x* VC0 Completion (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Completion credits are used for VC0 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transaction Completions. Port *x* is Ports 0, 1, 4, and 5 for register offsets A08h, A20h, A68h, and A80h, respectively. (Refer to Table 13-43.)				
2:0	***Reserved***	RsvdP	No	000b
8:3	**Completion Payload Credit** Default advertised Completion Payload credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is in units of 8. Each increment provides 8 Completion Payload credits (*for example*, Ah = 80 Completion Payload credits). Each credit means that 16 bytes of storage are reserved for Completion TLP Payload data. x1 Port = 64 Payload Credits x2 Port = 224 Payload Credits	RWS	Yes	Refer to Description
15:9	**Completion Header Credit** Default advertised Completion Header credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is 1 for 1. Each increment provides 1 Completion Header credit (*for example*, Ah = 10 Completion Header credits). Each credit means that storage is reserved for the entire Header of a Completion TLP. x1 Port = 5 Header Credits x2 Port = 26 Header Credits	RWS	Yes	Refer to Description
17:16	**UpdateFC High-Priority Threshold for Completion Payload Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	**UpdateFC High-Priority Threshold for Completion Header Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	***Not used***	RWS	Yes	000b
31:23	***Reserved***	RsvdP	No	0-0h

Register 13-238. A0Ch, A24h, A6Ch, A84h INCH Threshold Port *x* VC1 Posted (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Posted credits are used for VC1 Memory Write and Message transactions. Port *x* is Ports 0, 1, 4, and 5 for register offsets A0Ch, A24h, A6Ch, and A84h, respectively. (Refer to Table 13-43.)				
2:0	***Reserved***	RsvdP	No	000b
8:3	**Posted Payload Credit** Default advertised Posted Payload credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is in units of 8. Each increment provides 8 Posted Payload credits (*for example*, Ah = 80 Posted Payload credits). Each credit means that 16 bytes of storage are reserved for Posted TLP Payload data. The PEX 8604 hardwires this field to 00h (infinite credits). ***Note:*** *The default initial credit is infinite. If VC1 is enabled, the user must calculate and program the needed optimal VC1 initial credit values. These values should be programmed, using a serial EEPROM.*	RWS	Yes	00h
15:9	**Posted Header Credit** Default advertised Posted Header credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is 1 for 1. Each increment provides 1 Posted Header credit (*for example*, Ah = 10 Posted Header credits). Each credit means that storage is reserved for the entire Header of a Posted TLP. The PEX 8604 hardwires this field to 00h (infinite credits). ***Note:*** *The default initial credit is infinite. If VC1 is enabled, the user must calculate and program the needed optimal VC1 initial credit values. These values should be programmed, using a serial EEPROM.*	RWS	Yes	00h

Register 13-238. A0Ch, A24h, A6Ch, A84h INCH Threshold Port *x* VC1 Posted (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
17:16	**UpdateFC High-Priority Threshold for Posted Payload Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	**UpdateFC High-Priority Threshold for Posted Header Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	**Congested Port Weight** If the effective rate Setting times the negotiated Port Link width equates to less than x1 or greater than x8, the internal Credit Allocation logic rounds to x1 or x8, respectively. Refer to Section 9.3.5, "Credit Allocation When Common Pool Is Consumed," for further details. 000b = Request is weighted, based upon the Port's Link width relative to the effective Link widths of the other Half Station's Ports 001b = Increases the weight of a Request by 2x 010b = Increases the weight of a Request by 4x 011b = Increases the weight of a Request by 8x 100b = Port receives no credit out of the common pool, until a decongested state is reached 101b = Decreases the weight of a Request by 2x 110b = Decreases the weight of a Request by 4x 111b = Decreases the weight of a Request by 8x	RWS	Yes	000b
31:23	***Reserved***	RsvdP	No	0-0h

Register 13-239. A10h, A28h, A70h, A88h INCH Threshold Port *x* VC1 Non-Posted (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Non-Posted credits are used for VC1 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transactions. Port *x* is Ports 0, 1, 4, and 5 for register offsets A10h, A28h, A70h, and A88h, respectively. (Refer to Table 13-43.)				
8:0	**Non-Posted Payload Credit** The Non-Posted Payload is stored with the Non-Posted Header; therefore Non-Posted Payload credit is always available. Because of this, the PEX 8604 hardwires this field to 000h (infinite credits).	RsvdP	Yes	000h
15:9	**Non-Posted Header Credit** Default advertised Non-Posted Header credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is 1 for 1. Each increment provides 1 Non-Posted Header credit (*for example*, Ah = 10 Non-Posted Header credits). Each credit means that storage is reserved for the entire Header of a Non-Posted TLP. The PEX 8604 hardwires this field to 00h (infinite credits). ***Note:*** *The default initial credit is infinite. If VC1 is enabled, the user must calculate and program the needed optimal VC1 initial credit values. These values should be programmed, using a serial EEPROM.*	RWS	Yes	00h
17:16	**UpdateFC High-Priority Threshold for Non-Posted Payload Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	**UpdateFC High-Priority Threshold for Non-Posted Header Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	***Not used***	RWS	Yes	000b
31:23	***Reserved***	RsvdP	No	0-0h

Register 13-240. A14h, A2Ch, A74h, A8Ch INCH Threshold Port *x* VC1 Completion (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Completion credits are used for VC1 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transaction Completions. Port *x* is Ports 0, 1, 4, and 5 for register offsets A14h, A2Ch, A74h, and A8Ch, respectively. (Refer to Table 13-43.)				
2:0	***Reserved***	RsvdP	No	000b
8:3	**Completion Payload Credit** Default advertised Completion Payload credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is in units of 8. Each increment provides 8 Completion Payload credits (*for example*, Ah = 80 Completion Payload credits). Each credit means that 16 bytes of storage are reserved for Completion TLP Payload data. The PEX 8604 hardwires this field to 00h (infinite credits). ***Note:*** *The default initial credit is infinite. If VC1 is enabled, the user must calculate and program the needed optimal VC1 initial credit values. These values should be programmed, using a serial EEPROM.*	RWS	Yes	00h
15:9	**Completion Header Credit** Default advertised Completion Header credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is 1 for 1. Each increment provides 1 Completion Header credit (*for example*, Ah = 10 Completion Header credits). Each credit means that storage is reserved for the entire Header of a Completion TLP. The PEX 8604 hardwires this field to 00h (infinite credits). ***Note:*** *The default initial credit is infinite. If VC1 is enabled, the user must calculate and program the needed optimal VC1 initial credit values. These values should be programmed, using a serial EEPROM.*	RWS	Yes	00h
17:16	**UpdateFC High-Priority Threshold for Completion Payload Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	**UpdateFC High-Priority Threshold for Completion Header Credit** Refer to Section 9.2.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	***Not used***	RWS	Yes	000b
31:23	***Reserved***	RsvdP	No	0-0h

13.16.13 Device-Specific Registers – Physical Layer (Offsets B80h – C30h)

This section details the Device-Specific Physical Layer (PHY) registers located at offsets B80h through C30h. Table 13-44 defines the register map.

Other Device-Specific PHY registers are detailed in:

- Section 13.14.2, "Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)"
- Section 13.16.15, "Device-Specific Registers – Physical Layer (Offsets E40h – EFCh)"

Table 13-44. Device-Specific PHY Register Map (Offsets B80h – C30h) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Factory Test Only	Even Ports – Loopback Master Status/Control			B80h
Factory Test Only	Odd Ports – Loopback Master Status/Control			B84h
Factory Test Only	Even Ports 0, 4 – Receiver Error Counters			B88h
Factory Test Only	Odd Ports 1, 5 – Receiver Error Counters			B8Ch
Reserved				B90h – B94h
Factory Test Only		SerDes Drive Level 0		B98h
Reserved				B9Ch
Factory Test Only		SerDes Drive Level 2		BA0h
Reserved				BA4h
Factory Test Only		Post-Cursor Emphasis Level 0		BA8h
Reserved				BACh
Factory Test Only		Post-Cursor Emphasis Level 2		BB0h
Reserved				BB4h
Factory Test Only			Receiver Equalization Level 0	BB8h
Factory Test Only			Receiver Equalization Level 1	BBCh
Signal Detect Level				BC0h
Factory Test Only				BC4h – C24h
SerDes Control				C28h
Factory Test Only				C2Ch – C30h

Register 13-241. B80h Even Ports – Loopback Master Status/Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Port 0 Loopback Master Entry Failed** 1 = Indicates that Port 0 failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the Port 0* ***Even Port Physical Layer Command/Status*** *register Port x Ready as Loopback Master bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 220h[3]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
1	***Factory Test Only***	RsvdP	No	0
2	**Port 4 Loopback Master Entry Failed** 1 = Indicates that Port 4 failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the Port 4* ***Even Port Physical Layer Command/Status*** *register Port x Ready as Loopback Master bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 220h[11]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
7:3	***Factory Test Only/Reserved***	RsvdP	No	0-0h
8	**Port 0 External Loopback Enable** 1 = Allows Port 0 to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when the Port's Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
9	***Factory Test Only***	RsvdP	No	0
10	**Port 4 External Loopback Enable** 1 = Allows Port 4 to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when the Port's Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
15:11	***Factory Test Only/Reserved***	RsvdP	No	0-0h
16	**PRBS Pattern Sync Status Device Lane 0** Diagnoses broken Loopback wiring, because no errors can be detected and counted until pattern sync is detected. Sync achieved is Active-High. 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
17	**PRBS Pattern Sync Status Device Lane 1** Diagnoses broken Loopback wiring, because no errors can be detected and counted until pattern sync is detected. Sync achieved is Active-High. 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
23:18	***Factory Test Only***	RsvdP	No	0-0h
31:24	***Factory Test Only***	RWS	Yes	00h

Register 13-242. B84h Odd Ports – Loopback Master Status/Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Port 1 Loopback Master Entry Failed** 1 = Indicates that Port 1 failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the Port 1* ***Odd Port Physical Layer Command/Status*** *register Port x Ready as Loopback Master bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 224h[3]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
1	***Factory Test Only***	RsvdP	No	0
2	**Port 5 Loopback Master Entry Failed** 1 = Indicates that Port 5 failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the Port 5* ***Odd Port Physical Layer Command/Status*** *register Port x Ready as Loopback Master bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 224h[11]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
7:3	***Factory Test Only/Reserved***	RsvdP	No	0-0h
8	**Port 1 External Loopback Enable** 1 = Allows Port 1 to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when the Port's Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
9	***Factory Test Only***	RsvdP	No	0
10	**Port 5 External Loopback Enable** 1 = Allows Port 5 to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when the Port's Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
15:11	***Factory Test Only/Reserved***	RsvdP	No	0-0h
16	**PRBS Pattern Sync Status Device Lane 4** Diagnoses broken Loopback wiring, because no errors can be detected and counted until pattern sync is detected. Sync achieved is Active-High. 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
17	**PRBS Pattern Sync Status Device Lane 5** Diagnoses broken Loopback wiring, because no errors can be detected and counted until pattern sync is detected. Sync achieved is Active-High. 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
23:18	***Factory Test Only***	RsvdP	No	0-0h
31:24	***Factory Test Only***	RWS	Yes	00h

Register 13-243. B88h Even Ports 0, 4 – Receiver Error Counters (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Port 0 Receiver Error Counter** When read, returns the quantity of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	RW1C	No	00h
15:8	***Factory Test Only***	RsvdP	No	00h
23:16	**Port 4 Receiver Error Counter** When read, returns the quantity of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	RW1C	No	00h
31:24	***Factory Test Only***	RsvdP	No	00h

Register 13-244. B8Ch Odd Ports 1, 5 – Receiver Error Counters (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Port 1 Receiver Error Counter** When read, returns the quantity of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	RW1C	No	00h
15:8	***Factory Test Only***	RsvdP	No	00h
23:16	**Port 5 Receiver Error Counter** When read, returns the quantity of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	RW1C	No	00h
31:24	***Factory Test Only***	RsvdP	No	00h

Register 13-245. B98h SerDes Drive Level 0 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **Post-Cursor Emphasis Level 0** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset BA8h) default value, provides -3.5 dB of de-emphasis. However, it is also a Status register with provisional read-back data. The power-up reset default values of this register correspond to -3.5 dB drive levels, and can be overwritten by serial EEPROM and/or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Note:*** *Refer to Section 19.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **Post-Cursor Emphasis Level 0** register.*				
4:0	**SerDes 0 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Eh.	RWS	Yes	10h (2.5 GT/s, -3.5 db) 0Eh (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 0 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 1 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Eh.	RWS	Yes	10h (2.5 GT/s, -3.5 db) 0Eh (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 1 Auto Load Disable**	RWS	Yes	0
31:16	***Factory Test Only***	RsvdP	No	0000h

Register 13-246. BA0h SerDes Drive Level 2 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **Post-Cursor Emphasis Level 2** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset BB0h) default value, provides -3.5 dB of de-emphasis. However, it is also a Status register with provisional read-back data. The power-up reset default values of this register correspond to -3.5 dB drive levels, and can be overwritten by serial EEPROM and/or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Note:*** *Refer to Section 19.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **Post-Cursor Emphasis Level 2** register.*				
4:0	**SerDes 4 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Eh.	RWS	Yes	10h (2.5 GT/s, -3.5 db) 0Eh (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 4 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 5 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Eh.	RWS	Yes	10h (2.5 GT/s, -3.5 db) 0Eh (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 5 Auto Load Disable**	RWS	Yes	0
31:16	***Factory Test Only***	RsvdP	No	0000h

Register 13-247. BA8h Post-Cursor Emphasis Level 0 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **SerDes Drive Level 0** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset B98h) default value, provides -3.5 dB of de-emphasis. The power-up value can be overwritten by serial EEPROM and/or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Note:*** *Refer to Section 19.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **SerDes Drive Level 0** register.*				
4:0	**SerDes 0 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 db) 15h (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 0 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 1 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 db) 15h (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 1 Auto Load Disable**	RWS	Yes	0
31:16	***Factory Test Only***	RsvdP	No	0000h

Register 13-248. BB0h Post-Cursor Emphasis Level 2 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **SerDes Drive Level 2** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset BA0h) default value, provides -3.5 dB of de-emphasis. The power-up value can be overwritten by serial EEPROM and/or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Note:*** *Refer to Section 19.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **SerDes Drive Level 2** register.*				
4:0	**SerDes 4 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 db) 15h (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 4 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 5 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 db) 15h (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 5 Auto Load Disable**	RWS	Yes	0
31:16	***Factory Test Only***	RsvdP	No	0000h

Register 13-249. BB8h Receiver Equalization Level 0 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides the Receiver Equalization Level control for the lower SerDes.				
3:0	**SerDes 0 Receiver Equalization Level**	RWS	Yes	0h
7:4	**SerDes 1 Receiver Equalization Level**	RWS	Yes	0h
31:8	***Factory Test Only***	RsvdP	No	0000_00h

Rx Equalization[3:0]	Equalization	Rx Equalization[3:0]	Equalization
0h (default)	Off	7h to 9h	Medium
1h	Minimum	Ah to Dh	High to Medium
2h to 3h	Low	Eh to Fh	Maximum
4h to 6h	Low to Medium		

Register 13-250. BBCh Receiver Equalization Level 1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides the Receiver Equalization Level control for the upper SerDes.				
3:0	**SerDes 4 Receiver Equalization Level**	RWS	Yes	0h
7:4	**SerDes 5 Receiver Equalization Level**	RWS	Yes	0h
31:8	***Factory Test Only/Reserved***	RsvdP	No	0000_00h

Rx Equalization[3:0]	Equalization	Rx Equalization[3:0]	Equalization
0h (default)	Off	7h to 9h	Medium
1h	Minimum	Ah to Dh	High to Medium
2h to 3h	Low	Eh to Fh	Maximum
4h to 6h	Low to Medium		

Register 13-251. BC0h Signal Detect Level (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register provides the Receiver Signal Detect Level select. Each two-bit field in this register provides four Settings for detecting Electrical Idle Analog, for the corresponding SerDes. 00b = Approximately 50 to 80 mV 01b = Approximately 65 to 175 mV (default) 10b = Approximately 75 to 200 mV 11b = Approximately 120 to 240 mV				
1:0	**SerDes 0 Signal Detect Level**	RWS	Yes	01b
3:2	**SerDes 1 Signal Detect Level**	RWS	Yes	01b
15:4	***Factory Test Only***	RsvdP	No	000h
17:16	**SerDes 4 Signal Detect Level**	RWS	Yes	01b
19:18	**SerDes 5 Signal Detect Level**	RWS	Yes	01b
31:20	***Factory Test Only/Reserved***	RsvdP	No	000h

Register 13-252. C28h SerDes Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register controls SerDes logic parameters.				
2:0	**Receiver Detect Time Select** Selects the Receiver Detect timing. 000b = 1.0 µs 001b = 2.0 µs 010b = 4.0 µs (default) 011b = 5.0 µs 100b = 10.0 µs 101b = 20.0 µs 110b = 40.0 µs 111b = 50.0 µs	RWS	Yes	010b
3	***Reserved***	RsvdP	No	0
7:4	***Factory Test Only***	RWS	Yes	Fh
15:8	***Reserved***	RsvdP	No	00h

Register 13-252. C28h SerDes Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**Port 0 Electrical Idle Inference Disable** 0 = Electrical Idle inference is enabled, if the **Even Port Electrical Idle for Compliance Mask** register *SerDes x Mask Electrical Idle Detect* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 200h[9:8]) are Set, for the SerDes associated with the Port. 1 = Overall Electrical Idle inference logic is disabled on the corresponding Port. Electrical Idle inference during the *Recovery.Speed* state is not affected and will continue to operate.	RWS	Yes	0
17	**Port 1 Electrical Idle Inference Disable** 0 = Electrical Idle inference is enabled, if the **Odd Port Electrical Idle for Compliance Mask** register *SerDes x Mask Electrical Idle Detect* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 204h[9:8]) are Set, for the SerDes associated with the Port. 1 = Overall Electrical Idle inference logic is disabled on the corresponding Port. Electrical Idle inference during the *Recovery.Speed* state is not affected and will continue to operate.	RWS	Yes	0
19:18	***Factory Test Only***	RsvdP	No	00b
20	**Port 4 Electrical Idle Inference Disable** 0 = Electrical Idle inference is enabled, if the **Even Port Electrical Idle for Compliance Mask** register *SerDes x Mask Electrical Idle Detect* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 200h[9:8]) are Set, for the SerDes associated with the Port. 1 = Overall Electrical Idle inference logic is disabled on the corresponding Port. Electrical Idle inference during the *Recovery.Speed* state is not affected and will continue to operate.	RWS	Yes	0
21	**Port 5 Electrical Idle Inference Disable** 0 = Electrical Idle inference is enabled, if the **Odd Port Electrical Idle for Compliance Mask** register *SerDes x Mask Electrical Idle Detect* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 204h[9:8]) are Set, for the SerDes associated with the Port. 1 = Overall Electrical Idle inference logic is disabled on the corresponding Port. Electrical Idle inference during the *Recovery.Speed* state is not affected and will continue to operate.	RWS	Yes	0
31:22	***Factory Test Only***	RsvdP	No	0-0h

13.16.14 Device-Specific Registers – Port Configuration Header (Offsets E00h – E3Ch)

This section details the Device-Specific Port Configuration Header registers, for each Port. Table 13-45 defines the register map.

Table 13-45. Device-Specific Port Configuration Header Register Map (Port 0)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Command Port 1		PCI Command Port 0		E00h
Factory Test Only				E04h
PCI Command Port 5		PCI Command Port 4		E08h
Factory Test Only/Reserved				E0Ch – E1Ch
Bridge Control Port 1		Bridge Control Port 0		E20h
Factory Test Only				E24h
Bridge Control Port 5		Bridge Control Port 4		E28h
Factory Test Only/Reserved				E2Ch – E3Ch

Register 13-253. E00h PCI Command Port 0 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**I/O Access Enable** 0 = PEX 8604 ignores I/O Space accesses on Port 0's primary interface 1 = PEX 8604 responds to I/O Space accesses on Port 0's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8604 ignores Memory Space accesses on Port 0's primary interface 1 = PEX 8604 responds to Memory Space accesses on Port 0's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8604 Memory and I/O Request forwarding upstream. Neither affect Message (including INT*x* Interrupt Messages) forwarding nor Completions traveling upstream or downstream. 0 = PEX 8604 handles Memory and I/O Requests received on Port 0's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8604 returns a Completion with UR Completion status 1 = PEX 8604 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 13-254. E02h PCI Command Port 1 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**I/O Access Enable** 0 = PEX 8604 ignores I/O Space accesses on Port 1's primary interface 1 = PEX 8604 responds to I/O Space accesses on Port 1's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8604 ignores Memory Space accesses on Port 1's primary interface 1 = PEX 8604 responds to Memory Space accesses on Port 1's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8604 Memory and I/O Request forwarding upstream. Neither affect Message (including INT*x* Interrupt Messages) forwarding nor Completions traveling upstream or downstream. 0 = PEX 8604 handles Memory and I/O Requests received on Port 1's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8604 returns a Completion with UR Completion status 1 = PEX 8604 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 13-255. E08h PCI Command Port 4 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**I/O Access Enable** 0 = PEX 8604 ignores I/O Space accesses on Port 4's primary interface 1 = PEX 8604 responds to I/O Space accesses on Port 4's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8604 ignores Memory Space accesses on Port 4's primary interface 1 = PEX 8604 responds to Memory Space accesses on Port 4's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8604 Memory and I/O Request forwarding upstream. Neither affect Message (including INT*x* Interrupt Messages) forwarding nor Completions traveling upstream or downstream. 0 = PEX 8604 handles Memory and I/O Requests received on Port 4's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8604 returns a Completion with UR Completion status 1 = PEX 8604 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 13-256. E0Ah PCI Command Port 5 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**I/O Access Enable** 0 = PEX 8604 ignores I/O Space accesses on Port 5's primary interface 1 = PEX 8604 responds to I/O Space accesses on Port 5's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8604 ignores Memory Space accesses on Port 5's primary interface 1 = PEX 8604 responds to Memory Space accesses on Port 5's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8604 Memory and I/O Request forwarding upstream. Neither affect Message (including INT*x* Interrupt Messages) forwarding nor Completions traveling upstream or downstream. 0 = PEX 8604 handles Memory and I/O Requests received on Port 5's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8604 returns a Completion with UR Completion status 1 = PEX 8604 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 13-257. E20h Bridge Control Port 0 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 0** register *SERR# Enable* bit is Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 0** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 13-257. E20h Bridge Control Port 0 (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

Register 13-258. E22h Bridge Control Port 1 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 1** register *SERR# Enable* bit is Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 1** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 13-258. E22h Bridge Control Port 1 (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

Register 13-259. E28h Bridge Control Port 4 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 4** register *SERR# Enable* bit is Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 4** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 13-259. E28h Bridge Control Port 4 (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

Register 13-260. E2Ah Bridge Control Port 5 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 5** register *SERR# Enable* bit is Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 5** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 13-260. E2Ah Bridge Control Port 5 (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

13.16.15 Device-Specific Registers – Physical Layer (Offsets E40h – EFCh)

This section details the Device-Specific Physical Layer (PHY) registers located at offsets E40h through EFCh. Table 13-46 defines the register map.

Other Device-Specific PHY registers are detailed in:

- Section 13.14.2, "Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)"
- Section 13.16.13, "Device-Specific Registers – Physical Layer (Offsets B80h – C30h)"

Table 13-46. Device-Specific PHY Register Map (Offsets E40h – EFCh)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
CSR-Based SerDes Mode				E40h
Internal Output A Trigger State Change Storage Mask				E44h
Internal Output B Trigger State Change Storage Mask				E48h
Reserved				E4Ch – EECh
Physical Layer Control				EF0h
Reserved				EF4h – EFCh

Register 13-261. E40h CSR-Based SerDes Mode (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
0	**SerDes Mode Enable**	RW	Yes	0
3:1	**SerDes Station**	RW	Yes	000b
7:4	**SerDes Lane**	RW	Yes	0h
10:8	**SerDes Lane2**	RW	Yes	0h
11	**SerDes Lane Polarity**	RW	Yes	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-262. E44h Internal Output A Trigger State Change Storage Mask (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
17:0	**Internal Output A Trigger State Change Mask**	RW	Yes	0-0h
31:18	***Reserved***	RsvdP	No	0-0h

Register 13-263. E48h Internal Output B Trigger State Change Storage Mask (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
17:0	**Internal Output B Trigger State Change Mask**	RW	Yes	0-0h
31:18	***Reserved***	RsvdP	No	0-0h

Register 13-264. EF0h Physical Layer Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register contains the parameters for controlling Electrical Idle Inference, and other optional training sequence controls.				
0	**SSC RXFIFO Skew Check Disable** 1 = Disables Rx FIFO SKIP addition, when rxvalids are skewed between FIFOs within a SerDes quad. This control is applicable only during a Spread-Spectrum Clock (SSC)-enabled chip operation.	RWS	Yes	0
1	**SSC RXFIFO Skew Counter Threshold** Selects how many clocks that a SKIP addition is blocked while rxvalids are skewed. 0 = 32 cycles 1 = 64 cycles	RWS	Yes	0
2	**SSC RXFIFO PhyStatus Mode Select** Internal PHY Interface for the PCI Express architecture's (PIPE) Physical Layer Status (PhyStatus) signals are Lane-independent. 1 = PIPE PhyStatus on all Lanes, of each SerDes quad, will be copies of Lane 0 from that quad ***Note:*** *With SSC x8 operation, only SerDes Quads 0 and 1 are used. For SSC x4, only SerDes Quad 0 is used.*	RWS	Yes	0
3	**Symbol Framer Reset Release Time Select** Selects the quantity of clocks for release from LX_RX_SIGDET becoming true. 0 = 8-clock delay 1 = 64-clock delay	RWS	Yes	0
7:4	***Factory Test Only***	RWS	Yes	0-0h
9:8	**Inferred Electrical Idle Exit Time Select Code** When Electrical Idle has been inferred and the Electrical Idle Inference Exit Type is 1, this field selects the amount of time that the SerDes Receive Data path remains disabled. 00b = 2 µs 01b = 4 µs 10b = 8 µs 11b = 16 µs	RWS	Yes	00b
11:10	***Reserved***	RsvdP	No	00b
13:12	**Symbol Framer Detection Time Select Code** When Electrical Idle has been inferred and the Electrical Idle Inference Exit Type is 1, this field selects the amount of time that the symbol framer is allowed to obtain symbol lock. 00b = 128 ns 01b = 256 ns 10b = 512 ns 11b = 1 µs	RWS	Yes	00b
15:14	***Reserved***	RsvdP	No	00b

Register 13-264. EF0h Physical Layer Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**Electrical Idle Inference on EIOS Receipt Enable** Electrical Idle Inference on Electrical Idle Ordered-Set (EIOS) Receipt enable, for the corresponding Port. 0 = Electrical Idle inference is enabled upon EIOS receipt, if the **Even/Odd Port Electrical Idle for Compliance Mask** register *SerDes x Mask Electrical Idle Detect* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 200h[9:8], and Odd Ports, offset 204h[9:8]) are Set, for the SerDes associated with the Port 1 = Electrical Idle will be inferred as soon as an EIOS is received on any Lane of the corresponding Port	RWS	Yes	0
17	**Inferred Electrical Idle Inference Exit Type** Selects the method used to detect exit from Electrical Idle, after Electrical Idle has been inferred. 0 = **Fast Method** – Type 0 Exit mode is used, which uses conventional analog Electrical Idle Exit Detection circuitry 1 = **Slow Method** – Type 1 Exit mode is used, which uses the Symbol Framer Detection Time Select Code and Inferred Electrical Idle Exit Time Select Code Timers (fields [13:12 and 9:8], respectively)	RWS	Yes	0
31:18	***Reserved***	RsvdP	No	0-0h

13.16.16 Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F3Ch)

This section details the Device-Specific Source Queue Weight and Soft Error registers. Table 13-47 defines the register map.

Table 13-47. Device-Specific Source Queue Weight and Soft Error Register Map (Offsets F00h – F3Ch)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Factory Test Only		ECRC Check Enable for Ports 0, 1		F00h
Factory Test Only		ECRC Check Enable for Ports 4, 5		F04h
Factory Test Only				F08h
Reserved				F0Ch
Port Egress TLP Threshold				F10h
Reserved				F14h
Soft Error Counters 1				F18h
Reserved				F1Ch – F20h
Reserved		Soft Error Counters 4		F24h
Reserved		Soft Error Counters 5		F28h
Soft Error Counters 6				F2Ch
Soft Error Injection				F30h
Reserved				F34h – F3Ch

Register 13-265. F00h ECRC Check Enable for Ports 0, 1 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The Port 0 registers at offsets F00h and F04h are a shadow copy of each Port's **Advanced Error Capabilities and Control** register *ECRC Check Enable* bit (offset FCCh[8]). To enable or disable ECRC Check functionality, use the **Advanced Error Capabilities and Control** register for each Port. Software should not program the shadow registers.				
0	**ECRC Check Enable for Port 0** 0 = ECRC checking is disabled on Port 0 1 = ECRC checking is enabled on Port 0	RWS	Yes	0
7:1	***Reserved***	RsvdP	No	0-0h
8	**ECRC Check Enable for Port 1** 0 = ECRC checking is disabled on Port 1 1 = ECRC checking is enabled on Port 1	RWS	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h
31:16	***Factory Test Only***	RsvdP	No	0000h

Register 13-266. F04h ECRC Check Enable for Ports 4, 5 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The Port 0 registers at offsets F00h and F04h are a shadow copy of each Port's **Advanced Error Capabilities and Control** register *ECRC Check Enable* bit (offset FCCh[8]). To enable or disable ECRC Check functionality, use the **Advanced Error Capabilities and Control** register for each Port. Software should not program the shadow registers.				
0	**ECRC Check Enable for Port 4** 0 = ECRC checking is disabled on Port 4 1 = ECRC checking is enabled on Port 4	RWS	Yes	0
7:1	***Reserved***	RsvdP	No	0-0h
8	**ECRC Check Enable for Port 5** 0 = ECRC checking is disabled on Port 5 1 = ECRC checking is enabled on Port 5	RWS	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h
31:16	***Factory Test Only***	RsvdP	No	0000h

Register 13-267. F10h Port Egress TLP Threshold (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Caution: Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.				
10:0	**Port Lower TLP Counter** When Source Scheduling is disabled due to the Port Upper TLP Counter (threshold) being exceeded, Source Scheduling is re-enabled when the Port TLP Counter goes below the Port Lower TLP Counter (this threshold). Because the default Setting of this field is 7FFh (2,047), which is greater than the maximum amount of TLPs that can be queued in the PEX 8604, the Source Scheduler is disabled, by default.	RWS	Yes	7FFh
15:11	***Reserved***	RsvdP	No	0-0h
26:16	**Port Upper TLP Counter** When the Port TLP Counter is greater than or equal to this value, the Source Scheduler disables TLP Scheduling to this egress Port. Because the default Setting of this field is 7FFh (2,047), which is greater than the maximum amount of TLPs that can be queued in the PEX 8604, the Source Scheduler is disabled, by default.	RWS	Yes	7FFh
31:27	***Reserved***	RsvdP	No	0-0h

Register 13-268. F18h Soft Error Counters 1 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Port 0 Payload RAM 0 1-Bit Soft Error Counter Value**	RO	No	0
1	***Factory Test Only***	RsvdP	No	0
2	**Port 4 Payload RAM 0 1-Bit Soft Error Counter Value**	RO	No	0
7:3	***Factory Test Only/Reserved***	RsvdP	No	0-0h
8	**Port 0 Payload RAM 1 1-Bit Soft Error Counter Value**	RO	No	0
9	***Factory Test Only***	RsvdP	No	0
10	**Port 4 Payload RAM 1 1-Bit Soft Error Counter Value**	RO	No	0
15:11	***Factory Test Only/Reserved***	RsvdP	No	0-0h
16	**Port 1 Payload RAM 0 1-Bit Soft Error Counter Value**	RO	No	0
17	***Factory Test Only***	RsvdP	No	0
18	**Port 5 Payload RAM 0 1-Bit Soft Error Counter Value**	RO	No	0
23:19	***Factory Test Only/Reserved***	RsvdP	No	0-0h
24	**Port 1 Payload RAM 1 1-Bit Soft Error Counter Value**	RO	No	0
25	***Factory Test Only***	RsvdP	No	0
26	**Port 5 Payload RAM 1 1-Bit Soft Error Counter Value**	RO	No	0
31:27	***Factory Test Only/Reserved***	RsvdP	No	0-0h

Register 13-269. F24h Soft Error Counters 4 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Port 0 Header RAM 1-Bit Soft Error Counter Value**	RO	No	0
1	***Factory Test Only***	RsvdP	No	0
2	**Port 4 Header RAM 1-Bit Soft Error Counter Value**	RO	No	0
7:3	***Factory Test Only/Reserved***	RsvdP	No	0-0h
8	**Port 1 Header RAM 1-Bit Soft Error Counter Value**	RO	No	0
9	***Factory Test Only***	RsvdP	No	0
10	**Port 5 Header RAM 1-Bit Soft Error Counter Value**	RO	No	0
15:11	***Factory Test Only/Reserved***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-270. F28h Soft Error Counters 5 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Port 0 Payload Linked List RAM 1-Bit Soft Error Counter Value**	RO	No	0
1	***Factory Test Only***	RsvdP	No	0
2	**Port 4 Payload Linked List RAM 1-Bit Soft Error Counter Value**	RO	No	0
7:3	***Factory Test Only/Reserved***	RsvdP	No	0-0h
8	**Port 1 Payload Linked List RAM 1-Bit Soft Error Counter Value**	RO	No	0
9	***Factory Test Only***	RsvdP	No	0
10	**Port 5 Payload Linked List RAM 1-Bit Soft Error Counter Value**	RO	No	0
15:11	***Factory Test Only/Reserved***	RsvdP	No	0-0h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-271. F2Ch Soft Error Counters 6 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Destination Queue Link List RAM 1-Bit Soft Error Counter Value**	RO	No	00h
8	**Port 0 Source Queue Link List RAM 1-Bit Soft Error Counter Value**	RO	No	0
9	***Factory Test Only***	RsvdP	No	0
10	**Port 4 Source Queue Link List RAM 1-Bit Soft Error Counter Value**	RO	No	0
15:11	***Factory Test Only/Reserved***	RsvdP	No	0-0h
16	**Port 1 Source Queue Link List RAM 1-Bit Soft Error Counter Value**	RO	No	0
17	***Factory Test Only***	RsvdP	No	0
18	**Port 5 Source Queue Link List RAM 1-Bit Soft Error Counter Value**	RO	No	0
23:19	***Factory Test Only/Reserved***	RsvdP	No	0-0h
31:24	**Retry Buffer 1-Bit Soft Error Counter Value**	RO	No	00h

Register 13-272. F30h Soft Error Injection (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Destination Queue Link List RAM Port A 1-Bit Soft Error Injection Toggle** Every toggle injects an error.	RW	Yes	0
1	**Destination Queue Link List RAM Port A 2-Bit Soft Error Injection Toggle** Every toggle injects an error.	RW	Yes	0
2	**Destination Queue Link List RAM Port A Error Injection Field Select** 0 = Inject Soft error in the *ECC Code* field 1 = Inject Soft error in the *Data* field	RW	Yes	0
3	**Destination Queue Link List RAM Port B 1-Bit Soft Error Injection Toggle** Every toggle injects an error.	RW	Yes	0
4	**Destination Queue Link List RAM Port B 2-Bit Soft Error Injection Toggle** Every toggle injects an error.	RW	Yes	0
5	**Destination Queue Link List RAM Port B Error Injection Field Select** 0 = Inject Soft error in the *ECC Code* field 1 = Inject Soft error in the *Data* field	RW	Yes	0
7:6	***Reserved***	RsvdP	No	00b
8	**Retry Buffer 1-Bit Soft Error Injection Toggle** Every toggle injects an error.	RW	Yes	0
9	**Retry Buffer 2-Bit Soft Error Injection Toggle** Every toggle injects an error.	RW	Yes	0
10	**Retry Buffer Soft Error Injection Field Select** 0 = Inject Soft error in the *ECC Code* field 1 = Inject Soft error in the *Data* field	RW	Yes	0
31:11	***Reserved***	RsvdP	No	0-0h

13.16.17 Device-Specific Registers – Error Reporting (Offsets F40h – F4Ch)

This section details the Device-Specific Error Reporting registers, which shadow the corresponding **Device Control** register Error Reporting-related bits (offset 70h[2:0]), for each Port. Table 13-48 defines the register map.

Table 13-48. Device-Specific Error Reporting Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Error Reporting Enable for Ports 0, 1				F40h
Error Reporting Enable for Ports 4, 5				F44h
Reserved				F48h – F4Ch

Register 13-273. F40h Error Reporting Enable for Ports 0, 1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Port 0 Correctable Error Reporting Enable** Shadow copy of **Device Control** register *Correctable Error Reporting Enable* bit (offset 70h[0]), for Port 0.	RW	Yes	0
1	**Port 0 Non-Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Non-Fatal Error Reporting Enable* bit (offset 70h[1]), for Port 0.	RW	Yes	0
2	**Port 0 Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]), for Port 0.	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**Port 1 Correctable Error Reporting Enable** Shadow copy of **Device Control** register *Correctable Error Reporting Enable* bit (offset 70h[0]), for Port 1.	RW	Yes	0
9	**Port 1 Non-Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Non-Fatal Error Reporting Enable* bit (offset 70h[1]), for Port 1.	RW	Yes	0
10	**Port 1 Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]), for Port 1.	RW	Yes	0
15:11	***Reserved***	RsvdP	No	0-0h
18:16	***Factory Test Only***	RsvdP	No	000b
23:19	***Reserved***	RsvdP	No	0-0h
26:24	***Factory Test Only***	RsvdP	No	000b
31:27	***Reserved***	RsvdP	No	0-0h

Register 13-274. F44h Error Reporting Enable for Ports 4, 5 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Port 4 Correctable Error Reporting Enable** Shadow copy of **Device Control** register *Correctable Error Reporting Enable* bit (offset 70h[0]), for Port 4.	RW	Yes	0
1	**Port 4 Non-Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Non-Fatal Error Reporting Enable* bit (offset 70h[1]), for Port 4.	RW	Yes	0
2	**Port 4 Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]), for Port 4.	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**Port 5 Correctable Error Reporting Enable** Shadow copy of **Device Control** register *Correctable Error Reporting Enable* bit (offset 70h[0]), for Port 5.	RW	Yes	0
9	**Port 5 Non-Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Non-Fatal Error Reporting Enable* bit (offset 70h[1]), for Port 5.	RW	Yes	0
10	**Port 5 Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]), for Port 5.	RW	Yes	0
15:11	***Reserved***	RsvdP	No	0-0h
18:16	***Factory Test Only***	RsvdP	No	000b
23:19	***Reserved***	RsvdP	No	0-0h
26:24	***Factory Test Only***	RsvdP	No	000b
31:27	***Reserved***	RsvdP	No	0-0h

13.16.18 Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)

This section details the Device-Specific ARI Capability registers, which shadow ARI-related bits at offsets 8Ch[5] and 90h[5], for each Port. Table 13-49 defines the register map.

Table 13-49. Device-Specific ARI Capability Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device Control 2 for Port 0		Device Capability 2 for Port 0		F50h
Device Control 2 for Port 1		Device Capability 2 for Port 1		F54h
Factory Test Only				F58h – F5Ch
Device Control 2 for Port 4		Device Capability 2 for Port 4		F60h
Device Control 2 for Port 5		Device Capability 2 for Port 5		F64h
Factory Test Only/Reserved				F68h – F8Ch

Register 13-275. F50h Device Capability and Control 2 for Port 0 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 0				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 0				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 13-276. F54h Device Capability and Control 2 for Port 1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 1				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 1				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 13-277. F60h Device Capability and Control 2 for Port 4 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 4				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 4				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 13-278. F64h Device Capability and Control 2 for Port 5 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 5				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 5				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

13.17 Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

This section details the Advanced Error Reporting Extended Capability registers. Table 13-50 defines the register map.

Table 13-50. Advanced Error Reporting Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (138h or 148h) / Capability Version (1h)	PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status		FB8h
Uncorrectable Error Mask		FBCh
Uncorrectable Error Severity		FC0h
Correctable Error Status		FC4h
Correctable Error Mask		FC8h
Advanced Error Capabilities and Control		FCCh
Header Log 0		FD0h
Header Log 1		FD4h
Header Log 2		FD8h
Header Log 3		FDCh

Register 13-279. FB4h Advanced Error Reporting Extended Capability Header (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID**		RO	Yes	0001h
19:16	**Capability Version**		RO	Yes	1h
31:20	**Next Capability Offset** Program to 138h, which addresses the upstream Port/ NT Port Link Interface **Power Budget Extended Capability** structure.	Upstream	RO	Yes	138h
	Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	Downstream	RO	Yes	148h

Register 13-280. FB8h Uncorrectable Error Status (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Note: *The bits in this register can be masked by their respective* ***Uncorrectable Error Mask*** *register bits (offset FBCh).*					
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Surprise Down Error Status 0 = No error is detected 1 = Error is detected	Downstream	RW1CS[a]	Yes	0
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
13	**Flow Control Protocol Error Status** ***Reserved/Not supported***		RO	No	1
14	**Completion Timeout Status** ***Not applicable to switches.***		RsvdP	No	0
15	**Completer Abort Status**		RW1CS[a]	Yes	0
16	**Unexpected Completion Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
17	**Receiver Overflow Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
18	**Malformed TLP Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
19	**ECRC Error Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
20	**Unsupported Request Error Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Violation Error Status 0 = No violation detected 1 = Violation is detected	Downstream	RW1CS[a]	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

a. When the ***ECC Error Check Disable*** *register Software Force Error Enable bit (offset 1C8h[2]) is Set, Type changes from RW1CS to RW.*

Register 13-281. FBCh Uncorrectable Error Mask (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Uncorrectable Error Status*** *register bits (offset FB8h).*					
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Surprise Down Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Downstream	RWS	Yes	0
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
13	**Flow Control Protocol Error Mask** ***Reserved/Not supported***		RsvdP	No	0
14	**Completion Timeout Mask** ***Not applicable to switches.***		RsvdP	No	0
15	**Completer Abort Mask**		RWS	Yes	0
16	**Unexpected Completion Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
17	**Receiver Overflow Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
18	**Malformed TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
19	**ECRC Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
20	**Unsupported Request Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Violation Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Downstream	RWS	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 13-282. FC0h Uncorrectable Error Severity (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
5	**Surprise Down Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	Upstream	RO	No	1
		Downstream	RWS	Yes	1
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
13	**Flow Control Protocol Error Severity**		RO	No	1
14	**Completion Timeout Severity** ***Not applicable to switches.*** Because the Status and Mask are both ***reserved*** for this bit, Severity can be ignored.		RsvdP	No	0
15	**Completer Abort Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error reported as fatal		RWS	Yes	0

Register 13-282. FC0h Uncorrectable Error Severity (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
16	**Unexpected Completion Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
17	**Receiver Overflow Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
18	**Malformed TLP Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
19	**ECRC Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
20	**Unsupported Request Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Violation Error Severity 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	Downstream	RWS	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 13-283. FC4h Correctable Error Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be masked by their respective* ***Correctable Error Mask*** *register bits (offset FC8h).*				
0	**Receiver Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
5:1	***Reserved***	RsvdP	No	0-0h
6	**Bad TLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
7	**Bad DLLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
8	**REPLAY NUM Rollover Status** Replay Number Rollover status. 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
11:9	***Reserved***	RsvdP	No	000b
12	**Replay Timer Timeout Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
13	**Advisory Non-Fatal Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
31:14	***Reserved***	RsvdP	No	0-0h

a. When the ***ECC Error Check Disable*** *register Software Force Error Enable bit (offset 1C8h[2]) is Set, Type changes from RW1CS to RW.*

Register 13-284. FC8h Correctable Error Mask (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Correctable Error Status*** *register bits (offset FC4h).*				
0	**Receiver Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
5:1	***Reserved***	RsvdP	No	0-0h
6	**Bad TLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
7	**Bad DLLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
8	**REPLAY NUM Rollover Mask** Replay Number Rollover mask. 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
11:9	***Reserved***	RsvdP	No	000b
12	**Replay Timer Timeout Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
13	**Advisory Non-Fatal Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	1
31:14	***Reserved***	RsvdP	No	0-0h

Register 13-285. FCCh Advanced Error Capabilities and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
4:0	**First Error Pointer** Identifies the bit position of the first error reported in the **Uncorrectable Error Status** register (offset FB8h).	ROS	No	1Fh
5	**ECRC Generation Capable** 0 = ECRC generation is not supported 1 = ECRC generation is supported, but must be enabled	RO	Yes	1
6	**ECRC Generation Enable** 0 = ECRC generation is disabled 1 = ECRC generation is enabled	RWS	Yes	0
7	**ECRC Check Capable** 0 = ECRC checking is not supported 1 = ECRC checking is supported, but must be enabled	RO	Yes	1
8	**ECRC Check Enable** 0 = ECRC checking is disabled 1 = ECRC checking is enabled	RWS	Yes	0
31:9	***Reserved***	RsvdP	No	0-0h

Register 13-286. FD0h Header Log 0 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**TLP Header 0** First DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 13-287. FD4h Header Log 1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**TLP Header 1** Second DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 13-288. FD8h Header Log 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**TLP Header 2** Third DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 13-289. FDCh Header Log 3 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**TLP Header 3** Fourth DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Chapter 14 Non-Transparent Bridging – NT Mode Only

14.1 Introduction

Note: *Check the latest design guides, application notes and errata list for Non-Transparent (NT) usage.*

The PEX 8604 supports Non-Transparent (NT) bridge functionality (NT mode), which is used to implement High-Availability systems or Intelligent I/O modules using PCI Express technology. The following discusses the basic NT bridging concept, as it applies to a PCI Express system.

NT bridges allow systems to isolate Address spaces, by appearing as an endpoint to the Host. The NT bridge exposes a Type 0 Configuration Space register (CSR) Header and forwards transactions from one domain to the other, using address translation. The NT bridge is used to connect two independent address/Host domains. The NT bridge includes **Doorbell** registers, for transmitting interrupts from one side of the bridge to the other. The bridge also includes **Scratchpad** registers, accessible from both domains for inter-Host communication. The PEX 8604, with a single Port configured to operate in NT mode, supports the Intelligent Adapter Mode system model. NT mode is enabled/disabled by the STRAP_NT_ENABLE# input.

The following are PEX 8604 Non-Transparent Bridging (NTB) key elements:

- Device Type Identification
- NT Port Features
- Intelligent Adapter Mode
- NT Port Reset
- NT Port Memory-Mapped Base Address Registers
- Doorbell Registers
- Scratchpad Registers
- NT Base Address Registers
- Address Translation

14.1.1 Device Type Identification

Devices identify themselves by way of the Conventional PCI Configuration Space register (CSR) Header **PCI Class Code** register. A Transparent PCI-to-PCI bridge identifies itself as a PCI Class Code 060400h. An NT bridge identifies itself as "Other Bridge," 068000h, with a Type 0 Header, which is consistent with the use of other NT bridges available in the industry.

The **PCI Express Capability** register includes a *Device/Port Type* field (offset 68h[23:20]). In this register, a Transparent bridge/switch Port identifies itself as an *upstream or downstream Port*, while an NT bridge/switch NT Port identifies itself as a *PCI Express endpoint*.

14.1.2 NT Port Features

- Maps PEX 8604 Configuration registers into either 32- or 64-bit Memory space
- Base Address registers (BARs)
  - Implements four 32-bit, two 32-bit and one 64-bit, or two 64-bit BARs
  - Supports BAR Size programming, through the **BAR*x* Setup** register(s)
  - Allows BARs to be individually disabled, including Memory-Mapped BARs
- Supports Direct Address Translation
  - 32-to-32-bit address conversion
  - 32-to-64-bit address conversion
  - 64-to-32-bit address conversion
  - 64-to-64-bit address conversion
  - Requester ID (Bus Number, Device Number, and Function Number) conversion across the NT bridge
- **Doorbell** registers
- **Scratchpad** registers
- Supports Requester ID and Completion ID translation
- NT Port Link Interface *DL_Active* state change generates interrupt to Local Host
- Supports Cursor mechanism
- Supports Expansion ROM on either NT Port interface
- Supports End-to-end Cyclic Redundancy Check (ECRC)
- Provides ability to Clear *No Snoop* Transaction Layer Packet (TLP) attribute (if enabled)
- Programmable upstream Port and NT Port for the enabling of High Availability systems (Failover and Redundant systems)
- Brings down the NT Port Link when the Local Host domain is down (if enabled)
- Supports the Fencing mechanism
- Signals Device-Specific interrupt to the Local Host when the NT Port Link Interface detects TLP errors
- Signals Device-Specific interrupt to the Local Host when the NT Port Link Interface receives Error Messages (Safety bit-controllable)
- Disables NT Port Link Interface Hot Reset effect (enabled, by default)
- Supports Configuration Space access control
- Option to appear behind a PCI-to-PCI bridge (refer to STRAP_NT_P2P_EN# ball description)

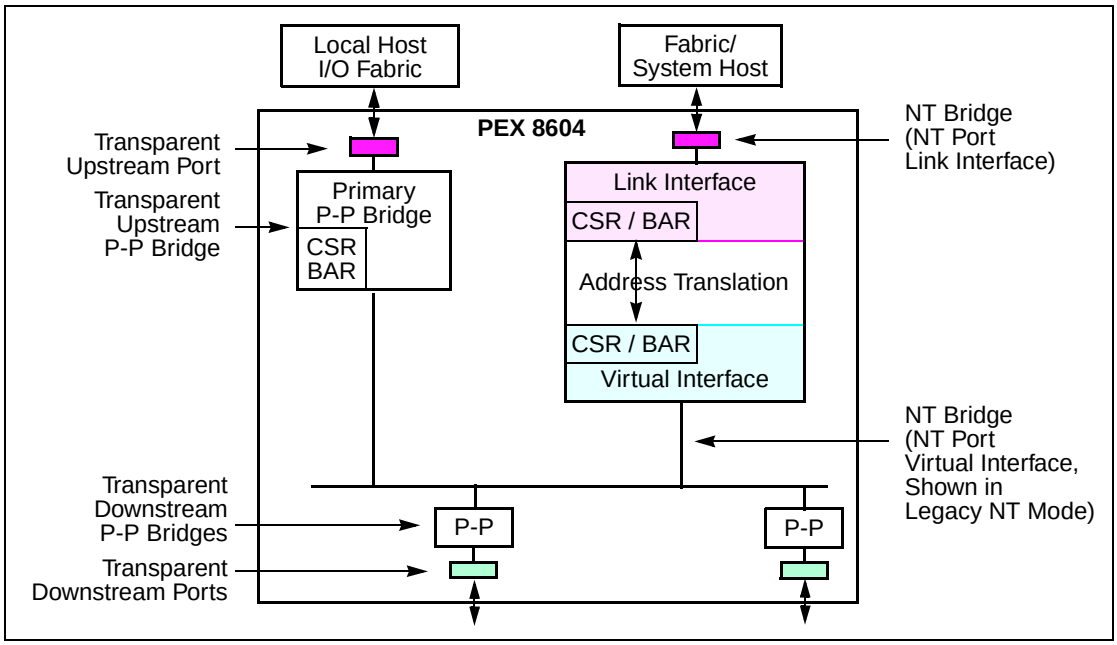
14.1.3 Intelligent Adapter Mode

The use of NT bridges in PCI systems is well-established for supporting intelligent adapters in enterprise and multi-Host systems. The same concept is used in PCI Express bridges and switches.

In Figure 14-1, there are two Type 0 CSR Headers in the NT bridge. The one nearer the internal virtual PCI Bus is referred to as the *Virtual Interface*. The one nearer the PCI Express Link is referred to as the *Link Interface*.

In Intelligent Adapter mode, the NT Port Link Interface is connected to the System Host domain. The System Host manages only the NT Port Link Interface Type 0 function. The Local Host manages all PEX 8604 Transparent Port Type 1 and NT Port Virtual Interface Type 0 functions. Cross-domain traffic is routed through an Address Translation mechanism. (Refer to Section 14.1.9.)

Figure 14-1. Intelligent Adapter Software Model



14.1.4 NT Port Reset

The section discusses NT mode exceptions and enhancements to Transparent mode PCI Express (standard) reset behavior.

14.1.4.1 Fundamental Reset (PEX_PERST#)

PEX_PERST# resets all PEX 8604 states, including NT Port states. This reset initializes all Sticky bits and Configuration registers in Virtual and Link spaces to default values.

14.1.4.2 Intelligent Adapter Mode NT Port Reset

When the Transparent upstream Port receives a Hot Reset or enters the *DL_Down* state, the PEX 8604, by default, propagates the in-band reset to all Transparent downstream Ports and connected downstream devices (to reset the downstream hierarchy), then resets the internal switch fabric and the NT Port Virtual Interface. There is no reset propagation to the NT Port Link Interface, and the Link-side remains intact.

When the NT Port Link Interface receives a Hot Reset or enters the *DL_Down* state, the NT Port Link Interface registers are reset, by default. This Soft Reset does not reset the Transparent Ports nor the NT Port Virtual Interface. Instead, when the NT Port Link Interface receives a Hot Reset (or enters the *DL_Down* state), the PEX_NT_RESET# output is asserted Low for 1 µs. The system can use this signal to trigger a reset of the entire Local subsystem.

The PEX 8604 supports an option that allows these Hot Reset conditions at its Transparent upstream Port and NT Port Link Interface to be masked (disabled) for all Ports, including the NT Port, by Setting the **Debug Control** register *Upstream Port and NT-Link DL_Down Reset Propagation Disable* bit (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[20]).

When software writes to the PEX 8604 Transparent upstream Port's **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]), the resulting Secondary Bus Reset is (as above) propagated to all PEX 8604 Transparent downstream Ports, and the Port states and NT Port Virtual Interface states are reset.

14.1.5 NT Port Memory-Mapped Base Address Registers

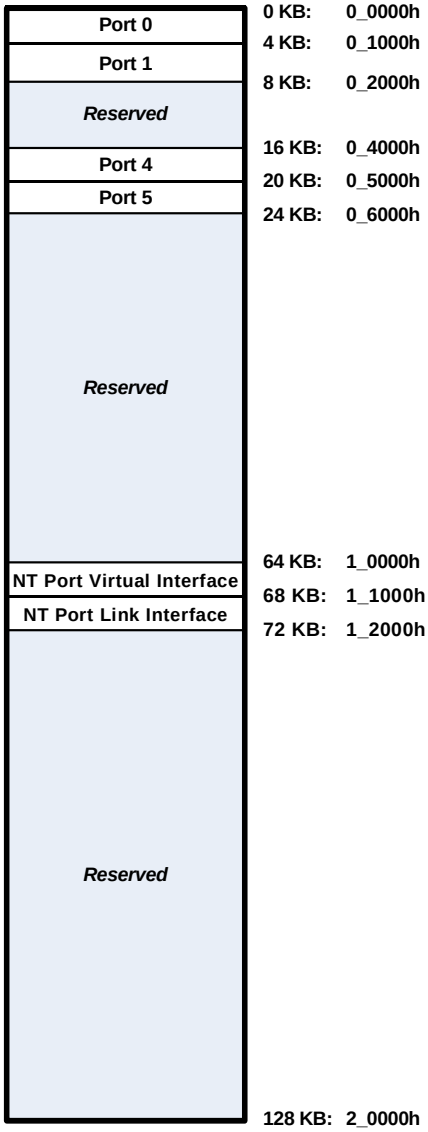
The NT Port Virtual and Link Interfaces individually claim 128 KB of memory, using **BAR0** and **BAR1**. The 128-KB space contains the CSRs for all PEX 8604 Ports. **BAR0** and **BAR1** can be programmed as one of the following:

- 32-bit BAR (**BAR1** is ***reserved***; default mode)
- 64-bit BAR, by programming the Configuration **BAR0/1 Setup** register (the NT Port Virtual Interface offset is D0h; the NT Port Link Interface offset is E4h)
- **BAR0** and **BAR1** can be completely disabled

Figure 14-2 provides a memory-mapped view of the PEX 8604 CSRs. This view is the same from the upstream Port, NT Port Virtual Interface, or NT Port Link Interface.

Figure 14-2. NT Mode Configuration Register Mapping to Memory-Mapped BAR

PEX 8604



14.1.6 Doorbell Registers

Doorbell registers are used to signal interrupts from one side of the NT bridge to the other. This section describes a typical set of Doorbell Control registers.

A 16-bit software-controlled Interrupt Request register and associated 16-bit Mask register are implemented for the NT Port Virtual and Link Interfaces. The Doorbell mechanisms consist of the following registers:

- **Virtual Interface IRQ Set**
- **Virtual Interface IRQ Clear**
- **Virtual Interface IRQ Mask Set**
- **Virtual Interface IRQ Mask Clear**
- **Link Interface IRQ Set**
- **Link Interface IRQ Clear**
- **Link Interface IRQ Mask Set**
- **Link Interface IRQ Mask Clear**

The Virtual Interface IRQ is for interrupts that exit the NT Port Virtual Interface. An interrupt is asserted on the NT Port Virtual Interface when one or more of the **Virtual Interface IRQ Set** register bits are Set by the NT Port Link Interface and their corresponding **Virtual Interface IRQ Mask Set** register bits are Cleared. An interrupt is de-asserted on the NT Port Virtual Interface when one or more of the **Virtual Interface IRQ Clear** register bits are Set from the NT Port Virtual Interface and their corresponding **Virtual Interface IRQ Mask Clear** register bits are Cleared. The interrupt is de-asserted when all Set bits are masked or Cleared.

The Link Interface IRQ is for interrupts that exit the NT Port Link Interface. An interrupt is asserted on the NT Port Link Interface when one or more of the **Link Interface IRQ Set** register bits are Set by the NT Port Virtual Interface and their corresponding **Link Interface IRQ Mask Set** register bits are Cleared. An interrupt is de-asserted on the NT Port Link Interface when one or more of the **Link Interface IRQ Clear** register bits are Set from the NT Port Link Interface and their corresponding **Link Interface IRQ Mask Clear** register bits are Cleared. The interrupt is de-asserted when all Set bits are masked or Cleared.

Because Memory Requests can access both sets of NT-Virtual and NT-Link Doorbell registers, software in either domain can generate Doorbell interrupts to both domains.

Internally, the **Set IRQ** and **Clear IRQ** registers are the same register. One location is used to Set bits and the other is used to Clear bits. The status can be read from either register.

In a PCI Express switch, interrupt state transitions (from Setting to Clearing, or vice versa) result in packets being transmitted upstream on the appropriate side of the bridge, when INT*x* are enabled (**PCI Command** register *Interrupt Disable* bit, offset 04h[10], is Cleared). Standard PCI Express Capability structures allow these interrupts to be configured as MSIs or INT*x*. When MSIs are enabled (**MSI Control** register *MSI Enable* bit, offset 48h[16], is Set), packets are transmitted only when interrupts transition from Clear IRQ to Set IRQ.

NT Port Doorbell interrupts can optionally use the PEX_INTA# output for interrupt signaling, instead of the INT*x* or MSI signaling mechanisms. PEX_INTA# output can be enabled for NT Port Doorbell interrupts, by Setting the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port, offset 1C8h[7]).

The PEX 8604 Virtual interrupts are de-asserted when the NT Port goes to the *DL_Down* state.

14.1.7 Scratchpad Registers

Scratchpad registers are readable and writable from both sides of the NT bridge, providing a generic means for inter-Host communication. A block of eight registers are provided, accessible in Memory space from the NT Port Virtual and Link Interfaces. These registers pass Control and Status information between Virtual and Link Interface devices or they can be generic RW registers. Reading from or writing to **Scratchpad** registers does not cause interrupts to assert – **Doorbell** registers are used for that purpose. **Scratchpad** registers are reset only by a Fundamental Reset (PEX_PERST#).

The NT bridge uses the Conventional PCI set of BARs in its Type 0 CSR Header to define Address ranges into the Memory space on the other side of the bridge. BARs define resource Address ranges that allow transaction forwarding to the opposite (other side) interface.

14.1.8 NT Base Address Registers

There are two sets of NT Base Address registers (BARs) – one each for the NT Port Virtual and Link Interfaces. Each BAR has its own **Setup** and **Address Translation** register:

- **BAR*x* Setup** registers enable/disable the BAR and define the window size and type. Program the **BAR*x* Setup** registers prior to allowing configuration software to assign a resource for these BARs. (Discussed further in Section 14.1.8.1.)
- **Memory BAR*x* Address Translation** registers allow for an address change on the upper bits (up to the size of the space). Program the **Memory BAR*x* Address Translation** registers, before generating traffic across the NT Port. This programming is typically performed by information downloaded from I^2C, software, and/or an optional serial EEPROM (if present) on the destination side. The source side does not need to know what the Address Translation is.
- The address could change size. *For example*, the PEX 8604 NT Port allows a 32-bit device to communicate to a 64-bit device, and vice versa. (The same is true when the addresses are the same size, as well – a 32-bit device can communicate with a 32-bit device, and a 64-bit can communicate with a 64-bit device.)

14.1.8.1 NT BAR*x* Setup Registers

PCI defines Base Address Registers (BARs) for a PCI device to claim Address space. For the PEX 8604, **BAR0** and **BAR1** provide Memory-Mapped access to the CSRs, while **BAR2**, **BAR3**, **BAR4**, and **BAR5** provide programmable window sizes to the other side of the NTB.

The **BAR*x* Setup** registers are used to program the window size of each BAR. Table 14-1 briefly describes each NT Port BAR. **BAR2**, **BAR3**, **BAR4**, and **BAR5** can be configured for accessing the Address space across the NT Port Virtual and Link Interfaces.

Each **BAR*x* Setup** register defines the memory window size that is to be assigned by a system enumerator (*that is*, BIOS and/or firmware). *For example*, if the window size must be 1 MB, Memory space, and cacheable region, the **BAR*x* Setup** register in 32-bit space will be FFF0_0008h (FFF0_0000h indicates the 1-MB space Request, bit 3 is the cacheable region, and bit 0 must be Memory space).

In most cases, the **BAR*x* Setup** registers are programmed using an optional serial EEPROM (if present), before the BIOS or firmware allocates the resources (because resource enumeration is done before the system software can access these devices).

Table 14-1. NT Port Virtual and Link Interface BARs

BAR	NT Port Virtual Interface Description	NT Port Link Interface Description
BAR0	All PEX 8604 Port Configuration registers are mapped into Memory space, using **BAR0** and **BAR1**. The Local Host, connected to the Transparent upstream Port, can use the Transparent upstream Port **BAR0/1** or NT Port Virtual Interface **BAR0/1** to access the PEX 8604 Port Configuration registers. The **NT Port Virtual Interface BAR0/1 Setup** register controls the **BAR0** and **BAR1** implementation, as follows: • Disables **BAR0** and **BAR1** • Enables **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) • Enables **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR) **BAR0** and **BAR1** claim 128-KB Memory space to the system.	All PEX 8604 Port Configuration registers are mapped into Memory space, using **BAR0** and **BAR1**. The System Host, connected to the NT Port, can use **BAR0/1** to access the PEX 8604 Port Configuration registers. The **NT Port Link Interface BAR0/1 Setup** register controls the **BAR0** and **BAR1** implementation, as follows: • Disables **BAR0** and **BAR1** • Enables **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) • Enables **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR) **BAR0** and **BAR1** claim 128-KB Memory space to the system.
BAR1	Configured by the **NT Port Virtual Interface BAR0/1 Setup** register. **BAR1** is implemented as an upper 32-bit address of the NT Port Virtual Interface memory-mapped 64-bit BAR; otherwise, it is ***reserved***.	Configured by the **NT Port Link Interface BAR0/1 Setup** register. **BAR1** is implemented as an upper 32-bit address of the NT Port Virtual Interface memory-mapped 64-bit BAR; otherwise, it is ***reserved***.
BAR2	Configured by the **NT Port Virtual Interface Memory BAR2 Setup** register. **BAR2** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR3** (**BAR2**/**3**). **BAR2** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR2 Setup** register. **BAR2** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR3** (**BAR2**/**3**). **BAR2** uses Direct Address Translation.
BAR3	Configured by the **NT Port Virtual Interface Memory BAR2/3 Setup** register. **BAR3** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR2** (**BAR2**/**3**). **BAR3** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR2/3 Setup** register. **BAR3** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR2** (**BAR2**/**3**). **BAR3** uses Direct Address Translation.
BAR4	Configured by the **NT Port Virtual Interface Memory BAR4 Setup** register. **BAR4** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR5** (**BAR4**/**5**). **BAR4** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR4 Setup** register. **BAR4** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR5** (**BAR4**/**5**). **BAR4** uses Direct Address Translation.
BAR5	Configured by the **NT Port Virtual Interface Memory BAR4/5 Setup** register. **BAR5** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR4** (**BAR4**/**5**). **BAR5** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR4/5 Setup** register. **BAR5** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR4** (**BAR4**/**5**). **BAR5** uses Direct Address Translation.

14.1.9 Address Translation

The Transparent bridge uses **Base** and **Limit** registers in I/O space, Non-Prefetchable Memory space, and Prefetchable Memory space to map transactions downstream, across the bridge. All downstream devices must be mapped in contiguous address regions, such that a single Address range in each space is sufficient. Upstream mapping is done by way of inverse decode, relative to the same registers. A Transparent bridge does not translate the addresses of forwarded transactions/packets.

In multi-domain systems, each Host domain has its own Address space, that is different from that of other Host domain(s). Hence, any transaction crossing the inter-domain boundary, by way of an NTB or other means, must support address, as well as Requester ID, translations.

Before a transaction (PCI Express packet) can go through the NT bridge (either from the Virtual-side to Link-side, or from Link-side to Virtual-side) in an inter-domain system, one or more sets of Memory resources must be assigned to the NT bridge. To request this resource from the system enumerator (BIOS and/or firmware), the NT bridge must be programmed with the **BAR*x* Setup** register(s). (Refer to Section 14.1.8.1.) The **BAR*x* Setup** register(s) requests the window space size, memory type, 32- or 64-bit space, prefetchable or non-prefetchable area, using one 32-bit register for 32-bit Address space or the two 32-bit registers (**BAR2/3** or **BAR4/5**) for 64-bit Address space. In return, the system enumerator assigns resources to the NT bridge in **BAR0** through **BAR5**. Any transactions that target **BAR2** through **BAR5** on the NT Port Link Interface result in a transaction across the NT bridge, to the secondary address domain.

Similarly, in NT PCI-to-PCI Bridge mode, the NT PCI-to-PCI bridge must be enumerated to accommodate the resources assigned to the NT endpoint, to allow packets to logically traverse the bridge. Its Device Number (on the Internal Virtual PCI Bus) value is the NT Port Number. Device enumeration minimally includes the **PCI Command**, **Bus Number**, and **Memory Base and Limit** and/or **Prefetchable Memory Base and Limit** registers (offsets 04h, 18h, and 20h, and/or 24h). The Internal NT Virtual Bus (connecting the NT PCI-to-PCI secondary interface and NT endpoint) can be assigned any available Bus Number within the upstream Port's range of Subordinate Bus Numbers.

In addition, the Lookup Table (LUT) register(s) and **Memory BAR*x* Address Translation** register(s) must be programmed. The LUTs are the Requester ID (Bus Number, Device Number, and Function Number) with the ability to disable features that allow Requester's transaction go through the NT bridge (if enabled). This adds security to the NT bridge, limiting the devices that can generate transactions across the NT bridge. LUTs also play a crucial role, because the Requester ID is also used to complete PCI Express Read Requests – during the PCI Express Read Request to the other domain side, the NT bridge uses its own Requester ID to translate the original PCI Read Request, and when the Completion returns, the NT bridge uses the original Requester ID to complete the transaction.

The Address Translation is used to re-direct the address of the PCI Express packet to a programmer-reserved area (instead of using the same address for both Host domains). Hence, any transaction targeting **BAR2** through **BAR5** can be translated (re-mapped) on the other side of the NT bridge while maintaining the offsets. These Translation registers can be changed during runtime, as long as there are no pending transactions.

The PEX 8604 NT Port Virtual and Link Interfaces support Direct Address Translation, described in the following section.

14.1.9.1 Direct Address Translation

The **BAR*x* Setup** registers define a mask that splits the address into an upper *Base* field and a lower *Offset* field. Translation then consists of replacing, under the maskable portion of the **BAR*x* Setup** register, the Address Base register bits with the corresponding Address Translation register bits. Accordingly, the Address Translation register value must be a multiple of the corresponding BAR size. Figure 14-3 illustrates Direct Address Translation.

The device(s) on the originating Host domain can communicate to a single device or multiple devices mapped to consecutive Memory Address space on the target Host domain, by using the Direct Address Translation mechanism. Figure 14-4 illustrates the entire Address map, claimed by the NT Port, mapped into the single target device. Figure 14-5 illustrates the entire Address map claimed by the NT Port, mapped into multiple target devices. Multiple devices must be in contiguous Memory ranges.

Figure 14-3. Direct Address Translation

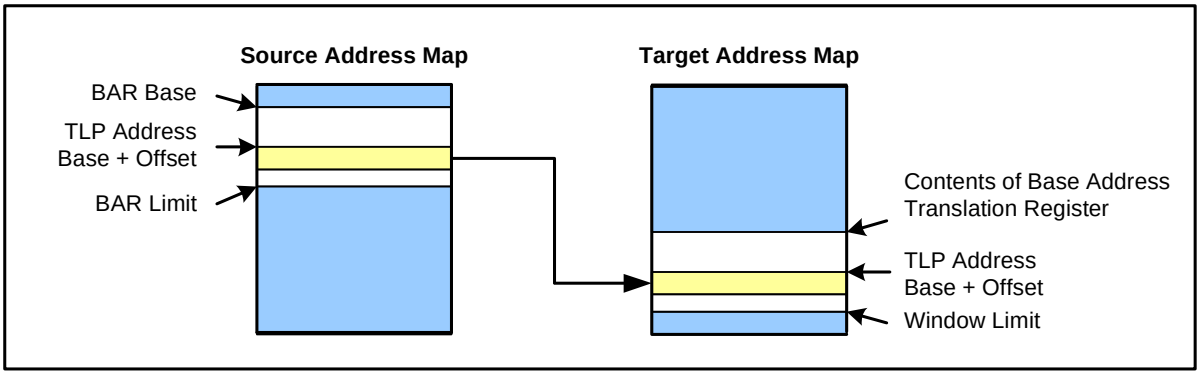


Figure 14-4. NT Port Mapped into Single Target Device

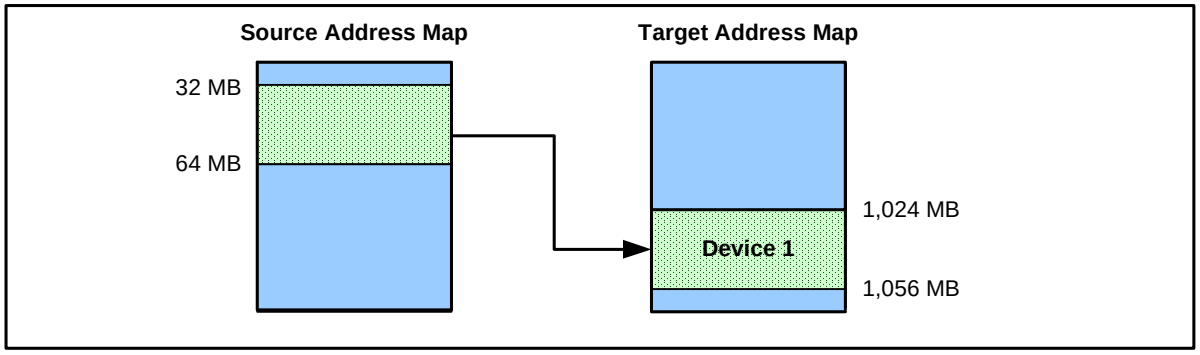
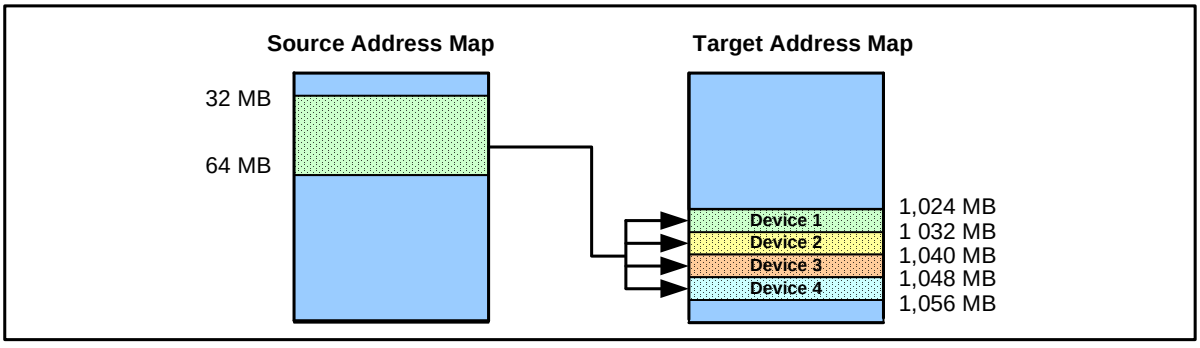


Figure 14-5. NT Port Mapped into Multiple Target Devices



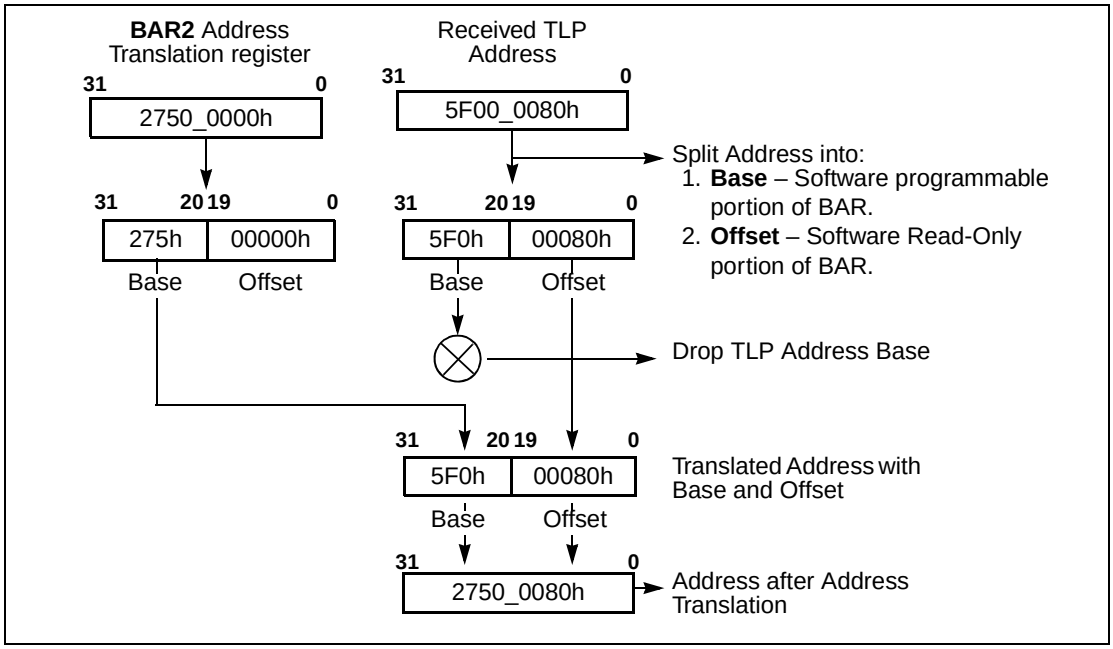
Address Translation Example

Assume the following:

1. NT Port Virtual Interface **BAR2** claims 128-KB Memory space (**BAR2 Setup** register = FFFE_0000h).
2. Configuration software assigns the 5F00_0000h address value to NT Port Virtual Interface **BAR2** and it is within the Transparent upstream Port Memory window.
3. Device driver software programs the **BAR2** Address Translation register to 2750_0000h.

The PEX 8604 receives a transaction to the NT Port Virtual Interface, with address 5F00_0080h. The received transaction address is hitting the NT Port Virtual Interface **BAR2**. The PEX 8604 claims the transaction and executes the address translation described in Figure 14-6.

Figure 14-6. Address Translation Example



14.2 NT PCI-to-PCI Bridge Mode

The PEX 8604 provides an option to insert a PCI-to-PCI bridge (NT PCI-to-PCI bridge) between the NT Port Virtual Interface and internal virtual PCI Bus. Without the NT PCI-to-PCI bridge, the NT Port is parallel to other Transparent downstream bridges within the device hierarchy. This mode is referred to as *Legacy NT mode*. (Refer to Figure 14-7.) With the NT PCI-to-PCI bridge, the NT Port Virtual Interface is connected under one of the downstream bridges. (Refer to Figure 14-8.)

The NT PCI-to-PCI bridge is not connected to a physical Link; therefore, there are some minor differences in the Configuration registers, particularly in some Link control functionality. Insertion of the NT PCI-to-PCI bridge does not affect packet latency, and is controlled by the STRAP_NT_P2P_EN# input, when NT mode is enabled.

Figure 14-7. Legacy NT Mode (STRAP_NT_P2P_EN#=H)

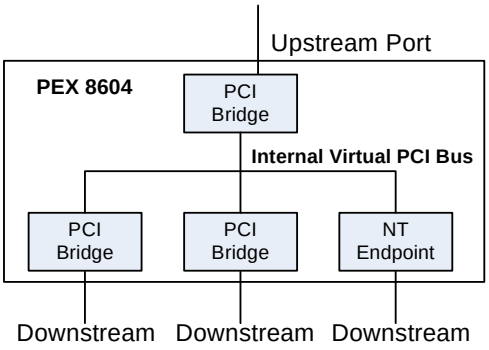
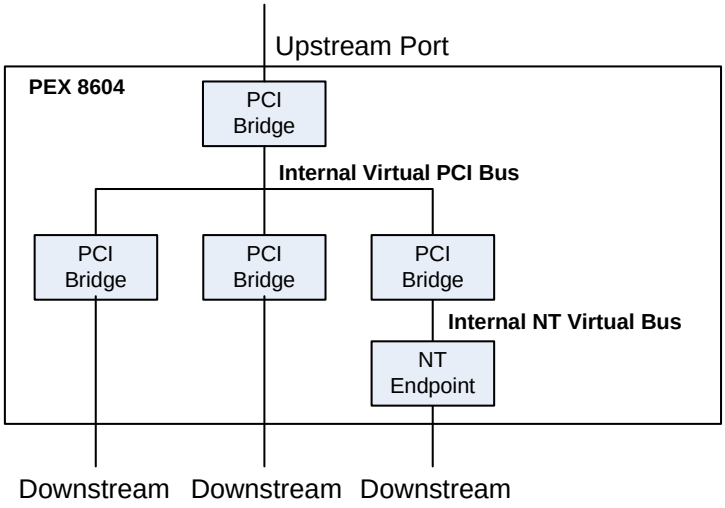


Figure 14-8. NT PCI-to-PCI Bridge Mode (STRAP_NT_P2P_EN#=L)



14.3 Requester ID Translation

Configuration, Message, and Completion transactions are ID-routed instead of address-routed. Of these, the NT Port forwards only the Completion transaction between the two Host domains. PCI Express switches and bridges use the Requester ID (defined in the Completion TLP Header) to route these packets.

The Requester ID consists of the following:

- Requester's PCI Bus Number
- Device Number
- Function Number

The Completer ID consists of the following:

- Completer's PCI Bus Number
- Device Number
- Function Number

Note: *The PCI Bus Number is unique for each Host domain.*

Figure 14-9 illustrates the Memory Request TLP Header format. Figure 14-10 illustrates the Completion TLP Header format.

Figure 14-9. Memory Request TLP Header Format

	Byte 0								Byte 1								Byte 2								Byte 3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Bytes 0-3	R	Fmtx1		Type					R	TC			R				TD	EP	Attr		R				Length							
Bytes 4-7	Requester ID																Tag								Last DW BE				1st DW BE			
Bytes 8-11	Address[63:32]																															
Bytes 12-15	Address[31:0]																								R							

Figure 14-10. Completion TLP Header Format

	Byte 0								Byte 1								Byte 2								Byte 3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Bytes 0-3	R	Fmt		Type					R	TC			R				TD	EP	Attr		R				Length							
Bytes 4-7	Completer ID																Completer Status			BCM	Byte Count											
Bytes 8-11	Requester ID																Tag								R	Lower Address						

14.3.1 Transaction Sequence

To implement a transaction sequence:

1. Requester inserts ID information into the Memory Read TLP that it generates on the initiating Host domain.
2. Switches and bridges between the transaction initiator and PEX 8604 NT Port route this Memory Read TLP, based upon the address.
3. NT Port replaces the Memory Read TLP Requester ID with its ID, and conducts the address translation before it forwards this Requester ID-translated TLP to the target Host domain, because the NT Port is the transaction initiator in the target Host domain.
4. Switches and bridges between the PEX 8604 NT Port and target device route this Memory Read TLP, based upon the address.
5. When the target device generates the Completion TLP, it copies the Memory Read TLP Requester ID into the corresponding Completion TLP *Requester ID* field and inserts its ID into the TLP *Completer ID* field.
6. Switches and bridges between the target device and PEX 8604 NT Port route the Completion TLP, based upon Requester ID (in this case, NT Bridge ID) information.
7. NT Port restores the original Requester ID value from the Configuration register and implements another Requester ID and Completer ID translation for the Completion TLP, before it forwards the Completion TLP to the Requester Host domain.
8. Switches and bridges between the PEX 8604 NT Port and Requester route the Completion TLP, based upon the Requester ID (in this case, NT Bridge ID).
9. Requester accepts and processes the Completion TLP.

14.3.2 Transaction Originating in Local Host Domain

The translation of outgoing Requests from the NT Port Virtual Interface to the NT Port Link Interface uses an 8-entry LUT, as discussed in Section 15.14.2, "NT Port Virtual Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses D94h – DB0h)." Each LUT entry supports all outgoing Requests and any quantity of outstanding Requests made by a single device or function. If a device uses Phantom Function Numbers to increase the maximum quantity of outstanding transactions, each phantom function consumes an LUT entry. Configure the LUT by a serial EEPROM, I^2C, and/or local firmware, so it is possible to transmit Requests to the System Host domain, which provides a measure of security and protection.

When a Memory Request arrives at the NT Port Virtual Interface, the packet Requester ID is associated with this LUT. If it attains one of the enabled LUT entries, the corresponding entry address (TxIndex) is inserted into the *Function Number* field of the packet's Requester ID. Conversely, if it does not match one of the enabled LUT entries, an Unsupported Request (UR) Completion is returned.

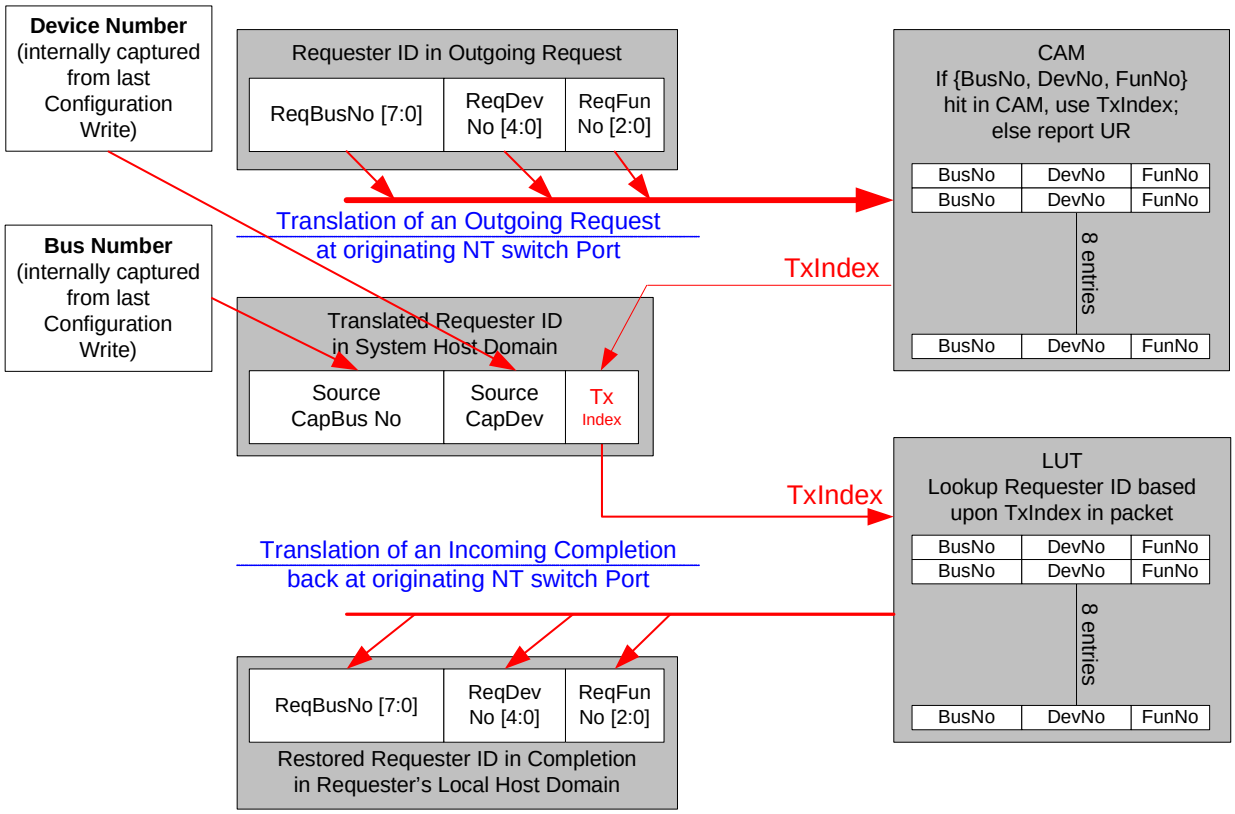
At the same time, the contents of the NT Port Link Interface **Bus Number** and **Device Number Capture** registers (the values used during the last CSR Write to the Port) are copied into the packet Requester ID's *Bus Number* and *Device Number* fields.

A Completion, with translated Requester ID, returned from the System Host domain to the PEX 8604, is recognized when its Requester ID Bus Number and Device Number match the NT Port Link Interface captured Bus Number and Device Number. (Refer to Figure 14-11.)

When the original Requester ID is restored, the following occurs:

1. TxIndex is retrieved from the *Function Number* field of the Completion TLP Requester ID.
2. TxIndex is used to look up the same 8-entry LUT, to restore the original Requester ID.
3. If the selected entry is valid, the restored Requester ID is placed into the Completion *TLP Requester* field; otherwise, an Unexpected Completion is reported.
4. Completion TLP *Completer ID* field is replaced by the NT Port Virtual Interface captured Bus Number, Device Number, and Function Number.
5. Translated Completion TLP is forwarded to the original Requester, in the Local Host domain.

Figure 14-11. Requester ID Translation for Request Originating in Local Host Domain



14.3.3 Transaction Originating in System Host Domain

Transactions originating in the System Host domain use a Receive LUT, with 32 entries, as discussed in Section 16.15.1, "NT Port Link Interface Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses DB4h – DF0h)." This data structure supports up to 32 devices (elsewhere in the System Host domain) that are transmitting Requests through the associated NT Port. Because the Function Number is not used in the LUT association, a separate LUT entry is not required for each requesting or phantom function device. Configure the LUT before transmitting Requests through the NT Port. This Requester registration process, which cannot be accomplished by a peer, is an effective security and protection mechanism.

When a Request is received from the System Host domain and routed to the NT Port, its Requester ID is translated again – Bus Number and Device Number, but not Function Number. The received Memory Request TLP Requester ID is associated with this LUT, and the address (RxIndex) of the corresponding matching entry is substituted into the *Device Number* field of the Memory Request's TLP *Requester ID* field.

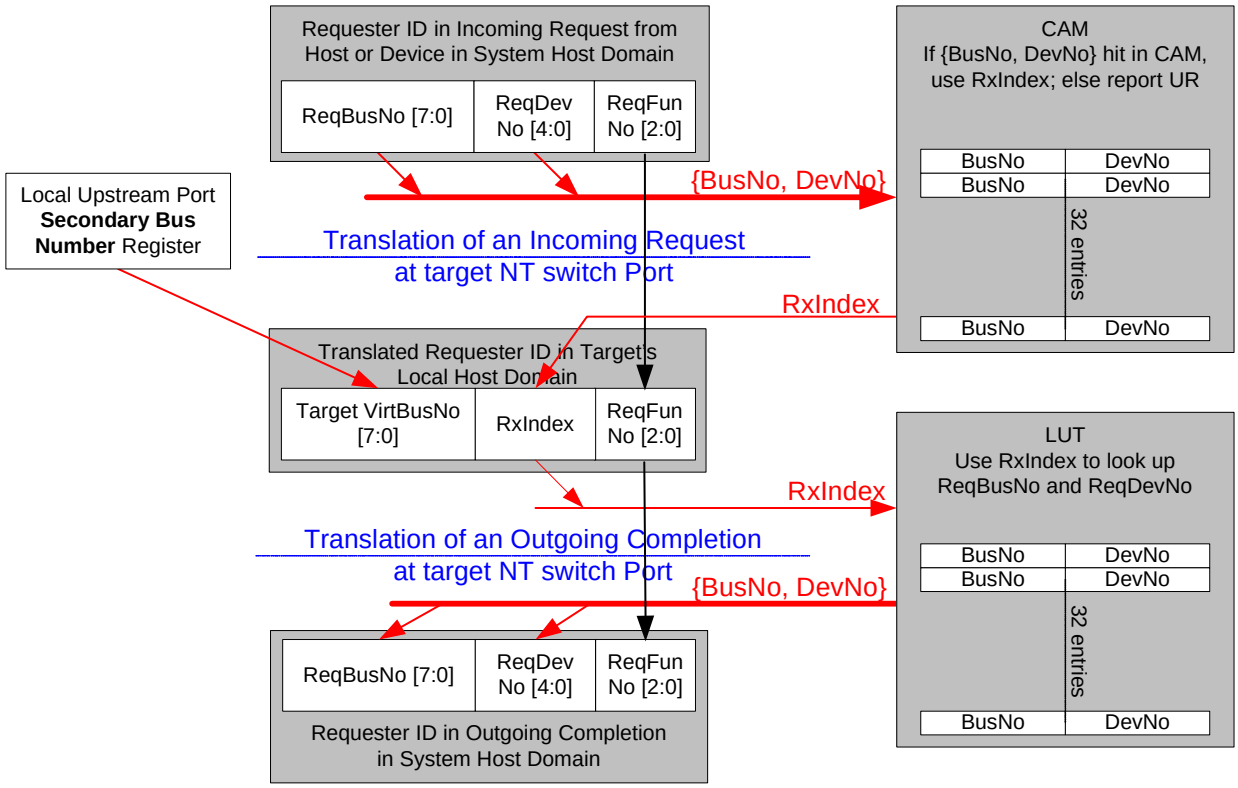
If no match is found, or the matched entry is not enabled, the Request receives a UR response. If a match is found, and matched entry is enabled, the PEX 8604 internal virtual PCI Bus Number is copied into the packet Requester ID's *Bus Number* field. The translated Memory Request TLP is address-translated and forwarded into the Local Host domain.

The PEX 8604 internal virtual PCI Bus Number is sufficient to route the Completion from the Completer back to the NT Port in the Completer's domain, because the NT Port is the only possible Requester on the switch internal virtual PCI Bus. Elsewhere within the PCI Express hierarchy, the Bus Number is sufficient to route the Completion back into the switch containing the NT Port.

The inverse translation occurs when a Completion passes through the NT bridge from the Local Host domain to the System Host domain. The RxIndex is retrieved from the *Device Number* field of the received Completion TLP *Requester ID* Header field, and used to look up the 32-entry LUT. The Completion TLP *Requester ID*, *Bus Number*, and *Device Number* fields are replaced by the decoded LUT-entry Bus Number and Device Number values, if the entry is valid; otherwise, an Unexpected Completion is reported.

The Completion TLP Completer ID is replaced by the NT Port Link Interface captured Bus Number, Device Number, and Function Number values before forwarding the Completion TLP to the System Host domain. (Refer to Figure 14-12.)

Figure 14-12. Requester ID Translation for Request Originating in System Host Domain



14.4 Traffic Class Translation

For Memory Requests originating from the NT Port, the Traffic Class (TC) Translation registers can be programmed to translate the original Traffic Class of the TLP to a higher-priority Traffic Class (TC[7-1]). This TC translation allows use for both VC resources available in the PEX 8604, for traffic differentiation and Quality of Service (QoS). Most Root Complexes implement a single Virtual Channel (VC). With a single VC implementation, there is no differentiation of traffic, because all Requests and Completions are queued, in order, in the same VC resources. Moreover, typically, Root Complexes support a single Traffic Class, TC0, when generating Requests.

The NT Port can be used to provide a separate path to the CPU. However, because the Root Complex can support only TC0, the TC translation allows the PEX 8604 to modify the Traffic Class for incoming TLPs, thus providing traffic differentiation.

For Posted TLPs (Memory Writes) received at the NT Port Link Interface, the PEX 8604 modifies the current TC in the packet Header, with the programmed TC. The updated TLP can make use of the multiple Virtual Channels available in the PEX 8604.

For Non-Posted TLPs (Memory Reads), the PEX 8604 changes the TC of the Memory Read Request so that it can take advantage of any additional VC resources. When the Target responds with a Completion, the PEX 8604 changes the Completion TC of the Completion back to the original TC (TC0), before the TC is forwarded out from the NT Port Link Interface. The TC Translation registers are located in the NT Port Link Interface, at register offset 960h.

14.5 NT Port Power Management Handling

14.5.1 Active State Power Management

The NT Port Link Interface endpoint supports the Active State Power Management (ASPM) L0s and L1 Link PM states. The NT Port Virtual Interface endpoint implements the CSRs for ASPM support. However, it does not enter into the low-power states, because there is no physical Link associated with it.

The PEX 8604 Transparent Ports also support the ASPM L0s and L1 Link PM states in Transparent mode.

14.5.2 PCI-PM and PME Turn Off Support

When NT mode is enabled, the NT Port Link Interface Type 0 endpoint behaves as any other endpoints in the PCI Express PCI-PM D3hot Device PM state. Once in the D3hot Device PM state, the NT Port Link Interface Type 0 endpoint Requests PCI-PM L1 Link PM state entry and finally settles in the L1 Link PM state. Only Configuration accesses and Messages to the NT Port Link Interface Type 0 endpoint are supported in the D3hot Device PM state. The Root Complex transmits PME_Turn_Off Messages when the NT Host decides to turn Off the main power and Reference Clock. The PEX 8604 NT Port Link Interface Type 0 endpoint indicates its readiness to lose power, by transmitting a PME_TO_Ack Message toward the upstream device. The PME_TO_Ack Message is transmitted when there are no pending TLPs to transmit upstream, toward the NT Port Link Interface. The Port Requests the L2/L3 Ready Link PM state, by transmitting PM_Enter_L23 Data Link Layer Packets (DLLPs) to the upstream device after transmitting a PME_TO_Ack TLP. The Port settles into the L3 Link PM state when the Power Controller removes the main power and Reference Clock.

When the PME_Turn_Off Message is received on the PEX 8604 Transparent upstream Port, the Port broadcasts this Message to all PEX 8604 downstream devices, including the NT Port Virtual Interface Type 0 endpoint. After the PME_TO_Ack Message is received from all downstream devices and the PEX 8604 NT Port Virtual Interface Type 0 endpoint, the PEX 8604 Transparent upstream Port transmits an aggregated PME_TO_Ack Message to the upstream component after it finishes transmitting all pending TLPs to the upstream component. When NT mode is enabled, the PEX 8604 Transparent downstream Ports allow the attached devices to enter the PCI-PM-compatible L1 Link PM state. The PEX 8604 NT Port Virtual Interface Type 0 endpoint never enters the PCI-PM L1 Link PM state.

14.5.3 Message Generation

The PEX 8604 NT Port Link Interface Type 0 endpoint never generates PM_PME Messages. The PEX 8604 NT Port Virtual Interface Type 0 endpoint never receives Set_Slot_Power_Limit Messages nor generates PM_PME Messages.

14.6 Expansion ROM

The NT Port Link Interface supports Expansion ROM, by default. Expansion ROM support can be moved from the NT Port Link Interface to the NT Port Virtual Interface, by Setting the **Ingress Control** register *Expansion ROM Virtual Side* bit (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 660h[23]).

The NT Port supports 16- or 32-KB-sized Expansion ROM, based upon the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 268h[16]) value.

Note: *Expansion ROM can be enabled in either the NT Port Virtual Interface or NT Port Link Interface, but not both simultaneously. Expansion ROM is enabled, by default, in the NT Port Link Interface (**Ingress Control** register Expansion ROM Virtual Side bit is Cleared).*

14.7 NT Port Interrupts

The NT Port Virtual and Link Interfaces can both generate interrupts in response to specific events. The NT Port must not receive any INT*x* Message Requests. If the NT Port receives an INT*x* Message Request, the Request is handled as a Malformed TLP error.

14.7.1 NT Port Virtual Interface Interrupts

The NT Port Virtual Interface generates interrupts to the Local Host for the following reasons (all are masked, by default, and must not be masked to be enabled):

- Doorbell interrupts
- NT Port Link Interface detected an Correctable TLP error
- NT Port Link Interface detected an Uncorrectable TLP error (option to signal Fatal and/or Non-Fatal)
- NT Port Link Interface *DL_Active* state change
- NT Port Link Interface received an Uncorrectable Error Message

NT-Virtual Doorbell interrupts and NT-Link errors and events can use the INT*x*, MSI, or PEX_INTA# signaling mechanisms (all mutually exclusive), as follows:

- PEX_INTA# output can be enabled for NT-Virtual Doorbell interrupts, by Setting the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port, offset 1C8h[7]).
- PEX_INTA# output can be enabled for NT-Link Error and Event interrupts, by Setting the register's *Enable PEX_INTA# Interrupt Output(s) for Device-Specific Error-Triggered Interrupts* bit (offset 1C8h[5])

Refer to Section 14.1.6 for Doorbell interrupt details.

The NT Port Virtual Interface de-asserts INT*x* or PEX_INTA# interrupts in response to one or more of the following conditions:

- NT Port Virtual Interface **PCI Command** register *Interrupt Disable* bit (offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- NT Port Link goes down (DL_Down condition) or the NT Port Link Interface receives a Hot Reset
- Software Clears the *Interrupt Status* bit, or Sets the *Doorbell Interrupt Request Clear* bit

In NT PCI-to-PCI Bridge mode, for tracking purposes, an NT Port Virtual Interface-generated interrupt is treated like an event that is external to the PCI-to-PCI bridge. If software asserts a Secondary Bus Reset from this PCI-to-PCI bridge, the PCI-to-PCI bridge de-asserts the NT Port Virtual Interface interrupt.

When the NT Port Link Interface detects Correctable TLP errors, the NT Port Virtual Interface signals the interrupt to the Local Host, if the interrupt signaling is enabled and not masked (**Link Error Status Virtual** register *Link Side Correctable Error Status* bit is Set, and **Link Error Mask Virtual** register *Link Side Correctable Error Mask* bit is Cleared (NT Port Virtual Interface as Port 0, offsets FE0h[0] and FE4h[0]), respectively).

When the NT Port Link Interface detects Uncorrectable TLP errors, the NT Port Virtual Interface signals the interrupt to the Local Host, if the interrupt signaling is enabled and not masked (**Link Error Status Virtual** register *Link Side Uncorrectable Error Status* bit is Set, and **Link Error Mask Virtual** register *Link Side Uncorrectable Error Mask* bit is Cleared (NT Port Virtual Interface as Port 0, offsets FE0h[1] and FE4h[1]), respectively).

An NT Port Link Interface *DL_Active* state change occurs upon detection of an NT Port Link Interface *DL_Down* state rise edge and fall edge. This signals the interrupt to the Local Host, if the interrupt signaling enabled and not masked (**Link Error Status Virtual** register *Link Side DL Active Change Status* bit is Set, and **Link Error Mask Virtual** register *Link Side DL Active Change Mask* bit is Cleared (NT Port Virtual Interface as Port 0, offsets FE0h[2] and FE4h[2]), respectively).

When the NT Port Link Interface receives an Uncorrectable Error Message, the NT Port Virtual Interface signals the interrupt to the Local Host, if the interrupt signaling is enabled and not masked (**Link Error Status Virtual** register *Link Side Uncorrectable Error Message Drop Status* bit is Set, and **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit is Cleared (NT Port Virtual Interface as Port 0, offsets FE0h[3] and FE4h[3]), respectively).

14.7.2 NT Port Link Interface Interrupts

The NT Port Link Interface generates interrupts to the System Host for NT-Link Doorbell interrupts detected at the NT Port Link Interface ingress Port (interrupts are masked, by default). The NT Port Link Interface should not detect any Device-Specific errors.

NT-Link Doorbell interrupts can use the INT*x*, MSI, or PEX_INTA# signaling mechanisms (all mutually exclusive). PEX_INTA# output can be enabled for NT-Link Doorbell interrupts, by Setting the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for NT-Link Doorbell-Generated Interrupts* bit (NT Port Link Interface, offset 1C8h[7]). Refer to Section 14.1.6 for Doorbell interrupt details.

The NT Port Link Interface de-asserts INT*x* or PEX_INTA# interrupts in response to one or more of the following conditions:

- NT Port Link Interface **PCI Command** register *Interrupt Disable* bit (offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- NT Port Link goes down (DL_Down condition) or the NT Port Link Interface receives a Hot Reset
- Software Clears the *Interrupt Status* bit, or Sets the *Doorbell Interrupt Request Clear* bit

14.8 NT Port Error Handling

The PEX 8604 NT Port Virtual Interface endpoint logs TLP errors, for TLPs that travel from the NT Port Virtual Interface to the NT Port Link Interface. The PEX 8604 signals Error Messages to the Local Host (Host closest to the upstream Port). The PEX 8604 provides an option to communicate this error condition to the System Host (Host closest to the NT Port), by signaling an interrupt.

The PEX 8604 NT Port Link Interface endpoint logs TLP errors, for TLPs that travel from the NT Port Link Interface to the NT Port Virtual Interface. The PEX 8604 signals Error Messages to the System Host (Host closest to the NT Port).

When the PEX 8604 receives a TLP, it performs the following:

1. TLP integrity check,
2. Address decode,
3. Address translation,
4. Requester ID translation, and
5. ECRC re-generation,

before transmitting the TLP through the NT Port. If the PEX 8604 detects an ECRC error, it corrupts the re-generated ECRC before transmitting the TLP through the NT Port. The PEX 8604 also provides options for dropping error-detected ECRC or endpoint (EP) TLPs (**Ingress Control Shadow** register *Drop ECRC TLPs* and *Drop EP TLPs* bits (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 664h[8, 4], respectively)).

The PEX 8604 does not generate the ECRC for a TLP that passes through the NT Port, if the received TLP does not have its *TD* bit Set.

The PEX 8604 drops all TLPs traveling from the NT Port Virtual Interface to the NT Port Link Interface, if the internal RAM Fatal ECC error is detected, until the PEX 8604 receives a Hot Reset from a Local Host.

14.8.1 NT Port Link Interface Error Handling

If the NT Port Link Interface receives an Uncorrectable Error message, it reports a Malformed TLP error, by default. However, if the **Ingress Control Shadow** register *NT Error Message Drop* bit (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 664h[11]) is Set, the NT Port Link Interface drops the Message, and logs the error in the **Link Error Status Virtual** register *Link Side Uncorrectable Error Message Drop Status* bit (NT Port Virtual Interface as Port 0, offset FE0h[3]. If the corresponding **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit (NT Port Virtual Interface as Port 0, offset FE4h[3]) is Set, the NT Port Virtual signals an interrupt (INT*x*, MSI, or PEX_INTA#) to the Local Host through the upstream Port, if interrupts are enabled.

14.8.2 NT PCI-to-PCI Bridge Mode Error Handling

In NT PCI-to-PCI Bridge mode, for the NT Port Virtual Interface to generate an Error Message, the following error-forwarding *Enable* bits, in both the NT PCI-to-PCI bridge and the upstream Port, must be Set:

- **PCI Command** register (offset 04h)
  - *SERR# Enable* (bit 8)
- **Bridge Control** register (offset 3Ch)
  - *SERR# Enable* (bit 17)
- **Device Control** register (offset 70h)
  - *Correctable Error Reporting Enable* (bit 0)
  - *Non-Fatal Error Reporting Enable* (bit 1)
  - *Fatal Error Reporting Enable* (bit 2)

When the NT Port Virtual Interface generates an error Message, the NT PCI-to-PCI bridge also logs the error status in the following NT PCI-to-PCI Bridge mode registers, while sending the Message in the upstream direction:

- **Secondary Status** register (offset 1Ch)
  - *Received System Error* (bit 30)
- **PCI Status** register (offset 04h)
  - *Signaled System Error* (bit 30)

14.9 Cursor Mechanism

A software application can use the Device-Specific Cursor Mechanism to access the PEX 8604 NT Port Configuration Space registers. The registers that support the Device-Specific Cursor Mechanism are the **Configuration Address Window** and **Configuration Data Window** registers (offsets F8h and FCh, respectively). A software application can also:

- Select the Configuration Register offset, by using the **Configuration Address Window** register
- Perform Read accesses to the **Configuration Data Window** register, to read to the selected Configuration register
- Perform Write accesses to the **Configuration Data Window** register, to write to the selected Configuration register

Configuration transactions have access to this Device-Specific Cursor Mechanism, if NT mode is enabled.

For details regarding the **Configuration Address Window** and **Configuration Data Window** registers, refer to:

- Section 15.10, "NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)"
- Section 16.10, "NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)"

14.10 Port Programmability

The PEX 8604 supports the capability of programming the upstream Port and NT Port Number. The Configuration register for the upstream Port and NT Port is in the **Debug Control** register *Upstream Port ID* and *NT Port Number* fields (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[11:8, 27:24], respectively). This register is updated, based upon the external STRAP_NT_ENABLE# and STRAP_NT_UPSTRM_PORTSEL[3:0] inputs, by default. A serial EEPROM, I^2C, and/or software can be used to override the external strap values.

A software application can change the upstream Port and NT Port location to another Port Number during runtime, or as part of a failover sequence. It is recommended that the PEX 8604 be in an Idle state (no traffic) when changing the upstream Port and NT Port Numbers during runtime. During a failover sequence, application software must be able to handle all spurious TLPs that it receives as a result of the failover process.

Chapter 15 NT Port Virtual Interface Registers – NT Mode Only

15.1 Introduction

Note: *Check the latest design guides, application notes and errata list for Non-Transparent (NT) usage.*

The NT Port includes two sets of Configuration, Capability, Control, and Status registers, to support the Virtual and Link Interfaces. This chapter defines the NT Port Virtual Interface registers. Other registers are defined in:

- Chapter 13, "Transparent Port Registers"
- Chapter 16, "NT Port Link Interface Registers – NT Mode Only"

Note: *For Chip-specific registers (those that exist only in Port 0), if Port 0 is a Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.*

All PEX 8604 registers can be accessed by Configuration or Memory Requests.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI Express Base r2.0*

15.2 NT Port Virtual Interface Type 0 Register Map

Table 15-1 defines the NT Port Virtual Interface Type 0 register mapping.

Table 15-1. NT Port Virtual Interface Type 0 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)		Capability Pointer (40h)	00h … 34h … 3Ch
	Next Capability Pointer (48h)	Capability ID (01h)	40h
NT Port Virtual Interface PCI Power Management Capability Registers (Offsets 40h – 44h)			44h
	Next Capability Pointer (68h)	Capability ID (05h)	48h
NT Port Virtual Interface MSI Capability Registers (Offsets 48h – 64h)			… 64h
	Next Capability Pointer (A4h)	Capability ID (10h)	68h
NT Port Virtual Interface PCI Express Capability Registers (Offsets 68h – A0h)			… A0h
	Next Capability Pointer (C8h)	SSID/SSVID Capability ID (0Dh)	A4h
NT Port Virtual Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)			… C4h
	Next Capability Pointer 3 (00h)	Capability ID 3 (09h)	C8h
NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)			… FCh
Next Capability Offset (FB4h)	1h	PCI Express Extended Capability ID (0003h)	100h
NT Port Virtual Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)			… 134h
Reserved			138h – 144h
Next Capability Offset (448h or 950h)	1h	PCI Express Extended Capability ID (0002h)	148h
NT Port Virtual Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)			… 1BCh

Table 15-1. NT Port Virtual Interface Type 0 Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)		1C0h …
Next Capability Offset (950h)	1h PCI Express Extended Capability ID (000Bh)	448h
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)		…
Next Capability Offset 2 (C34h)	1h PCI Express Extended Capability ID 2 (000Bh)	950h
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)		…
Next Capability Offset 4 (000h)	1h PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)		… C88h
NT Port Virtual Interface NT Bridging-Specific Registers (Offsets C8Ch – EECh)		C8Ch … EECh
NT Port Virtual Interface Device-Specific Registers (Offsets E40h – F8Ch)		EF0h … F8Ch
Reserved	F90h –	FB0h
Next Capability Offset (148h)	1h PCI Express Extended Capability ID (0001h)	FB4h
NT Port Virtual Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)		… FDCh
NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)		FE0h … FFCh

15.3 Register Access

The PEX 8604 NT Port Virtual Interface implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) comprise the PCI-compatible Configuration Space, and the upper 960 Dwords (offsets 100h through FFFh) comprise the PCI Express Extended Configuration Space. The PEX 8604 supports three mechanisms for accessing the NT Port Virtual Interface registers:

- PCI Express Base r2.0 Configuration Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

15.3.1 *PCI Express Base r2.0* Configuration Mechanism

The *PCI Express Base r2.0* Configuration mechanism is divided into two mechanisms:

- **PCI r3.0-Compatible Configuration Mechanism** – Provides Conventional PCI access to the first 256 bytes (the bytes at offsets 00h through FFh) of the NT Port Virtual Interface Configuration Register space
- **PCI Express Enhanced Configuration Access Mechanism** – Provides access to the entire 4-KB Configuration Space

Both are described in the sections that follow.

15.3.1.1 *PCI r3.0*-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PEX 8604 NT Port Virtual Interface's first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration Space. (Refer to Figure 15-1.)

The mechanism uses PCI Type 0 and Type 1 Configuration transactions to access the PEX 8604 Configuration registers. All Ports capture the Bus Number and Device Number assigned by the upstream device on the PCI Express Link attached to the PEX 8604 upstream Port, as required by the *PCI Express Base r2.0*.

The PEX 8604 decodes all Type 1 Configuration accesses received on its upstream Port, when any of the following conditions exist:

- If the Bus Number specified in the Configuration access is the Bus Number of the PEX 8604 internal virtual PCI Bus, the PEX 8604 automatically converts the Type 1 Configuration access into the appropriate Type 0 Configuration access for the specified device.
  - If the specified device corresponds to the NT Port Virtual Interface (or to the PCI-to-PCI bridge in one of the PEX 8604 Transparent downstream Ports), the PEX 8604 processes the Read or Write Request
  - If the specified Device Number does not correspond to any of the PEX 8604 downstream Port Device Numbers nor NT Port Number, the PEX 8604 responds with an Unsupported Request (UR)

This mechanism uses the same Request format as the PCI Express Enhanced Configuration Access Mechanism. For PCI-compatible Configuration Requests, the *Extended Register Address* field must be all zeros (0).

Because the mechanism is limited to the first 256 bytes of the NT Port Virtual Interface Configuration register space, one of the following must be used to access beyond Byte FFh:

- PCI Express Enhanced Configuration Access Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

15.3.1.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism uses a flat, Root Complex Memory-Mapped Address space to access the device Configuration registers. In this case, the Memory address determines the Configuration register accessed, and the Memory data returns the addressed register's contents. The Root Complex converts the Memory transaction into a Configuration transaction.

This mechanism can be used to access all PEX 8604 Configuration registers.

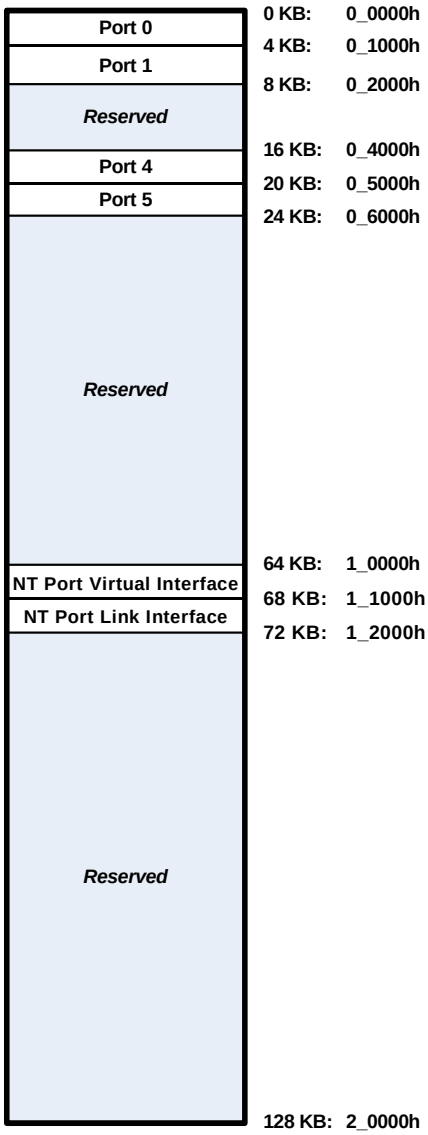
15.3.2 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the registers for all Ports within a single 128-KB Memory map, as illustrated in Figure 15-1. This Memory map is identical for Upstream Port **BAR0/1**, NT Port Virtual Interface **BAR0/1**, and NT Port Link Interface **BAR0/1**. The registers of each Port are located within a 4-KB range.

When the NT Port is enabled at Fundamental Reset, the NT Port Virtual and Link Interface registers use the *PCI r3.0* Type 0 Configuration Space Header. In NT PCI-to-PCI Bridge mode (STRAP_NT_P2P_EN#=L), the NT PCI-to-PCI bridge (between the NT Port Virtual Interface and internal virtual PCI Bus) registers use the *PCI r3.0* Type 1 Configuration Space Header, and are mapped to the 4-KB Address space of the Port Number that is assigned as the NT Port (indicated in the **Debug Control** register *NT Port Number* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[27:24])).

To use this mechanism, use the PCI r3.0-Compatible Configuration Mechanism to program the PEX 8604 NT Port Virtual Interface **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively). After the PEX 8604 NT Port Virtual Interface Memory-Mapped register Base address is Set, the PEX 8604 Configuration Space registers are accessed, using Memory Reads and Writes to the 4-KB range, starting at offset 64 KB (1_0000h, Virtual Interface) and offset 68 KB (1_1000h, Link Interface).

Figure 15-1. NT Mode Configuration Register Mapping to Memory-Mapped BAR



15.3.3 Device-Specific Cursor Mechanism

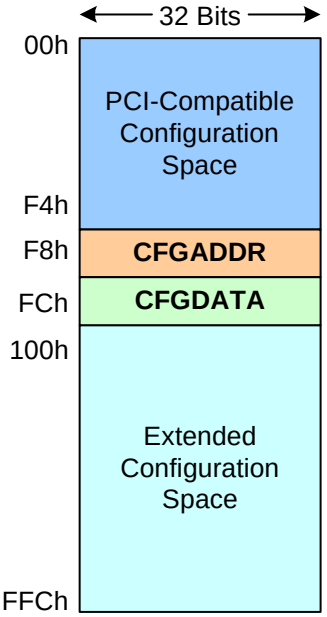
The Device-Specific Cursor mechanism is provided for use in development systems that can only generate *PCI r3.0* Configuration cycles (*that is*, the system cannot use either the Device-Specific Memory-Mapped Configuration Mechanism, nor generate Extended Configuration Requests to access the Extended Configuration Space).

In Figure 15-2, the software uses the **Configuration Address Window** (CFGADDR) register (offset F8h) to point to the NT Port Virtual or Link Interface Configuration Space registers, including the PCI Express Extended Configuration Space registers (offsets 100h through FFFh).

Software uses the **Configuration Data Window** (CFGDATA) register (offset FCh) to write to or read from the selected Configuration Space registers.

Refer to Section 15.10, "NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)," for the register descriptions.

Figure 15-2. Configuration Space View



15.4 Register Descriptions

The remainder of this chapter details the PEX 8604 NT Port Virtual Interface registers, including:

- Bit/field names
- Description of register functions in the PEX 8604 NT Port Virtual and Link Interfaces
- Type (*such as* RW or HwInit; refer to Table 13-5, "Register Types, Grouped by User Accessibility," for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8604 serial EEPROM and/or I^2C/SMBus Initialization feature
- Default power-on/reset value

15.5 NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header registers. Table 15-2 defines the register map.

Table 15-2. NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
PCI Class Code			PCI Revision ID	08h
PCI BIST ***(Not Supported)***	PCI Header Type	Master Latency Timer ***(Not Supported)***	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Base Address 2				18h
Base Address 3				1Ch
Base Address 4				20h
Base Address 5				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capability Pointer (40h)	34h
Reserved				38h
Max_Lat ***(Reserved)***	Min_Gnt ***(Reserved)***	PCI Interrupt Pin	PCI Interrupt Line	3Ch

Register 15-1. 00h PCI Configuration ID

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8604, if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	8604h

Register 15-2. 04h PCI Command/Status

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Command			
0	**I/O Access Enable** The PEX 8604 does not claim I/O resources, nor does it forward I/O transactions through the NT Port. The value of this register is "Don't Care."	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8604 ignores Memory Space Requests on the NT Port Virtual Interface 1 = PEX 8604 accepts Memory Space Requests received on the NT Port Virtual Interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8604 forwarding of Memory Requests upstream. Does not affect Message forwarding nor Completions. 0 = PEX 8604 handles Memory Requests received on the NT Port Link Interface as Unsupported Requests (UR); for Non-Posted Requests, the PEX 8604 returns a Completion with UR Completion status 1 = PEX 8604 forwards Memory Requests in the upstream direction	RW	Yes	0
3	**Special Cycle Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
4	**Memory Write and Invalidate Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
5	**VGA Palette Snoop** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
6	**Parity Error Response Enable** Controls bit 24 (*Master Data Parity Error Detected*).	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
8	**SERR# Enable** Controls bit 30 (*Signaled System Error*). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the NT Port Virtual Interface to the Root Complex	RW	Yes	0
9	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
10	**Interrupt Disable** 0 = NT Port Virtual Interface is enabled to generate INT*x* Interrupt Messages 1 = NT Port Virtual Interface is prevented from generating INT*x* Interrupt Messages	RW	Yes	0
15:11	***Reserved***	RsvdP	No	0-0h

Register 15-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Status			
18:16	***Reserved***	RsvdP	No	000b
19	**Interrupt Status** 0 = No INT*x* interrupt is pending 1 = INT*x* interrupt is pending internally to the NT Port Virtual Interface –or– PEX_INTA# (if enabled) is asserted	RO	No	0
20	**Capability List** Capability function is supported. Set, as required by the *PCI Express Base r2.0*.	RO	Yes	1
21	**66 MHz Capable** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0

Register 15-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**Master Data Parity Error Detected** If bit 6 (*Parity Error Response Enable*) is Set, the NT Port Virtual Interface Sets this bit when the NT Port: • Forwards the poisoned Transaction Layer Packet (TLP) Write Request from the NT Port Link Interface to the NT Port Virtual Interface, –or– • Receives a Completion marked as poisoned on the NT Port Virtual Interface If the *Parity Error Response Enable* bit is Cleared, the PEX 8604 never Sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported***	RsvdP	No	00b
27	**Signaled Target Abort** The NT Port Virtual Interface Sets this bit if any of the following conditions exist: • NT Port Virtual Interface receives a Completion (from a Transparent Port) that has a Completion status of Completer Abort (CA), –or– • NT Port Virtual Interface receives a Memory Request targeting a PEX 8604 register, and the Payload Length (indicated within the Memory Request Header) is greater than 1 DWord • NT Port Virtual Interface receives a Memory Request targeting a PEX 8604 register address within a non-existent Port • NT Port Virtual Interface receives a Memory Write Request targeting enabled Expansion ROM Address space (Expansion ROM Base Address Register (BAR), offset 30h) ***Note:*** *When Set during a forwarded Completion, the* ***Uncorrectable Error Status*** *register Completer Abort Status bit (offset FB8h[15]) is not Set.*	RW1C	Yes	0
28	**Received Target Abort** ***Reserved***	RsvdP	No	0
29	**Received Master Abort** ***Reserved***	RsvdP	No	0
30	**Signaled System Error** If bit 8 (*SERR# Enable*) is Set, the NT Port Virtual Interface Sets this bit when transmitting an ERR_FATAL or ERR_NONFATAL Message to the upstream Port.	RW1C	Yes	0
31	**Detected Parity Error** This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility. 1 = NT Port Virtual Interface received a Poisoned TLP, regardless of the bit 6 (*Parity Error Response Enable*) state	RW1C	Yes	0

Register 15-3. 08h PCI Class Code and Revision ID

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Revision ID				
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the Silicon Revision (BAh), the PLX-assigned Revision ID for this version of the PEX 8604. The PEX 8604 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	BAh
PCI Class Code				**068000h**
15:8	**Register-Level Programming Interface**	RO	Yes	00h
23:16	**Sub-Class Code** Other bridge devices.	RO	Yes	80h
31:24	**Base Class Code** Bridge devices.	RO	Yes	06h

Register 15-4. 0Ch Miscellaneous Control

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Cache Line Size				
7:0	**Cache Line Size** System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8604 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	**Master Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00h
PCI Header Type				
22:16	**Configuration Layout Type** Type 0 Configuration Header for the NT Port.	RO	No	00h
23	**Multi-Function Device** 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	No	0
PCI BIST				
31:24	**PCI BIST** ***Not supported*** Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

Register 15-5. 10h Base Address 0 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Notes: *By default, NT Port Virtual Interface* ***BAR0*** *is enabled and* ***BAR1*** *is disabled, to provide a 32-bit* ***BAR0*** *for register access.* ***BAR1*** *can be enabled (by serial EEPROM and/or I²C), to provide a 64-bit* ***BAR0/1****, by programming the* ***NT Port Virtual Interface BAR0/1 Setup*** *register BAR0/1 Enable field (NT Port Virtual Interface, offset D0h[1:0]) to 11b (which enables both* ***BAR0*** *and* ***BAR1****).* *When software writes to the NT Port Virtual Interface* ***BAR0****, the value is automatically copied to the* ***NT Port Virtual Interface BAR0 (Shadow Copy)*** *register (NT Port Virtual Interface, offset D68h).*				
0	**Memory Space Indicator** When enabled, the Base Address register maps PEX 8604 Port Configuration registers into Memory space. ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Base Address register maps the PEX 8604 Port Configuration registers into Non-Prefetchable Memory space	RO	Yes	0
16:4	***Reserved***	RsvdP	No	0-0h
31:17	**Base Address 0** 128-KB-aligned Base address used for Memory-Mapped access to the 128-KB block of all PEX 8604 registers (4 KB, per Port).	RW	Yes	0-0h

Register 15-6. 14h Base Address 1 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *When software writes to the NT Port Virtual Interface* ***BAR1****, the value is automatically copied to the* ***NT Port Virtual Interface BAR1 (Shadow Copy)*** *register (NT Port Virtual Interface, offset D6Ch).*				
31:0	**Upper 32-Bit Address for Memory-Mapped BAR** For 64-bit addressing (**BAR0/1**), Base Address 1 (**BAR1**) extends Base Address 0 (**BAR0**) to provide the upper 32 Address bits when the **Base Address 0** register *Memory Map Type* field (offset 10h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	RO when the **Base Address 0** register (**BAR0**) is not enabled as a 64-bit BAR (*Memory Map Type* field (offset 10h[2:1]) is not programmed to 10b).	RO	Yes	0000_0000h

Register 15-7. 18h Base Address 2 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *When software writes to the NT Port Virtual Interface* ***Base Address 2*** *register (**BAR2**), the value is automatically copied to the* ***NT Port Virtual Interface*** *BAR2 (Shadow Copy) register (NT Port Virtual Interface, offset D70h).*				
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 2** Resolution is 1 MB.	RW	Yes	000h

Register 15-8. 1Ch Base Address 3 (NT Port Virtual Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Notes: *When software writes to the NT Port Virtual Interface* ***Base Address 3*** *register (**BAR3**), the value is automatically copied to the* ***NT Port Virtual Interface*** *BAR3 (Shadow Copy) register (NT Port Virtual Interface, offset D74h).* *This register has RW privilege if* ***BAR2/3*** *is configured as a 64-bit BAR (**Base Address 2** register Memory Map Type field (NT Port Virtual Interface, offset 18h[2:1]), is programmed to 10b).*					
0	**Memory Space Indicator** **BAR3** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR2/3**. 0 = Memory space only supported	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 18h[2:1]=00b	RsvdP	No	00b
		Offset 18h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 18h[2:1]=00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 18h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 3**		RW	Yes	000h

Register 15-9. 20h Base Address 4 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *When software writes to the NT Port Virtual Interface* ***Base Address 4*** *register (**BAR4**), the value is automatically copied to the* ***NT Port Virtual Interface*** *BAR4 (Shadow Copy) register (NT Port Virtual Interface, offset D78h).*				
0	**Memory Space Indicator** 0 = Memory space only supported	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 4**	RW	Yes	000h

Register 15-10. 24h Base Address 5 (NT Port Virtual Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Notes: *When software writes to the NT Port Virtual Interface* ***Base Address 5*** *register (**BAR5**), the value is automatically copied to the* ***NT Port Virtual Interface*** *BAR5 (Shadow Copy) register (NT Port Virtual Interface, offset D7Ch).* *This register has RW privilege if* ***BAR4/5*** *is configured as a 64-bit BAR (**Base Address 4** register Memory Map Type field (NT Port Virtual Interface, offset 20h[2:1]), is programmed to 10b).*					
0	**Memory Space Indicator** **BAR5** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR4/5**. 0 = Memory space only supported	Offset 20h[2:1]=00b	RsvdP	No	0
		Offset 20h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 20h[2:1]=00b	RsvdP	No	00b
		Offset 20h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 20h[2:1]=00b	RsvdP	Yes	0
		Offset 20h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 20h[2:1]=00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 20h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 5**		RW	Yes	000h

Register 15-11. 2Ch Subsystem ID and Subsystem Vendor ID

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Subsystem Vendor ID				
15:0	**Subsystem Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I²C.	RO	Yes	10B5h
Subsystem ID				
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8604, if not overwritten by serial EEPROM and/or I²C.	RO	Yes	8604h

Register 15-12. 30h Expansion ROM Base Address

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *Expansion ROM can be enabled in either the NT Port Virtual or Link Interface, but not both simultaneously. Expansion ROM is enabled, by default, in the NT Port Link Interface (**Ingress Control** register Expansion ROM Virtual Side bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 660h[23]) is Cleared).*					
0	**Expansion ROM Enable** 0 = NT Port Virtual Interface Expansion ROM is disabled	NT Port Link Interface, offset 30h[0]=1	RsvdP	No	0
	1 = NT Port Virtual Interface Expansion ROM is enabled, and NT Port Link Interface Expansion ROM is disabled	NT Port Link Interface, offset 30h[0]=0	RW	Yes	0
		NT Port Link Interface, offset 30h[0]=1	RsvdP	No	0
13:1	***Reserved***		RsvdP	No	0-0h
31:14	**Expansion ROM Base Address** If the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 268h[16]) value is 0, the Expansion ROM size is 16 KB (default value is FFFF_C001h). Bit 14 is RW. If the *Expansion ROM Size* bit value is 1, the Expansion ROM size is 32 KB (default value is FFFF_8001h). Bit 14 is RO.	When Bit 0 = 0	RsvdP	No	0-0h
		When Bit 0 = 1	RW	Yes	0-0h

Register 15-13. 34h Capability Pointer

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability Pointer** Default 40h points to the **PCI Power Management Capability** structure.	RO	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 15-14. 3Ch PCI Interrupt

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	PCI Interrupt Line			
7:0	**Interrupt Line Routing Value** Communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture-specific. The value is used by device drivers and operating systems.	RW	Yes	00h
	PCI Interrupt Pin			
15:8	**Interrupt Pin** Identifies the Conventional PCI Interrupt Message(s) the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8604. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
	Min_Gnt			
23:16	**Minimum Grant** ***Reserved*** Does not apply to PCI Express.	RsvdP	No	00h
	Max_Lat			
31:24	**Maximum Latency** ***Reserved*** Does not apply to PCI Express.	RsvdP	No	00h

15.6 NT Port Virtual Interface PCI Power Management Capability Registers (Offsets 40h – 44h)

This section details the NT Port Virtual Interface PCI Power Management Capability registers. Table 15-3 defines the register map.

Table 15-3. NT Port Virtual Interface PCI Power Management Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions ***(Reserved)***	PCI Power Management Status and Control		44h

Register 15-15. 40h PCI Power Management Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability ID** Default = 01h – only value allowed.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	RO	Yes	48h
18:16	**Version** Default = 011b – only value allowed.	RO	Yes	011b
19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.	RsvdP	No	0
20	***Reserved***	RsvdP	No	0
21	**Device-Specific Initialization** 0 = Device-Specific Initialization is ***not*** required	RO	Yes	0
24:22	**AUX Current** The PEX 8604 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.	RO	Yes	000b
25	**D1 Support** ***Not supported*** 0 = PEX 8604 does ***not support*** the D1 Device PM state	RsvdP	No	0
26	**D2 Support** ***Not supported*** 0 = PEX 8604 does ***not support*** the D2 Device PM state	RsvdP	No	0
31:27	**PME Support** The default value is applied to bits [31, 30, and 27] only. PME Messages are disabled, by default. ***Note:*** *This field is **reserved** in NT PCI-to-PCI Bridge mode.*	RO	Yes	0000_0b

Register 15-16. 44h PCI Power Management Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Power Management Status and Control				
1:0	**Power State** Used to determine the current Device PM state of the Port, and to Set the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	RO	Yes	1
7:4	***Reserved***	RsvdP	No	0h
8	**PME Enable** Tied to 0, because the PEX 8604 does ***not*** generate PME in PCI Express mode. ***Note:*** *This bit is **reserved** in NT PCI-to-PCI Bridge mode.*	RsvdP	No	0
12:9	**Data Select** Initially writable by serial EEPROM and/or I²C only[a]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I²C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	RO	Yes	0h
14:13	**Data Scale** Writable by serial EEPROM and/or I²C only[a]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h, and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h.	RO	Yes	00b
15	**PME Status** 0 = PME is not being generated by the NT Port ***Note:*** *This bit is **reserved** in NT PCI-to-PCI Bridge mode.*	RsvdP	No	0

Register 15-16. 44h PCI Power Management Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Power Management Control/Status Bridge Extensions				
21:16	***Reserved***	RsvdP	No	0-0h
22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
PCI Power Management Data				
31:24	**Data** Writable by serial EEPROM and/or I^2C only[a]. There are four supported *Data Select* values (0h, 3h, 4h, and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	RO	Yes	00h

*a. With no serial EEPROM nor previous I^2C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

15.7 NT Port Virtual Interface MSI Capability Registers (Offsets 48h – 64h)

The registers detailed in Section 13.8, "MSI Capability Registers (Offsets 48h – 64h)," are also applicable to the NT Port Virtual Interface. Table 15-4 defines the register map used by the NT Port Virtual Interface.

Table 15-4. NT Port Virtual Interface MSI Capability Register Map[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
MSI Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address				4Ch
MSI Upper Address				50h
Reserved		MSI Data		54h
MSI Mask				58h
MSI Status				5Ch
Reserved				60h – 64h

*a. Offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*

15.8 NT Port Virtual Interface PCI Express Capability Registers (Offsets 68h – A0h)

The registers detailed in Section 13.9, "PCI Express Capability Registers (Offsets 68h – A0h)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-5 (register map; offsets 7Ch and 80h are ***reserved***), and Register 15-17 through Register 15-22.

Table 15-5. NT Port Virtual Interface PCI Express Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capability		Next Capability Pointer (A4h)	Capability ID (10h)	68h
Device Capability				6Ch
Device Status		***Not Supported/Reserved***	Device Control	70h
Link Capability				74h
Link Status		***Reserved***	Link Control	78h
Reserved				7Ch – 88h
Device Capability 2				8Ch
Device Status 2 ***(Reserved)***		Device Control 2		90h
Reserved				94h
Link Status 2		Link Control 2		98h
Reserved				9Ch – A0h

Register 15-17. 68h PCI Express Capability List and Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Express Capability List				
7:0	**Capability ID** Program to 10h, by default, as required by the *PCI Express Base r2.0*.	RO	Yes	10h
15:8	**Next Capability Pointer** Program to A4h, to point to the **Subsystem Capability** structure.	RO	Yes	A4h
PCI Express Capability				
19:16	**Capability Version** The PEX 8604 NT Port Virtual Interface programs this field to 2h, as required by the *PCI Express Base r2.0*.	RO	Yes	2h
23:20	**Device/Port Type** Default = PCI Express Endpoint device.	RO	Yes	0h
24	**Slot Implemented** ***Not valid for PCI Express Endpoint devices*** ***Note:*** *This bit is also **reserved** in NT PCI-to-PCI Bridge mode.*	RsvdP	No	0
29:25	**Interrupt Message Number** The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.	RO	Yes	00_000b
31:30	***Reserved***	RsvdP	No	00b

Register 15-18. 6Ch Device Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
2:0	**Maximum Payload Size Supported** Maximum Payload Size Port limitations are as follows: Because there are x1 and x2 Ports in the Port configuration, the Maximum Payload Size for each Port is limited to 512 bytes. 000b = NT Port Virtual Interface supports a 128-byte maximum payload 001b = NT Port Virtual Interface supports a 256-byte maximum payload 010b = NT Port Virtual Interface supports a 512-byte maximum payload No other encodings are supported.	HwInit	Yes	100b
4:3	**Phantom Functions Supported** ***Not supported***	RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum *Tag* field is 5 bits 1 = Maximum *Tag* field is 8 bits	RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** 111b = No Limit	RO	Yes	111b
11:9	**Endpoint L1 Acceptable Latency** 111b = No Limit	RO	Yes	111b
14:12	***Reserved***	RsvdP	No	000b
15	**Role-Based Error Reporting**	RO	Yes	1
17:16	***Reserved***	RsvdP	No	00b
25:18	**Captured Slot Power Limit Value** For the NT Port Virtual Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	RO	Yes	00h
27:26	**Captured Slot Power Limit Scale** For the NT Port Virtual Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	RO	Yes	00b
31:28	***Reserved***	RsvdP	No	0h

Register 15-19. 70h Device Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Device Control			
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report Correctable errors to the Local Host	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report Non-Fatal errors to the Local Host	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report Fatal errors to the Local Host	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report UR errors to the Local Host	RW	Yes	0
4	**Enable Relaxed Ordering** ***Not supported***	RsvdP	No	0
7:5	**Maximum Payload Size** The NT Port Virtual Interface power-on/reset value is 000b, to support a Maximum Payload Size of 128 bytes. Software can change this field to configure the NT Port Virtual Interface to support other Payload sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capability** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]), for the NT Port Virtual and Link Interfaces. (Requester and Completer domains must possess the same Maximum Payload Size.) 000b = NT Port Virtual Interface supports a 128-byte maximum payload 001b = NT Port Virtual Interface supports a 256-byte maximum payload 010b = NT Port Virtual Interface supports a 512-byte maximum payload No other encodings are supported. ***Note:*** *Software must halt all transactions through the NT Port before changing this field.*	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported***	RsvdP	No	0
9	**Phantom Functions Enable** ***Not supported***	RsvdP	No	0
10	**AUX Power PM Enable** ***Not supported***	RsvdP	No	0
11	**Enable No Snoop** ***Not supported***	RsvdP	No	0
14:12	**Maximum Read Request Size** ***Not supported***	RsvdP	No	000b
15	***Reserved***	RsvdP	No	0

Register 15-19. 70h Device Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Device Status			
16	**Correctable Error Detected** Set when the NT Port Virtual Interface detects a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable*) state. 0 = NT Port Virtual Interface did not detect a Correctable error 1 = NT Port Virtual Interface detected a Correctable error	RW1C	Yes	0
17	**Non-Fatal Error Detected** Set when the NT Port Virtual Interface detects a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable*) state. 0 = NT Port Virtual Interface did not detect a Non-Fatal error 1 = NT Port Virtual Interface detected a Non-Fatal error	RW1C	Yes	0
18	**Fatal Error Detected** Set when the NT Port Virtual Interface detects a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable*) state. 0 = NT Port Virtual Interface did not detect a Fatal error 1 = NT Port Virtual Interface detected a Fatal error	RW1C	Yes	0
19	**Unsupported Request Detected** Set when the NT Port Virtual Interface detects a UR, regardless of the bit 3 (*Unsupported Request Reporting Enable*) state. 0 = NT Port Virtual Interface did not detect a UR 1 = NT Port Virtual Interface detected a UR	RW1C	Yes	0
20	**AUX Power Detected** ***Not supported***	RsvdP	No	0
21	**Transactions Pending** ***Not supported*** Because the PEX 8604 NT Port is a bridging device, it does not track Completion for the corresponding Non-Posted transactions. Therefore, the NT Port Virtual Interface does not implement Transactions Pending.	RsvdP	No	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 15-20. 74h Link Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
3:0	**Supported Link Speeds** Indicates the NT Port Virtual Interface's supported Link speed. 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s and 2.5 GT/s Link speeds are supported All other encodings are ***reserved***.	RO	Yes	0010b (STRAP_RESERVED17#=H) 0001b (STRAP_RESERVED17#=L)
9:4	**Maximum Link Width** The PEX 8604 maximum Link width is x2 = 00_0010b. Valid widths are x1 or x2. Actual maximum Link width is Set by the STRAP_PORTCFG[1:0] inputs. 00_0000b = ***Reserved*** 00_0001b = x1 00_0010b = x2 All other encodings are ***not supported***.	ROS	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.	RO	Yes	11b

Register 15-20. 74h Link Capability *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the **Common Physical Layer Command/Status** register *N_FTS Value* (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 238h[15:8]) value and Link speed. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = NT Port Virtual Interface L0s Link PM state Exit Latency is 512 ns to less than 1 µs at 5.0 GT/s 101b = NT Port Virtual Interface L0s Link PM state Exit Latency is 1 µs to less than 2 µs at 2.5 GT/s All other encodings are ***reserved***. ***Note:*** *The NT Port Virtual Interface never enters the L0s Link PM state, because there is no physical Link attached to it.*	RO	No	100b (5.0 GT/s) 101b (2.5 GT/s)
17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = NT Port Virtual Interface L1 Link PM state Exit Latency is 1 µs to less than 2 µs at 5.0 GT/s 010b = NT Port Virtual Interface L1 Link PM state Exit NT Latency is 2 µs to less than 4 µs at 2.5 GT/s All other encodings are ***reserved***. ***Note:*** *The NT Port Virtual Interface never enters the L1 Link PM state, because there is no physical Link attached to it.*	RO	Yes	001b (5.0 GT/s) 010b (2.5 GT/s)
18	**Clock Power Management**	RO	Yes	0
23:19	***Reserved*** ***Note:*** *Bits [21:19] are also* ***reserved*** *in NT PCI-to-PCI Bridge mode.*	RsvdP	No	0-0h
31:24	**Port Number** The NT Port Number value is selected by the STRAP_NT_UPSTRM_PORTSEL[3:0] inputs. All other encodings are ***reserved***. 00h = Port 0 01h = Port 1 04h = Port 4 05h = Port 5	ROS	No	Set by STRAP_NT_UPSTRM_PORTSEL[3:0] input levels

Register 15-21. 78h Link Status and Control

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Link Control			
1:0	**Active State Power Management (ASPM) Control** The NT Port Virtual Interface ignores this register value, because no external Port connection exists.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**Read Request Return Parameter Control** Read Request Return Parameter "R" control. Read Completion Boundary (RCB).	RO	Yes	0
4	**Link Disable** ***Reserved*** for the NT Port Virtual Interface.	RsvdP	No	0
5	**Retrain Link** ***Reserved*** for the NT Port Virtual Interface.	RsvdP	No	0
6	**Common Clock Configuration** The NT Port Virtual Interface ignores this register value, because no external Port connection exists.	RW	Yes	0
7	**Extended Sync** The NT Port Virtual Interface ignores this register value, because no external Port connection exists.	RW	Yes	0
15:8	***Reserved***	RsvdP	No	00h
	Link Status			
19:16	**Current Link Speed** Indicates the negotiated Link speed of the Port's PCI Express Link. 0001b = 2.5 GT/s Link speed 0010b = 5.0 GT/s Link speed All other encodings are ***reserved***. The value in this field is undefined when the Link is not up.	RO	No	0001b
25:20	**Negotiated Link Width** Reports the Link status of the NT Port Link Interface. Dependent upon the configuration of the physical Ports. Link width is determined by the negotiated value with the attached Lane/Port. 00_0000b = Link is down (default) 00_0001b = x1 or Port is in the *DL_Down* state 00_0010b = x2 All other encodings are ***not supported***.	RO	No	00_0000b
26	**Training Error** ***Reserved*** for the NT Port Virtual Interface.	RsvdP	No	0
27	**Link Training** ***Reserved*** for the NT Port Virtual Interface. Always read as 0.	RsvdP	No	0
28	**Slot Clock Configuration** Because there is no external connection to the NT Port Virtual Interface, this bit is always Cleared, which indicates that the PEX 8604 uses an independent clock.	HwInit	Yes	0
31:29	***Reserved***	RsvdP	No	000b

Register 15-22. 98h Link Status and Control 2

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Link Control 2				
3:0	**Target Link Speed** 0001b = 2.5 GT/s Link speed supported 0010b = 5.0 GT/s Link speed supported All other encodings are ***reserved***.	RWS	Yes	0010b
4	**Enter Compliance**	RWS	Yes	0
5	**Hardware Autonomous Speed Disable** ***Reserved*** Initial transition to the highest supported common Link speed is not blocked by this bit.	RsvdP	No	0
6	**Selectable De-Emphasis** ***Reserved***	RsvdP	Yes	0
9:7	**Transmit Margin** Intended for debug and compliance testing only.	RWS	Yes	000b
10	**Enter Modified Compliance** Intended for debug and compliance testing only.	RWS	Yes	0
11	**Compliance SOS** 1 = Link Training and Status State Machine (LTSSM) must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern	RWS	Yes	0
12	**Compliance De-Emphasis** Sets the de-emphasis level in the *Polling.Compliance* state, if the entry occurred due to bit 4 (*Enter Compliance*) being Set.	RWS	Yes	0
15:13	***Reserved***	RsvdP	No	000b
Link Status 2				
16	**Current De-Emphasis Level** Reflects the de-emphasis level. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB (Link is operating at 2.5 GT/s)	RO	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
31:17	***Reserved***	RsvdP	No	0-0h

15.9 NT Port Virtual Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)

The registers detailed in Section 13.10, "Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)," are also applicable to the NT Port, except as defined in Table 15-6 (register map) and Register 15-23.

Table 15-6. NT Port Virtual Interface Subsystem ID and Subsystem Vendor ID Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	Next Capability Pointer (C8h) / SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID	Subsystem Vendor ID	A8h
Reserved	ACh –	C4h

Register 15-23. A4h Subsystem Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**SSID/SSVID Capability ID** Detects the SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the *PCI-to-PCI Bridge r1.2*.	RO	Yes	0Dh
15:8	**Next Capability Pointer** Program to C8h, to point to the **Vendor-Specific Capability 3** structure.	RO	Yes	C8h
31:16	***Reserved***	RsvdP	No	0000h

15.10 NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)

This section details the NT Port Virtual Interface Vendor-Specific Capability 3 registers, which include the **Memory BAR*x* Setup** registers and **Configuration Address** and **Data Window** registers. Table 15-7 defines the register map used by the NT Port.

The **NT Port Virtual Interface BAR*x* Setup** (offsets D0h through E0h) register values are shadowed in the corresponding **NT Port Virtual Interface BAR*x* Setup Shadow** registers (offsets D80h through D90h, respectively). When software writes to an **NT Port Virtual Interface BAR*x* Setup** register, the value is automatically copied to the corresponding **NT Port Virtual Interface BAR*x* Setup** (**Shadow Copy)** register. If the **NT Port Virtual Interface BAR*x* Setup** registers are programmed by serial EEPROM, the **NT Port Virtual Interface BAR*x* Setup** (**Shadow Copy)** registers must also be programmed by serial EEPROM, to the same respective register values.

The Cursor Mechanism registers at offsets F8h and FCh provide a means for accessing PCI Express Extended Configuration Space registers (offsets 100h through FFFh) within the NT Port Virtual and Link Interfaces, when only standard PCI Configuration transactions (that do not support the *Extended Register Number* field within the Completion Request Header) are available. The Cursor Mechanism can generally access only those registers that are defined by the *PCI Express Base r2.0*, and not the Device-Specific registers. However, if Port 0 is a Legacy NT Port, the Cursor Mechanism in the NT Port Virtual Interface registers can also access the Device-Specific registers.

Table 15-7. NT Port Virtual Interface Vendor-Specific Capability 3 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Vendor-Specific Capability 3	Next Capability Pointer 3 (00h)	Capability ID 3 (09h)	C8h
Vendor-Specific Header 3 ***(Reserved)***			CCh
NT Port Virtual Interface BAR0/1 Setup			D0h
NT Port Virtual Interface Memory BAR2 Setup			D4h
NT Port Virtual Interface Memory BAR2/3 Setup			D8h
NT Port Virtual Interface Memory BAR4 Setup			DCh
NT Port Virtual Interface Memory BAR4/5 Setup			E0h
Reserved			E4h – F4h
Configuration Address Window	***Reserved***		F8h
Configuration Data Window			FCh

Register 15-24. C8h Vendor-Specific Capability 3

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
7:0	**Capability ID 3**	RO	Yes	09h
15:8	**Next Capability Pointer 3** 00h = This capability is the last capability in the Linked List	RO	Yes	00h
31:16	**Length** Quantity of bytes in this Capability structure.	RO	Yes	0038h

Register 15-25. CCh Vendor-Specific Header 3

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	***Reserved***	RO	Yes	0380_0002h

Register 15-26. D0h NT Port Virtual Interface BAR0/1 Setup

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The NT Port Virtual Interface **BAR0/1 Setup (Shadow Copy)** register (offset D80h) must be programmed with the same value as this register.*				
1:0	**BAR0/1 Enable** 00b = Disables Virtual Interface **BAR0** and **BAR1** 01b = ***Reserved*** 10b = Enables Virtual Interface **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) 11b = Enables Virtual Interface **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR)	RW	Yes	10b
2	**BAR0 Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
31:3	***Reserved***	RsvdP	No	0-0h

Register 15-27. D4h NT Port Virtual Interface Memory BAR2 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *The NT Port Virtual Interface **Memory BAR2 Setup (Shadow Copy)** register (offset D84h) must be programmed with the same value as this register. This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR2 Type** 00b = **BAR2** is implemented as a 32-bit Memory BAR 10b = **BAR2/3** is implemented as a 64-bit Memory BAR No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR2 Size** Specifies the Address Range size requested by **BAR2**. 0 = Corresponding **BAR2** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR2** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR2 Enable** 0 = **BAR2** is disabled, all **BAR2** bits read 0 1 = **BAR2** is enabled	Field [2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	BAR2 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 15-28. D8h NT Port Virtual Interface Memory BAR2/3 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *The NT Port Virtual Interface* ***Memory BAR2/3 Setup (Shadow Copy)*** *register (offset D88h) must be programmed with the same value as this register. This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR3 Type** 00b = Selects 32-bit Memory BAR (**BAR3**) No other encodings are allowed.		RO	No	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***	Offset D4h[2:1] (*BAR2 Type*) = 00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset D4h[2:1] (*BAR2 Type*) = 10b	RWS	Yes	0_000h
30:20	**BAR3 Size** Specifies the Address Range size requested by **BAR3**. 0 = Corresponding **BAR3** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR3** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR3 Enable** **32-Bit BAR** 0 = **BAR3** is disabled 1 = **BAR3** is enabled as a 32-bit BAR	Offset D4h[2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	64-Bit BAR 0 = **BAR2/3** is disabled, all **BAR2/3** bits read 0 1 = **BAR2/3** is enabled as a 64-bit BAR	Offset D4h[2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 15-29. DCh NT Port Virtual Interface Memory BAR4 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *The NT Port Virtual Interface* ***Memory BAR4 Setup (Shadow Copy)*** *register (offset D8Ch) must be programmed with the same value as this register. This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR4 Type** 00b = **BAR4** is implemented as a 32-bit Memory BAR (**BAR4**) 10b = **BAR4/5** is implemented as a 64-bit Memory BAR (**BAR4/5**) No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding **BAR4** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR4** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR4 Enable** 0 = **BAR4** is disabled, all **BAR4** bits read 0 1 = **BAR4** is enabled	Field [2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	BAR4 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 15-30. E0h NT Port Virtual Interface Memory BAR4/5 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *The NT Port Virtual Interface* ***Memory BAR4/5 Setup (Shadow Copy)*** *register (offset D90h) must be programmed with the same value as this register. This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR5 Type** 00b = Selects 32-bit Memory BAR (**BAR5**) No other encodings are allowed.		RO	No	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***	Offset DCh[2:1] (*BAR4 Type*) = 00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset DCh[2:1] (*BAR4 Type*) = 10b	RWS	Yes	0_000h
30:20	**BAR5 Size** Specifies the Address Range size requested by **BAR5**. 0 = Corresponding **BAR5** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR5** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR5 Enable** **32-Bit BAR** 0 = **BAR5** is disabled 1 = **BAR5** is enabled as a 32-bit BAR	Offset DCh[2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	64-Bit BAR 0 = **BAR4/5** is disabled, all **BAR4/5** bits read 0 1 = **BAR4/5** is enabled as a 64-bit BAR	Offset DCh[2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 15-31. F8h Configuration Address Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	***Reserved***	RsvdP	No	0000h
25:16	**Register Offset**	RW	Yes	0-0h
30:26	***Reserved***	RsvdP	No	0-0h
31	**Interface Select** 0 = Access is to the NT Port Link Interface Type 0 Configuration Space register 1 = Access is to the NT Port Virtual Interface Type 0 Configuration Space register	RW	Yes	0

Register 15-32. FCh Configuration Data Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Register Data** Software selects a register by writing into the NT Port Virtual Interface Configuration Address window, then reads from or writes to that register using this register.	RW	Yes	0000_0000h

15.11 NT Port Virtual Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)

The registers detailed in Section 13.11, "Device Serial Number Extended Capability Registers (Offsets 100h – 134h)," are also applicable to the NT Port. Table 15-8 defines the register map used by all Ports.

Table 15-8. NT Port Virtual Interface Device Serial Number Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h)	Capability Version (1h) / PCI Express Extended Capability ID (0003h)	100h
Serial Number (Lower DW)		104h
Serial Number (Upper DW)		108h
Reserved	10Ch –	134h

15.12 NT Port Virtual Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)

The registers detailed in Section 13.13, "Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)," are also applicable to the NT Port Virtual Interface, except for the Next Capability Offset value, as defined in Table 15-9 (register map), and Register 15-33 through Register 15-35.

Table 15-9. NT Port Virtual Interface Virtual Channel Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (448h or 950h) / Capability Version (1h)	PCI Express Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2		150h
Port VC Status ***(Reserved)***	Port VC Control	154h
VC0 Resource Capability		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
VC1 Resource Capability		164h
VC1 Resource Control		168h
VC1 Resource Status	***Reserved***	16Ch
Reserved		170h – 1A4h
NT Port Virtual Interface WRR Port Arbitration Table Registers (Offsets 1A8h – 1BCh) (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)		1A8h … 1BCh

Register 15-33. 148h Virtual Channel Extended Capability Header

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID** Program to 0002h, as required by the *PCI Express Base r2.0*.		RO	No	0002h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.		RO	No	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability** structure, offset 448h.	NT Port is Port 0	RO	No	448h
	Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset 950h.	Otherwise	RO	No	950h

Register 15-34. 160h VC0 Resource Status

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	***Reserved***	RsvdP	No	0000h
16	**Port Arbitration Table Status** 0 = Hardware has finished loading values stored in the Port Arbitration Table, after software Sets the **VC0 Resource Control** register *Load Port Arbitration Table* bit (offset 15Ch[16]) 1 = Port Arbitration Table entry was written to by software	RO	No	0
17	**VC0 Negotiation Pending** 0 = VC0 negotiation is complete 1 = VC0 initialization is not complete for the NT Port Virtual Interface	RO	Yes	0
31:18	***Reserved***	RsvdP	No	0-0h

Register 15-35. 16Ch VC1 Resource Status

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	***Reserved***	RsvdP	No	0000h
16	**Port Arbitration Table Status** ***Not supported***	RO	No	0
17	**VC1 Negotiation Pending** 0 = VC1 negotiation is complete 1 = VC1 initialization or disabling is pending for the NT Port Virtual Interface	RO	Yes	0
31:18	***Reserved***	RsvdP	No	0-0h

15.12.1 NT Port Virtual Interface WRR Port Arbitration Table Registers (Offsets 1A8h – 1BCh)

The registers detailed in Section 13.13.1, "WRR Port Arbitration Table Registers (Offsets 1A8h – 1BCh)," are also applicable to the NT Port Virtual Interface if the NT Port is the upstream Port (refer to the Note). Port Arbitration Table phases are used to determine Port weighting during "Weighted Round-Robin with 32 Phases" Port arbitration.

Table 15-10 defines the register map used by the NT Port Virtual Interface. The numbers along the top of the table indicate the 4-bit fields of each 32-bit register. There are 32 phases, and any active Port Number can go into each Port *x* Phase *x* box.

Notes: ***The Port Arbitration Table is used only when Weighted Round-Robin (WRR) with 32-phase Port Arbitration is selected.*** *The Arbiter is parked on the upstream Port, if the upstream Port is Port 0 through Port 3. Moreover, the fields within this register are valid only on the upstream Port.If the upstream Port is on a higher-numbered Port, the Arbiter is parked on Port 0. Furthermore, the fields within this register are valid only on Port 0 and* ***reserved*** *on all other Ports.*

This register structure is reserved in NT PCI-to-PCI Bridge mode.

Table 15-10. NT Port Virtual Interface WRR Port Arbitration Table Register Map (When WRR is enabled)

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	
Port *x* Phase 7	Port *x* Phase 6	Port *x* Phase 5	Port *x* Phase 4	Port *x* Phase 3	Port *x* Phase 2	Port *x* Phase 1	Port *x* Phase 0	1A8h
Port *x* Phase 15	Port *x* Phase 14	Port *x* Phase 13	Port *x* Phase 12	Port *x* Phase 11	Port *x* Phase 10	Port *x* Phase 9	Port *x* Phase 8	1ACh
Port *x* Phase 23	Port *x* Phase 22	Port *x* Phase 21	Port *x* Phase 20	Port *x* Phase 19	Port *x* Phase 18	Port *x* Phase 17	Port *x* Phase 16	1B0h
Port *x* Phase 31	Port *x* Phase 30	Port *x* Phase 29	Port *x* Phase 28	Port *x* Phase 27	Port *x* Phase 26	Port *x* Phase 25	Port *x* Phase 24	1B4h
Reserved								1B8h – 1BCh

15.13 NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)

The registers detailed in Section 13.14, "Device-Specific Registers (Offsets 1C0h – 51Ch)," and Section 13.16, "Device-Specific Registers (Offsets 530h – F8Ch)" (for offsets 558h through C88h), are unique to the PEX 8604 and not referenced in the *PCI Express Base r2.0*. These registers are also applicable to the NT Port Virtual Interface, except as defined in Table 15-11 (register map) through Table 15-15, and Register 15-36 through Register 15-65.

Other NT Port Virtual Interface Device-Specific registers are detailed in:

- Section 15.15, "NT Port Virtual Interface Device-Specific Registers (Offsets E40h – F8Ch)"
- Section 15.17, "NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)"

Note: It is recommended that these registers not be changed from their default values.

Table 15-11. NT Port Virtual Interface Device-Specific Register Map (Offsets 1C0h – C88h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Virtual Interface Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)		1C0h … 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)		200h … 25Ch
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch) (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)		260h … 26Ch
Factory Test Only/Reserved		270h – 288h
Device-Specific Registers – Miscellaneous Control (Offset 28Ch)		28Ch
Device-Specific Registers – I^2C Slave Interface (Offsets 290h – 2C4h)		290h … 2C4h
Device-Specific Registers – Bus Number CAM (Offsets 2C8h – 304h)		2C8h … 304h
Device-Specific Registers – I/O CAM (Offsets 308h – 340h)		308h … 340h
Device-Specific Registers – SMBus Slave Interface (Offset 344h)		344h
Device-Specific Registers – Address-Mapping CAM (Offsets 348h – 444h)		348h … 444h

Table 15-11. NT Port Virtual Interface Device-Specific Register Map (Offsets 1C0h – C88h) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (950h)	1h / PCI Express Extended Capability ID (000Bh)	448h
Device-Specific Registers – Vendor-Specific Dual Cast Extended Capability (Offsets 448h – 51Ch)		… 51Ch
Reserved		520h – 540h
Device-Specific Registers – Read Pacing (Offsets 544h – 554h) (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)		544h … 554h
Factory Test Only		558h – 570h
Device-Specific Registers – Port Configuration (Offsets 574h – 628h)		574h … 628h
Device-Specific Registers – General-Purpose Input/Output (Offsets 62Ch – 65Ch) (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)		62Ch … 65Ch
NT Port Virtual Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)		660h … 67Ch
Device-Specific Registers – IOCAM Base and Limit Upper 16 Bits (Offsets 680h – 6BCh)		680h … 6BCh
Device-Specific Registers – Base Address Shadow (Offsets 6C0h – 73Ch)		6C0h … 73Ch
Device-Specific Registers – Virtual Channel Resource Control Shadow (Offsets 740h – 83Ch)		740h … 83Ch
Reserved		840h – 93Ch
Device-Specific Registers – Ingress Credit Handler Port Pool (Offsets 940h – 94Ch)		940h … 94Ch
Next Capability Offset 2 (C34h)	1h / PCI Express Extended Capability ID 2 (000Bh)	950h
NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)		… 95Ch
Factory Test Only		960h – 974h
Reserved		978h – 9FCh

Table 15-11. NT Port Virtual Interface Device-Specific Register Map (Offsets 1C0h – C88h) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch)		A00h … B7Ch
Device-Specific Registers – Physical Layer (Offsets B80h – C30h)		B80h … C30h
Next Capability Offset 4 (000h)	1h PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)		… C88h

15.13.1 NT Port Virtual Interface Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)

The registers detailed in Section 13.14.1, "Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-12 (register map; offset 1E4h is ***reserved***), and Register 15-36 through Register 15-40.

Table 15-12. NT Port Virtual Interface Device-Specific Error Checking and Debug Register Map (Ports[a])

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device-Specific Error Status for Egress ECC Error				1C0h
Device-Specific Error Mask for Egress ECC Error				1C4h
ECC Error Check Disable				1C8h
Error Handler 32-Bit Error Status ***(Factory Test Only)***				1CCh
Error Handler 32-Bit Error Mask ***(Factory Test Only)***				1D0h
Factory Test Only				1D4h
Reserved		Clock Enable		1D8h
Debug Control				1DCh
Power Management Hot Plug User Configuration (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)				1E0h
Reserved				1E4h
Bad TLP Counter				1E8h
Bad DLLP Counter				1ECh
Reserved				1F0h
Reserved		Software Lane Status		1F4h
ACK Transmission Latency Limit (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)				1F8h
Factory Test Only				1FCh

a. Certain registers are Port-specific, others are Chip-specific; all are Device-specific.

Register 15-36. 1DCh Debug Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Notes: *The first Configuration register programmed by the serial EEPROM* ***must*** *be the* ***Debug Control*** *register (Port 0, offset 1DCh), serial EEPROM locations 4h through 9h, as listed in Table 6-1.* *If Port 0 is a Legacy NT Port, this register is loaded from the NT Port Virtual Interface register offset 1DCh location in the serial EEPROM.* *In NT mode, all registers that are programmed by serial EEPROM for the Port that is the designated NT Port, must be programmed into the NT Port Virtual Interface (rather than the numbered Port).* *The NT Port Virtual Interface register offset 1DCh default value is loaded into both Port 0 and the NT Port Virtual Interface; if any other Port is the NT Port, the Port 0 default value is loaded into Port 0, and the NT Port Virtual Interface value is loaded into the NT Port.*				
3:0	***Factory Test Only***	RO	No	Fh
4	**UPCFG Timer Enable** Reflects the STRAP_UPCFG_TIMER_EN# input state. 0 = Upconfigure Timer is disabled 1 = Upconfigure Timer is enabled	RWS	Yes	0 (STRAP_UPCFG_TIMER_EN#=H) 1 (STRAP_UPCFG_TIMER_EN#=L)
5	**SMBus Enable** Reflects the STRAP_SMBUS_EN# input state. 0 = SMBus Slave interface is disabled for device configuration (I^2C mode is enabled) 1 = SMBus Slave interface is enabled for device configuration (SMBus mode is enabled)	RWS	Yes	0 (STRAP_SMBUS_EN#=H) 1 (STRAP_SMBUS_EN#=L)
6	**NT P2P Enable** Reflects the STRAP_NT_P2P_EN# input state. This bit and its corresponding input must ***not*** be toggled at runtime. 0 = NT PCI-to-PCI bridge mode is disabled (STRAP_NT_P2P_EN#=H) (Legacy NT mode is enabled) 1 = NT PCI-to-PCI bridge mode is enabled (STRAP_NT_P2P_EN#=L)	RWS	Yes	0 (STRAP_NT_P2P_EN#=H) 1 (STRAP_NT_P2P_EN#=L)
7	***Factory Test Only***	RWS	Yes	0

Register 15-36. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
11:8	**Upstream Port ID** Upstream Port Number – Reads the external Strap value on the STRAP_UPSTRM_PORTSEL[3:0] inputs, at Reset de-assertion. When bit 15 (*Hardware/Software Configuration Mode Control*) is Cleared, software is not allowed to change this value.	RO	Yes	Set by STRAP_UPSTRM_PORTSEL[3:0] input levels or by serial EEPROM, or by I^2C followed by a Soft Reset
	When bit 15 (*Hardware/Software Configuration Mode Control*) is Set, Upstream Port Number can be Set by software, using the values defined below. All other encodings are ***reserved***. ***Note:*** *Port 0 is recommended for the upstream Port designation.* 0h = Port 0 1h = Port 1 4h = Port 4 5h = Port 5	RW[a]	Yes	

Register 15-36. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
13:12	**Interrupt Fencing Mode Select** ***Note:*** *A Fundamental Reset is needed to recover from Fencing errors.* **Mode 1 (Default)** **1.** When the PEX 8604 receives a packet with a Fatal error (Malformed, DLL Protocol error) from an external device, or the device detects a Credit Overflow, Receiver Overflow, or Surprise Link Down, the switch logs the Header on the NT Port Virtual Interface, sends a Fatal Error Message to the Host, then asserts FATAL_ERR#. **2.** When the PEX 8604 detects an internal Fatal error (ECC failure), the switch sends a Fatal Interrupt Message to the Host and asserts FATAL_ERR#. In certain situations, delivery of the interrupt is not guaranteed; however, the signal is always asserted upon a Fatal event. **Mode 2 (Generate Internal Reset)** Upon Fatal error (internal or external) detection, an internal Chip Level reset is asserted (equivalent to an In-Band Reset from the upstream Port). No error Messages are generated, and no attempt is made to block packets in transit. **Mode 3 (Block All Packet Transmission)** Upon Fatal error (internal or external) detection, the NT Port Virtual Interface logs the error in the NT Port Virtual Interface Error Status register, then asserts FATAL_ERR#. This Fatal error detection blocks all Ports from sending out TLPs. No error Messages are generated. If a packet is already in transmission, an EDB is inserted to cancel the packet. **Mode 4 (Block All Packet Transmission and Create Surprise Down)** In addition to all the Mode 3 actions, the PEX 8604 forces the upstream Link to go down, thus causing a Surprise Down event on the Link, so that the Host is notified. 00b = Mode 1 (default) 01b = Mode 2 – Generate Internal Reset 10b = Mode 3 – Block All Packet Transmission 11b = Mode 4 – Block All Packet Transmission and Create Surprise Down	RWS	Yes	00b

Register 15-36. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
14	***Factory Test Only***	RWS	Yes	0
15	**Hardware/Software Configuration Mode Control** Allows software to configure which Port is the upstream Port, as well as which Port is a Legacy NT Port. 0 = Upstream Port and NT Port selection by the STRAP_UPSTRM_PORTSEL[3:0] and STRAP_NT_UPSTRM_PORTSEL[3:0] inputs, respectively, which can be overridden by the serial EEPROM and/or I^2C configuration mechanism. Cannot be changed by in-band software during runtime. 1 = In-band software can change which Port is configured to be the upstream Port and NT Port, by writing new values to fields [11:8 and 27:24] (*Upstream Port ID* and *NT Port Number*, respectively), followed by issuance of a Hot Reset to the upstream Port. Bit 20 (*Upstream Port and NT-Link Port DL_Down Reset Propagation Disable*) must be Cleared.	RWS	Yes	0

Register 15-36. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**Upstream Hot Reset Control** 0 = Reset all logic, except Sticky bits and Device-Specific registers 1 = Reset only the Configuration Space registers of all Ports defined by the *PCI Express Base r2.0* ***Note:*** *Only a Fundamental Reset serial EEPROM load affects this bit.*	RWS	Yes	1
17	**Disable Serial EEPROM Load on Hot Reset** 0 = Enables serial EEPROM load upon upstream Port or NT Port Link Interface Hot Reset or *DL_Down* state 1 = Disables serial EEPROM load upon upstream Port or NT Port Link Interface Hot Reset or *DL_Down* state	RWS	Yes	0
18	**NT Mode Enable** NT mode (Intelligent Adapter) is enabled by the STRAP_NT_ENABLE# input, which is overridden by the value of this bit if this register is programmed by the serial EEPROM upon Fundamental Reset. Software, serial EEPROM load upon upstream Port or NT Port Link Interface Hot Reset or *DL_Down* state, and/or I^2C are not allowed to change this value. 0 = NT mode is disabled (STRAP_NT_ENABLE#=H) 1 = NT mode is enabled (STRAP_NT_ENABLE#=L)	HwInit	Yes (Serial EEPROM only)	Set by STRAP_NT_ENABLE# input level or by serial EEPROM
19	**NT Port DL_Down Reset Propagation Disable** Setting this bit: • Enables the upstream Port to ignore a Hot Reset training sequence, • Blocks the PEX 8604 from manifesting an internal reset due to a DL_Down event, and • Prevents the downstream Ports from issuing a Hot Reset to downstream devices when a Hot Reset or DL_Down event occurs on the upstream Link.	RWS	Yes	0

Register 15-36. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20	**Upstream Port and NT-Link Port DL_Down Reset Propagation Disable** Setting this bit: • Enables the upstream Port and NT-Link Port to ignore a Hot Reset training sequence, • Blocks the PEX 8604 from manifesting an internal reset due to a DL_Down event, and • Blocks the PEX 8604 NT Port Link Interface from manifesting an internal reset due to a DL_Down event on the NT Port Link, and • Prevents the downstream Ports from issuing a Hot Reset to downstream devices when a Hot Reset or DL_Down event occurs on the upstream Link **This bit typically should be Set for NT mode.**	RWS	Yes	0
21	**Cut-Thru Enable** 0 = Disables Cut-Thru support 1 = Enables Cut-Thru support	RWS	Yes	1
22	***Reserved***	RsvdP	No	0
23	***Factory Test Only***	RWS	Yes	0

Register 15-36. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
27:24	**NT Port Number** When bit 18 (*NT Mode Enable*) is Set, and bit 15 (*Hardware/Software Configuration Mode Control*) is Cleared, the NT Port Number is Set by the STRAP_NT_UPSTRM_PORTSEL[3:0] inputs. This field is "Don't Care" for Transparent mode. Software is not allowed to change this value.	HwInit	Yes	Set by STRAP_NT_UPSTRM_PORTSEL[3:0] input levels or by serial EEPROM, or by I^2C followed by a Soft Reset
	When bits 18 (*NT Mode Enable*) and 15 (*Hardware/Software Configuration Mode Control*) are both Set, the NT Port Number selected by this field is Set by software, using the values defined below. All other encodings are ***reserved***. 0h = Port 0 1h = Port 1 4h = Port 4 5h = Port 5	R/W[a]	Yes	
28	**Virtual Interface Access Enable** When the serial EEPROM is not present, the default value is 1; otherwise, the default value is 0. 0 = Retries Type 0 Configuration TLP received on the NT Port Virtual Interface 1 = Accepts Type 0 Configuration TLP on the NT Port Virtual Interface ***Notes:*** *This bit does not affect the PEX 8604 in Transparent mode, nor does it affect other transaction types.* *Set this bit to enable Configuration access to the NT Port Virtual Interface.*	RW	Yes	1
29	**Link Interface Access Enable** 0 = Retries Type 0 Configuration Request received on the NT Port Link Interface 1 = Accepts Type 0 Configuration Request received on the NT Port Link Interface ***Notes:*** *This bit does not affect the PEX 8604 in Transparent mode.* *Set this bit to enable Configuration access to the NT Port Link Interface.*	RW	Yes	0

Register 15-36. 1DCh Debug Control
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
30	**Inhibit EEPROM NT-Link Load on Hot Reset** Inhibits serial EEPROM load of NT Port Link Interface registers when any one of the following conditions exist: • **Upstream Port Hot Reset** – Bits [17:16] (*Disable Serial EEPROM Load on Hot Reset* and *Upstream Hot Reset Control*, respectively) are Cleared • **Upstream Port *DL_Down* state** – Bits [20, 17:16] (*Upstream Port and NT-Link Port DL_Down Reset Propagation Disable*, *Disable Serial EEPROM Load on Hot Reset*, and *Upstream Hot Reset Control*, respectively) are Cleared • **NT Port Link Interface Hot Reset or *DL_Down* state** – Bit 17 (*Disable Serial EEPROM Load on Hot Reset*) is Cleared	RW	Yes	1
31	**Load Only EEPROM NT-Link on Hot Reset** Load only serial EEPROM NT Port Link Interface register entries when any one of the following conditions exist: • **Upstream Port Hot Reset** – Bits [17:16] (*Disable Serial EEPROM Load on Hot Reset* and *Upstream Hot Reset Control*, respectively) are Cleared • **Upstream Port *DL_Down* state** – Bits [20, 17:16] (*Upstream Port and NT-Link Port DL_Down Reset Propagation Disable*, *Disable Serial EEPROM Load on Hot Reset*, and *Upstream Hot Reset Control*, respectively) are Cleared • **NT Port Link Interface Hot Reset or *DL_Down* state** – Bit 17 (*Disable Serial EEPROM Load on Hot Reset*) is Cleared	RW	Yes	1

a. Although these bits are RW, do not change by software.

Register 15-37. 1E0h Power Management Hot Plug User Configuration

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *This register is* ***reserved*** *in NT PCI-to-PCI Bridge mode.*				
11:0	***Reserved***	RsvdP	No	0-0h
12	**NT Hot Plug Enable** Can be programmed only by serial EEPROM and/or I²C.	RO	Yes	0
16:13	***Reserved***	RsvdP	No	0-0h
17	**40-Pin I/O Expander Enable** 0 = Enables 16-pin I/O Expanders for all downstream Ports that implement Serial Hot Plug 1 = Enables 40-pin I/O Expanders for all downstream Ports that implement Serial Hot Plug ***Note:*** *Value of 1 can be enabled only by serial EEPROM (that is, neither software nor I²C can be used to enable the 40-Pin I/O Expander).*	RW	Yes (See Note)	0
31:18	***Reserved***	RsvdP	No	0-0h

Register 15-38. 1E8h Bad TLP Counter

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Bad TLP Counter** Value reflects errors detected on the NT Port Link Interface. Counts the quantity of TLPs received with bad Link Cyclic Redundancy Check (LCRC), or quantity of TLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 15-39. 1ECh Bad DLLP Counter

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Bad DLLP Counter** Value reflects errors detected on the NT Port Link Interface. Counts the quantity of DLLPs received with bad LCRC, or quantity of DLLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 15-40. 1F8h ACK Transmission Latency Limit

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The value of this register should be valid after Link negotiation. ***Note:*** *This register is* ***reserved*** *in NT PCI-to-PCI Bridge mode.*				
11:0	**ACK Transmission Latency Limit** Acknowledge Control Packet (ACK) Transmission Latency Limit. The value of this field changes, based upon Negotiated Link Width (offset 78h[25:20]) encoding after the Link is up. x1 Link width = 255d x2 Link width = 217d	RWS	Yes	0EDh
15:12	***Reserved***	RsvdP	No	0h
23:16	**Upper 8 Bits of the Replay Timer Limit** The value in this register is a multiplier of the default internal timer values that are compliant to the *PCI Express Base r2.0*. These bits should normally remain the default value, 00h.	RWS	Yes	00h
30:24	***Reserved***	RsvdP	No	00h
31	**ACK Transmission Latency Timer Status** Indicates the written status of field [11:0] (*ACK Transmission Latency Limit*). After the register is written, either by software and/or serial EEPROM, this bit is Set, and Cleared only by a Fundamental Reset.	RO	No	0

15.13.2 NT Port Virtual Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)

The registers detailed in Section 13.16.5, "Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-13 (register map), and Register 15-41 and Register 15-42.

Table 15-13. NT Port Virtual Interface Device-Specific Ingress Control and Port Enable Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Ingress Control				660h
Ingress Control Shadow				664h
Reserved		Port Enable Status		668h
Factory Test Only	Negotiated Link Width for Ports 0, 4, 5			66Ch
Reserved				670h
Reserved		Port Cut-Thru Enable Status		674h
Ingress PLL RAM ECC 1-Bit Counter				678h
Factory Test Only				67Ch

Register 15-41. 660h Ingress Control (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
25:0	***Factory Test Only***	RWS	Yes	0-0h
26	**Disable Upstream Port BAR0 and BAR1** 0 = Enables the upstream Port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively) 1 = Disables the upstream Port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively)	RWS	Yes	0
27	***Not used***	RWS	Yes	0
28	**Disable VGA BIOS Memory Access Decoding** 0 = Enables the **Bridge Control** register *VGA 16-Bit Decode Enable*, *VGA Enable*, and *ISA Enable* bits (offset 3Ch[20:18], respectively), and enables decoding of the PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are blocked) 1 = Disables the **Bridge Control** register *VGA 16-Bit Decode Enable*, *VGA Enable*, and *ISA Enable* bits (offset 3Ch[20:18], respectively), and disables decoding of the PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are ***not*** blocked)	RWS	Yes	0
30:29	***Factory Test Only***	RWS	Yes	00b
31	***Not used***	RWS	Yes	0

Register 15-42. 664h Ingress Control Shadow (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	***Factory Test Only***	RWS	Yes	0
1	**Use Serial EEPROM Values for Ingress Credit Initialization** Allow Configuration with a Device Number that is not 0, that is accessing downstream devices, to be forwarded. When the Device Number is 0, the Configuration terminates in a UR. 0 = Use default values for ingress credit initialization 1 = Use serial EEPROM values for ingress credit initialization	RWS	Yes	0
3:2	***Factory Test Only***	RWS	Yes	00b
4	**Drop EP TLPs** Drop Endpoint TLPs. 1 = Endpoint TLP was dropped	RWS	Yes	0
5	**No Special Treatment for Relaxed Ordering Traffic** The PEX 8604 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, then that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled by Setting this bit. 1 = Device-Specific Relaxed Ordering Completion will not be flagged to egress block	RWS	Yes	0
7:6	***Factory Test Only***	RWS	Yes	00b
8	**Drop ECRC TLPs** Drop End-to-end Cyclic Redundancy Check (ECRC) TLPs. 1 = ECRC TLP was dropped	RWS	Yes	0
10:9	**ACK TLP Counter Timeout** Sets the quantity of ingress TLP Acknowledgements (ACKs) pending, which causes a high-priority ACK to be sent. 00b = 16 TLPs 01b = 8 TLPs 10b = 4 TLPs 11b = Feature is disabled	RWS	Yes	00b
31:11	***Factory Test Only***	RWS	Yes	0-0h

15.13.3 NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)

The registers detailed in Section 13.16.10, "Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)," are also applicable to the NT Port, except for the Next Capability Offset value, as defined in Table 15-14 (register map) and Register 15-43.

Table 15-14. NT Port Virtual Interface Device-Specific, Vendor-Specific Extended Capability 2 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 2 (C34h) / Capability Version 2 (1h)	PCI Express Extended Capability ID 2 (000Bh)	950h
Vendor-Specific Header 2		954h
Hardwired Device ID	Hardwired Vendor ID	958h
Reserved	PLX Hardwired Revision ID	95Ch

Register 15-43. 950h Vendor-Specific Extended Capability 2

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID 2** Program to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 2**	RO	Yes	1h
31:20	**Next Capability Offset 2** Program to C34h, which addresses the **Vendor-Specific Extended Capability 4** structure.	RO	Yes	C34h

15.13.4 NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)

This section details the NT Port Virtual Interface Device-Specific, Vendor-Specific Extended Capability 4 registers, which include the **Memory BAR*x* Address Translation**, **Doorbell**, and **Scratchpad** registers. Table 15-15 defines the register map used by the NT Port Virtual Interface.

Table 15-15. NT Port Virtual Interface Device-Specific, Vendor-Specific Extended Capability 4 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 4 (000h)	Capability Version 4 (1h) / PCI Express Extended Capability ID 4 (000Bh)	C34h
Vendor-Specific Header 4		C38h
Memory BAR2 Address Translation Lower		C3Ch
Memory BAR3 Address Translation Upper		C40h
Memory BAR4 Address Translation Lower		C44h
Memory BAR5 Address Translation Upper		C48h
Reserved	Virtual Interface IRQ Set	C4Ch
Reserved	Virtual Interface IRQ Clear	C50h
Reserved	Virtual Interface IRQ Mask Set	C54h
Reserved	Virtual Interface IRQ Mask Clear	C58h
Reserved	Link Interface IRQ Set	C5Ch
Reserved	Link Interface IRQ Clear	C60h
Reserved	Link Interface IRQ Mask Set	C64h
Reserved	Link Interface IRQ Mask Clear	C68h
NT Port SCRATCH0		C6Ch
NT Port SCRATCH1		C70h
NT Port SCRATCH2		C74h
NT Port SCRATCH3		C78h
NT Port SCRATCH4		C7Ch
NT Port SCRATCH5		C80h
NT Port SCRATCH6		C84h
NT Port SCRATCH7		C88h

Register 15-44. C34h Vendor-Specific Extended Capability 4

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID 4** Program to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 4**	RO	Yes	1h
31:20	**Next Capability Offset 4** 000h = This extended capability is the last capability in the PEX 8604 Extended Capabilities list	RO	Yes	000h

Register 15-45. C38h Vendor-Specific Header 4

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**Vendor-Specific ID 4** ID Number of this Extended Capability structure.	RO	Yes	0003h
19:16	**Vendor-Specific Rev 4** Version Number of this structure.	RO	Yes	0h
31:20	**Vendor-Specific Length 4** Quantity of bytes in the entire structure.	RO	Yes	078h

Register 15-46. C3Ch Memory BAR2 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR2 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR2** is enabled (**NT Port Virtual Interface Memory BAR2 Setup** register *BAR2 Enable* bit, offset D4h[31], is Set).	RW	Yes	000h

Register 15-47. C40h Memory BAR3 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	Offset D8h[31]=0	RsvdZ	No	0_0000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset D8h[31]=1	RW	Yes	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR3 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR3** is enabled (**NT Port Virtual Interface Memory BAR2/3 Setup** register *BAR3 Enable* bit, offset D8h[31], is Set).		RW	Yes	000h

Register 15-48. C44h Memory BAR4 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR4 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR4** is enabled (**NT Port Virtual Interface Memory BAR4 Setup** register *BAR4 Enable* bit, offset DCh[31], is Set).	RW	Yes	000h

Register 15-49. C48h Memory BAR5 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	Offset E0h[31]=0	RsvdZ	No	0_0000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset E0h[31]=1	RW	Yes	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR5 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR5** is enabled (**NT Port Virtual Interface Memory BAR4/5 Setup** register *BAR5 Enable* bit, offset E0h[31], is Set).		RW	Yes	000h

Register 15-50. C4Ch Virtual Interface IRQ Set

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note:	*The bits in this register can be masked by their respective **Virtual Interface IRQ Mask Set** register bits (offset C54h).*			
15:0	**SET_IRQ** Set Virtual IRQ. Controls the state of the Virtual Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Sets the corresponding Interrupt Request. The Virtual Interface interrupt is asserted if the following conditions exist: • This register (offset C4Ch or C50h) value is non-zero, and, • Corresponding **Virtual Interface IRQ Mask Set** or **Virtual Interface IRQ Mask Clear** register (offset C54h or C58h, respectively) *Interrupt Mask* bit is not Set, and, • Interrupts (either INT*x* or MSIs) are enabled	RW1S	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 15-51. C50h Virtual Interface IRQ Clear

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note:	*The bits in this register can be masked by their respective **Virtual Interface IRQ Mask Clear** register bits (offset C58h).*			
15:0	**CLR_IRQ** Clear Virtual IRQ. Controls the state of the Virtual Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding Interrupt Request. The Virtual Interface interrupt is de-asserted if the following conditions exist: • This register (offset C50h or C4Ch) value is zero (0), –or– • **Virtual Interface IRQ Mask Set** or **Virtual Interface IRQ Mask Clear** register (offset C54h or C58h, respectively) masks all its **Set** or **Clear** register (offset C50h or C4Ch) *Set* bits, and • INT*x* interrupts are enabled	RW1C	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 15-52. C54h Virtual Interface IRQ Mask Set

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Virtual Interface IRQ Set*** *register bits (offset C4Ch).*				
15:0	**SET_IRQM** Virtual Interface interrupt IRQ Mask Set. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding *Interrupt Mask* bit. 0 = Corresponding **Virtual Interface IRQ Set** register (offset C4Ch) *Interrupt Request* bit is not masked 1 = Corresponding **Virtual Interface IRQ Set** register (offset C4Ch) *Interrupt Request* bit is masked/disabled	RW1S	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 15-53. C58h Virtual Interface IRQ Mask Clear

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Virtual Interface IRQ Clear*** *register bits (offset C50h).*				
15:0	**CLR_IRQM** Clear Virtual IRQ Mask. Controls the state of the Virtual Interface *Interrupt Request* bits. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding *Interrupt Mask* bit. 0 = Corresponding **Virtual Interface IRQ Clear** register (offset C50h) *Interrupt Request* bit is not masked 1 = Corresponding **Virtual Interface IRQ Clear** register (offset C50h) *Interrupt Request* bit is masked/disabled	RW1C	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 15-54. C5Ch Link Interface IRQ Set

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be masked by their respective* ***Link Interface IRQ Mask Set*** *register bits (offset C64h).*				
15:0	**SET_IRQ** Set Link IRQ. Controls the state of the Link Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Sets the corresponding Interrupt Request. The Link Interface interrupt is asserted if the following conditions exist: • This register (offset C5Ch or C60h) value is non-zero, and, • Corresponding **Link Interface IRQ Mask Set** or **Link Interface IRQ Mask Clear** register (offset C64h or C68h, respectively) *Interrupt Mask* bit is not Set, and, • Interrupts (either INT*x* or MSIs) are enabled	RW1S	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 15-55. C60h Link Interface IRQ Clear

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be masked by their respective* ***Link Interface IRQ Mask Clear*** *register bits (offset C68h).*				
15:0	**CLR_IRQ** Clear Virtual IRQ. Controls the state of the Virtual Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding Interrupt Request. The Virtual Interface interrupt is de-asserted if the following conditions exist: • This register (offset C60h or C5Ch) value is zero (0), –or– • **Link Interface IRQ Mask Set** or **Link Interface IRQ Mask Clear** register (offset C64h or C68h, respectively) masks all its **Set** or **Clear** register (offset C60h or C5Ch) *Set* bits, and • INT*x* interrupts are enabled	RW1C	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 15-56. C64h Link Interface IRQ Mask Set

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Link Interface IRQ Set*** *register bits (offset C5Ch).*				
15:0	**SET_IRQM** Link Interface Interrupt IRQ Mask Set. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Sets the corresponding *Interrupt Mask* bit. 0 = Corresponding **Link Interface IRQ Set** register (offset C5Ch) *Interrupt Request* bit is not masked 1 = Corresponding **Link Interface IRQ Set** register (offset C5Ch) *Interrupt Request* bit is masked/disabled	RW1S	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 15-57. C68h Link Interface IRQ Mask Clear

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Link Interface IRQ Clear*** *register bits (offset C60h).*				
15:0	**CLR_IRQM** Link Interface Interrupt IRQ Mask Clear. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding *Interrupt Mask* bit. 0 = Corresponding **Link Interface IRQ Clear** register (offset C60h) *Interrupt Request* bit is not masked 1 = Corresponding **Link Interface IRQ Clear** register (offset C60h) *Interrupt Request* bit is masked/disabled	RW1C	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 15-58. C6Ch NT Port SCRATCH0

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**Scratchpad 0** 32-bit Scratchpad 0 register.	RW	Yes	0000_0000h

Register 15-59. C70h NT Port SCRATCH1

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**Scratchpad 1** 32-bit Scratchpad 1 register.	RW	Yes	0000_0000h

Register 15-60. C74h NT Port SCRATCH2

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**Scratchpad 2** 32-bit Scratchpad 2 register.	RW	Yes	0000_0000h

Register 15-61. C78h NT Port SCRATCH3

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**Scratchpad 3** 32-bit Scratchpad 3 register.	RW	Yes	0000_0000h

Register 15-62. C7Ch NT Port SCRATCH4

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
31:0	**Scratchpad 4** 32-bit Scratchpad 4 register.	RW	Yes	0000_0000h

Register 15-63. C80h NT Port SCRATCH5

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 5** 32-bit Scratchpad 5 register.	RW	Yes	0000_0000h

Register 15-64. C84h NT Port SCRATCH6

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 6** 32-bit Scratchpad 6 register.	RW	Yes	0000_0000h

Register 15-65. C88h NT Port SCRATCH7

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 7** 32-bit Scratchpad 7 register.	RW	Yes	0000_0000h

15.14 NT Port Virtual Interface NT Bridging-Specific Registers (Offsets C8Ch – EECh)

Table 15-16 defines the register map of the NT Port Virtual Interface NT Bridging-Specific registers.

Table 15-16. NT Port Virtual Interface NT Bridging-Specific Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Reserved	C8Ch –	D64h
NT Port Virtual Interface NT Bridging-Specific Registers – Base Address and Base Address Setup (Offsets D68h – D90h) (Shadow Copy) (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)		D68h … D90h
NT Port Virtual Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses D94h – DB0h)		D94h … DB0h
Reserved	DB4h –	EECh

15.14.1 NT Port Virtual Interface NT Bridging-Specific Registers – Base Address and Base Address Setup (Offsets D68h – D90h)

The registers in this section are shadow copies of the NT Port Virtual Interface Base Address register (BAR) and BAR Configuration registers, and valid only for Port 0. If Port 0 is the NT Port, the registers are in Virtual Interface Configuration Space. Table 15-17 defines the register map.

Notes: ***This register structure is reserved in NT PCI-to-PCI Bridge mode.***

It is recommended that these registers not be changed from their default values.

Table 15-17. NT Port Virtual Interface NT Bridging-Specific Base Address Register (BAR) and BAR*x* Setup Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
BAR0 (Shadow Copy)	D68h
BAR1 (Shadow Copy)	D6Ch
BAR2 (Shadow Copy)	D70h
BAR3 (Shadow Copy)	D74h
BAR4 (Shadow Copy)	D78h
BAR5 (Shadow Copy)	D7Ch
BAR0/1 Setup (Shadow Copy)	D80h
Memory BAR2 Setup (Shadow Copy)	D84h
Memory BAR2/3 Setup (Shadow Copy)	D88h
Memory BAR4 Setup (Shadow Copy)	D8Ch
Memory BAR4/5 Setup (Shadow Copy)	D90h

Register 15-66. D68h BAR0 (Shadow Copy)
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note:	*This register is a shadow copy of the NT Port Virtual Interface **Base Address 0** (**BAR0**) register (offset 10h).*			
0	**Memory Space Indicator** Virtual Side **BAR0** is configured by serial EEPROM and the Local Host. By default, Configuration **BAR0/1 Setup** register selects 32-bit Memory **BAR0**. 0 = Memory space only supported	RsvdP	No	0
2:1	**Memory Map Type** Reflection of the BAR configuration, as specified in the **BAR0/1 Setup (Shadow Copy)** register (offset D80h). 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
16:4	***Reserved***	RsvdP	No	0-0h
31:17	**Base Address 0** 128-KB Base address in which to map the PEX 8604 Configuration Space registers into Memory space.	RW	Yes	0-0h

Register 15-67. D6Ch BAR1 (Shadow Copy)
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note:	*This register is a shadow copy of the NT Port Virtual Interface **Base Address 1** (**BAR1**) register (offset 14h).*			
31:0	**Upper 32-Bit BAR0 of Virtual NT Port** **BAR1** is the upper 32 bits of 64-bit **BAR0/1**, Base Address 1 extends Base Address 0 to provide the upper 32 Address bits when the **BAR0 (Shadow Copy)** register *Memory Map Type* field (offset D68h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **BAR0 (Shadow Copy)** register is not enabled as a 64-bit BAR (*Memory Map Type* field (offset D68h[2:1]) is not programmed to 10b).	RsvdP	Yes	0000_0000h

Register 15-68. D70h BAR2 (Shadow Copy)
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *This register is a shadow copy of the NT Port Virtual Interface* ***Base Address 2*** *(**BAR2**) register (offset 18h).*				
0	**Memory Space Indicator** 0 = Memory space only supported	RO	No	0
2:1	**Memory Map Type** Reflection of the BAR configuration, as specified in the **Memory BAR2 Setup (Shadow Copy)** register (offset D84h). 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 2**	RW	Yes	000h

Register 15-69. D74h BAR3 (Shadow Copy)
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Notes: *This register is a shadow copy of the NT Port Virtual Interface* ***Base Address 3*** *(**BAR3**) register (offset 1Ch).* *This register has RW privilege if **BAR2/3** is configured as a 64-bit BAR (**BAR2 (Shadow Copy)** register Memory Map Type field, offset D70h[2:1], is programmed to 10b).*					
0	**Memory Space Indicator** 0 = Memory space only supported	Offset D70h[2:1]=00b	RsvdP	No	0
		Offset D70h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** Reflection of the BAR configuration, as specified in the **Memory BAR2/3 Setup (Shadow Copy)** register (offset D88h). 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset D70h[2:1]=00b	RsvdP	No	00b
		Offset D70h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset D70h[2:1]=00b	RsvdP	No	0
		Offset D70h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset D70h[2:1]=00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset D70h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 3**		RW	Yes	000h

Register 15-70. D78h BAR4 (Shadow Copy)
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *This register is a shadow copy of the NT Port Virtual Interface* ***Base Address 4*** *(**BAR4**) register (offset 20h).*				
0	**Memory Space Indicator** 0 = Memory space only supported	RO	No	0
2:1	**Memory Map Type** Reflection of the BAR configuration, as specified in the **Memory BAR4 Setup (Shadow Copy)** register (offset D8Ch). 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 4**	RW	Yes	000h

Register 15-71. D7Ch BAR5 (Shadow Copy)
(Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Notes: *This register is a shadow copy of the NT Port Virtual Interface* ***Base Address 5*** *(**BAR5**) register (offset 24h).* *This register has RW privilege if **BAR4/5** is configured as a 64-bit BAR (**BAR4 (Shadow Copy)** register Memory Map Type field, offset D78h[2:1], is programmed to 10b).*					
0	**Memory Space Indicator** 0 = Memory space only supported	Offset D78h[2:1]=00b	RsvdP	No	0
		Offset D78h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** Reflection of the BAR configuration, as specified in the **Memory BAR4/5 Setup (Shadow Copy)** register (offset D90h). 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset D78h[2:1]=00b	RsvdP	No	00b
		Offset D78h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset D78h[2:1]=00b	RsvdP	No	0
		Offset D78h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset D78h[2:1]=00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset D78h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 5**		RW	Yes	000h

Register 15-72. D80h BAR0/1 Setup (Shadow Copy) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *This register must be programmed with the same value as the* ***NT Port Virtual Interface BAR0/1 Setup*** *register (offset D0h).*				
1:0	**Type Selector** 00b = Disables Virtual Interface **BAR0** and **BAR1** 01b = ***Reserved*** 10b = Enables Virtual Interface **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) 11b = Enables Virtual Interface **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR)	RW	Yes	10b
2	**BAR0 Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
31:3	***Reserved***	RsvdP	No	0-0h

Register 15-73. D84h Memory BAR2 Setup (Shadow Copy) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *This register must be programmed with the same value as the* ***NT Port Virtual Interface Memory BAR2 Setup*** *register (offset D4h). This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR2 Type** 00b = **BAR2** is implemented as a 32-bit Memory BAR 10b = **BAR2/3** is implemented as a 64-bit Memory BAR No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR2 Size** Specifies the Address Range size requested by **BAR2**. 0 = Corresponding **BAR2** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR2** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR2 Enable** 0 = **BAR2** is disabled, all **BAR2** bits read 0 1 = **BAR2** is enabled	Field [2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	BAR2 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 15-74. D88h Memory BAR2/3 Setup (Shadow Copy) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note: *This register must be programmed with the same value as the* ***NT Port Virtual Interface Memory BAR2/3 Setup*** *register (offset D8h). This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR3 Type** 00b = Selects 32-bit Memory BAR (**BAR3**) No other encodings are allowed.		RO	No	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR3 Size** Specifies the Address Range size requested by **BAR3**. 0 = Corresponding **BAR3** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR3** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR3 Enable** **32-Bit BAR** 0 = **BAR3** is disabled 1 = **BAR3** is enabled as a 32-bit BAR	Offset D84h[2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	64-Bit BAR 0 = **BAR2/3** is disabled, all **BAR2/3** bits read 0 1 = **BAR2/3** is enabled as a 64-bit BAR	Offset D84h[2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 15-75. D8Ch Memory BAR4 Setup (Shadow Copy) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note: *This register must be programmed with the same value as the* ***NT Port Virtual Interface Memory BAR4 Setup*** *register (offset DCh). This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR4 Type** 00b = **BAR4** is implemented as a 32-bit Memory BAR 10b = **BAR4/5** is implemented as a 64-bit Memory BAR		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding **BAR4** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR4** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR4 Enable** 0 = **BAR4** is disabled, all **BAR4** bits read 0 1 = **BAR4** is enabled	Field [2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	BAR4 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 15-76. D90h Memory BAR4/5 Setup (Shadow Copy) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *This register must be programmed with the same value as the* ***NT Port Virtual Interface Memory BAR4/5 Setup*** *register (offset E0h). This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR5 Type** 00b = Selects 32-bit Memory BAR (**BAR5**) No other encodings are allowed.		RO	No	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR5 Size** Specifies the Address Range size requested by **BAR5**. 0 = Corresponding **BAR5** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR5** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR5 Enable** **32-Bit BAR** 0 = **BAR5** is disabled 1 = **BAR5** is enabled as a 32-bit BAR	Offset D8Ch[2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	64-Bit BAR 0 = **BAR4/5** is disabled, all **BAR4/5** bits read 0 1 = **BAR4/5** is enabled as a 64-bit BAR	Offset D8Ch[2:1] (*BAR4 Type*) = 10b	RW	Yes	0

15.14.2 NT Port Virtual Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses D94h – DB0h)

This section describes the NT Port Virtual Interface NT Bridging-Specific Requester ID Translation Lookup Table (LUT) Entry registers. The NT Port uses these registers for Requester ID translation when it forwards:

- Memory Requests from the NT Port Virtual Interface to the NT Port Link Interface, –or–
- Completion TLPs from the NT Port Link Interface to the NT Port Virtual Interface

If the application needs to send traffic through the NT Port Virtual Interface, program the registers listed in this group with the corresponding Requester's Requester ID, then Set the *LUT Entry_n Enable* bit (bit 31) of each register accordingly.

Table 15-18 defines the register and address locations, as they relate to Register 15-77.

Table 15-18. NT Port Virtual Interface NT Bridging-Specific Requester ID Translation Lookup Table Entry_*n* Register Locations

ADDR Location	Lookup Table Entry_*n*	ADDR Location	Lookup Table Entry_*n*
D94h	0	DA4h	4
D98h	1	DA8h	5
D9Ch	2	DACh	6
DA0h	3	DB0h	7

Register 15-77. D94h – DB0h NT Port Virtual Interface Requester ID Translation LUT Entry_*n* (where *n* = 0 through 7)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
2:0	**Requester ID on Virtual Side**	**Function Number** LUT Entry_*n* Requester Function Number.	RW	Yes	000b
7:3		**Device Number** LUT Entry_*n* Requester Device Number.	RW	Yes	0000_0b
15:8		**Bus Number** LUT Entry_*n* Requester Bus Number.	RW	Yes	00h
29:16	***Reserved***		RsvdP	No	0-0h
30	**LUT Entry_*n* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Virtual Interface to the NT Port Link Interface, and re-calculates the ECRC. If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Link Interface to the NT Port Virtual Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
31	**LUT Entry_*n* Enable** 0 = Disables 1 = Enables		RW	Yes	0

15.15 NT Port Virtual Interface Device-Specific Registers (Offsets E40h – F8Ch)

The registers detailed in Section 13.16, "Device-Specific Registers (Offsets 530h – F8Ch)" (for offsets E40h through F8Ch), are unique to the PEX 8604 and not referenced in the *PCI Express Base r2.0*. These registers are also applicable to the NT Port Virtual Interface, except as defined in Table 15-19 (register map) and Table 15-22, and Register 15-78 through Register 15-81.

Other NT Port Virtual Interface Device-Specific registers are detailed in:

- Section 15.13, "NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)"
- Section 15.17, "NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)"

Note: It is recommended that these registers not be changed from their default values.

Table 15-19. NT Port Virtual Interface Device-Specific Register Map (Offsets E40h – F8Ch)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Virtual Interface Device-Specific Registers – Physical Layer (Offsets E40h – EFCh)	E40h … EFCh
NT Port Virtual Interface Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F3Ch)	F00h … F3Ch
Device-Specific Registers – Error Reporting (Offsets F40h – F4Ch)	F40h … F4Ch
NT Port Virtual Interface Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)	F50h … F8Ch

15.15.1 NT Port Virtual Interface Device-Specific Registers – Physical Layer (Offsets E40h – EFCh)

A Physical Layer (PHY) register detailed in Section 13.16.15, "Device-Specific Registers – Physical Layer (Offsets E40h – EFCh)," is also applicable to the NT Port Virtual Interface, except as defined in Table 15-20 (register map; offsets E40h through E48h are ***reserved***).

Table 15-20. NT Port Virtual Interface Device-Specific PHY Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				E40h – EECh
Physical Layer Control				EF0h
Reserved				EF4h – EFCh

15.15.2 NT Port Virtual Interface Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F3Ch)

Device-Specific registers detailed in Section 13.16.16, "Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F3Ch)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-21 (register map; offsets F10h, F18h, and F24h through F30h are ***reserved***).

Table 15-21. NT Port Virtual Interface Source Queue Weight and Soft Error Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Factory Test Only		ECRC Check Enable for Ports 0, 1		F00h
Factory Test Only		ECRC Check Enable for Ports 4, 5		F04h
Factory Test Only				F08h
Reserved				F0Ch – F3Ch

15.15.3 NT Port Virtual Interface Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)

The Alternative Routing-ID Interpretation (ARI) Capability registers detailed in Section 13.16.18, "Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-22 (register map), and Register 15-78 through Register 15-81.

Table 15-22. NT Port Virtual Interface Device-Specific ARI Capability Register Map (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device Control 2 for Port 0	Device Capability 2 for Port 0	F50h
Device Control 2 for Port 1	Device Capability 2 for Port 1	F54h
Factory Test Only		F58h – F5Ch
Device Control 2 for Port 4	Device Capability 2 for Port 4	F60h
Device Control 2 for Port 5	Device Capability 2 for Port 5	F64h
Factory Test Only/Reserved		F68h – F8Ch

Register 15-78. F50h Device Capability and Control 2 for Port 0 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 0					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 0					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 15-79. F54h Device Capability and Control 2 for Port 1 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 1					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 1					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 15-80. F60h Device Capability and Control 2 for Port 4 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 4					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 4					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 15-81. F64h Device Capability and Control 2 for Port 5 (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 5					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 5					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

15.16 NT Port Virtual Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

The registers detailed in Section 13.17, "Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)," are also applicable to the NT Port Virtual Interface, except for the Next Capability Offset value, as defined in Table 15-23 (register map), Register 15-82, and the exceptions indicated in the note.

Notes: *Data Link Protocol and Surprise Down PCI Express errors are not valid for the NT Port Virtual nor Link Interfaces, and therefore do not affect register offsets FB8h, FBCh, and FC0h in NT mode.*

Receiver, Bad TLP, Bad DLLP, Replay Number Rollover, and Replay Timer Timeout PCI Express errors are not valid for the NT Port Virtual nor Link Interfaces, and therefore do not affect register offsets FC4h and FC8h in NT mode.

Table 15-23. NT Port Virtual Interface Advanced Error Reporting Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (148h)	Capability Version (1h) / PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status		FB8h
Uncorrectable Error Mask		FBCh
Uncorrectable Error Severity		FC0h
Correctable Error Status		FC4h
Correctable Error Mask		FC8h
Advanced Error Capabilities and Control		FCCh
Header Log 0		FD0h
Header Log 1		FD4h
Header Log 2		FD8h
Header Log 3		FDCh

Register 15-82. FB4h Advanced Error Reporting Extended Capability Header

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID**	RO	Yes	0001h
19:16	**Capability Version**	RO	Yes	1h
31:20	**Next Capability Offset** Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	RO	Yes	148h

15.17 NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)

This section details the NT Port Virtual Interface Device-Specific Link Error registers, located at offsets FE0h through FFCh. These Device-Specific registers are unique to the NT Port Virtual Interface, and not referenced in the *PCI Express Base r2.0*. Table 15-24 defines the register map used by the NT Port Virtual Interface.

Other NT Port Virtual Interface Device-Specific registers are detailed in:

- Section 15.13, "NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)"
- Section 15.15, "NT Port Virtual Interface Device-Specific Registers (Offsets E40h – F8Ch)"

Note: It is recommended that these registers not be changed from their default values.

Table 15-24. NT Port Virtual Interface Device-Specific Register Map – Link Error (Offsets FE0h – FFCh) (Port 0, when Port 0 is the NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Link Error Status Virtual		FE0h
Link Error Mask Virtual		FE4h
Reserved		FE8h – FFCh

Register 15-83. FE0h Link Error Status Virtual (Port 0, when Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be masked by their respective* ***Link Error Mask Virtual*** *register bits (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h).*				
0	**Link Side Correctable Error Status** 1 = NT Port Link Interface detected a Correctable TLP error, and signaled the interrupt to the Local Host	RW1CS	Yes	0
1	**Link Side Uncorrectable Error Status** 1 = NT Port Link Interface detected an Uncorrectable TLP error, and signaled the interrupt to the Local Host	RW1CS	Yes	0
2	**Link Side DL Active Change Status** 1 = NT Port Link Interface *DL_Active* state change occurred upon detection of an NT Port Link Interface *DL_Down* state rise edge and fall edge	RW1CS	Yes	0
3	**Link Side Uncorrectable Error Message Drop Status** 1 = NT Port Link Interface received an Uncorrectable Error Message, and signaled the interrupt to the Local Host	RW1CS	Yes	0
31:4	***Reserved***	RsvdP	No	0000_000h

Register 15-84. FE4h Link Error Mask Virtual (Port 0, when Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Link Error Status Virtual*** *register bits (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h).*				
0	**Link Side Correctable Error Mask** 0 = No effect on reporting activity 1 = *Link Side Correctable Error Status* bit is masked/disabled	RWS	Yes	1
1	**Link Side Uncorrectable Error Mask** 0 = No effect on reporting activity 1 = *Link Side Uncorrectable Error Status* bit is masked/disabled	RWS	Yes	1
2	**Link Side DL Active Change Mask** 0 = No effect on reporting activity 1 = *Link Side DL Active Change Status* bit is masked/disabled	RWS	Yes	1
3	**Link Side Uncorrectable Error Message Drop Mask** 0 = No effect on reporting activity 1 = *Link Side Uncorrectable Error Message Drop Status* bit is masked/disabled	RWS	Yes	1
31:4	***Reserved***	RsvdP	No	0000_000h

Chapter 16 NT Port Link Interface Registers – NT Mode Only

16.1 Introduction

Note: *Check the latest design guides, application notes and errata list for Non-Transparent (NT) usage.*

The NT Port includes two sets of Configuration, Capability, Control, and Status registers, to support the Link and Virtual Interfaces. This chapter defines the NT Port Link Interface registers. Other registers are defined in:

- Chapter 13, "Transparent Port Registers"
- Chapter 15, "NT Port Virtual Interface Registers – NT Mode Only"

Note: *For Chip-specific registers (those that exist only in Port 0), if Port 0 is a Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.*

All PEX 8604 registers can be accessed by Configuration or Memory Requests.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI Express Base r2.0*

16.2 NT Port Link Interface Type 0 Register Map

Table 16-1 defines the NT Port Link Interface Type 0 register mapping.

Table 16-1. NT Port Link Interface Type 0 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
NT Port Link Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)		Capability Pointer (40h)	00h … 34h … 3Ch
	Next Capability Pointer (48h)	Capability ID (01h)	40h
NT Port Link Interface PCI Power Management Capability Registers (Offsets 40h – 44h)			44h
	Next Capability Pointer (68h)	Capability ID (05h)	48h
NT Port Link Interface MSI Capability Registers (Offsets 48h – 64h)			… 64h
	Next Capability Pointer (A4h)	Capability ID (10h)	68h
NT Port Link Interface PCI Express Capability Registers (Offsets 68h – A0h)			… A0h
	Next Capability Pointer (C8h)	SSID/SSVID Capability ID (0Dh)	A4h
NT Port Link Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)			… C4h
	Next Capability Pointer 3 (00h)	PCI Express Capability ID 3 (09h)	C8h
NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)			… FCh
Next Capability Offset (FB4h)	1h	PCI Express Extended Capability ID (0003h)	100h
NT Port Link Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)			… 134h
Next Capability Offset (148h)	1h	PCI Express Extended Capability ID (0004h)	138h
NT Port Link Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)			… 144h
Next Capability Offset (950h)	1h	PCI Express Extended Capability ID (0002h)	148h
NT Port Link Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)			… 1BCh

Table 16-1. NT Port Link Interface Type 0 Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)		1C0h …
Next Capability Offset 2 (C34h)	1h PCI Express Extended Capability ID 2 (000Bh)	950h
NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)		…
Next Capability Offset 4 (000h)	1h PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)		… C88h
NT Port Link Interface NT Bridging-Specific Registers (Offsets C8Ch – EFCh)		C8Ch … EFCh
NT Port Link Interface Device-Specific Registers – Source Queue Weight (Offsets F00h – F3Ch)		F00h … F3Ch
Reserved		F40h – FB0h
Next Capability Offset (138h)	1h PCI Express Extended Capability ID (0001h)	FB4h
NT Port Link Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)		… FDCh
Reserved		FE0h – FFCh

16.3 Register Access

The PEX 8604 NT Port Link Interface implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) comprise the PCI-compatible Configuration Space, and the upper 960 Dwords (offsets 100h through FFFh) comprise the PCI Express Extended Configuration Space. The PEX 8604 supports three mechanisms for accessing the NT Port Link Interface registers:

- PCI Express Base r2.0 Configuration Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

16.3.1 *PCI Express Base r2.0* Configuration Mechanism

The *PCI Express Base r2.0* mechanism is divided into two mechanisms:

- **PCI r3.0-Compatible Configuration Mechanism** – Provides Conventional PCI access to the first 256 bytes (the bytes at offsets 00h through FFh) of the NT Port Link Interface Configuration Register space
- **PCI Express Enhanced Configuration Access Mechanism** – Provides access to the entire 4-KB Configuration Space

Both are described in the sections that follow.

The PEX 8604 decodes Type 0 Configuration transactions received on its NT Port Link Interface. The PEX 8604 reads from or writes to the NT Port Link Interface register, as specified in the original Type 0 Configuration access.

16.3.1.1 *PCI r3.0*-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration Space consists of the first 256 bytes of the NT Port Link Interface Configuration Space. (Refer to Figure 16-1.) The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PEX 8604 NT Port Link Interface's first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration Space.

This mechanism uses the same Request format as the PCI Express Enhanced Configuration Access Mechanism. For PCI-compatible Configuration Requests, the *Extended Register Address* field must be all zeros (0).

Because the mechanism is limited to the first 256 bytes of the NT Port Link Interface Configuration Register space, one of the following must be used to access beyond Byte FFh:

- PCI Express Enhanced Configuration Access Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

16.3.1.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism uses a flat, Root Complex Memory-Mapped Address space to access the device Configuration registers. In this case, the Memory address determines the Configuration register accessed, and Memory data returns the addressed register contents. The Root Complex converts the Memory transaction into a Configuration transaction before transmitting this access to the downstream devices.

This mechanism is used to access the NT Port Link Interface Type 0 registers:

- NT Port Link Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)
- NT Port Link Interface PCI Power Management Capability Registers (Offsets 40h – 44h)
- NT Port Link Interface MSI Capability Registers (Offsets 48h – 64h)
- NT Port Link Interface PCI Express Capability Registers (Offsets 68h – A0h)
- NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)
- NT Port Link Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)
- NT Port Link Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)
- NT Port Link Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)
- NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)
- NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)
- NT Port Link Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

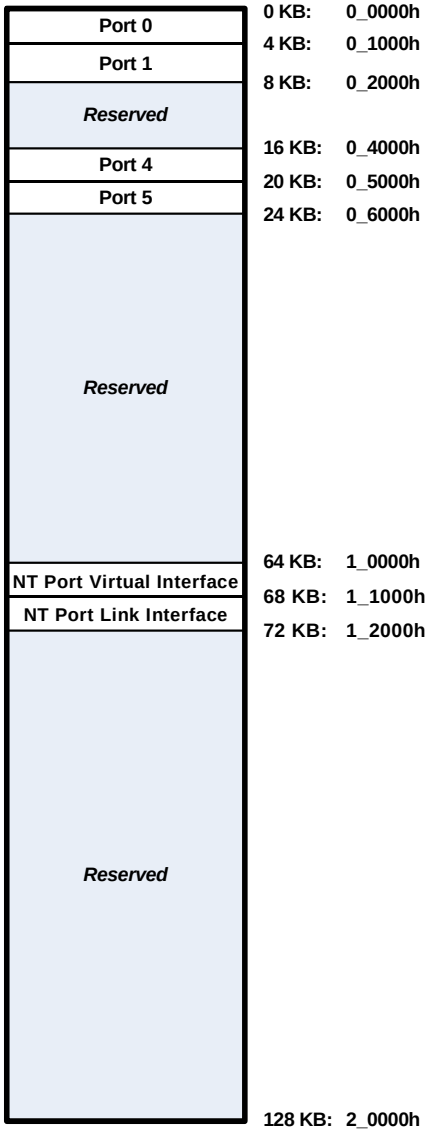
16.3.2 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the registers for all Ports within a single 128-KB Memory map, as illustrated in Figure 16-1. This Memory map is identical for Upstream Port **BAR0/1**, NT Port Virtual Interface **BAR0/1**, and NT Port Link Interface **BAR0/1**. The registers of each Port are located within a 4-KB range.

When the NT Port is enabled at Fundamental Reset, the NT Port Virtual and Link Interface registers use the *PCI r3.0* Type 0 Configuration Space Header. In NT PCI-to-PCI Bridge mode (STRAP_NT_P2P_EN#=L), the NT PCI-to-PCI bridge (between the NT Port Virtual Interface and internal virtual PCI Bus) registers use the *PCI r3.0* Type 1 Configuration Space Header, and are mapped to the 4-KB Address space of the Port Number that is assigned as the NT Port (indicated in the **Debug Control** register *NT Port Number* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1DCh[27:24])).

To use this mechanism, use the PCI r3.0-Compatible Configuration Mechanism to program the PEX 8604 upstream Port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively). After the PEX 8604 NT Port Link Interface Memory-Mapped register Base address is Set, the PEX 8604 Configuration Space registers are accessed, using Memory Reads and Writes to the 4-KB range, starting at offset 64 KB (1_0000h, Virtual Interface) and offset 68 KB (1_1000h, Link Interface).

Figure 16-1. NT Mode Configuration Register Mapping to Memory-Mapped BAR



16.3.3 Device-Specific Cursor Mechanism

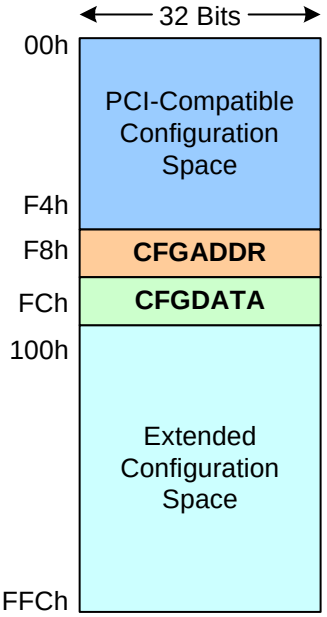
The Device-Specific Cursor mechanism is provided for use in development systems that can only generate *PCI r3.0* Configuration cycles (*that is*, the system cannot use either the Device-Specific Memory-Mapped Configuration Mechanism, nor generate Extended Configuration Requests to access the Extended Configuration Space).

In Figure 16-2, the software uses the **Configuration Address Window** (CFGADDR) register (offset F8h) to select the NT Port Link or Virtual Interface Configuration Space registers, including the PCI Express Extended Configuration Space registers (offsets 100h through FFFh).

Software uses the **Configuration Data Window** (CFGDATA) register (offset FCh) to write to or read from the selected Configuration Space registers.

Refer to Section 16.10, "NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)," for the register descriptions.

Figure 16-2. Configuration Space View



16.4 Register Descriptions

The remainder of this chapter details the PEX 8604 NT Port Link Interface registers, including:

- Bit/field names
- Description of register functions in the PEX 8604 NT Port Link and Virtual Interfaces
- Type (*such as* RW or HwInit; refer to Table 13-5, "Register Types, Grouped by User Accessibility," for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8604 serial EEPROM and/or I^2C/SMBus Initialization feature
- Default power-on/reset value

16.5 NT Port Link Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the NT Port Link Interface PCI-Compatible Type 0 Configuration Header registers. Table 16-2 defines the register map.

Table 16-2. NT Port Link Interface PCI-Compatible Type 0 Configuration Header Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
PCI Class Code			PCI Revision ID	08h
PCI BIST ***(Not Supported)***	PCI Header Type	Master Latency Timer ***(Not Supported)***	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Base Address 2				18h
Base Address 3				1Ch
Base Address 4				20h
Base Address 5				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capability Pointer (40h)	34h
Reserved				38h
Max_Lat ***(Reserved)***	Min_Gnt ***(Reserved)***	PCI Interrupt Pin	PCI Interrupt Line	3Ch

Register 16-1. 00h PCI Configuration ID

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8604, if not overwritten by serial EEPROM or I^2C.	RO	Yes	8604h

Register 16-2. 04h PCI Command/Status

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	PCI Command			
0	**I/O Access Enable** The NT Port Link Interface ignores the value of this register, because it does ***not support*** I/O resources.	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8604 ignores Memory Space Requests received on the NT Port Link Interface 1 = PEX 8604 accepts Memory Space Requests received on the NT Port Link Interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8604 forwarding of Memory Requests upstream. Does not affect Message forwarding nor Completions. 0 = PEX 8604 handles Memory Requests received on the NT Port Virtual Interface as Unsupported Requests (UR); for Non-Posted Requests, the PEX 8604 returns a Completion with UR Completion status 1 = PEX 8604 forwards Memory Requests from the NT Port Virtual Interface to the Link Interface	RW	Yes	0
3	**Special Cycle Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
4	**Memory Write and Invalidate Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
5	**VGA Palette Snoop** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
6	**Parity Error Response Enable** Controls bit 24 (*Master Data Parity Error Detected*).	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
8	**SERR# Enable** Controls bit 30 (*Signaled System Error*). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the NT Port Link Interface to the Root Complex	RW	Yes	0
9	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
10	**Interrupt Disable** 0 = NT Port Link Interface is enabled to generate INT*x* Interrupt Messages 1 = NT Port Link Interface is prevented from generating INT*x* Interrupt Messages	RW	Yes	0
15:11	***Reserved***	RsvdP	No	0-0h

Register 16-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	PCI Status			
18:16	***Reserved***	RsvdP	No	000b
19	**Interrupt Status** 0 = No INT*x* interrupt is pending 1 = INT*x* interrupt is pending internally to the NT Port Link Interface –or– PEX_INTA# (if enabled) is asserted	RO	No	0
20	**Capability List** Capability function is supported. Set, as required by the *PCI Express Base r2.0*.	RO	Yes	1
21	**66 MHz Capable** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
24	**Master Data Parity Error Detected** If bit 6 (*Parity Error Response Enable*) is Set, the NT Port Link Interface Sets this bit when the NT Port: • Forwards the poisoned Transaction Layer Packet (TLP) Write Request from the NT Port Virtual Interface to the NT Port Link Interface, –or– • Receives a Completion marked as poisoned on the NT Port Link Interface If the *Parity Error Response Enable* bit is Cleared, the PEX 8604 never Sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Always Cleared.	RsvdP	No	00b
27	**Signaled Target Abort** The NT Port Link Interface Sets this bit if either of the following conditions exist: • NT Port Link Interface receives a Completion (from the Local Host) that has a Completion status of Completer Abort (CA), –or– • NT Port Link Interface receives a Memory-Mapped access with a Payload length greater than 1 DWord ***Note:*** *When Set during a forwarded Completion, the* ***Uncorrectable Error Status*** *register Completer Abort Status bit (offset FB8h[15]) is not updated, because the NT Port does not log the corresponding Requests that it forwards.*	RW1C	Yes	0

Register 16-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
28	**Received Target Abort** ***Reserved***	RsvdP	No	0
29	**Received Master Abort** ***Reserved***	RsvdP	No	0
30	**Signaled System Error** If bit 8 (*SERR# Enable*) is Set, the NT Port Link Interface Sets this bit when transmitting an ERR_FATAL or ERR_NONFATAL Message to its upstream device. This error is natively reported by the **Device Status** register *Fatal Error Detected* and *Non-Fatal Error Detected* bits (offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	**Detected Parity Error** This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility. 1 = NT Port Link Interface received a Poisoned TLP, regardless of the bit 6 (*Parity Error Response Enable*) state	RW1C	Yes	0

Register 16-3. 08h PCI Class Code and Revision ID

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Revision ID				
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the Silicon Revision (BAh), the PLX-assigned Revision ID for this version of the PEX 8604. The PEX 8604 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	BAh
PCI Class Code				**068000h**
15:8	**Register-Level Programming Interface** Cleared, as required by the *PCI r3.0* for other bridge devices.	RO	Yes	00h
23:16	**Sub-Class Code** Other bridge devices.	RO	Yes	80h
31:24	**Base Class Code** Bridge devices.	RO	Yes	06h

Register 16-4. 0Ch Miscellaneous Control

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Cache Line Size				
7:0	**Cache Line Size** System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8604 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	**Master Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00h
PCI Header Type				
22:16	**Configuration Layout Type** Type 0 Configuration Header for the NT Port.	RO	Yes	00h
23	**Multi-Function Device** 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	Yes	0
PCI BIST				
31:24	**PCI BIST** ***Not supported*** Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

Register 16-5. 10h Base Address 0 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *By default, NT Port Link Interface* ***BAR0*** *is enabled and* ***BAR1*** *is disabled, to provide a 32-bit* ***BAR0*** *for register access.* ***BAR1*** *can be enabled (by serial EEPROM and/or I²C), to provide a 64-bit* ***BAR0/1****, by programming the* ***NT Port Link Interface BAR0/1 Setup*** *register BAR0/1 Enable field (NT Port Link Interface, offset E4h[1:0]) to 11b (which enables both* ***BAR0*** *and* ***BAR1****).*				
0	**Memory Space Indicator** When enabled, the Base Address register maps PEX 8604 Port Configuration registers into Memory space. ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Base Address register maps the PEX 8604 Port Configuration registers into Non-Prefetchable Memory space	RO	Yes	0
16:4	***Reserved***	RsvdP	No	0-0h
31:17	**Base Address 0** 128-KB-aligned Base address used for Memory-Mapped access to the 128-KB block of all PEX 8604 registers (4 KB, per Port).	RW	Yes	0-0h

Register 16-6. 14h Base Address 1 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Upper 32-Bit Address for Memory-Mapped BAR** For 64-bit addressing (**BAR0/1**), Base Address 1 (**BAR1**) extends Base Address 0 (**BAR0**) to provide the upper 32 Address bits when the **Base Address 0** register *Memory Map Type* field (offset 10h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	RO when the **Base Address 0** register (**BAR0**) is not enabled as a 64-bit BAR (*Memory Map Type* field (offset 10h[2:1]) is not programmed to 10b).	RO	Yes	0000_0000h

Register 16-7. 18h Base Address 2 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 2** Resolution is 1 MB.	RW	Yes	000h

Register 16-8. 1Ch Base Address 3 (NT Port Link Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *This register has RW privilege if* ***BAR2/3*** *is configured as a 64-bit BAR (**Base Address 2** register Memory Map Type field (NT Port Link Interface, offset 18h[2:1]), is programmed to 10b).*					
0	**Memory Space Indicator** **BAR3** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR2/3**. 0 = Implemented as a Memory BAR in 32-Bit mode	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 18h[2:1]=00b	RsvdP	No	00b
		Offset 18h[2:1]=10b	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 18h[2:1]=00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 18h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 3**		RW	Yes	000h

Register 16-9. 20h Base Address 4 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR; otherwise, ***reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 4**	RW	Yes	000h

Register 16-10. 24h Base Address 5 (NT Port Link Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *This register has RW privilege if* ***BAR4/5*** *is configured as a 64-bit BAR (**Base Address 4** register Memory Map Type field (NT Port Link Interface, offset 20h[2:1]), is programmed to 10b).*					
0	**Memory Space Indicator** **BAR5** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR4/5**. 0 = Implemented as a Memory BAR in 32-Bit mode	Offset 20h[2:1]=00b	RsvdP	No	0
		Offset 20h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 20h[2:1]=00b	RsvdP	No	00b
		Offset 20h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 20h[2:1]=00b	RsvdP	No	0
		Offset 20h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 20h[2:1]=00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 20h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 5**		RW	Yes	000h

Register 16-11. 2Ch Subsystem ID and Subsystem Vendor ID

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Subsystem Vendor ID				
15:0	**Subsystem Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM or I²C.	RO	Yes	10B5h
Subsystem ID				
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8604, if not overwritten by serial EEPROM and/or I²C.	RO	Yes	8604h

Register 16-12. 30h Expansion ROM Base Address

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *Expansion ROM can be enabled in either the NT Port Link or Virtual Interface, but not both simultaneously. Expansion ROM is enabled, by default, in the NT Port Link Interface (**Ingress Control** register Expansion ROM Virtual Side bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 660h[23]) is Cleared).*					
0	**Expansion ROM Enable** 0 = NT Port Link Interface Expansion ROM is disabled	NT Port Virtual Interface, offset 30h[0]=1	RsvdP	No	0
	1 = NT Port Link Interface Expansion ROM is enabled, and NT Port Virtual Interface Expansion ROM is disabled	NT Port Virtual Interface, offset 30h[0]=0	RO	Yes	0
		NT Port Virtual Interface, offset 30h[0]=1	RsvdP	No	0
13:1	***Reserved***		RsvdP	No	0-0h
31:14	**Expansion ROM Base Address** If the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 268h[16]) value is 0, the Expansion ROM size is 16 KB (default value is FFFF_C001h). Bit 14 is RW. If the *Expansion ROM Size* bit value is 1, the Expansion ROM size is 32 KB (default value is FFFF_8001h). Bit 14 is RO.	When Bit 0 = 0	RsvdP	No	0-0h
		When Bit 0 = 1	RW	Yes	0-0h

Register 16-13. 34h Capability Pointer

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability Pointer** Default 40h points to the **PCI Power Management Capability** structure.	RO	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 16-14. 3Ch PCI Interrupt

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	PCI Interrupt Line			
7:0	**Interrupt Line Routing Value** Communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture-specific. The value is used by device drivers and operating systems.	RW	Yes	00h
	PCI Interrupt Pin			
15:8	**Interrupt Pin** Identifies the Conventional PCI Interrupt Message(s) the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8604. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
	Min_Gnt			
23:16	**Minimum Grant** ***Reserved*** Does not apply to PCI Express.	RsvdP	No	00h
	Max_Lat			
31:24	**Maximum Latency** ***Reserved*** Does not apply to PCI Express.	RsvdP	No	00h

16.6 NT Port Link Interface PCI Power Management Capability Registers (Offsets 40h – 44h)

This section details the NT Port Link Interface PCI Power Management Capability registers. Table 16-3 defines the register map.

Table 16-3. NT Port Link Interface PCI Power Management Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions ***(Reserved)***	PCI Power Management Status and Control		44h

Register 16-15. 40h PCI Power Management Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Capability ID** Default = 01h – only value allowed.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	RO	Yes	48h
18:16	**Version** Default = 011b – only value allowed.	RO	Yes	011b
19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.	RsvdP	No	0
20	***Reserved***	RsvdP	No	0
21	**Device-Specific Initialization** 0 = Device-Specific Initialization is ***not*** required	RO	Yes	0
24:22	**AUX Current** The PEX 8604 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.	RO	Yes	000b
25	**D1 Support** ***Not supported*** 0 = PEX 8604 does ***not support*** the D1 Device PM state	RsvdP	No	0
26	**D2 Support** ***Not supported*** 0 = PEX 8604 does ***not support*** the D2 Device PM state	RsvdP	No	0
31:27	**PME Support** The default value is applied to bits [31, 30, and 27] only. PME Messages are disabled, by default. ***Note:*** *This field is **reserved** in NT PCI-to-PCI Bridge mode.*	RO	Yes	0000_0b

Register 16-16. 44h PCI Power Management Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Power Management Status and Control				
1:0	**Power State** Used to determine the current Device PM state of the Port, and to Set the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	RO	Yes	1
7:4	***Reserved***	RsvdP	No	0h
8	**PME Enable** Default value of 0 indicates that PME generation is disabled. ***Note:*** *This bit is **reserved** in NT PCI-to-PCI Bridge mode.*	RsvdP	No	0
12:9	**Data Select** Initially writable by serial EEPROM and/or I²C only[a]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I²C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	RO	Yes	0h
14:13	**Data Scale** Writable by serial EEPROM and/or I²C only[a]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h, and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h.	RO	Yes	00b
15	**PME Status** 0 = PME is not being generated by the NT Port ***Note:*** *This bit is **reserved** in NT PCI-to-PCI Bridge mode.*	RsvdP	No	0

Register 16-16. 44h PCI Power Management Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Power Management Control/Status Bridge Extensions				
21:16	***Reserved***	RsvdP	No	0-0h
22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
PCI Power Management Data				
31:24	**Data** Writable by serial EEPROM and/or I^2C only[a]. There are four supported *Data Select* values (0h, 3h, 4h, and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	RO	Yes	00h

*a. With no serial EEPROM nor previous I^2C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

16.7 NT Port Link Interface MSI Capability Registers (Offsets 48h – 64h)

The registers detailed in Section 13.8, "MSI Capability Registers (Offsets 48h – 64h)," are also applicable to the NT Port Link Interface, except as defined in Table 16-4 (register map), and Register 16-17 through Register 16-19.

Table 16-4. NT Port Link Interface MSI Capability Register Map[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
MSI Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address				4Ch
MSI Upper Address				50h
Reserved		MSI Data		54h
MSI Mask				58h
MSI Status				5Ch
Reserved				60h – 64h

*a. Offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*

Register 16-17. 48h MSI Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
MSI Capability Header				
7:0	**Capability ID** Program to 05h, as required by the *PCI r3.0*.	RO	Yes	05h
15:8	**Next Capability Pointer** Program to 68h, to point to the **PCI Express Capability** structure.	RO	Yes	68h
MSI Control				
16	**MSI Enable** 0 = MSIs for the NT Port Link Interface are disabled 1 = MSIs for the NT Port Link Interface are enabled, and INT*x* Interrupt Messages and PEX_INTA# output assertion are disabled	RW	Yes	0
19:17	**Multiple Message Capable** 000b = NT Port Link Interface can request only one Vector 001b through 111b = NT Port Link Interface can request two Vectors	RO	Yes	001b
22:20	**Multiple Message Enable** 000b = NT Port Link Interface is allocated one Vector, by default 001b through 111b = NT Port Link Interface is allocated two Vectors ***Note:*** *This field should not be programmed with a value larger than that of field [19:17] (Multiple Message Capable). If the value of this field is larger than that of field [19:17], the Multiple Message Capable value takes effect.*	RW	Yes	000b
23	**MSI 64-Bit Address Capable** 0 = PEX 8604 is capable of generating MSI 32-bit addresses (**MSI Address** register, offset 4Ch, is the Message address) 1 = PEX 8604 is capable of generating MSI 64-bit addresses (**MSI Address** register, offset 4Ch, is the lower 32 bits of the Message address, and **MSI Upper Address** register, offset 50h, is the upper 32 bits of the Message address)	RO	Yes	1
24	**Per Vector Masking Capable** 0 = PEX 8604 does not have Per Vector Masking capability 1 = PEX 8604 has Per Vector Masking capability	RO	Yes	1
31:25	***Reserved***	RsvdP	No	0-0h

Register 16-18. 58h MSI Mask

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
The interrupt sources in the NT Port Link Interface are grouped into two categories – Device-Specific errors and NT-Link Doorbell-generated interrupts. The quantity of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the quantity of MSI Vectors that can be requested is: • **Two** – Both interrupt categories generate their own MSI Vector • **One** – Both interrupt categories generate the same MSI Vector ***Notes:*** *The offset for this register changes from 58h, to 54h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be used to mask their respective **MSI Status** register bits (offset 5Ch).*					
0	**MSI Mask for Device-Specific Errors** MSI mask for Device-Specific Error interrupts.	Offset 48h[22:20]≥001b	RW	Yes	0
	MSI Mask for Shared Interrupt Sources MSI mask for both interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one Vector.	Offset 48h[22:20]=000b	RsvdP	No	0
1	**MSI Mask for NT-Link Doorbell-Generated Interrupts** Refer to the NT Port registers located at offsets C5Ch through C68h.	Offset 48h[22:20]≥001b	RW	Yes	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0
31:2	***Reserved***		RsvdP	No	0-0h

Register 16-19. 5Ch MSI Status

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
The interrupt sources in the NT Port Link Interface are grouped into two categories – Device-Specific errors and NT-Link Doorbell-generated interrupts. The quantity of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the quantity of MSI Vectors that can be requested is: • **Two** – Both interrupt categories generate their own MSI Vector • **One** – Both interrupt categories generate the same MSI Vector ***Notes:*** *The offset for this register changes from 5Ch, to 58h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be masked by their respective **MSI Mask** register bits (offset 58h).*					
0	**MSI Pending Status for Device-Specific Errors** MSI pending status for Device-Specific Error interrupts.	Offset 48h[22:20]≥001b	RO	Yes	0
	MSI Pending Status for Shared Interrupt Sources MSI pending status for both interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one Vector.	Offset 48h[22:20]=000b	RsvdP	No	0
1	**MSI Pending Status for NT-Link Doorbell-Generated Interrupts** Refer to the NT Port registers located at offsets C5Ch through C68h.	Offset 48h[22:20]≥001b	RO	Yes	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0
31:2	***Reserved***		RsvdP	No	0-0h

16.8 NT Port Link Interface PCI Express Capability Registers (Offsets 68h – A0h)

The registers detailed in Section 13.9, "PCI Express Capability Registers (Offsets 68h – A0h)," are also applicable to the NT Port Link Interface, except as defined in Table 16-5 (register map; offsets 7Ch, 80h, and 90h are ***reserved***), and Register 16-20 through Register 16-25.

Table 16-5. NT Port Link Interface PCI Express Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capability		Next Capability Pointer (A4h)	Capability ID (10h)	68h
Device Capability				6Ch
Device Status		***Not Supported/Reserved***	Device Control	70h
Link Capability				74h
Link Status		***Reserved***	Link Control	78h
Reserved				7Ch – 94h
Link Status 2		Link Control 2		98h
Reserved				9Ch – A0h

Register 16-20. 68h PCI Express Capability List and Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Express Capability List				
7:0	**Capability ID** Program to 10h, by default.	RO	Yes	10h
15:8	**Next Capability Pointer** Program to A4h, to point to the **Subsystem Capability** structure.	RO	Yes	A4h
PCI Express Capability				
19:16	**Capability Version** The PEX 8604 NT Port Link Interface programs this field to 2h, as required by the *PCI Express Base r2.0*.	RO	Yes	2h
23:20	**Device/Port Type** Default = PCI Express Endpoint device.	RO	No	0h
24	**Slot Implemented** ***Not valid for PCI Express Endpoint devices*** ***Note:*** *This bit is also* ***reserved*** *in NT PCI-to-PCI Bridge mode.*	RsvdP	No	0
29:25	**Interrupt Message Number** The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.	RO	Yes	00_000b
31:30	***Reserved***	RsvdP	No	00b

Register 16-21. 6Ch Device Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
2:0	**Maximum Payload Size Supported** Maximum Payload Size Port limitations are as follows: Because there are x1 and x2 Ports in the Port configuration, the Maximum Payload Size for each Port is limited to 512 bytes. 000b = NT Port Link Interface supports a 128-byte maximum payload 001b = NT Port Link Interface supports a 256-byte maximum payload 010b = NT Port Link Interface supports a 512-byte maximum payload No other encodings are supported.	HwInit	Yes	100b
4:3	**Phantom Functions Supported** ***Not supported***	RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum *Tag* field is 5 bits 1 = Maximum *Tag* field is 8 bits	RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** 111b = No Limit	RO	Yes	111b
11:9	**Endpoint L1 Acceptable Latency** 111b = No Limit	RO	Yes	111b
14:12	***Reserved***	RsvdP	No	000b
15	**Role-Based Error Reporting**	RO	Yes	1
17:16	***Reserved***	RsvdP	No	00b
25:18	**Captured Slot Power Limit Value** For the NT Port Link Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	RO	Yes	00h
27:26	**Captured Slot Power Limit Scale** For the NT Port Link Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	RO	Yes	00b
31:28	***Reserved***	RsvdP	No	0h

Register 16-22. 70h Device Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Device Control			
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report Correctable errors to the System Host	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report Non-Fatal errors to the System Host	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report Fatal errors to the System Host	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report UR errors as error Messages with a programmed uncorrectable error severity	RW	Yes	0
4	**Enable Relaxed Ordering** ***Not supported***	RsvdP	No	0
7:5	**Maximum Payload Size** The NT Port Link Interface power-on/reset value is 000b, to support a Maximum Payload Size of 128 bytes. Software can change this field to configure the NT Port Link Interface to support other Payload sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capability** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]), for the NT Port Virtual and Link Interfaces. (Requester and Completer domains must possess the same Maximum Payload Size.) 000b = NT Port Link Interface supports a 128-byte maximum payload 001b = NT Port Link Interface supports a 256-byte maximum payload 010b = NT Port Link Interface supports a 512-byte maximum payload No other encodings are supported. ***Note:*** *Software must halt all transactions through the NT Port before changing this field.*	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported***	RsvdP	No	0
9	**Phantom Functions Enable** ***Not supported***	RsvdP	No	0
10	**AUX Power PM Enable** ***Not supported***	RsvdP	No	0
11	**Enable No Snoop** ***Not supported***	RsvdP	No	0
14:12	**Maximum Read Request Size** ***Not supported***	RsvdP	No	000b
15	***Reserved***	RsvdP	No	0

Register 16-22. 70h Device Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Device Status			
16	**Correctable Error Detected** Set when the NT Port Link Interface detects a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable*) state. 0 = NT Port Link Interface did not detect a Correctable error 1 = NT Port Link Interface detected a Correctable error	RW1C	Yes	0
17	**Non-Fatal Error Detected** Set when the NT Port Link Interface detects a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable*) state. 0 = NT Port Link Interface did not detect a Non-Fatal error 1 = NT Port Link Interface detected a Non-Fatal error	RW1C	Yes	0
18	**Fatal Error Detected** Set when the NT Port Link Interface detects a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable*) state. 0 = NT Port Link Interface did not detect a Fatal error 1 = NT Port Link Interface detected a Fatal error	RW1C	Yes	0
19	**Unsupported Request Detected** Set when the NT Port Link Interface detects a UR, regardless of the bit 3 (*Unsupported Request Reporting Enable*) state. 0 = NT Port Link Interface did not detect a UR 1 = NT Port Link Interface detected a UR	RW1C	Yes	0
20	**AUX Power Detected** ***Not supported***	RsvdP	No	0
21	**Transactions Pending** ***Not supported*** Because the PEX 8604 NT Port is a bridging device, it does not track Completion for the corresponding Non-Posted transactions. Therefore, the NT Port Link Interface does not implement this bit.	RsvdP	No	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 16-23. 74h Link Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
3:0	**Supported Link Speeds** Indicates the NT Port Link Interface's supported Link speed. 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s and 2.5 GT/s Link speeds are supported All other encodings are ***reserved***.	RO	Yes	0010b (STRAP_RESERVED17#=H) 0001b (STRAP_RESERVED17#=L)
9:4	**Maximum Link Width** The PEX 8604 maximum Link width is x2 = 00_0010b. Valid widths are x1 or x2. Actual maximum Link width is Set by the STRAP_PORTCFG[1:0] inputs. 00_0000b = ***Reserved*** 00_0001b = x1 00_0010b = x2 All other encodings are ***not supported***.	ROS	No	Set by STRAP_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 574h[1:0])
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported All other encodings are ***reserved***.	RO	Yes	01b
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the **Common Physical Layer Command/Status** register *N_FTS Value* field (NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 238h[15:8]) value and Link speed. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = NT Port Link Interface L0s Link PM state Exit Latency is 512 ns to less than 1 µs at 5.0 GT/s 101b = NT Port Link Interface L0s Link PM state Exit Latency is 1 µs to less than 2 µs at 2.5 GT/s All other encodings are ***reserved***.	RO	No	100b (5.0 GT/s) 101b (2.5 GT/s)

Register 16-23. 74h Link Capability *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = NT Port Link Interface L1 Link PM state Exit Latency is 1 µs to less than 2 µs at 5.0 GT/s 010b = NT Port Link Interface L1 Link PM state Exit Latency is 2 µs to less than 4 µs at 2.5 GT/s All other encodings are ***reserved***.	RO	Yes	001b (5.0 GT/s) 010b (2.5 GT/s)
18	**Clock Power Management**	RO	Yes	0
23:19	***Reserved*** ***Note:*** *Bits [21:19] are also* ***reserved*** *in NT PCI-to-PCI Bridge mode.*	RsvdP	No	0-0h
31:24	**Port Number** The NT Port Number value is selected by the STRAP_NT_UPSTRM_PORTSEL[3:0] inputs. All other encodings are ***reserved***. 00h = Port 0 01h = Port 1 04h = Port 4 05h = Port 5	ROS	No	Set by STRAP_NT_UPSTRM_PORTSEL[3:0] input levels

Register 16-24. 78h Link Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Link Control			
1:0	**Active State Power Management (ASPM) Control** 00b = Disable[a] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**Read Request Return Parameter Control** Read Request Return Parameter "R" control. Read Completion Boundary (RCB).	RO	Yes	0
4	**Link Disable** ***Reserved*** for the NT Port Link Interface.	RsvdP	No	0
5	**Retrain Link** ***Reserved*** for the NT Port Link Interface. Always read as 0.	RsvdP	No	0
6	**Common Clock Configuration** 0 = NT Port Link Interface and the device at the other end of the corresponding Port's PCI Express Link use an asynchronous Reference Clock source 1 = NT Port Link Interface and the device at the other end of the corresponding Port's PCI Express Link use a common (synchronous) Reference Clock source (constant phase relationship)	RW	Yes	0
7	**Extended Sync** When Set, causes the NT Port Link Interface to transmit: • 4,096 FTS Ordered-Sets in the L0s Link PM state, • Followed by a single SKIP Ordered-Set prior to entering the L0 Link PM state, • Finally, transmission of 1,024 TS1 Ordered-Sets in the *Recovery* state.	RW	Yes	0
15:8	***Reserved***	RsvdP	No	00h

Register 16-24. 78h Link Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Link Status			
19:16	**Current Link Speed** Indicates the negotiated Link speed of the Port's PCI Express Link. 0001b = 2.5 GT/s Link speed 0010b = 5.0 GT/s Link speed All other encodings are ***reserved***. The value in this field is undefined when the Link is not up.	RO	No	0001b
25:20	**Negotiated Link Width** Dependent upon the configuration of the physical Ports. Link width is determined by the negotiated value with the attached Lane/Port. 00_0000b = Link is down (default) 00_0001b = x1 or Port is in the *DL_Down* state 00_0010b = x2 All other encodings are ***not supported***.	RO	No	00_0000b
26	***Reserved***	RsvdP	No	0
27	**Link Training** ***Reserved*** for the NT Port Link Interface.	RsvdP	No	0
28	**Slot Clock Configuration** Set by the upstream Port or NT Port Link Interface, but not both. 0 = Indicates that the PEX 8604 uses an independent clock 1 = Indicates that the PEX 8604 uses the same physical Reference Clock that the platform provides on the connector	HwInit	Yes	0
31:29	***Reserved***	RsvdP	No	000b

a. The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.

Register 16-25. 98h Link Status and Control 2

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Link Control 2				
3:0	**Target Link Speed** 0001b = 2.5 GT/s Link speed supported 0010b = 5.0 GT/s Link speed supported All other encodings are ***reserved***.	RWS	Yes	0010b
4	**Enter Compliance**	RWS	Yes	0
5	**Hardware Autonomous Speed Disable** ***Reserved*** Initial transition to the highest supported common Link speed is not blocked by this bit.	RsvdP	No	0
6	**Selectable De-Emphasis** ***Reserved***	RsvdP	Yes	0
9:7	**Transmit Margin** Intended for debug and compliance testing only.	RWS	Yes	000b
10	**Enter Modified Compliance** Intended for debug and compliance testing only.	RWS	Yes	0
11	**Compliance SOS** 1 = Link Training and Status State Machine (LTSSM) must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern	RWS	Yes	0
12	**Compliance De-Emphasis** Sets the de-emphasis level in the *Polling.Compliance* state, if the entry occurred due to bit 4 (*Enter Compliance*) being Set.	RWS	Yes	0
15:13	***Reserved***	RsvdP	No	000b
Link Status 2				
16	**Current De-Emphasis Level** Reflects the de-emphasis level. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB (Link is operating at 2.5 GT/s)	RO	No	0 (5.0 GT/s) 1 (2.5 GT/s)
31:17	***Reserved***	RsvdP	No	0-0h

16.9 NT Port Link Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)

The registers detailed in Section 13.10, "Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)," are also applicable to the NT Port, except as defined in Table 16-6 (register map) and Register 16-26.

Table 16-6. NT Port Link Interface Subsystem ID and Subsystem Vendor ID Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	Next Capability Pointer (C8h) / SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID	Subsystem Vendor ID	A8h
Reserved	ACh –	C4h

Register 16-26. A4h Subsystem Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**SSID/SSVID Capability ID** Detects the SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the *PCI-to-PCI Bridge r1.2*.	RO	Yes	0Dh
15:8	**Next Capability Pointer** Program to C8h, to point to the **Vendor-Specific Capability 3** structure.	RO	Yes	C8h
31:16	***Reserved***	RsvdP	No	0000h

16.10 NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)

This section details the NT Port Link Interface Vendor-Specific Extended Capability 3 registers. Table 16-7 defines the register map used by the NT Port.

The Cursor Mechanism registers at offsets F8h and FCh provide a means for accessing PCI Express Extended Configuration Space registers (offsets 100h through FFFh) within the NT Port Link and Virtual Interfaces, when only standard PCI Configuration transactions (that do not support the *Extended Register Number* field within the Completion Request Header) are available.

Table 16-7. NT Port Link Interface Vendor-Specific Extended Capability 3 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Vendor-Specific Extended Capability 3	Next Capability Pointer 3 (00h) / PCI Express Capability ID 3 (09h)	C8h
Vendor-Specific Header 3 ***(Reserved)***		CCh
Reserved		D0h – E0h
NT Port Link Interface BAR0/1 Setup		E4h
NT Port Link Interface Memory BAR2 Setup		E8h
NT Port Link Interface Memory BAR2/3 Setup		ECh
NT Port Link Interface Memory BAR4 Setup		F0h
NT Port Link Interface Memory BAR4/5 Setup		F4h
Configuration Address Window	***Reserved***	F8h
Configuration Data Window		FCh

Register 16-27. C8h Vendor-Specific Extended Capability 3

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**PCI Express Capability ID 3**	RO	Yes	09h
15:8	**Next Capability Pointer 3** 00h = This capability is the last capability in the Linked list	RO	Yes	00h
31:16	**Length** Quantity of bytes in this Capability structure.	RO	Yes	0038h

Register 16-28. CCh Vendor-Specific Header 3

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	***Reserved***	RO	Yes	0380_0002h

Register 16-29. E4h NT Port Link Interface BAR0/1 Setup

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	**BAR0/1 Enable** 00b = Disables Link Interface **BAR0** and **BAR1** 01b = ***Reserved*** 10b = Enables Link Interface **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) 11b = Enables Link Interface **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR)	RW	No	10b
2	**BAR0 Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	No	0
31:3	***Reserved***	RsvdP	No	0-0h

Register 16-30. E8h NT Port Link Interface Memory BAR2 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
0	**Type Selector**		RsvdP	No	0
2:1	**BAR2 Type** 00b = **BAR2** is implemented as a 32-bit Memory BAR 10b = **BAR2/3** is implemented as a 64-bit Memory BAR No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR2 Size** Specifies the Address Range size requested by **BAR2**. 0 = Corresponding **BAR2** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR2** bits are RW bits		RW	Yes	0-0h
31	**BAR2 Enable** 0 = **BAR2** is disabled, all **BAR2** bits read 0 1 = **BAR2** is enabled	Field [2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	BAR2 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 16-31. ECh NT Port Link Interface Memory BAR2/3 Setup

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note: *This register has RW privilege if* ***BAR2/3*** *is configured as a 64-bit BAR (**NT Port Link Interface Memory BAR2 Setup** register BAR2 Type field, offset E8h[2:1], is programmed to 10b).*					
0	**Type Selector**	Offset E8h[2:1]=00b	RsvdP	No	0
		Offset E8h[2:1]=10b	RW	Yes	0
2:1	**BAR3 Type** 00b = **BAR3** is implemented as a 32-bit Memory BAR No other encodings are allowed.	Offset E8h[2:1]=00b	RsvdP	No	00b
		Offset E8h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset E8h[2:1]=00b	RsvdP	No	0
		Offset E8h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset E8h[2:1]=00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset E8h[2:1]=10b	RW	Yes	0_000h
30:20	**BAR3 Size** Specifies the Address Range size requested by **BAR3**. 0 = Corresponding **BAR3** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR3** bits are RW bits		RW	Yes	0-0h
31	**BAR3 Enable** **32-Bit BAR** 0 = **BAR3** is disabled 1 = **BAR3** is enabled as a 32-bit BAR	Offset E8h[2:1]=00b	RW	Yes	0
	64-Bit BAR 0 = **BAR2/3** is disabled, all **BAR2/3** bits read 0 1 = **BAR2/3** is enabled as a 64-bit BAR	Offset E8h[2:1]=10b	RW	Yes	0

Register 16-32. F0h NT Port Link Interface Memory BAR4 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
0	**Type Selector**		RsvdP	No	0
2:1	**BAR4 Type** 00b = **BAR4** is implemented as a 32-bit Memory BAR (**BAR4**) 10b = **BAR4/5** is implemented as a 64-bit Memory BAR (**BAR4/5**) No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding **BAR4** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR4** bits are RW bits		RW	Yes	0-0h
31	**BAR4 Enable** 0 = **BAR4** is disabled, all **BAR4** bits read 0 1 = **BAR4** is enabled	Field [2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	BAR4 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 16-33. F4h NT Port Link Interface Memory BAR4/5 Setup

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note: *This register has RW privilege if* ***BAR4/5*** *is configured as a 64-bit BAR (**NT Port Link Interface Memory BAR4 Setup** register BAR4 Type field, offset F0h[2:1], is programmed to 10b).*					
0	**Type Selector**	Offset F0h[2:1]=00b	RsvdP	No	0
		Offset F0h[2:1]=10b	RW	Yes	0
2:1	**BAR5 Type** 00b = **BAR5** is implemented as a 32-bit Memory BAR No other encodings are allowed.	Offset F0h[2:1]=00b	RsvdP	No	00b
		Offset F0h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset F0h[2:1]=00b	RsvdP	No	0
		Offset F0h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset F0h[2:1]=00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset F0h[2:1]=10b	RW	Yes	0_000h
30:20	**BAR5 Size** Specifies the Address Range size requested by **BAR5**. 0 = Corresponding **BAR5** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR5** bits are RW bits		RW	Yes	0-0h
31	**BAR5 Enable** **32-Bit BAR** 0 = **BAR5** is disabled 1 = **BAR5** is enabled as a 32-bit BAR	Offset F0h[2:1]=00b	RW	Yes	0
	64-Bit BAR 0 = **BAR4/5** is disabled, all **BAR4/5** bits read 0 1 = **BAR4/5** is enabled as a 64-bit BAR	Offset F0h[2:1]=10b	RW	Yes	0

Register 16-34. F8h Configuration Address Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	***Reserved***	RsvdP	No	0000h
25:16	**Register Offset**	RW	Yes	0-0h
30:26	***Reserved***	RsvdP	No	0-0h
31	**Interface Select** 0 = Access is to the NT Port Link Interface Type 0 Configuration Space register 1 = Access is to the NT Port Virtual Interface Type 0 Configuration Space register	RW	Yes	0

Register 16-35. FCh Configuration Data Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Register Data** Software selects a register by writing into the NT Port Link Interface Configuration Address window, then reads from or writes to that register using this register.	RW	Yes	0000_0000h

16.11 NT Port Link Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)

The registers detailed in Section 13.11, "Device Serial Number Extended Capability Registers (Offsets 100h – 134h)," are also applicable to the NT Port. Table 16-8 defines the register map used by all Ports.

Table 16-8. NT Port Link Interface Device Serial Number Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h) / Capability Version (1h)	PCI Express Extended Capability ID (0003h)	100h
Serial Number (Lower DW)		104h
Serial Number (Upper DW)		108h
Reserved		10Ch – 134h

16.12 NT Port Link Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)

The registers detailed in Section 13.12, "Power Budget Extended Capability Registers (Offsets 138h – 144h)," are also applicable to the NT Port Link Interface. Table 16-9 defines the register map.

Table 16-9. NT Port Link Interface Power Budget Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (148h) / Capability Version (1h)	PCI Express Extended Capability ID (0004h)	138h
Reserved	Data Select	13Ch
Power Budget Data		140h
Power Budget Capability		144h

16.13 NT Port Link Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)

The registers detailed in Section 13.13, "Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)," are also applicable to the NT Port Link Interface, except as defined in Table 16-10 (register map; offsets 1A8h through 1B4h are ***reserved***) and Register 16-36.

Table 16-10. NT Port Link Interface Virtual Channel Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (950h) / Capability Version (1h)	PCI Express Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2		150h
Port VC Status ***(Reserved)***	Port VC Control	154h
VC0 Resource Capability		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
VC1 Resource Capability		164h
VC1 Resource Control		168h
VC1 Resource Status	***Reserved***	16Ch
Reserved	170h –	1BCh

Register 16-36. 148h Virtual Channel Extended Capability Header

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID** Program to 0002h, as required by the *PCI Express Base r2.0*.	RO	No	0002h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.	RO	No	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset 950h.	RO	No	950h

16.14 NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)

The registers detailed in Section 13.14, "Device-Specific Registers (Offsets 1C0h – 51Ch)," and Section 13.16, "Device-Specific Registers (Offsets 530h – F8Ch)" (for offsets A00h through C88h), are unique to the PEX 8604 and not referenced in the *PCI Express Base r2.0*. These registers are also applicable to the NT Port Link Interface, except as defined in Table 16-11 (register map; offsets 200h through 57Ch, 680h through 94Ch, and 964h through C30h, are ***reserved***, and offset 960h is associated with an NT Port Link Interface-specific register) through Table 16-16, and Register 16-37 through Register 16-45.

Another NT Port Link Interface Device-Specific register is detailed in Section 16.16, "NT Port Link Interface Device-Specific Registers – Source Queue Weight (Offsets F00h – F3Ch)."

Note: It is recommended that these registers not be changed from their default values.

Table 16-11. NT Port Link Interface Device-Specific Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Link Interface Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)		1C0h … 1FCh
Reserved		200h – 65Ch
NT Port Link Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)		660h … 67Ch
Reserved		980h – 94Ch
Next Capability Offset 2 (C34h)	1h / PCI Express Extended Capability ID 2 (000Bh)	950h
NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)		… 95Ch
NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)		960h
Reserved		964h – C30h
Next Capability Offset 4 (000h)	1h / PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)		… C88h

16.14.1 NT Port Link Interface Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)

The registers detailed in Section 13.14.1, "Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)," are also applicable to the NT Port Link Interface, except as defined in Table 16-12 (register map; offsets 1C0h, 1C4h, 1CCh through 1DCh, and 1F4h are ***reserved***), and Register 16-37 through Register 16-39.

Table 16-12. NT Port Link Interface Device-Specific Error Checking and Debug Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Reserved	1C0h –	1C4h
ECC Error Check Disable		1C8h
Reserved	1CCh –	1DCh
Power Management Hot Plug User Configuration (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)		1E0h
Egress Control and Status (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)		1E4h
Bad TLP Counter		1E8h
Bad DLLP Counter		1ECh
Reserved	1F0h –	1F4h
ACK Transmission Latency Limit (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)		1F8h
Factory Test Only		1FCh

Register 16-37. 1C8h ECC Error Check Disable

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**ECC 1-Bit Error Check Disable** 0 = RAM 1-Bit Soft Error Check enabled 1 = Disables RAM 1-Bit Soft Error Check	RWS	Yes	0
1	**ECC 2-Bit Error Check Disable** 0 = RAM 2-Bit Soft Error Check enabled 1 = Disables RAM 2-Bit Soft Error Check	RWS	Yes	0
2	**Software Force Error Enable** 1 = **Correctable Error Status** and **Uncorrectable Error Status** registers (offsets FC4h and FB8h, respectively) change from RW1CS to RW	RWS	Yes	0
3	**Software Force Non-Posted Request** 1 = Enables handling of errors associated with Posted TLPs as if those errors are associated with Non-Posted TLPs	RWS	Yes	0
4	***Reserved***	RsvdP	No	0
5	**Enable PEX_INTA# Interrupt Output(s) for Device-Specific Error-Triggered Interrupts** 0 = Device-Specific Error Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = Device-Specific Error Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
6	**Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts** 0 = General-Purpose Input/Output (GPIO) Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = GPIO Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
7	**Enable PEX_INTA# Interrupt Output(s) for NT-Link Doorbell-Generated Interrupts** 0 = NT Port Link Interface Doorbell Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = NT Port Link Interface Doorbell Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
8	**Disable Sending MSI if MSI Is Enabled after Interrupt Status Set** 0 = Does not disable sending an MSI, if MSIs are enabled after an *Interrupt Status* bit is Set 1 = Disables sending an MSI, if MSIs are enabled after an *Interrupt Status* bit is Set ***Note:*** *This bit must remain Cleared, for compliance to specifications governing the MSI Capability.*	RWS	Yes	0
31:9	***Reserved***	RsvdP	No	0-0h

Register 16-38. 1E0h Power Management Hot Plug User Configuration

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *This register is* ***reserved*** *in NT PCI-to-PCI Bridge mode.*				
0	**L0s Entry Idle Counter** Traffic idle time to meet to enter the L0s Link PM state. 0 = Idle condition must last 1 µs 1 = Idle condition must last 4 µs	RW	Yes	0
1	***Factory Test Only***	RW	Yes	0-0h
2	**NT Virtual MPS CSR Select** NT Port Virtual Interface Maximum Payload Size register select. 0 = NT Port Virtual Interface uses the NT Port Link Interface's Maximum Payload Size (offset 70h[7:5]) 1 = NT Port Virtual Interface uses its own Maximum Payload Size (offset 70h[7:5])	RW	Yes	0
7:3	***Factory Test Only***	RW	Yes	0-0h
8	**DLLP Timeout Link Retrain Disable** Disable Link retraining when no Data Link Layer Packets (DLLPs) are received for more than 256 µs. 0 = Enables Link retraining when no DLLPs are received for more than 256 µs (default) 1 = DLLP Timeout is disabled	RW	Yes	0
9	***Factory Test Only***	RW	Yes	0
10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met	RW	Yes	0
31:11	***Reserved***	RsvdP	No	0-0h

Register 16-39. 1F8h ACK Transmission Latency Limit

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The value of this register should be valid after Link negotiation. ***Note:*** *This register is* ***reserved*** *in NT PCI-to-PCI Bridge mode.*				
11:0	**ACK Transmission Latency Limit** Acknowledge Control Packet (ACK) Transmission Latency Limit. The value of this field changes, based upon the Negotiated Link Width (offset 78h[25:20]), after the Link is up. x1 Link width = 255d x2 Link width = 217d	RWS	Yes	0FFh
15:12	***Reserved***	RsvdP	No	0h
23:16	**Upper 8 Bits of the Replay Timer Limit** The value in this register is a multiplier of the default internal timer values that are compliant to the *PCI Express Base r2.0*. These bits should normally remain the default value, 00h.	RWS	Yes	00h
30:24	***Reserved***	RsvdP	No	00h
31	**ACK Transmission Latency Timer Status** Indicates the written status of field [11:0] (*ACK Transmission Latency Limit*). After the register is written, either by software and/or serial EEPROM, this bit is Set, and Cleared only by a Fundamental Reset.	RO	No	0

16.14.2 NT Port Link Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)

The registers detailed in Section 13.16.5, "Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)," are also applicable to the NT Port Link Interface, except as defined in Table 16-13 (register map; offsets 660h, 664h, and 674h through 678h are ***reserved***).

Table 16-13. NT Port Link Interface Device-Specific Ingress Control and Port Enable Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				660h – 664h
Reserved		Port Enable Status		668h
Factory Test Only	Negotiated Link Width for Ports 0, 4, 5			66Ch
Reserved				670h
Reserved				670h – 67Ch

16.14.3 NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)

The registers detailed in Section 13.16.10, "Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)," are also applicable to the NT Port, except for the Next Capability Offset value, as defined in Table 16-14 (register map) and Register 16-40.

Table 16-14. NT Port Link Interface Device-Specific, Vendor-Specific Extended Capability 2 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 2 (C34h)	Capability Version 2 (1h) / PCI Express Extended Capability ID 2 (000Bh)	950h
Vendor-Specific Header 2		954h
Hardwired Device ID	Hardwired Vendor ID	958h
Reserved	PLX Hardwired Revision ID	95Ch

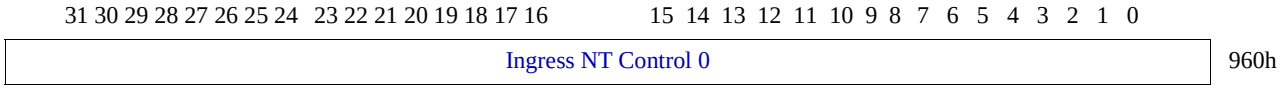
Register 16-40. 950h Vendor-Specific Extended Capability 2

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID 2** Program to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 2**	RO	Yes	1h
31:20	**Next Capability Offset 2** Program to C34h, which addresses the **Vendor-Specific Extended Capability 4** structure.	RO	Yes	C34h

16.14.4 NT Port Link Interface Device-Specific Registers – Ingress NT Control (Offset 960h)

This section details the Device-Specific Ingress NT Control register, which is specific to the NT Port Link Interface. Table 16-15 defines the register map.

Table 16-15. NT Port Link Interface Ingress NT Control Register Map



Register 16-41. 960h Ingress NT Control 0

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *Use of this register is described in Section 14.4, "Traffic Class Translation."*				
0	**TC Change Enable** Traffic Class Change enable. 0 = No change 1 = Perform TC change on Egress TLPs	RW	Yes	0
1	**BAR2_32_bit_ok**	RW	Yes	0
2	**BAR3_32_bit_ok**	RW	Yes	0
3	**BAR4_32_bit_ok**	RW	Yes	0
4	**BAR5_32_bit_ok**	RW	Yes	0
5	**BAR2_64_bit_ok**	RW	Yes	0
6	**BAR4_64_bit_ok**	RW	Yes	0
9:7	**Link to Virtual TC**	RW	Yes	000b
31:10	***Reserved***	RsvdP	No	0-0h

16.14.5 NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)

The registers detailed in Section 15.13.4, "NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)," are also applicable to the NT Port Link Interface, except as defined in Table 16-16 (register map), and Register 16-42 through Register 16-45.

Table 16-16. NT Port Link Interface Device-Specific, Vendor-Specific Extended Capability 4 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 4 (000h)	Capability Version 4 (1h) / PCI Express Extended Capability ID 4 (000Bh)	C34h
Vendor-Specific Header 4		C38h
Memory BAR2 Address Translation Lower		C3Ch
Memory BAR3 Address Translation Upper		C40h
Memory BAR4 Address Translation Lower		C44h
Memory BAR5 Address Translation Upper		C48h
Reserved	Virtual Interface IRQ Set	C4Ch
Reserved	Virtual Interface IRQ Clear	C50h
Reserved	Virtual Interface IRQ Mask Set	C54h
Reserved	Virtual Interface IRQ Mask Clear	C58h
Reserved	Link Interface IRQ Set	C5Ch
Reserved	Link Interface IRQ Clear	C60h
Reserved	Link Interface IRQ Mask Set	C64h
Reserved	Link Interface IRQ Mask Clear	C68h
NT Port SCRATCH0		C6Ch
NT Port SCRATCH1		C70h
NT Port SCRATCH2		C74h
NT Port SCRATCH3		C78h
NT Port SCRATCH4		C7Ch
NT Port SCRATCH5		C80h
NT Port SCRATCH6		C84h
NT Port SCRATCH7		C88h

Register 16-42. C3Ch Memory BAR2 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR2 Base Translation Address** Base Translation address when **BAR2** is enabled (**NT Port Link Interface Memory BAR2 Setup** register *BAR2 Enable* bit, offset E8h[31], is Set).	RW	Yes	000h

Register 16-43. C40h Memory BAR3 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	Offset ECh[31]=0	RsvdP	No	0_0000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset ECh[31]=1	RW	Yes	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR3 Base Translation Address** Base Translation address when **BAR3** is enabled (**NT Port Link Interface Memory BAR2/3 Setup** register *BAR3 Enable* bit, offset ECh[31], is Set).		RW	Yes	000h

Register 16-44. C44h Memory BAR4 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR4 Base Translation Address** Base Translation address when **BAR4** is enabled (**NT Port Link Interface Memory BAR4 Setup** register *BAR4 Enable* bit, offset F0h[31], is Set).	RW	Yes	000h

Register 16-45. C48h Memory BAR5 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	Offset F4h[31]=0	RsvdP	No	0_0000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset F4h[31]=1	RW	Yes	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR5 Base Translation Address** Base Translation address when **BAR5** is enabled (**NT Port Link Interface Memory BAR4/5 Setup** register *BAR5 Enable* bit, offset F4h[31], is Set).		RW	Yes	000h

16.15 NT Port Link Interface NT Bridging-Specific Registers (Offsets C8Ch – EFCh)

Table 16-17 defines the register map of the NT Port Link Interface NT Bridging-Specific registers.

Table 16-17. NT Port Link Interface NT Bridging-Specific Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
Reserved				C8Ch –	DB0h
NT Port Link Interface Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses DB4h – DF0h)					DB4h … DF0h
Reserved				DF4h –	EFCh

16.15.1 NT Port Link Interface Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses DB4h – DF0h)

This section describes the NT Port Link Interface NT Bridging-Specific Requester ID Translation Lookup Table (LUT) Entry registers. The NT Port uses these registers for Requester ID translation when it forwards:

- Memory Requests from the NT Port Link Interface to the NT Port Virtual Interface, –or–
- Completion TLPs from the NT Port Virtual Interface to the NT Port Link Interface

If the application needs to send traffic through the NT Port Link Interface, program the registers listed in this group with the corresponding Requester's Requester ID, then Set the *LUT Entry_n Enable* and *LUT Entry_m Enable* bits (bits 0 and 16, respectively) for each LUT entry, as needed.

Table 16-18 defines the register and address locations, as they relate to Register 16-46.

Table 16-18. NT Port Link Interface NT Bridging-Specific Requester ID Translation LUT Entry_*n*_*m* Register Locations

ADDR Location	Lookup Table Entry_*n*_*m*	ADDR Location	Lookup Table Entry_*n*_*m*
DB4h	0_1	DD4h	16_17
DB8h	2_3	DD8h	18_19
DBCh	4_5	DDCh	20_21
DC0h	6_7	DE0h	22_23
DC4h	8_9	DE4h	24_25
DC8h	10_11	DE8h	26_27
DCCh	12_13	DECh	28_29
DD0h	14_15	DF0h	30_31

Register 16-46. DB4h – DF0h NT Port Link Interface Requester ID Translation LUT Entry_*n_m* (where *n_m* = 0_1 through 30_31)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
0	**LUT Entry_*n* Enable** 0 = Disables 1 = Enables		RW	Yes	0
1	**LUT Entry_*n* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Link Interface to the NT Port Virtual Interface, and re-calculates the ECRC. If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Virtual Interface to the NT Port Link Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
2	***Reserved***		RsvdP	No	0
7:3	**Requester ID on Link Side**	**Device Number** LUT Entry_*n* Requester Device Number.	RW	Yes	0000_0b
15:8		**Bus Number** LUT Entry_*n* Requester Bus Number.	RW	Yes	00h
16	**LUT Entry_*m* Enable** 0 = Disables 1 = Enables		RW	Yes	0
17	**LUT Entry_*m* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Link Interface to the NT Port Virtual Interface, and re-calculates the ECRC. If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Virtual Interface to the NT Link Virtual Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
18	***Reserved***		RsvdP	No	0
23:19	**Requester ID on Link Side**	**Device Number** LUT Entry_*m* Requester Device Number.	RW	Yes	0000_0b
31:24		**Bus Number** LUT Entry_*m* Requester Bus Number.	RW	Yes	00h

16.16 NT Port Link Interface Device-Specific Registers – Source Queue Weight (Offsets F00h – F3Ch)

Register offset F10h, detailed in Section 13.16.16, "Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F3Ch)," is also applicable to the NT Port Link Interface. The remaining registers within the register set are ***reserved*** in the NT Port Link Interface, as defined in the Table 16-19 register map.

Other NT Port Link Interface Device-Specific registers are detailed in Section 16.14, "NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)."

Table 16-19. NT Port Link Interface Device-Specific Source Queue Weight Register Map (Offsets F00h – F3Ch)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				F00h – F0Ch
Port Egress TLP Threshold				F10h
Reserved				F14h – F3Ch

16.17 NT Port Link Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

The registers detailed in Section 13.17, "Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)," are also applicable to the NT Port Link Interface, except as defined in Table 16-20 (register map), Register 16-47, and the exceptions indicated in the note.

Notes: *Data Link Protocol and Surprise Down PCI Express errors are not valid for the NT Port Link nor Virtual Interfaces, and therefore do not affect register offsets FB8h, FBCh, and FC0h in NT mode.*

Receiver, Bad TLP, Bad DLLP, Replay Number Rollover, and Replay Timer Timeout PCI Express errors are not valid for the NT Port Link nor Virtual Interfaces, and therefore do not affect register offsets FC4h and FC8h in NT mode.

Table 16-20. NT Port Link Interface Advanced Error Reporting Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (138h)	Capability Version (1h) / PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status		FB8h
Uncorrectable Error Mask		FBCh
Uncorrectable Error Severity		FC0h
Correctable Error Status		FC4h
Correctable Error Mask		FC8h
Advanced Error Capabilities and Control		FCCh
Header Log 0		FD0h
Header Log 1		FD4h
Header Log 2		FD8h
Header Log 3		FDCh

Register 16-47. FB4h Advanced Error Reporting Extended Capability Header

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID**	RO	Yes	0001h
19:16	**Capability Version**	RO	Yes	1h
31:20	**Next Capability Offset** Program to 138h, which addresses the upstream Port/NT Port Link Interface **Power Budget Extended Capability** structure.	RO	Yes	138h

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Chapter 17 Dual Clocking Support

17.1 Introduction

The Dual Clocking feature allows the PEX 8604 to be used in a Spread Spectrum Clocking (SSC) environment and communicate with devices that are operating in a Constant Frequency Clocking (CFC) environment. This capability is necessary for systems in which the upstream Port connects to the SSC source, while downstream Ports connect to Links running on CFC domains.

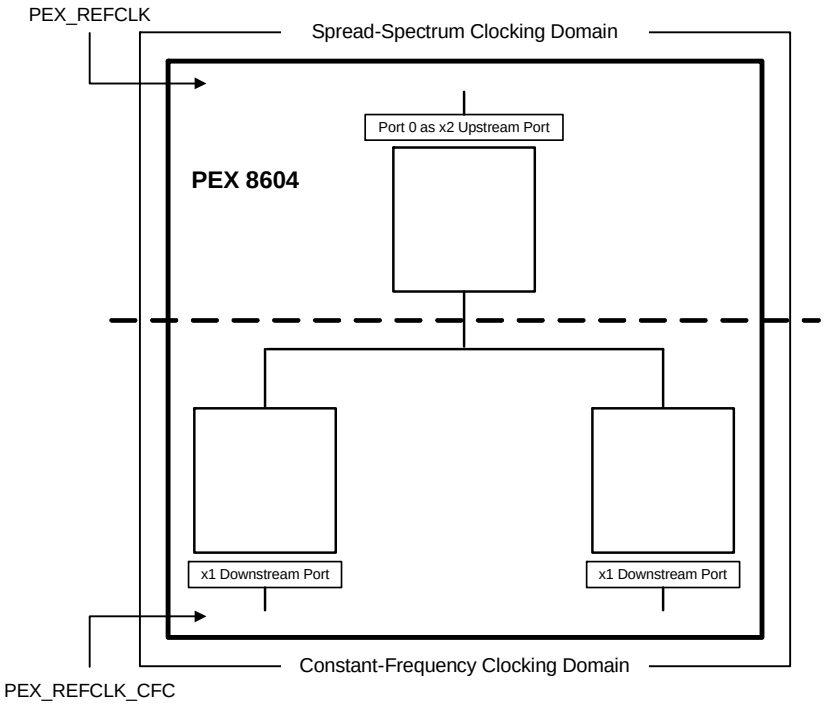
The SSC isolated Port does not have to be the upstream Port; however, it does need to be Port 0, because all the SSC resources are located in Port 0. Port 0 must be connected to an SSC domain, and the other Ports must be connected to a CFC domain, as illustrated in Figure 17-1.

Most systems support SSC; however, the *PCI Express Base r2.0* specifies that REFCLKs of two interconnected devices must be within a ±300 ppm frequency tolerance of one another.

The *PCI Express Base r2.0* specifies that the data rate of two connected Ports must be within ±300 ppm from one another. The *PCI Express Base r2.0* also specifies that the data rate can be SSC modulation, which is defined as a +0/-5,000 ppm modulation from the base frequency. This essentially requires that if one device is using a SSC clock, then the other device must use the same clock, to be able to track the frequency modulation. Therefore, a device on a system that supports SSC clocking cannot be connected to a device on another system that does not use SSC. If a system supports SSC, all devices in the PCI Express interconnect must have the same Reference Clock source, to allow traffic to communicate between them. However, this is not practical in the case of chassis-to-chassis or blade-to-blade PCI Express traffic. If each chassis or blade has its own SSC source, special clock isolation circuitry is required to enable such configurations to communicate between themselves. For this reason, the PEX 8604 supports two REFCLK inputs that allow traffic to move from the SSC clock domain on the upstream Port to a CFC clock domain on the downstream Ports, thereby allowing two different chassis or blades to communicate with one another.

The SSC domain runs at a frequency between 99.5 and 100 MHz. The CFC domain runs at a frequency of 100 MHz. Because the SSC and CFC domain average frequencies are not identical, the PEX 8604 provides buffering and flow control to ensure that data does not overflow nor underflow as it passes from one clock domain to the other. Dual Clocking support is provided in fan-in/fan-out configurations when Port 0 is programmed to a x2 Link width.

Figure 17-1. PEX 8604 in a Dual Clock System



17.2 Dual Clocking Operation

Dual Clocking is enabled when the following conditions are met:

- STRAP_SSC_ISO_ENABLE# input is pulled or tied Low to VSS (GND)
- Port 0's Link width is x2

When Dual Clocking is enabled, the REFCLK balls are mapped as follows:

- PEX_REFCLKn and PEX_REFCLKp signal balls become the SSC domain Clock signals
- PEX_REFCLK_CFCn and PEX_REFCLK_CFCp signal balls become the CFC domain Clock signals

If the system design does not use Dual Clocking, the STRAP_SSC_ISO_ENABLE# input must be pulled or tied High to VDD25, and the PEX_REFCLK_CFCn and PEX_REFCLK_CFCp signals must remain floating. If the PEX 8604 uses SSC on its upstream Port, or the upstream Port is not configured to Port 0, the PEX_REFCLKn and PEX_REFCLKp signals must be shared by all downstream devices. If the PEX 8604 uses a Constant Frequency source on its upstream Port, each downstream device can use an independent CFC REFCLK source, provided that it meets the *PCI Express Base r2.0*-defined PCI Express frequency tolerance of ±300 ppm.

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Chapter 18 Test and Debug

18.1 Introduction

This chapter describes the following test- and debug-related information:

- Physical Layer Loopback Operation
- User Test Pattern
- Pseudo-Random Bit Sequence
- Using the Even/Odd Port SerDes Quad x Diagnostic Data Registers
- Pseudo-Random and Bit-Pattern Generation
- PHY Testability Features
- JTAG Interface
- Lane Good Status LEDs

18.2 Physical Layer Loopback Operation

18.2.1 Overview

Physical Layer (PHY) Loopback functions are used to test the SerDes in the PEX 8604, connections between devices, and SerDes of external devices, as well as various PEX 8604 and external digital logic. The PEX 8604 supports four types of Loopback operations, as described in Table 18-1. Additional information regarding each type is provided in the sections that follow.

Table 18-1. Loopback Operations

Operation	Description
Analog Loopback Master Mode	This mode depends upon an external device or passive connection (*such as* a cable) to loopback the transmitted data to the PEX 8604, without SKIP Ordered-Set clock compensation. If an external device is used, it must not include its Elastic buffer in the Slave Loopback data path, so that SKIP Ordered-Sets are not inserted. A device's re-transmitted Receive data must be sent back to the Master, synchronous to the Master's Transmit Reference Clock. *That is*, the Slave device re-serializes the Transmit data, using the recovered clock from the received data. In that mode, the PRBS generator and checker should be used to create and check the data pattern.
Digital Loopback Master Mode	This mode depends upon an external device to loopback the transmitted data that includes at least its Elastic buffer in the Loopback data path, allowing for reliable loopback testing, in case the two devices have asynchronous Reference Clock sources with Parts per Million (PPM) offsets. The Master's pattern generator inserts SKIP Ordered-Sets at regular intervals, and its received data checker can handle PPM offset clock compensation, by way of SKIP symbol addition or deletion. The PEX 8604 provides a User Test Pattern generator and checker that can be used for Digital loopback testing.
Analog Loopback Slave Mode	The PEX 8604 enters this mode when an external device transmits Training Sets with the *Loopback* Training Control Bit Set and the **Common Physical Layer Safety and Test** register *Analog Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[21]) is Set. Another way to unconditionally force the Slave into Analog loopback is described later in Section 18.2.4. While in this mode, the received data is looped back from the SerDes 10-bit Receive interface to the 10-bit Transmit interface. Internal to the SerDes, the serial-to-parallel and parallel-to-serial converters are included in the Loopback data path. The re-serialized data is transmitted back to the Master device synchronous to that Master's Reference Clock. This is because the recovered clock is fed back around to the Transmit interface and used as the Tx clock.
Digital Loopback Slave Mode	The PEX 8604 enters this mode when an external device transmits Training Sets with the *Loopback* Training Control Bit Set and the **Common Physical Layer Safety and Test** register *Analog Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[21]) is Cleared. This is the default Loopback mode for the LTSSM Slave *Loopback.Active* state. In this mode, the data is looped back at the 8-bit level, which includes the PEX 8604's Elastic buffer, 8b/10b decoder, and 8b/10b encoder in the Slave Loopback data path. Asynchronous clock compensation can occur in the Elastic buffer through SKIP symbol addition or deletion, depending upon clock PPM offsets and fill threshold decoding. The Master data pattern checker must be able to handle the presence of SKIP Ordered-Sets and variations in their contents.

18.2.2 Analog Loopback Master Mode

Analog Loopback Master mode is typically used for Analog Far-End testing (refer to Figure 18-1), with a shallow Loopback path Slave device, to determine overall Bit Error rates. However, it can also be used for passive external serial loopback with a cable. Looping back with a cable includes the internal circuitry, package connections to bond pads, package balls, board traces, and any connectors that might be in the test data path, as illustrated in Figure 18-2. A PRBS pattern is typically used for this mode, because it is appropriate for bit error rate testing. A User Test Pattern (UTP) is ***not*** recommended for this application – refer to Section 18.3 for details.

Figure 18-1. Analog Far-End Loopback

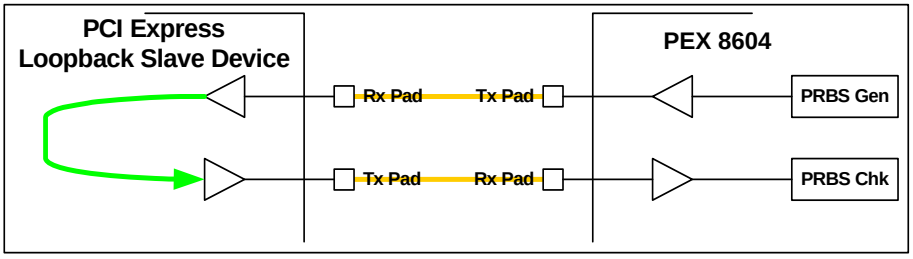
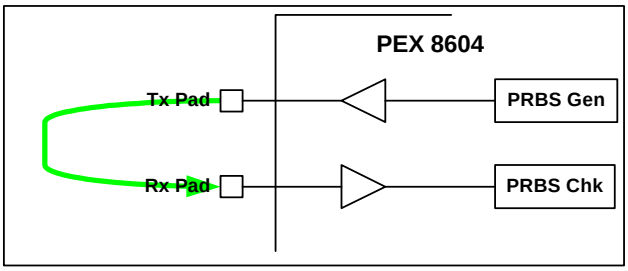


Figure 18-2. Cable Loopback



18.2.2.1 Initiating Far-End Analog Operations in PEX 8604 Master Devices

Note: *Initiating a Master Loopback operation on an upstream Port can cause a Deadlock condition to occur, unless an I^2C Slave interface is used to write and read Configuration Space register bits instead of writing them through upstream Port Configuration transactions. Therefore, it is recommended to restrict Analog Master loopback testing to downstream Ports when external devices are used.*

One way to test Master Analog loopback with passive cables is to have an upstream Port connected to a Root Complex, for Configuration Write/Read transactions that are used to Set and monitor the key device register bits. In that case, only downstream Ports would be test-capable, to avoid potential Deadlock conditions on the upstream Port. Alternatively, an I^2C Slave interface and Rapid Development Kit (RDK) software could be used to write to or read from the registers. This makes any Port testable. The user has the option of attaching one or more cables to the appropriate high-speed Tx and Rx differential pairs that belong to the Ports being tested.

Loopback cables can be attached before or after a standard power-up initialization sequence. If the cables are attached before power-up, use a serial EEPROM to program the **Even/Odd Port Physical Layer Command/Status** register *Port x Loopback Command* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 220h[8, 0], and Odd Ports, offset 224h[8, 0]) for the Port being tested. The Port's *Port x Loopback Command* bit arms the Port to enter the Master *Loopback.Entry* state. When written from a serial EEPROM, the bit's assertion is present before the Ports begin Link training. In that case, the Ports directly transition to the LTSSM *Loopback* state from the LTSSM *Configuration* state. The LTSSM exits the *Polling* state and enters the *Configuration.LinkWidth.Start* state, then immediately transitions to the Master *Loopback.Entry* state.

At this point, users can sample the Port's **Even/Odd Port Physical Layer Command/Status** register *Port x Ready as Loopback Master* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 220h[11, 3], and Odd Ports, offset 224h[11, 3]), to determine whether the bit is Set, which indicates that the Master has reached the LTSSM *Loopback.Active* state. At this time, the PRBS engine can be enabled, by Setting the **Even/Odd Port User Test Pattern Delay** register *SerDes x PRBS Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[25:24], and Odd Ports, offset 25Ch[25:24]) associated with the SerDes assigned to the Port being tested.

The PRBS Receive data checker first synchronizes the de-serialized parallel data words from the returned pattern with a reference PRBS pattern generator. At this point, users should check the Lane synchronization status in the **Even/Odd Port Loopback Master Status/Control** register *PRBS Pattern Sync Status Device Lane x* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset B80h[17:16], and Odd Ports, offset B84h[17:16]). If there is no synchronization, there is likely a physical connection problem. Once synchronized, the PRBS checker looks for errors, on a continuous basis. Any errors detected are logged in one or more of the **Even/Odd Port SerDes Quad *x* Diagnostic Data** register RO bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 240h and 244h, bits [30 and 23:0]). The errors can be retrieved, by reading the appropriate bit.

If the *Port x Loopback Command* bits are not Set through the serial EEPROM, the Ports' Loopback Training Sets can be used to cause the Ports to linkup, by way of a Configuration cross-link track, resulting with the Ports being in L0 Link PM state. This linkup of a Port, in response to its own Training Sets, only works if the Port's **Even/Odd Port Loopback Master Status/Control** register *Port x External Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset B80h[10, 8], and Odd Ports, offset B84h[10, 8]) is Set by serial EEPROM. Once the Port is in the L0 Link PM state, Configuration Space register programming can then be performed manually, to invoke a Master Loopback operation.

Once the Ports linkup, users can direct the Ports into an Analog Loopback Master condition, by writing the *Port x Loopback Command* bit(s), through the upstream Port and/or I^2C Slave interface. However, this is not sufficient to initiate the LTSSM transition from the L0 Link PM state, to the *Loopback* state. The Link must pass through a *Recovery* substate, before the *Port x Loopback Command* bits can be sampled and allow the LTSSM to pass through the *Recovery* state to the *Loopback* state. To cause the Port to enter the *Recovery* state, users must Set the Port's **Link Control** register *Retrain Link* bit (offset 78h[5]). At this point, users should monitor the Port's *Port x Ready as Loopback Master* bit(s), and when Set, the PRBS engine(s) can be enabled, as previously described.

If loopback cables are attached after the device powers up, then those Ports whose Lanes are floating unconnected did not detect Receivers. Therefore, those Ports are not trained up to the L0 Link PM state.

If the Port's *Port x Loopback Command* and *Port x External Loopback Enable* bit(s) for the downstream Ports to be tested are written ***before*** the cables are attached, then once cabled, there is Receiver detection, the Port(s) go through Link training, and then exit the LTSSM *Configuration* state and directly enter the *Loopback* state.

However, if the Port's *Port x Loopback Command* and *Port x External Loopback Enable* bit(s) are Set ***after*** the cables are attached, the Ports do not recognize their own Training Sets and will likely cycle back and forth between *Configuration* and *Detect*. Therefore, users must at least Set the *Port x External Loopback Enable* bit for the Ports being tested, by way of serial EEPROM, if the PEX 8604 is powered up before the cables are attached. Users can then program the Port's *Port x Loopback Command* bit(s). In addition to this, a forced retrain is also needed, to enter into the *Loopback* state through the *Recovery* state, as previously described.

18.2.3 Digital Loopback Master Mode

The only difference between Analog and Digital Loopback Master modes is that the external device is assumed to have at least an Elastic buffer in the Loopback data path. Because of this, SKIP Ordered-Sets must be included in the test data pattern, which precludes use of the PRBS engine.

Figure 18-3 illustrates a Far-End Digital Loopback Master connection and data path.

The PEX 8604 provides a User Test Pattern engine on a per-Lane basis, for Digital Far-End Loopback testing. The user pattern itself, however, is common to all Lanes where it is enabled. Details on the use of the User Test Pattern registers and controls are described later in Section 18.5.

What is important to note about the data path (not shown in Figure 18-3) is that the pattern generators and checkers in the PEX 8604 Digital Loopback Master have 8/10b encode, 10b/8b decode, and Elastic buffers included in the Tx/Rx path. The scramblers and de-scramblers are disabled. Therefore, the Digital Loopback Slave device must not scramble the returning data. The 10-bit data can be decoded to 8-bit, and encoded back to 10-bit as an option, and will not affect the UTP pattern checker in the PEX 8604, unless there is a coding error.

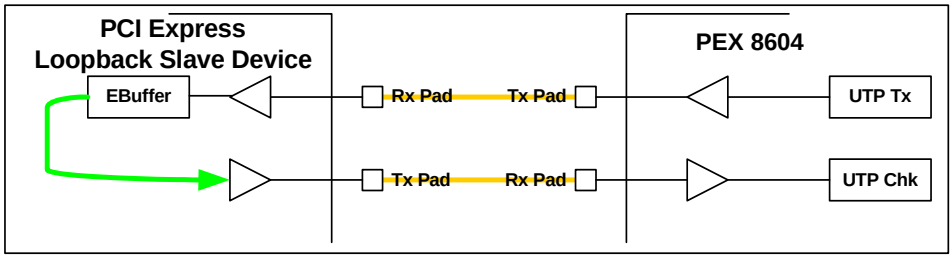
Digital Loopback Master mode is established by either programming method previously described in Section 18.2.2 for Analog Loopback Master mode. The Port's **Even/Odd Port Physical Layer Command/Status** register *Port x Loopback Command* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 220h[8, 0], and Odd Ports, offset 224h[8, 0]) can be Set with a serial EEPROM, causing Loopback to be entered directly from the LTSSM *Configuration* state. Otherwise, the Port's *Port x Loopback Command* bit can be Set after linkup, and then the Port's **Link Control** register *Retrain Link* bit (offset 78h[5]) can be used to move the Port to the *Loopback* state, through the LTSSM *Recovery* state.

Once Digital Loopback Master mode is established, Configuration Space register Writes are used to establish a User Test Pattern transmission, as well as error checking, which are described later in Section 18.3.

The UTP is multiplexed, unconditionally, onto the Transmit data path, upon Setting one or more of the **Even/Odd Port User Test Pattern Delay** register *SerDes x User Test Pattern Enable* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[17:16], and Odd Ports, offset 25Ch[17:16]).

Note: *It is important to verify that the LTSSM is in a Master Loopback.Active state, before writing 1 to the SerDes x User Test Pattern Enable bits. Therefore, do not use the serial EEPROM to Set the SerDes x User Test Pattern Enable bits. (Refer to Section 18.4 for details.)*

Figure 18-3. Digital Far-End Loopback



18.2.4 Analog Loopback Slave Mode

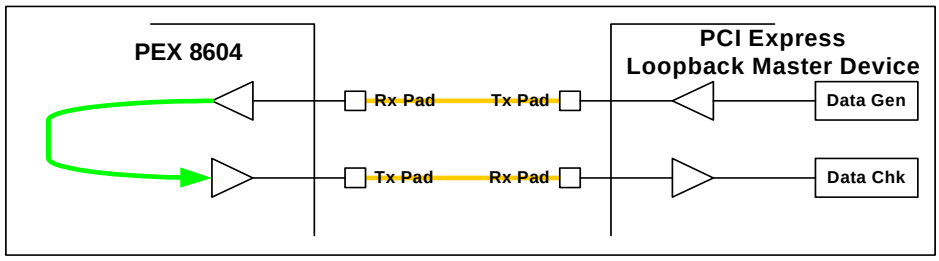
The PEX 8604 becomes an Analog Loopback Slave (as illustrated in Figure 18-4) if it receives Training Sets with the *Loopback* Training Control Bit Set while the **Common Physical Layer Safety and Test** register *Analog Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[21]) is Set. It is recommended that the *Analog Loopback Enable* bit be Set first, before bringing the PEX 8604 into an LTSSM Slave *Loopback.Active* state.

As previously described, Analog Loopback does not have only pure analog circuitry in the Slave's data path. While in this mode, the received data and recovered clock are looped back from the SerDes Parallel Receive Data interface to the Parallel Transmit interface. Internal to the SerDes, the serial-to-parallel and parallel-to-serial converters are included in the Loopback data path. The re-serialized data is transmitted back to the Master device, synchronous to that Master's Reference Clock.

The multiplexing control that enables Parallel data from the Receive path, directly back to the Transmit path, is held off from asserting until the Slave reaches the *Loopback.Active* state. Then, the Parallel Recovered data and clock are multiplexed back into the SerDes Parallel Transmit interface. That multiplexer remains effective until the PEX 8604 Loopback Slave exits the *Loopback.Active* state. There are alternate ways to transition out of the Slave *Loopback.Active* state:

- If the Loopback is operating at Gen 2 (5.0 GT/s) Link speed, receipt of four consecutive Electrical Idle Ordered-Sets (EIOS) causes a Loopback exit
- If the Link is operating at Gen 1 (2.5 GT/s) Link speed, then receipt of a single EIOS, or detection of Electrical Idle entry, causes an exit
- If the Slave device appears to be "stuck" in the *Loopback.Active* state, toggling of the Port's **Even/Odd Port Physical Layer Command/Status** register *Port x Loopback Command* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 220h[8, 0], and Odd Ports, offset 224h[8, 0]), from 0 to 1 to 0, breaks the LTSSM out of Loopback Slave operation

Figure 18-4. Analog Loopback Slave Mode



Analog Loopback Slave mode is most suitable for a PRBS test pattern. However, because the PEX 8604 includes only the SerDes in the Loopback data path, and the Transmit data is clocked out at the recovered clock frequency, the Master can include SKIP Ordered-Sets in its data pattern, regardless of whether the system uses synchronous or asynchronous clocking, as long as it can tolerate the presence of SKIP Ordered-Sets in the data pattern. In this case, the Master sees its own SKIP Ordered-Sets returned to it, at the same intervals and positions in the data pattern.

If the Master device is not capable of bringing the PEX 8604 to a Slave *Loopback.Active* state (*such as* a Bit Error Rate Tester (BERT) as the Master) through the LTSSM state transition arcs previously described, there is a way to unconditionally force the Slave into Analog Loopback Slave mode, through device Configuration Space register Writes to the appropriate bit states. The *BERT Loopback Path Enable* bits (**Even/Odd Port Physical Layer Test** register *Lane x Parallel Loopback Path Enable* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 228h[26, 24], and Odd Ports, offset 22Ch[26, 24])) are first Set for all device Lanes associated with the Port being tested.

Next, the **Common Physical Layer Safety and Test** register *Analog Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[21]) is Set. The Lanes enabled by the BERT's *Lane x Parallel Loopback Path Enable* bits immediately go into an Analog Loopback path mode, ***regardless of the Slave's current LTSSM state***.

Concurrently Setting the *Analog Loopback Enable* and BERT's *Lane x Parallel Loopback Path Enable* bits, for all Lanes of the Port being tested, changes the Loopback data path, as described; however, that does not guarantee that the SerDes Transmitters are powered on and operating at the correct speed. Other PHY Safety bits can be used to ensure that the SerDes are powered up and ready to be placed into Analog Loopback Slave mode. The **Even/Odd Port Disable/Quiet/Test Pattern Rate** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 230h and 234h) contains useful bits for controlling loopback operations:

- *Disable Port x* bits – Even Ports, offset 230h[2, 0], and Odd Ports, offset 234h[2, 0]
- *Hold Port x Quiet* bits – Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]
- *Port x Test Pattern x Rate* bits – Even Ports, offset 230h[18, 16], and Odd Ports, offset 234h[18, 16]

The Port's *Hold Port x Quiet* bit holds the Port in the *Detect.Quiet* state once it enters that state, and does not allow the LTSSM to advance. The Port's *Hold Port x Quiet* bits also keep the SerDes Transmitters and Receivers powered on, as long as the Port's *Disable Port x* bit is not Set. The Port's *Port x Test Pattern x Rate* bit, if Set, forces the Port's SerDes to shift their Link speed to Gen 2 (5.0 GT/s) **if** the Port's *Hold Port x Quiet* bit is also Set.

When forcing the PEX 8604 into Analog Loopback Slave mode with a BERT attached, the Port's LTSSM looks at whatever the BERT is transmitting on the attached Lanes. Because the BERT does not transmit Training Sets, the LTSSM detects Receivers, goes to the *Polling* state, times out, and then returns to the *Detect* state to try again. The LTSSM should remain in the *Detect.Quiet* state once it returns to that state. The Port's *Hold Port x Quiet* bit, therefore, should be Set, to hold the PEX 8604 in a stable LTSSM *Detect.Quiet* state, that keeps the SerDes powered on and prevents additional state transitions. If it is necessary for the BERT to test the SerDes at the Gen 2 rate, Set the Port's *Port x Test Pattern x Rate* bit before Setting its *Hold Port x Quiet* bit.

To Set the necessary bits prior to BERT testing, for the Port being tested:

1. Use I^2C to Set the Port's **Even/Odd Port Quiet** register *Hold Port x Quiet* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8]).
2. If Analog Loopback Slave mode must operate at the Gen 2 rate (5.0 GT/s), Set the Port's **Even/Odd Port Test Pattern Rate** register *Port x Test Pattern x Rate* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 230h[18, 16], and Odd Ports, offset 234h[18, 16]).
3. Set the BERT's **Even/Odd Port Physical Layer Test** register *Lane x Parallel Loopback Path Enable* bit(s) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 228h[26, 24], and Odd Ports, offset 22Ch[26, 24]).
4. Set the **Common Physical Layer Safety and Test** register *Analog Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[21]).

   The Slave device should now be in Analog Loopback Slave, properly powered, and at the correct Link speed for BERT testing.

18.2.5 Digital Loopback Slave Mode

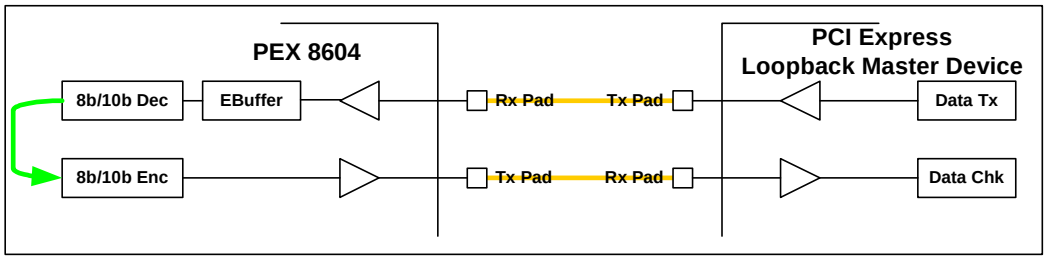
When a PEX 8604 Port is in the LTSSM Slave *Loopback.Active* state, it automatically becomes a Digital Loopback Slave, by default. The Port enters this state after it receives Training Sets with the *Loopback* Training Control Bit Set.

When a PEX 8604 Port is a Digital Loopback Slave, it includes the Elastic buffer, 8b/10b decoder, and 8b/10b encoder in the Loopback data path. The Loopback Master must provide the test data pattern and data pattern checker (*such as* a PEX 8604 User Test Pattern). The Loopback Master must also transmit SKIP Ordered-Sets with the data pattern. Depending upon the PEX 8604 Reference Clock source's PPM offset, the PEX 8604 Digital Loopback Slave's Elastic buffers can compensate for the offset, by returning more or fewer SKIP symbols than the PEX 8604 received from the Master. Therefore, the Master's data pattern checker must make provisions for this when decoding for errors.

This mode is ***not*** suitable for a PRBS pattern as transmitted from the Master, because neither device can compensate for Reference Clock offset differences, should they exist.

Unlike Analog Loopback Slave mode (described in Section 18.2.4), there is no way to unconditionally force the Loopback path into Digital Loopback Slave mode, through the use of PHY-related register bits – the Slave must be brought into the mode by a Master-connected device, through standard LTSSM tracks.

Figure 18-5. Digital Loopback Slave Mode



18.3 User Test Pattern

The PEX 8604 provides a User Test Pattern (UTP) Transmit and Receive data checker, for Digital Far-End Loopback testing. (Refer to Figure 18-3.) After LTSSM Loopback Master mode is established, Configuration Writes are used to fill the **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 210h through 21Ch). One or more **Even/Odd Port User Test Pattern Delay** register *SerDes x User Test Pattern Enable* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[17:16], and Odd Ports, offset 25Ch[17:16]) are used to start the UTP transmission, on the Lanes assigned to each bit. The UTP logic assumes that there is asynchronous clocking between the PEX 8604 Loopback Master and the connected Slave device. Therefore, the expectation is that there is at least a clock-crossing boundary in the Slave device's Loopback data path (*such as* an Elastic buffer). SKIP Ordered-Sets are inserted into the user's test data pattern, at the nearest data pattern boundary according to the programmed SKIP interval. That interval is determined by the **Common Physical Layer Safety and Test** register *SKIP Ordered-Set Interval* field (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[19:8]) value. The default interval is 1,180 symbol times.

The Test Pattern checker ignores SKIP Ordered-Sets returned by the Loopback Slave, because the quantity of SKIP symbols received can be different from the quantity transmitted. All other data is compared to the transmitted data, and errors are logged in the **Even/Odd Port SerDes Quad *x* Diagnostic Data** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 240h and 244h).

The 16-byte UTP is loaded into the **Physical Layer User Test Pattern, Bytes *x* through *y*** registers. The pattern is common to all Lanes. Prior to transmission, the 8b/10b encoder converts the 16 bytes to 10-bit encoded data. Pattern bytes only go out as control symbols (k-bit set), if the Lane's **Common Physical Layer Command/Status** register *User Test Pattern K-Code Flag* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 238h[31:16]) is Set.

Caution: ***Use caution when Setting User Test Pattern K-Code Flag bits, because UTP logic does not check the validity of Control characters.***

The UTP Transmitter logic does not immediately transmit the UTP bytes upon being enabled – a fixed, 4-byte sync pattern (5243h) is continuously transmitted first. The sync word detection validates the physical Loopback wiring and connected device Loopback path, to qualify the UTP transmission's initiation. The sync DWord allows the Pattern Checking logic to determine the starting boundary of the received pattern byte sequence. Sync detection also enables Received Data error checking and logging. Unfortunately, there are no sync-acquired status bits in the Physical Layer registers, like there are for PRBS; therefore, it is not possible to verify that the sync pattern has been detected. However, a single UTP Error Count is logged if the sync pattern is not detected within 256 ns from the initial transmission of the sync DWord. Therefore, a single Error Count may, or may not, indicate the absence of received sync data (*for example*, a good sync could have been followed by a single bit error).

Notes: *There are no explicit Control bits for deliberately injecting UTP errors into the transmission, to test the error checking ability. However, one way of testing the ability is to write a test pattern byte to a different value after the transmission has started. That usually causes a temporary unequal boundary condition, which will log an error. While not guaranteed to inject an error, this method is useful for testing error checking ability.*

A UTP is not recommended for Master mode far-end cable testing, especially when initiated by way of serial EEPROM from a power-up sequence. If a UTP is enabled and looped back before Link training begins, the symbol framers will not have seen any COM symbols, and the true 10-bit symbol boundaries are unknown. The framer requires three COMs in a row, in the same bit position, to achieve symbol lock. Neither the sync pattern, nor the user pattern, would be detected in this case, and the test is certain to fail.

In addition to the 16-byte pattern registers, the UTP is enabled on a per-Lane basis, by Setting the **Even/Odd Port User Test Pattern Delay** register *SerDes x User Test Pattern Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[17:16], and Odd Ports, offset 25Ch[17:16]), for the SerDes associated with the Port being tested.

Note: *The UTP is unconditionally multiplexed onto the Transmit data path, upon Setting the SerDes x User Test Pattern Enable bits. Therefore, it is necessary to verify that the LTSSM is in an LTSSM Master Loopback.Active state* ***before*** *writing a value of 1 to those Enable bits.* ***Do not use a serial EEPROM to Set the SerDes x User Test Pattern Enable bits.***

UTP testing results can be monitored in one of the **Even/Odd Port SerDes Quad *x* Diagnostic Data** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 240h and 244h). Each register can be used to examine the Error Count in the *UTP/PRBS Error Counter* field [23:16], and expected/actual data of the first failing byte (fields [7:0 and 15:8], respectively). The *Status* bits are on a per-Lane basis associated with a SerDes quad. **The important field in these registers is the *SerDes Diagnostic Data Select* field [25:24].** When the Lane code for the quad is written to that field, the UTP status for that Lane appears in the *Status* fields. Bit 30 of the register (*PRBS Counter/-UTP Counter*) is a pattern type indicator, and is Cleared when UTP is enabled for a Lane.

Notes: *Use of the Diagnostic registers is explained in Section 18.5.*

The UTP and PRBS Enables are mutually exclusive, and must not be Set concurrently. *If both Enables are simultaneously Set, the resulting operation is undefined. The UTP/PRBS Error Counter field continues to count, until it saturates at 255. To clear the Counter and allow it to begin logging errors again, write all zeros (0) to that field. Alternatively, the Counter status is Cleared if the SerDes x User Test Pattern Enable bit for that Lane is Cleared, and then Set again.*

18.4 Pseudo-Random Bit Sequence

A Pseudo-Random Bit Sequence (PRBS) generator and checker are useful as a diagnostic/debugging tool, and for measuring short- or long-term bit error rates in PCI Express systems. The PEX 8604 also uses a specially enabled power-up self-test that runs after reset, as a wafer sort test for use on automated test equipment. PRBS pattern generators and checkers reside within the SerDes_rclk_blk modules, because they transmit and receive 10- or 20-bit data directly to/from the SerDes quads. Locating them in the modules helps ensure tight timing and short trace length on SerDes Tx and Rx parallel data.

The PEX 8604 PRBS logic is enabled by one or more of the **Even/Odd Port User Test Pattern Delay** register *SerDes x PRBS Enable* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[25:24], and Odd Ports, offset 25Ch[25:24]), for the SerDes associated with the Port being tested. Prior to enabling PRBS, an externally connected PCI Express device must be in an LTSSM Slave *Loopback.Active* state. Furthermore, the reference clocking between the two devices must be synchronous. (*That is*, the returning PRBS pattern must have its transmission clock source synchronous to the PEX 8604 Reference Clock.) The PEX 8604 PRBS pattern generator does not insert any SKIP Ordered-Sets, and, if the Slave device inserts SKIP Ordered-Sets into the returning pattern, they cannot be ignored by the PRBS checker (it causes an error). Alternatively, the PRBS pattern can be used to test an external cable Loopback, after the correct LTSSM Master *Loopback.Active* state is reached, as described in Section 18.2.2.

After a PEX 8604 Lane's PRBS engine is enabled, the PRBS engine immediately begins to transmit the PRBS pattern on that Lane. No 8b/10b encoding is performed. The PRBS pattern generator produces 10- or 20-bit symbols on every Clock cycle, depending upon the current Link speed. The symbols are written directly into the SerDes Tx data Port, for immediate transmission.

The PRBS Receive Data Checking logic first synchronizes the de-serialized 10- or 20-bit Parallel Data symbols from the SerDes Rx data Port, using a reference PRBS pattern generator. After pattern synchronization is achieved, the Receive data checker begins comparing the Rx data symbols on a continuous basis, to discover any mismatch between a symbol's expected and received values.

Note: *Error checking cannot begin until synchronization is achieved; therefore, it is important to monitor the pattern synchronization status, before checking the error status. Synchronization status is available in the* ***Even/Odd Port Loopback Master Status/Control*** *register PRBS Pattern Sync Status Device Lane x bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset B80h[17:16], and Odd Ports, offset B84h[17:16]).* ***This status should always be checked.*** *If there is no synchronization, there is likely a physical connection problem. Any errors detected are logged in one or more of the* ***Even/Odd Port SerDes Quad x Diagnostic Data*** *registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 240h and 244h). Use of these registers is explained in Section 18.5.*

It is possible to inject errors into a PRBS pattern while it is transmitting on a per-Lane basis, for testing the ability to find and count errors, by programming the **Even/Odd Port SerDes Quad *x* Diagnostic Data** register *PRBS Error Injection* field(s) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 240h and 244h, field [29:26]) to 1h. When enabled, an error is injected, by corrupting a single bit in one PRBS pattern symbol once every 127 words.

PRBS testing results can be monitored in one of the **Even/Odd Port SerDes Quad *x* Diagnostic Data** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 240h and 244h). Each register can be used to examine the Error Count in the *UTP/PRBS Error Counter* field [23:16], and expected/actual data of the first failing byte (fields [7:0 and 15:8], respectively). The *Status* bits are on a per-Lane basis associated with a SerDes quad. **The important field in these registers is the *SerDes Diagnostic Data Select* field [25:24].** When the Lane code for the quad is written to that field, the PRBS status for that Lane appears in the *Status* fields. Bit 30 of the register (*PRBS Counter/-UTP Counter*) is a pattern type indicator, and is Set when PRBS is enabled for a Lane.

Notes: *Use of the Diagnostic registers is explained in Section 18.5.*

The UTP and PRBS Enables are mutually exclusive, and must not be Set concurrently. *If both Enables are simultaneously Set, the resulting operation is undefined. The UTP/PRBS Error Counter field continues to count, until it saturates at 255. To Clear the Counter and allow it to begin logging errors again, write all zeros (0) to that field. Alternatively, the Counter status is Cleared if the SerDes x User Test Pattern Enable bit for that Lane is Cleared, and then Set again.*

The PRBS Error Count does not necessarily represent a true Bit Error rate. The PRBS checker detects one or more mismatched bits in each examined symbol, on a symbol-per-core-clock basis. Therefore, the Error Counter advances one count for every symbol mismatch, regardless of how many bits are in error for that failing symbol.

18.4.1 Physical Layer Built-In Self-Test

The PEX 8604 also uses the PRBS engines in a special power-up self-test of all SerDes. This is called *Physical Layer Built-In Self-Test (PHY BIST)*, and is intended for production wafer sorting, to screen out die that have basic SerDes Rx/Tx data/clock circuitry faults. The test uses the Internal Serial Loopback mode, whereby the serial Tx data is looped back to the serial Rx data path prior to the differential pad buffer cells. PHY BIST is enabled with a unique code (5h; LHLH) applied to the STRAP_TESTMODE[3:0] device Ports, and runs at Gen 2 (5.0 GT/s) Link speed.

Note: *If the SerDes must be brought up to 5.0 GT/s, it must be done without bringing the Link up in the same way that the Functional logic would bring the SerDes up. Instead, the PHY BIST uses the PIPE interface Rate signaling sequence, to change the speed before it starts up the PRBS generators, and then checks for Sync and Data errors.*

After the PHY Reset is released, the PHY BIST logic starts up if PHY BIST is enabled. If enabled, Internal Serial Loopback mode, as well as the PRBS engines for all device Lanes, are also enabled. PRBS Loopback pattern generation runs for 16 ms, and then stops. Any errors detected are logged in a special status, that is enabled onto the GPIO[5, 3:0] balls. Table 18-2 lists the GPIO[5, 3:0] mappings of the PHY BIST Status signals, for automated test equipment sensing and debug.

Table 18-2. PHY BIST Status at Device Ports

Device Ball Name	PHY BIST Status
GPIO0	PHY BIST Error Status
GPIO1	PHY BIST Done Status
GPIO2	PHY BIST All Sync OK Status
GPIO3	PHY SerDes Quad 0 BIST Error Status
GPIO5	PHY SerDes Quad 2 BIST Error Status

18.5 Using the Even/Odd Port SerDes Quad *x* Diagnostic Data Registers

Each SerDes quad has its own Diagnostic Data register. The **Even/Odd Port SerDes Quad *x* Diagnostic Data** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 240h and 244h) contents reflect the performance of the SerDes selected by the registers' *SerDes Diagnostic Data Select* field [25:24], as defined in Table 18-3. This control is specific to this register (which reports results of UTP and PRBS tests).

When field [25:24] is Cleared, the information in that Diagnostic Data register is for the first SerDes within that SerDes quad. When field [25:24] is programmed to 01b, the information in that Diagnostic Data register is for the second SerDes within that SerDes quad. Following this pattern, a value of 10b indicates the third SerDes within that SerDes quad, and a value of 11b indicates the fourth SerDes within that SerDes quad. If a SerDes module does not exist in that position, the bits are "***Factory Test Only***," ***reserved*** (RsvdP), and not serial EEPROM nor I^2C writable.

Table 18-3. Even/Odd Port SerDes Quad *x* Diagnostic Data Register Contents (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 240h and 244h)

Register Offset	Register	*SerDes Diagnostic Data Select* Field [25:24] Value			
		00b	01b	10b	11b
240h	**Even Ports – SerDes Quad 0 Diagnostic Data**	SerDes 0	SerDes 1	***Reserved***	***Reserved***
244h	**Odd Ports – SerDes Quad 2 Diagnostic Data**	SerDes 4	SerDes 5	***Reserved***	***Reserved***

18.6 Pseudo-Random and Bit-Pattern Generation

Each SerDes quad has an associated PRBS generator and checker. The PRBS generator is based upon a 7-bit **Linear Feedback Shift** register (**LFSR**), which can generate up to (2^7 - 1) unique patterns. The PRBS logic is assigned to a SerDes in the quad, by manipulating the appropriate **Even/Odd Port SerDes Quad *x* Diagnostic Data** register *SerDes Diagnostic Data Select* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 240h and 244h, field [25:24]). The PRBS bit stream is used for Analog Far-End Loopback testing.

The PEX 8604 also provides a method of creating a repeating programmable bit pattern. Each of the four 32-bit **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 210h through 21Ch) are loaded with a 32-bit data pattern. After a Port is established as a Loopback Master, Set the appropriate **Even/Odd Port User Test Pattern Delay** register *SerDes x User Test Pattern Enable* bit(s) (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[17:16], and Odd Ports, offset 25Ch[17:16]), for the SerDes associated with that Port. The PEX 8604 proceeds to transmit the data pattern on all Lanes, starting with Byte 0 of the **Physical Layer User Test Pattern, Bytes 0 through 3** register and continuing, in sequence, through Byte 3 of the **Physical Layer User Test Pattern, Bytes 12 through 15** register. SKIP Ordered-Sets are inserted at the proper intervals, which makes this method appropriate for Digital Far-End Loopback testing. The received pattern is compared to the transmitted pattern. Any errors are logged and can be retrieved, by reading the appropriate **Even/Odd Port SerDes Quad *x* Diagnostic Data** register RO bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets 240h and 244h, bits [30 and 23:0]).

To produce a pseudo-clock bitstream in Analog Loopback mode, Set the registers as follows:

1. In the Slave device, enable Analog Loopback by Setting the **Common Physical Layer Safety and Test** register *Analog Loopback Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 23Ch[21]).
2. In the PEX 8604 Loopback Master device, Set the Port's **Even/Odd Port Physical Layer Command/Status** register *Port x Loopback Command* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 220h[8, 0], and Odd Ports, offset 224h[8, 0]).
3. Check whether loopback is successful, by reading the Port's **Even/Odd Port Physical Layer Command/Status** register *Port x Ready as Loopback Master* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 220h[11, 3], and Odd Ports, offset 224h[11, 3]) in the same Nibble that was Set in step 2. The Nibble value is 9h if Loopback was successful.
4. Set the **Even/Odd Port User Test Pattern Delay** register *SerDes x PRBS Enable* bit (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset 258h[25:24], and Odd Ports, offset 25Ch[25:24]) for the SerDes associated with the Port selected in step 2.
5. Check the **Even/Odd Port Loopback Master Status/Control** register *PRBS Pattern Sync Status Device Lane x* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port – Even Ports, offset B80h[17:16], and Odd Ports, offset B84h[17:16]). A bit returning a value of 1 indicates that the looped-back PRBS pattern is detected at the Master's Receiver.
6. Exit Loopback mode, by Clearing the following bits:
   a. *SerDes x PRBS Enable* bit, for the SerDes (selected in step 4) used by the Port selected in step 2.
   b. *Port x Loopback Command* bit, for the Port selected in step 2.

   Clearing these bits causes both sides of the Link to exit their LTSSM *Loopback* states, and return to the L0 Link PM state.

18.7 PHY Testability Features

The PEX 8604 includes several Configuration bits to ease PHY testability. Features include:

- Full support of the standard and modified compliance patterns
- Register controllability of the common block and Lane-specific inputs of the SerDes

Table 18-4 describes the Configuration bits.

Table 18-4. Configuration Bits to Ease PHY Testability

Register Bit(s)[a]	Description
SerDes x Mask Electrical Idle Detect **Even/Odd Port** **Electrical Idle for Compliance Mask** registers (Even Ports, offset 200h[9:8], and Odd Ports, offset 204h[9:8])	When any one of these bits is Set, the Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.
SerDes x Mask Receiver Not Detected **Even/Odd Port** **Receiver Detect Mask** registers (Even Ports, offset 200h[17:16], and Odd Ports, offset 204h[17:16])	When any one of these bits is Set, the PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.
Test Pattern x **Physical Layer User Test Pattern,** **Bytes *x* through *y*** registers (offsets 210h through 21Ch)	A 16-byte test pattern can be written to these four registers. When UTP transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 18.2.3 for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.
Port x Scrambler Disable Command **Even/Odd Port** **Physical Layer Command/Status** registers (Even Ports, offset 220h[9, 1], and Odd Ports, offset 224h[9, 1])	Unconditionally disables the data scramblers on the Lanes of the corresponding Port, and causes the *Scrambler Disable* Training Control Bit to be Set in transmitted Training Sets. There is one bit for each Port.
Disable Port x **Even/Odd Port** **Disable** registers (Even Ports, offset 230h[2, 0], and Odd Ports, offset 234h[2, 0])	When Set, LTSSM remains in the *Detect.Quiet* state on Port 0, if it is currently in, or returns to, that state. Unconditionally disables the corresponding Port. This is different from the LTSSM *Disabled* state, in that the Port does not attempt to enter this state. If the Port is idle, it ceases attempting to detect a Receiver. If the Port is up, it immediately returns to the *Detect.Quiet* state and remains there. No Electrical Idle Ordered-Set (EIOS) is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. The Port remains disabled until its *Disable Port x* bit is Cleared. While the Port is disabled, Receiver termination is disabled and the SerDes that belong to the disabled Port are placed into the L1 Link PM state.
Hold Port x Quiet **Even/Odd Port** **Quiet** registers (Even Ports, offset 230h[10, 8], and Odd Ports, offset 234h[10, 8])	When Set, the LTSSM remains in the *Detect.Quiet* state if it is currently in, or returns to, that state. Unlike the *Disable Port x* bits, these bits do not force the LTSSM into the *Detect.Quiet* state. Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed into the L0 Link PM state. This Port can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state.

Table 18-4. Configuration Bits to Ease PHY Testability *(Cont.)*

Register Bit(s)[a]	Description
Port x Test Pattern x Rate **Even/Odd Port** **Test Pattern Rate** registers (Even Ports, offset 230h[18, 16], and Odd Ports, offset 234h[18, 16])	The corresponding Port transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if the Port's *Hold Port x Quiet* bit is also Set (manual rate selection is enabled only when the *Hold Port x Quiet* bit is Set).
Port x Receiver Error Counter **Even/Odd Port** **Receiver Error Counters** registers (offsets B88h and B8Ch)	Contains four 8-bit fields that, when read, return the quantity of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in these registers; otherwise, this register is RO.

a. All registers listed in this table are located in Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port.

18.8 JTAG Interface

The PEX 8604 provides a Joint Test Action Group (JTAG) Boundary Scan interface, which is used to debug board connectivity for each ball.

18.8.1 *IEEE 1149.1* and *IEEE 1149.6* Test Access Port

The *IEEE Standard 1149.1* Test Access Port (TAP), commonly called the *JTAG Debug Port*, is an architectural standard described in the *IEEE Standard 1149.1-1990*. The *IEEE Standard 1149.6-2003* defines extensions to *1149.1* to support PCI Express SerDes testing. These standards describe methods for accessing internal device facilities, using a four- or five-signal interface.

The JTAG Debug Port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the *IEEE Standard 1149.1-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- **JTAG Signals** – JTAG Debug Port implements the four required JTAG signals – JTAG_TCK, JTAG_TDI, JTAG_TDO, JTAG_TMS – and optional JTAG_TRST# signal
- **Clock Requirements** – JTAG_TCK signal frequency ranges from 0 to 20 MHz
- **JTAG Reset Requirements** – Refer to Section 18.8.4

18.8.2 JTAG Instructions

The JTAG Debug Port provides the *IEEE Standard 1149.1-1990* BYPASS, EXTEST, SAMPLE, PRELOAD, CLAMP, and IDCODE instructions. *IEEE Standard 1149.6-2003* EXTEST_PULSE and EXTEST_TRAIN instructions are also supported. Table 18-5 lists the JTAG instructions, along with their input codes; Instruction Length is 29 bits.

The PEX 8604 returns the JTAG IDCODE values listed in Table 18-6.

Table 18-5. JTAG Instructions

Instruction	Input Code	Comments
BYPASS	1FFF_FFFFh	*IEEE Standard 1149.1-1990*
EXTEST	1FFF_FFE8h	
SAMPLE	1FFF_FFF8h	
PRELOAD	1FFF_FFF8h	
EXTEST_PULSE	1FF7_FFE8h	*IEEE Standard 1149.6-2003*
EXTEST_TRAIN	1FD3_FFE8h	
CLAMP	1FFF_FFEFh	*IEEE Standard 1149.1-1990*
IDCODE	1FFF_FFFEh	

Table 18-6. JTAG IDCODE Values

Units	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
Bits	0000b	1000_0110_0000_1000b	001_1100_1101b	1
Hex	0h	8608h	1CDh	1h

18.8.3 JTAG Boundary Scan

Boundary Scan Description Language (BSDL), IEEE Standard 1149.1-1994, is a supplement to the *IEEE Standard 1149.1-1990* and *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*. BSDL, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, allows a rigorous description of testability features in components which comply with the standard. This standard is used by automated test pattern generation tools for package interconnect tests, and Electronic Design Automation (EDA) tools for synthesized Test logic and verification. BSDL supports robust extensions that can be used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of BSDL include the logical Port description, physical ball map, instruction set, and **Boundary** register description.

The logical Port description assigns symbolic names to the device's signal balls. Each ball includes a logical type of *in*, *out*, *in out*, *buffer*, or *linkage* that defines the logical direction of signal flow.

The physical ball map correlates the device's logical Ports to the physical balls of a specific package. A BSDL description can include several physical ball maps, and maps are provided with a unique name.

Instruction Set statements describe the bit patterns that must be shifted into the **Instruction** register to place the device in the various test modes defined by the standard. Instruction Set statements also support descriptions of instructions that are unique to the PEX 8604.

The **Boundary** register description lists each cell or shift stage of the **Boundary** register. Each cell has a unique number – the cell numbered 0 is the closest to the JTAG Test Data Output (JTAG_TDO), and the cell with the highest number is closest to the JTAG Test Data Input (JTAG_TDI). Each cell includes additional information, *such as*:

- Cell type
- Logical Port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

Note: *The PEX 8604 requires Fundamental Reset (PEX_PERST# input assertion and de-assertion) and active REFCLK to initialize the switch, prior to using the JTAG interface.*

18.8.4 JTAG Reset Input – JTAG_TRST#

The JTAG_TRST# input is the asynchronous reset input to the JTAG TAP Controller logic. JTAG_TRST# assertion places the PEX 8604's TAP Controller into the *Test-Logic-Reset* state, which selects the PEX 8604 standard logic path (core-to-I/O), as required for typical functionality of the switch. JTAG_TRST# de-assertion enables the TAP Controller for test and debug functionality, such as boundary scan.

- If JTAG functionality is required, the JTAG_TRST# input should be transitioned from Low-to-High once during PEX 8604 power-up, along with PEX_PERST# de-assertion. In any JTAG state, the JTAG TAP Controller can be returned to the *Test-Logic-Reset* (initial) state, by holding the JTAG_TMS input High while clocking the JTAG_TCK input at least five times.
- If the PEX 8604's JTAG TAP Controller is not intended to be used by the design, an external pull-down resistor is recommended on the JTAG_TRST# input, because its internal pull-down resistor is weak.

18.9 Lane Good Status LEDs

The PEX 8604 provides Lane Good outputs, PEX_LANE_GOOD[5, 4, 1, 0]#, that can directly drive external common anode LED modules, to provide visual indication that the PHY of that Lane's Link is trained to at least x1 width.

Software can determine:

- Which Lanes have completed PHY linkup, by performing a Memory Read of the **Software Lane Status** register *Lane x Up Status* bits (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset 1F4h[5, 4, 1, 0], which correspond to Lanes [5, 4, 1, 0], respectively).
- Whether the Link for each Port has trained, by reading either the Port's **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]), or Port's **VC0 Resource Status** register *VC0 Negotiation Pending* and **VC1 Resource Status** register *VC1 Negotiation Pending* bits (offsets 160h[17] and 16Ch[17], respectively). If the *Data Link Layer Link Active* bit is Set, or *VC0 Negotiation Pending* and/or *VC1 Negotiation Pending* bit is Cleared, the Link has completed Flow Control (FC) initialization.

  The **Link Status** register can be read by either a PCI Express Configuration Request or Memory Read. The **VC0 Resource Status** and **VC1 Resource Status** registers can be read by either a PCI Express Enhanced Configuration access or Memory Read.
- The negotiated Link width of each Port, by reading the Port's **Link Status** register *Negotiated Link Width* field (offset 78h[25:20]). This register can be read by either a Configuration Request or Memory Read.

Table 18-7 describes the relationship of the LED On/Off patterns, as they relate to the Lane status indicated by PEX_LANE_GOOD[5, 4, 1, 0]#.

Table 18-7. PEX_LANE_GOOD[5, 4, 1, 0]# LED On/Off Patterns, by State

State	LED Pattern
Lane is disabled	Off
Lane is enabled, 5.0 GT/s	On
Lane is enabled, 2.5 GT/s, reduced Lanes are up	Blinking, 0.5 seconds On, 0.5 seconds Off

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Chapter 19 Electrical Specifications

19.1 Introduction

This chapter provides the PEX 8604 electrical specifications.

19.2 Power-Up/Power-Down Sequence

The PEX 8604 does not have power sequencing requirements. The power rails can be powered up and powered down, in any sequence.

19.3 Absolute Maximum Ratings

Warning: ***Maximum limits indicate the temperatures and voltages above which permanent damage can occur. Proper operation at these conditions is not guaranteed, and continuous operation of the PEX 8604 at these limits is not recommended.***

Table 19-1. Absolute Maximum Rating (All Voltages Referenced to VSS System Ground)

Item	Symbol	Absolute Maximum Rating	Units
I/O Interface Supply Voltage	VDD25	-0.5 to +3.6	V
PLL Supply Voltage	VDD25A	-0.5 to +3.6	V
Core (Logic) Supply Voltage	VDD10	-0.3 to +1.5	V
SerDes Analog Supply Voltage	VDD10A	-0.3 to +1.5	V
Input Voltage (2.5V Interface)	V_I	-0.3 to +3.6	V
Operating Ambient Temperature Commercial Industrial	T_A	 0 to +70 -40 to +85	 °C °C
Storage Temperature	T_{STG}	-65 to +150	°C

19.4 Power Characteristics

Table 19-2. Operating Condition Power Supply Rails

Symbol	Parameter	Min	Typ	Max	Units
VDD10	Digital Core Supply {1.0V ±5%}	0.95	1.0	1.05	V
VDD10A	Analog SerDes Supply {1.0V ±5%}	0.95	1.0	1.05	V
VDD25	I/O Supply {2.5V ±10%}	2.25	2.50	2.75	V
VDD25A	Phase-Locked Loop (PLL) Supply {2.5V ±10%}	2.25	2.50	2.75	V

19.5 Power Consumption Estimates

Table 19-3 and Table 19-4 list the PEX 8604 power consumption estimates at Gen 1 and Gen 2 Link speeds, respectively.

Table 19-3. PEX 8604 Gen 1 (2.5 GT/s) Power Consumption Estimates (Watts)

Lanes	Ports	Core Digital (VDD10) (Amps)		SerDes Analog (VDD10A) (Amps)		SerDes Digital (VDD10) (Amps)		PLL and I/O (VDD25A/VDD25) (Amps)		Total (Watts)	
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ[a]	Max[b, c]
4	4	0.83	1.83	0.17	0.27	0.03	0.06	0.02	0.03	1.10	2.34

a. Typical power based upon 35% traffic, all Lanes in active L0 Link PM state, typical power rails (1.0V/2.5V).

b. Maximum power based upon 85% traffic, idle Lanes in active L0s Link PM state, maximum power rails (1.05V/2.75V).

c. Maximum power is at high temperature and Fast/Fast (FF) process corner silicon.

Table 19-4. PEX 8604 Gen 2 (5.0 GT/s) Power Consumption Estimates (Watts)

Lanes	Ports	Core Digital (VDD10) (Amps)		SerDes Analog (VDD10A) (Amps)		SerDes Digital (VDD10) (Amps)		PLL and I/O (VDD25A/VDD25) (Amps)		Total (Watts)	
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ[a]	Max[b, c]
4	4	1.00	2.03	0.19	0.31	0.04	0.07	0.02	0.03	1.29	2.61

a. Typical power based upon 35% traffic, all Lanes in active L0 Link PM state, typical power rails (1.0V/2.5V).

b. Maximum power based upon 85% traffic, idle Lanes in active L0s Link PM state, maximum power rails (1.05V/2.75V).

c. Maximum power is at high temperature and Fast/Fast (FF) process corner silicon.

19.6 I/O Interface Signal Groupings

Table 19-5. Signal Group PCI Express Analog Interface

Signal Group	Signal Type	Signals	Notes
(a)	PCI Express Output (Transmit)	PEX_PETn[5, 4, 1, 0], PEX_PETp[5, 4, 1, 0]	Refer to Table 19-7 and Table 19-8
(b)	PCI Express Input (Receive)	PEX_PERn[5, 4, 1, 0], PEX_PERp[5, 4, 1, 0]	Refer to Table 19-7 and Table 19-9
(c)	PCI Express Differential Clock Input	PEX_REFCLKn, PEX_REFCLKp, PEX_REFCLK_CFCn, PEX_REFCLK_CFCp	Refer to Table 19-7 and Table 19-10
(d)	SerDes External Resistor	REXT_A[1:0], REXT_B[1:0]	1.43KΩ ±1%, and refer to Table 19-7

Table 19-6. Signal Group Digital Interface

Signal Group	Signal Type	Signals	Note
(e1)	Digital Input[a]	JTAG_TCK, JTAG_TDI, JTAG_TMS, JTAG_TRST#, STRAP_DEBUG_SEL0, STRAP_FAST_BRINGUP#, STRAP_NT_ENABLE#, STRAP_NT_UPSTRM_PORTSEL[3:0], STRAP_PLL_BYPASS#, STRAP_PORTCFG[1:0], STRAP_PROBE_MODE#, STRAP_RESERVED16, STRAP_RESERVED17#, STRAP_SERDES_MODE_EN#, STRAP_SSC_ISO_ENABLE#, STRAP_TESTMODE[3:0], STRAP_UPSTRM_PORTSEL[3:0]	Refer to Table 19-7
(e2)	Digital Input[a]	I2C_ADDR[2:0]	
(f)	Digital Input with Internal Pull-up Resistor	PEX_PERST#, SHPC_INT#, STRAP_NT_P2P_EN#, STRAP_SMBUS_EN#, STRAP_UPCFG_TIMER_EN#	
(g)	Digital Tri-State Output (8 mA)	EE_DI, FATAL_ERR#, JTAG_TDO, PEX_NT_RESET#, STRAP_SPARE0#	
(h)	Bidirectional with Internal Pull-up Resistor (8 mA Drive)	EE_CS#, EE_DO, EE_SK, GPIO[30, 29, 16:0], PEX_LANE_GOOD[5, 4, 1, 0]#, STRAP_SPARE1#	
(i)	Bidirectional (Open Drain) with Internal Pull-up Resistor	PEX_INTA#	
(j)	Bidirectional (Open Drain) Schmitt Trigger Input	I2C_SCL0, I2C_SCL1, I2C_SDA0, I2C_SDA1	

a. These signals must be pulled or tied High to VDD25 or Low to VSS (GND), per the instructions provided in Section 3.4, "Signal Ball Descriptions."

Table 19-7. Analog and Digital Interfaces (All Signal Groups) – DC Electrical Characteristics

Symbol	Signal Group	Parameter	Min	Typ	Max	Unit	Conditions
I_{OL}	(g) (h) (i) (j)	Output Low Current	13	22	32	mA	V_{OLmax} = 0.7V
I_{OH}	(g) (h)	Output High Current	8	16	27	mA	V_{OHmin} = 1.7V
V_{IL}	(e1) (e2) (f) (h) (i) (j)	Input Low Voltage	-0.3		0.7	V	
V_{IH}	(e1) (e2) (f) (h) (i) (j)	Input High Voltage	1.7		2.8	V	Refer to Note 1.
V_T	(e1) (e2) (h) (i)	Threshold Point	0.97	1.05	1.14	V	
C_{PIN}	(a) (b) (c) (d) (e1) (e2) (f) (g) (h) (i) (j)	Ball Capacitance			5	pF	
$I_{LEAKAGE}$	(g)	Tri-State Leakage			±10	µA	
	(e1) (f)	Input Leakage			±10	µA	
	(e2)	Input Leakage	-22.6		-47.5	µA	
	(f) (h) (i)	Pull-Up Leakage	-22.6		-47.5	µA	
R_{PU}	(f) (h) (i)	Pull-Up Impedance	74K	111K	178K	Ω	
V_T	(j)	Schmitt Trigger Rising Threshold	1.2	1.3	1.4	V	
		Schmitt Trigger Falling Threshold	0.84	0.93	1.01	V	
V_{HYS}	(j)	Input Hysteresis	360	370	390	mV	

Note:

1. *The specified maximum V_{IH} is for recommended operating conditions. Because these I/O buffers are 3.3V tolerant, a maximum V_{IH} of 3.6V can safely be applied to these signal balls.*

Table 19-8. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm. UI does not account for variations caused by Spread-Spectrum Clock (SSC). Refer to Note 1.
$V_{TX-DIFF-PP}$	Differential Peak-to-Peak Output Voltage	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Measured with compliance test load. $V_{TX-DIFF-PP} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
$V_{TX-DIFF-PP-LOW}$	Low Power Differential Peak-to-Peak Output Voltage	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	Measured with compliance test load. $V_{TX-DIFF-PP-LOW} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ Must be implemented with no de-emphasis.
$V_{TX-DE-RATIO-3.5dB}$	Tx De-Emphasis Level Ratio	3.0 (min) 4.0 (max)	3.0 (min) 4.0 (max)	dB	Ratio of the $V_{TX-DIFF-PP}$ of the 2nd and following bits after a transition, divided by the $V_{TX-DIFF-PP}$ of the 1st bit after a transition. Refer to Note 2.
$V_{TX-DE-RATIO-6dB}$	Tx De-Emphasis Level Ratio	N/A	5.5 (min) 6.5 (max)	dB	Ratio of the $V_{TX-DIFF-PP}$ of the 2nd and following bits after a transition, divided by the $V_{TX-DIFF-PP}$ of the 1st bit after a transition. Refer to Note 2.
$T_{MIN-PULSE}$	Instantaneous Pulse Width (including all jitter sources)	Not specified	0.9 (min)	UI	Measured relative to rising/falling pulse. Refer to Note 3.
T_{TX-EYE}	Minimum Tx Eye Width	0.75 (min)	0.75 (min)	UI	Does not include SSC nor REFCLK jitter. Includes Rj at 10^{-12}. Refer to Notes 3 and 4.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	0.125 (max)	Not specified	UI	Measured differentially at zero crossing points, after applying the 2.5 GT/s Clock Recovery function. Refer to Note 3.
$T_{TX-HF-DJ-DD}$	Tx Deterministic Jitter > 1.5 MHz	Not specified	0.15 (max)	UI	Deterministic jitter only. Refer to Note 3.
$T_{TX-LF-RMS}$	Tx RMS Jitter < 1.5 MHz	Not specified	3.0	ps RMS	Total energy measured over a 10-kHz to 1.5-MHz range.
$T_{TX-RISE-FALL}$	Tx Rise and Fall Time	0.125 (min)	0.15 (min)	UI	Measured differentially from 20 to 80% of swing. Refer to Note 3.
$T_{RF-MISMATCH}$	Tx Rise/Fall Mismatch	Not specified	0.1 (max)	UI	Measured from 20 to 80% differentially. Refer to Note 3.

Table 19-8. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
BW_{TX-PLL}	Maximum Tx PLL Bandwidth	22 (max)	16 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 5.
$BW_{TX-PLL-LO-3DB}$	Minimum Tx PLL Bandwidth for 3-dB Peaking	1.5 (min)	8 (min)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Notes 5 and 7.
$BW_{TX-PLL-LO-1DB}$	Minimum Tx PLL Bandwidth for 1-dB Peaking	Not specified	5 (min)	MHz	
$PKG_{TX-PLL1}$	TX PLL Peaking with 8-MHz Minimum Bandwidth	Not specified	3.0 (max)	dB	
$PKG_{TX-PLL2}$	TX PLL peaking with 5-MHz Minimum Bandwidth	Not specified	1.0 (max)	dB	Refer to Note 7.
$RL_{TX-DIFF}$	TX Differential Return Loss (Package + Silicon)	10 (min)	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz	dB	
RL_{TX-CM}	TX Common Mode Return Loss (Package + Silicon)	6 (min)	6 (min)	dB	S_{11} parameter. 2.5 GT/s – Measured over 0.05- to 1.25-GHz range. 5.0 GT/s – Measured over 0.05- to 2.5-GHz range.
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80 (min) 120 (max)	120 (max)	Ω	Tx DC Differential mode low impedance. Parameter is captured for 5.0 GHz by $RL_{TX-DIFF}$.
$V_{TX-CM-AC-PP}$	Tx AC Common Mode Voltage (5.0 GT/s)	Not specified	100 (max)	mVPP	Refer to Note 6.
$V_{TX-CM-AC-P}$	Tx AC Common Mode Voltage (2.5 GT/s)	20 (max)	Not specified	mVPP	Refer to Note 6.
$I_{TX-SHORT}$	Tx Short Circuit Current Limit	90 (max)	90 (max)	mA	Total current the Transmitter can provide when shorted to its ground.
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage	0 (min) 3.6 (max)	0 (min) 3.6 (max)	V	Allowed DC common mode voltage, under any conditions.

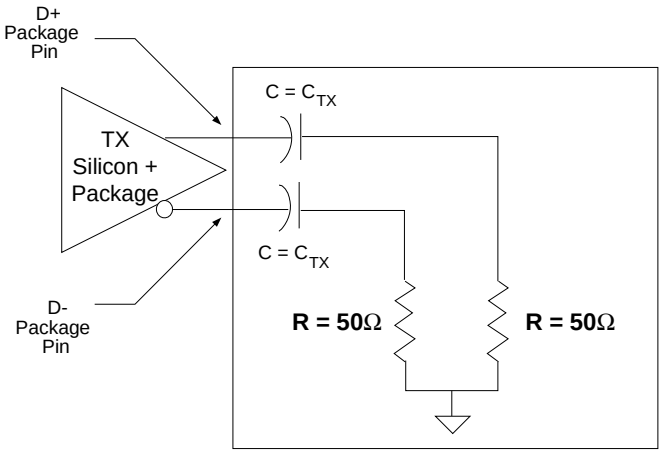
Table 19-8. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 Link PM state and Electrical Idle	0 (min) 100 (max)	0 (min) 100 (max)	mV	$\lvert V_{TX-CM-DC}$ [during L0] - $V_{TX-CM-Idle-DC}$ [during Electrical Idle]$\rvert \leq 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert$ / 2 [L0] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert$ / 2 [Electrical Idle]
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0 (min) 25 (max)	0 (min) 25 (max)	mV	$\lvert V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\rvert \leq 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\lvert V_{TX-D+}\rvert$ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\lvert V_{TX-D-}\rvert$
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Peak Output Voltage	0 (min) 20 (max)	0 (min) 20 (max)	mV	$V_{TX-IDLE-DIFFp} = \lvert V_{TX-Idle-D+} - V_{TX-Idle-D-}\rvert \leq 20$ mV Voltage must be high-pass filtered, to remove any DC component.
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Peak Output Voltage	Not specified	0 (min) 5 (max)	mV	$V_{TX-IDLE-DIFF-DC} = \lvert V_{TX-Idle-D+} - V_{TX-Idle-D-}\rvert \leq 5$ mV Voltage must be high-pass filtered, to remove any AC component.
$V_{TX-RCV-DETECT}$	Amount of Voltage Change Allowed during Receiver Detection	600 (max)	600 (max)	mV	Total amount of voltage change that a Transmitter can apply, to sense whether a low-impedance Receiver is present.
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	20 (min)	20 (min)	ns	Minimum time a Transmitter must be in Electrical Idle. Used by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle Ordered-Set (EIOS).
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum Time to Transition to a Valid Electrical Idle after Sending an Electrical Idle Ordered-Set	8 (max)	8 (max)	ns	After sending the required EIOS, the Transmitter must meet all Electrical Idle specifications within this time. This is measured from the end of the last UI of the last EIOS to the Tx in Electrical Idle.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum Time to Transition to Valid Differential Signaling after Leaving Electrical Idle	8 (max)	8 (max)	ns	Maximum time to transition to valid differential signaling, after leaving Electrical Idle. This is considered a de-bounce time to the Tx.
$T_{CROSSLINK}$	Cross-Link Random Timeout	1.0 (max)	1.0 (max)	ms	Random timeout that helps resolve potential conflicts in the cross-link configuration.
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	500 ps + 2 UI (max)	500 ps + 4 UI (max)	ps	Static skew between any two Lanes within a single Transmitter.
C_{TX}	AC-Coupling Capacitor	75 (min) 200 (max)	75 (min) 200 (max)	nF	All Transmitters shall be AC-coupled. The AC coupling is required either within the media, or within the transmitting component itself.

Notes:

1. *SSC permits a +0, -5,000 ppm modulation of the clock frequency, at a modulation rate not to exceed 33 kHz.*
2. *Specified at the measurement point into a timing and voltage compliance test load, as illustrated in Figure 19-1.*

Figure 19-1. Compliance Test/Measurement Load



3. *Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurements at 5.0 GT/s must de-convolve effects of the compliance test board, to yield an effective measurement at the Tx balls. 2.5 GT/s can be measured within 200 mils of the Tx device's balls; however, de-convolution is recommended. At least 10^6 UI of data must be acquired.*
4. *Transmitter jitter is measured by driving the Tx under test with a low jitter "ideal" clock and connecting the device under test (DUT) to a reference load.*
5. *The Tx PLL bandwidth must lie between the minimum and maximum ranges listed in Table 19-8. PLL peaking must lie below the values listed in Table 19-8.*

   The PLL bandwidth extends from zero (0) up to the value(s) specified in Table 19-8.
6. *Measurement is made over at least 10^6 UI.*
7. *A single combination of PLL bandwidth and peaking is specified for 2.5 GT/s implementations. For 5.0 GT/s, two 20 combinations of PLL bandwidth and peaking are specified to permit designers to make a tradeoff between the two parameters. If the PLL's minimum bandwidth is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's minimum bandwidth is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. In both cases, the maximum PLL bandwidth is 16 MHz.*

Table 19-9. 2.5 and 5.0 GT/s PCI Express Receiver (Signal Group b) – AC and DC Characteristics

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	UI does not account for variations caused by SSC.
$V_{RX-DIFF-PP-CC}$	Differential Rx Peak-to-Peak Voltage for Common REFCLK Rx Architecture	0.175 (min) 1.2 (max)	0.120 (min) 1.2 (max)	V	$V_{RX-DIFF-PP} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$
T_{RX-EYE}	Receiver Eye Time Opening	0.40 (min)	N/A	UI	Minimum eye time at Rx pins to yield a 10^{-12} Bit Error Rate. Receiver eye margins are defined into a 2 x 50Ω reference load.
$T_{RX-TJ-CC}$	Maximum Rx Inherent Timing Error	N/A	0.40 (max)	UI	Maximum Rx inherent total timing error for common REFCLK Rx architecture. Refer to Note 1.
$T_{RX-DJ-DD-CC}$	Maximum Rx Inherent Deterministic Timing Error	N/A	0.30 (max)	UI	Maximum Rx inherent deterministic timing error for common REFCLK Rx architecture. Refer to Note 1.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Delta between the Median and Deviation from the Median	0.3 (max)	Not specified	UI	
$T_{RX-MIN-PULSE}$	Minimum Width Pulse at Rx	Not specified	0.6 (min)	UI	Measured to account for worst Tj at 10^{-12} Bit Error Rate.
$V_{RX-MAX-MIN-RATIO}$	Minimum/ Maximum Pulse Voltage on Consecutive UI	Not specified	5 (max)	Ratio	Rx eye must simultaneously meet V_{RX-EYE} limits.
$BW_{RX-PLL-HI}$	Maximum Rx PLL Bandwidth	22 (max)	16 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 2.
$BW_{RX-PLL-LO-3DB}$	Minimum Rx PLL Bandwidth for 3-dB Peaking	1.5 min	8 (min)	MHz	
$BW_{RX-PLL-LO-1DB}$	Minimum Rx PLL Bandwidth for 1-dB Peaking	Not specified	5 (min)	MHz	
$PKG_{RX-PLL1}$	Rx PLL Peaking with 8-MHz Minimum Bandwidth	Not specified	3.0	dB	
$PKG_{RX-PLL2}$	Rx PLL Peaking with 5-MHz Minimum Bandwidth	Not specified	1.0	dB	

Table 19-9. 2.5 and 5.0 GT/s PCI Express Receiver (Signal Group b) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$RL_{RX-DIFF}$	Rx Differential Return Loss (Package + Silicon)	10 (min)	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz	dB	Refer to Note 3.
RL_{RX-CM}	Common Mode Return Loss	6 (min)	6 (min)	dB	Refer to Note 3.
Z_{RX-DC}	Rx DC Single-Ended Impedance	40 (min) 60 (max)	40 (min) 60 (max)	Ω	Required Rx D+ and D- DC impedance (50Ω ±20% tolerance). Refer to Note 4.
$Z_{RX-DIFF-DC}$	DC Differential Rx Impedance	80 (min) 120 (max)	Not specified	Ω	Rx DC Differential mode impedance. Parameter is captured for 5.0 GHz by $RL_{RX-DIFF}$. Refer to Note 4.
$V_{RX-CM-AC-P}$	Rx AC Common Mode Voltage	150 (max)	150 (max)	mVP	Measured at Rx pins, into a pair of 50Ω terminations into Ground. Refer to Note 5.
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input Common Mode Input Impedance for Voltage >0 during Reset or Power-Down	50K (min)	50K (min)	Ω	Rx DC common mode impedance with the Rx terminations not powered, measured over the range 0 to 200 mV (with respect to Ground). Refer to Note 6.
$Z_{RX-HIGH-IMP-DC-NEG}$	DC Input Common Mode Input Impedance for Voltage <0 during Reset or Power-Down	1.0K (min)	1.0K (min)	Ω	Rx DC common mode impedance with the Rx terminations not powered, measured over the range -150 to 0 mV (with respect to Ground). Refer to Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65 (min) 175 (max)	65 (min) 175 (max)	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the Receiver's package pins.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Idle Detect Threshold Integration Time	10 (max)	10 (max)	ms	An un-expected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Total Lane-to-Lane Skew	20 (max)	8 (max)	ns	Across all Lanes on a Port. Includes variation in the length of a SKIP Ordered-Set at the Rx, as well as any delay differences arising from the interconnect itself. Refer to Note 7.

Notes:

1. *The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.*
2. *Two combinations of PLL bandwidth and peaking are specified at 5.0 GT/s, to permit designers to make trade-offs between the two parameters. If the PLL's minimum bandwidth is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's minimum bandwidth is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met.*

   A PLL bandwidth extends from zero up to the value(s) defined as the minimum or maximum in Table 19-9. For 2.5 GT/s, a single PLL bandwidth and peaking value of 1.5 to 22 MHz and 3.0 dB are defined.
3. *Measurements must be made for both common mode and differential return loss. In both cases, the DUT must be powered up and DC-isolated, and its D+/D- inputs must be in the low-Z state.*
4. *The Rx DC single-ended impedance must be present when the Receiver terminations are first enabled, to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately, and the Rx single-ended impedance (constrained by RL_{RX-CM} to 50Ω ± 20%) must be within the specified range by the time Detect is entered.*
5. *Common mode peak voltage is defined by the expression:*

   $max\{|(Vd+ - Vd-) - V\text{-}CMDC|\}$
6. *$Z_{RX-HIGH-IMP-DC-NEG}$ and $Z_{RX-HIGH-IMP-DC-POS}$ are defined, respectively, for negative and positive voltages at the input of the Receiver. Transmitter designers must comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.*
7. *The $L_{RX-SKEW}$ parameter exists to handle repeaters that re-generate REFCLK and introduce differing numbers of skips on different Lanes.*

Table 19-10. PCI Express Differential Clock (Signal Group c) – AC and DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{REFCLK}	Reference Clock Frequency		100		MHz	1
$T_{REFCLK-HF-RMS}$	High frequency jitter -> 1.5 MHz to Nyquist RMS jitter after applying filter functions, per the *PCI Express Base r2.0*			3.1	ps RMS	
$T_{REFCLK-LF-RMS}$	Low frequency jitter – 10 kHz to 1.5 MHz jitter after applying filter functions, per the *PCI Express Base r2.0*			3.0	ps RMS	
$T_{REFCLK-SSC-RES}$	SSC residual after applying filter functions, per the *PCI Express Base r2.0*			75	ps	
V_{SW}	Differential Voltage Swing (0-to-peak)	125	200	800	mV	
	Differential Voltage Swing (peak-to-peak)	250	400	1,600	mV	
T_R/T_F	Clock Input Rise/Fall Time	0.6		4.0	V/ns	2
DC_{REFCLK}	Input Clock Duty Cycle	45	50	55	%	
R_{TERM}	Input Parallel Termination (Single-ended)		50		Ω	
	Input Parallel Termination (Differential)		100		Ω	
PPM	Reference Clock Tolerance	-300		+300	ppm	

Notes:

1. *PEX_REFCLKn/p must be AC-coupled. Use a 0.01 to 0.1 µF capacitor.*
2. *Specified at 20 to 80% points at the package balls.*

19.7 Transmit Drive Characteristics

The Drive Current and Transmit Equalization functions are programmable, to allow for optimization of different backplane lengths and materials.

The Transmit Drive Level is programmable (5-bit, per SerDes/Lane), to provide differential swing within the range listed in Table 19-11. The **SerDes Drive Level *x*** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets B98h and BA0h) provide access to all 4 Lanes for Drive Level programmability.

The Transmitter also incorporates programmable (5-bit, per SerDes/Lane) de-emphasis, to provide equalization to compensate for FR4 channel effects within the range listed in Table 19-11. The **Post-Cursor Emphasis Level *x*** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets BA8h and BB0h) provide access to all 4 Lanes for de-emphasis programmability.

The Transmit_Drive_Level[4:0] and Post-Cursor_Emphasis_Level[4:0] bits are used together to program the differential swing, as well as the dB loss for optimum Tx drive across the intended backplane.

Table 19-11 lists all possible combinations of Tx DRV_LVL[4:0] and POST_CURSOR[4:0], to achieve minimum 800 mV transition amplitude and the resulting de-emphasis (in decibels, dB). Of these, only certain combinations yield the specified 3 to 4 dB or 5.5 to 6.5 dB de-emphasis, per the *PCI Express Base r2.0* (**highlighted in bold**). All combinations are listed, however, to provide maximum flexibility for fine-tuning the Tx drive characteristics to a specific backplane.

Table 19-11. Tx Programmable Drive and De-Emphasis Levels

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
01h	11h	820	789	0.34	
	12h	849	818	0.33	
	13h	876	845	0.31	
02h	10h	799	742	0.65	
	11h	830	773	0.61	
	12h	858	802	0.58	
	13h	884	829	0.56	
03h	10h	809	727	0.93	
	11h	839	758	0.88	
	12h	867	787	0.84	
	13h	893	814	0.80	
04h	10h	818	712	1.22	
	11h	848	743	1.15	
	12h	876	772	1.09	
	13h	901	799	1.04	

Table 19-11. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
05h	0Fh	797	664	1.59	
	10h	828	697	1.50	
	11h	857	728	1.41	
	12h	884	758	1.34	
	13h	909	785	1.27	
	1Fh	796	663	1.59	
06h	0Fh	806	649	1.88	
	10h	837	682	1.77	
	11h	866	714	1.68	
	12h	892	743	1.59	
	13h	916	770	1.51	
	1Fh	806	649	1.88	
07h	0Fh	816	635	2.18	
	10h	846	668	2.05	
	11h	874	700	1.94	
	12h	900	729	1.83	
	13h	924	756	1.74	
	1Fh	816	635	2.18	
08h	0Fh	825	620	2.48	
	10h	855	654	2.33	
	11h	883	685	2.20	
	12h	908	715	2.08	
	13h	931	742	1.98	
	1Fh	825	620	2.47	
09h	0Eh	802	571	2.95	
	0Fh	834	607	2.77	
	10h	863	640	2.60	
	11h	891	671	2.46	
	12h	916	701	2.33	
	13h	938	728	2.21	
	1Eh	802	571	2.96	
	1Fh	834	606	2.77	

Table 19-11. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
0Ah	0Eh	811	557	3.27	
	0Fh	843	593	3.06	
	10h	872	626	2.88	
	11h	899	658	2.71	
	12h	923	687	2.57	
	13h	945	714	2.43	
	1Eh	811	557	**3.27**	
	1Fh	843	593	**3.06**	
0Bh	0Eh	821	543	**3.58**	
	0Fh	851	579	**3.35**	
	10h	880	612	**3.15**	
	11h	906	644	2.97	
	12h	930	673	2.81	
	13h	951	700	2.66	
	1Eh	820	543	**3.58**	
	1Fh	851	579	**3.35**	
0Ch	0Dh	797	492	4.19	
	0Eh	829	530	**3.89**	
	0Fh	860	566	**3.64**	
	10h	888	599	**3.42**	
	11h	914	630	**3.22**	
	12h	937	660	**3.05**	
	13h	958	687	2.89	
	1Dh	797	492	4.19	
	1Eh	829	530	**3.89**	
	1Fh	860	565	**3.64**	
0Dh	0Dh	806	479	4.52	
	0Eh	838	517	4.20	
	0Fh	868	552	**3.93**	
	10h	896	586	**3.69**	-3.5 dB default for PEX 8604
	11h	921	617	**3.48**	
	12h	944	646	**3.29**	
	13h	964	673	**3.11**	
	1Dh	806	479	4.52	
	1Eh	838	516	4.20	
	1Fh	868	552	**3.93**	

Table 19-11. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
0Eh	0Dh	815	466	4.86	
	0Eh	847	503	4.51	
	0Fh	876	539	4.22	
	10h	903	572	**3.96**	
	11h	928	604	**3.73**	
	12h	950	633	**3.53**	
	13h	970	660	**3.34**	
	1Dh	815	466	4.86	
	1Eh	846	503	4.52	
	1Fh	876	539	4.22	
0Fh	0Dh	824	453	5.20	
	0Eh	855	490	4.83	
	0Fh	884	526	4.51	
	10h	911	559	4.23	
	11h	935	591	**3.98**	
	12h	957	620	**3.76**	
	13h	975	647	**3.56**	
	1Dh	823	453	5.20	
	1Eh	855	490	4.83	
	1Fh	884	526	4.51	
10h	0Ch	799	399	**6.02**	
	0Dh	832	439	**5.55**	
	0Eh	863	477	5.15	
	0Fh	892	513	4.81	
	10h	918	546	4.51	
	11h	942	578	4.25	
	12h	963	607	4.01	
	13h	981	634	3.79	
	1Ch	799	399	**6.02**	
	1Dh	832	439	**5.55**	
	1Eh	863	477	5.15	
	1Fh	892	513	4.81	

Table 19-11. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
11h	0Ch	808	387	**6.40**	
	0Dh	841	427	**5.89**	
	0Eh	871	464	5.46	
	0Fh	899	500	5.10	
	10h	925	533	4.78	
	11h	948	565	4.50	
	12h	969	594	4.24	
	13h	986	621	4.02	
	1Ch	808	387	**6.40**	
	1Dh	840	427	**5.89**	
	1Eh	871	464	5.46	
	1Fh	899	500	5.10	
12h	0Ch	816	374	6.77	
	0Dh	849	414	**6.23**	
	0Eh	879	452	**5.78**	
	0Fh	906	487	5.39	
	10h	932	521	5.05	
	11h	954	552	4.75	
	12h	974	582	4.48	
	13h	991	609	4.24	
	1Ch	816	374	6.78	
	1Dh	849	414	6.23	
	1Eh	879	452	5.78	
	1Fh	906	487	5.39	
13h	0Ch	825	362	7.16	
	0Dh	857	402	6.58	
	0Eh	886	439	6.09	
	0Fh	913	475	5.68	
	10h	938	509	5.32	
	11h	960	540	5.00	
	12h	980	569	4.72	
	13h	996	596	4.46	
	1Bh	795	326	7.76	
	1Ch	825	362	7.16	
	1Dh	856	402	6.58	
	1Eh	886	439	**6.09**	
	1Fh	913	475	**5.68**	

Table 19-11. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
14h	0Bh	799	308	8.29	
	0Ch	833	350	7.54	
	0Dh	864	389	6.93	
	0Eh	893	427	**6.41**	
	0Fh	920	463	**5.97**	
	10h	944	496	**5.59**	
	11h	966	528	5.25	
	12h	985	557	4.95	
	13h	1,001	584	4.68	
	1Bh	804	313	8.19	
	1Ch	833	349	7.54	
	1Dh	864	389	6.93	
	1Eh	893	427	**6.41**	
	1Fh	920	463	**5.97**	
15h	0Bh	808	296	8.73	
	0Ch	841	337	7.93	
	0Dh	872	377	7.28	
	0Eh	901	415	6.73	-6 dB default for PEX 8604
	0Fh	927	451	**6.26**	
	10h	950	484	**5.86**	
	11h	972	516	**5.50**	
	12h	990	545	5.19	
	13h	1,006	572	4.90	
	1Bh	812	301	8.62	
	1Ch	841	337	7.93	
	1Dh	872	377	7.28	
	1Eh	900	415	6.73	
	1Fh	927	451	**6.62**	

Table 19-11. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
16h	0Bh	816	284	9.18	
	0Ch	849	326	8.32	
	0Dh	879	365	7.63	
	0Eh	907	403	7.05	
	0Fh	933	439	6.56	
	10h	956	472	**6.13**	
	11h	977	504	**5.76**	
	12h	995	533	5.42	
	13h	1,010	560	5.12	
	1Bh	820	289	9.05	
	1Ch	849	325	8.33	
	1Dh	879	365	7.63	
	1Eh	907	403	7.05	
	1Fh	933	439	6.56	
17h	0Bh	824	272	9.63	
	0Ch	856	314	8.72	
	0Dh	886	354	7.98	
	0Eh	914	391	7.37	
	0Fh	939	427	6.85	
	10h	962	460	**6.40**	
	11h	982	492	**6.01**	
	12h	999	521	**5.65**	
	13h	1,014	548	5.34	
	1Bh	828	277	9.50	
	1Ch	856	314	8.72	
	1Dh	886	353	7.99	
	1Eh	914	391	7.37	
	1Fh	939	427	6.85	

Table 19-11. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
18h	0Ah	798	216	11.35	
	0Bh	832	260	10.10	
	0Ch	864	302	9.13	
	0Dh	893	342	8.35	
	0Eh	921	380	7.70	
	0Fh	945	415	7.15	
	10h	968	449	6.68	
	11h	987	480	**6.26**	
	12h	1,004	509	**5.89**	
	13h	1,018	537	**5.56**	
	1Ah	802	222	11.16	
	1Bh	836	266	9.96	
	1Ch	864	302	9.13	
	1Dh	893	342	8.35	
	1Eh	921	379	7.70	
	1Fh	945	415	7.15	
19h	0Ah	806	204	11.91	
	0Bh	840	249	10.57	
	0Ch	871	290	9.54	
	0Dh	900	330	8.71	
	0Eh	927	368	8.02	
	0Fh	951	404	7.45	
	10h	973	437	6.95	
	11h	992	469	6.51	
	12h	1,008	498	**6.12**	
	13h	1,021	525	**5.78**	
	1Ah	810	210	11.71	
	1Bh	844	254	10.42	
	1Ch	871	290	9.54	
	1Dh	900	330	8.71	
	1Eh	927	368	8.03	
	1Fh	951	404	7.45	

Table 19-11. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
1Ah	0Ah	814	193	12.49	
	0Bh	847	237	11.05	
	0Ch	878	279	9.95	
	0Dh	907	319	9.08	
	0Eh	933	357	8.35	
	0Fh	957	392	7.74	
	10h	978	426	7.22	
	11h	996	457	6.76	
	12h	1,012	487	**6.36**	
	13h	1,025	514	**6.00**	
	1Ah	818	199	12.28	
	1Bh	851	243	10.89	
	1Ch	878	279	9.96	
	1Dh	907	319	9.08	
	1Eh	933	357	8.35	
	1Fh	957	392	7.74	
1Bh	0Ah	821	182	13.09	
	0Bh	854	226	11.55	
	0Ch	885	268	10.38	
	0Dh	913	308	9.45	
	0Eh	939	346	8.68	
	0Fh	962	381	8.04	
	10h	983	415	7.50	
	11h	1,000	446	7.01	
	12h	1,016	475	6.59	
	13h	1,028	503	**6.22**	
	1Ah	826	188	12.86	
	1Bh	858	232	11.38	
	1Ch	885	268	10.38	
	1Dh	913	308	9.45	
	1Eh	939	345	8.69	
	1Fh	962	381	8.04	

Table 19-11. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
1Ch	0Ah	829	171	13.71	
	0Bh	861	215	12.06	
	0Ch	892	257	10.81	
	0Dh	919	297	9.82	
	0Eh	945	334	9.02	
	0Fh	967	370	8.35	
	10h	987	404	7.77	
	11h	1,004	435	7.27	
	12h	1,019	464	6.83	
	13h	1,031	491	**6.44**	
	19h	799	131	15.71	
	1Ah	833	177	13.46	
	1Bh	865	221	11.87	
	1Ch	891	257	10.81	
	1Dh	919	297	9.83	
	1Eh	944	334	9.02	
	1Fh	967	370	8.35	
1Dh	09h	802	114	16.95	
	0Ah	836	160	14.36	
	0Bh	868	204	12.58	
	0Ch	898	246	11.25	
	0Dh	925	286	10.20	
	0Eh	950	324	9.36	
	0Fh	972	359	8.65	
	10h	992	393	8.05	
	11h	1,008	424	7.52	
	12h	1,022	454	7.06	
	13h	1,034	481	6.65	
	19h	806	120	16.55	
	1Ah	841	166	14.09	
	1Bh	872	210	12.38	
	1Ch	898	246	11.25	
	1Dh	925	286	10.21	
	1Eh	950	323	9.36	
	1Fh	972	359	8.65	

Table 19-11. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
1Eh	09h	809	103	17.90	
	0Ah	843	149	15.04	
	0Bh	875	193	13.11	
	0Ch	904	235	11.69	
	0Dh	931	275	10.59	
	0Eh	955	313	9.69	
	0Fh	977	349	8.95	
	10h	996	382	8.32	
	11h	1,012	413	7.77	
	12h	1,025	443	7.29	
	13h	1,037	470	6.87	
	19h	814	109	17.44	
	1Ah	848	155	14.74	
	1Bh	879	199	12.90	
	1Ch	904	235	11.70	
	1Dh	931	275	10.59	
	1Eh	955	313	9.70	
	1Fh	977	348	8.95	
1Fh	09h	817	93	18.91	
	0Ah	850	139	15.75	
	0Bh	881	183	13.66	
	0Ch	910	225	12.15	
	0Dh	936	265	10.98	
	0Eh	960	302	10.04	
	0Fh	981	338	9.26	
	10h	999	371	8.60	
	11h	1,015	403	8.03	
	12h	1,028	432	7.53	
	13h	1,039	459	7.09	
	19h	821	99	18.40	
	1Ah	854	145	15.43	
	1Bh	885	188	13.44	
	1Ch	910	225	12.15	
	1Dh	936	264	10.98	
	1Eh	960	302	10.04	
	1Fh	981	338	9.26	

19.7.1 Default Transmit Settings

Table 19-12 lists the default values of the Transmit Drive and Post-Cursor De-Emphasis levels (**SerDes Drive Level *x*** and **Post-Cursor Emphasis Level *x*** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets B98h and BA0h, and offsets BA8h and BB0h, respectively)).

Table 19-12. Default Transmit Settings

Mode (dB)	Link Speed (GT/s)	DRV_LVL [4:0]	POST_CURSOR [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	Equalization[a] (dB)
-3.5	2.5	10h	0Dh	896	586	-3.69
-6	5.0	0Eh	15h	901	415	-6.73[b]

a. dB Equalization formula:

```
20 x log[(Non-Transition Amplitude) / (Transition Amplitude)]
```

b. The -6 dB Setting is slightly larger than the maximum -6.5 dB specification, to better compensate for FR4 loss characteristics across a typical backplane application.

19.8 Receive Characteristics

The Receiver circuit includes programmable equalization, to further compensate for the low-pass FR4 loss characteristics of the channel.

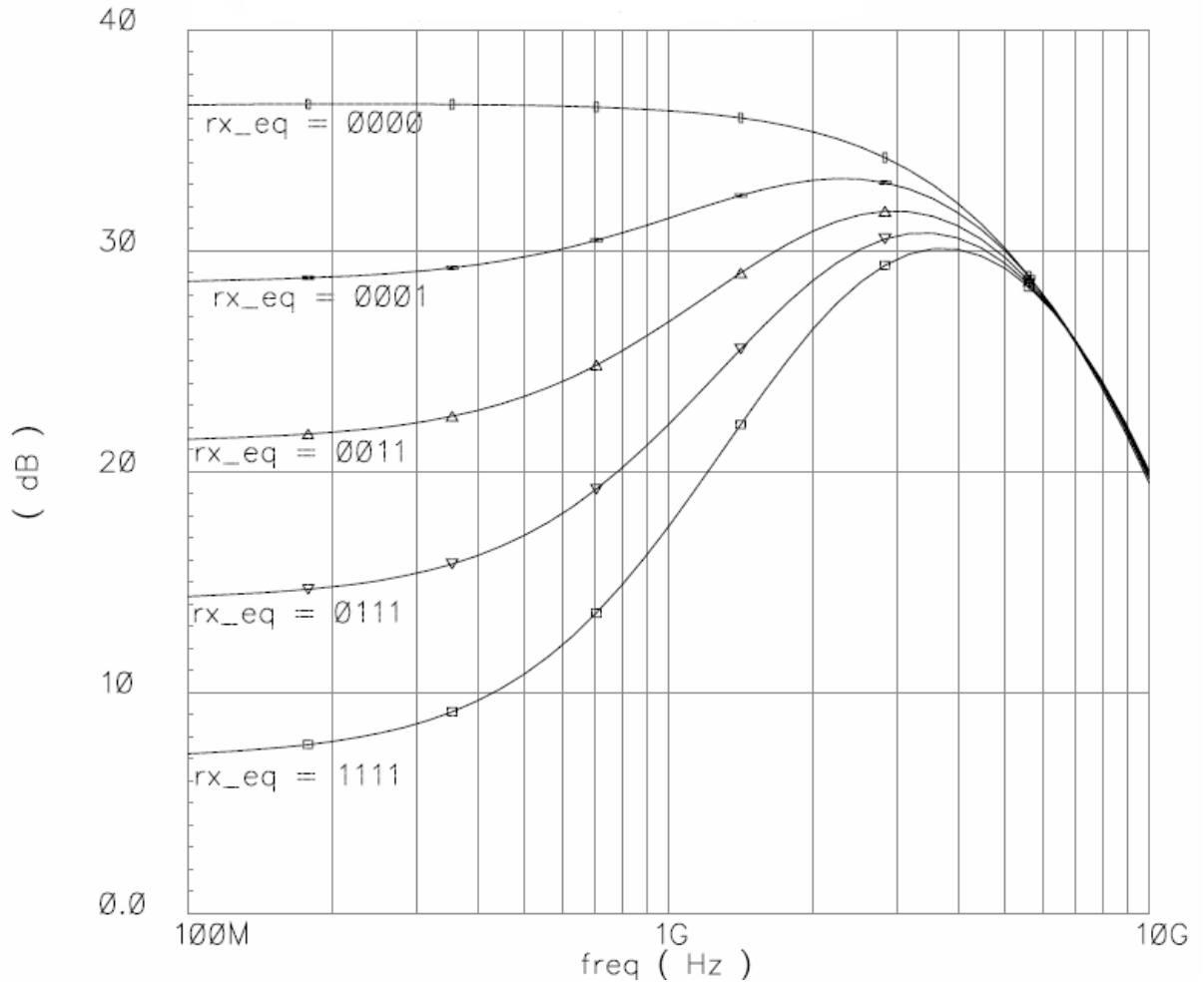
19.8.1 Receive Equalization

Table 19-13 lists the programmable bits used for controlling the Receiver circuit's electrical characteristics, to mitigate the effects of signal loss and distortion across the PCB channel. The **Receiver Equalization Level *x*** registers (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offsets BB8h and BBCh) provide access to all 4 Lanes for Rx Equalization programmability. Figure 19-2 illustrates the Rx Equalization frequency characteristics.

Table 19-13. Receiver Equalization Settings

Rx Equalization[3:0]	Equalization
0h (default)	Off
1h	Minimum
2h to 3h	Low
4h to 6h	Low to Medium
7h to 9h	Medium
Ah to Dh	High to Medium
Eh to Fh	Maximum

Figure 19-2. Rx Equalization Frequency Characteristics



19.8.2 Receiver Electrical Idle

The Receiver circuit contains a signal detect circuit that is used to detect signal idling at the input. The threshold to detect the idle level is programmable, using the **Signal Detect Level** register (Port 0, and also the NT Port Virtual Interface if Port 0 is a Legacy NT Port, offset BC0h). A value of 00b provides the lowest signal voltage level detection threshold.

Chapter 20 Thermal and Mechanical Specifications

20.1 Thermal Characteristics

The PEX 8604 does not include a heat sink. The information described in this section is based upon sample thermal performance when a heat sink is used with the PEX 8604, and is provided for reference only.

20.1.1 Sample Thermal Data

Table 20-1 lists sample thermal data for the PEX 8604 at Commercial temperature, as well as a recommendation for Industrial Temperature Range support.

Table 20-1. Sample Thermal Data (15 x 15 mm^2 PBGA Package)[a, b]

Maximum Power (Watts)[c]	Heat Sink (Yes/No)	Airflow Velocity (m/s)	Θ_{JA} (°C/W)		Θ_{JC} (°C/W)	Heat SInk
			4-Layer JEDEC Board	8-Layer JEDEC Board		
2.61	No	0	20.45	14.37	6.12	N/A
		1	18.34	13.08		
		2	17.50	12.63		
	Yes	0	17.92	13.13		15 x 15 mm^2 and 10-mm-height heat sink, TIM chomerics T412, 0.23-mm thick and 1.41 W/mK Thermal conductivity[d]
		1	13.85	10.73		
		2	12.69	10.08		
		1	N/A	11.8		19 x 19 x 25 Alpha N19-25B, 8 x 8 thermal balls[e]
		2		8.6		

a. *The Maximum Operating Junction Temperature is 110°C. The Maximum Junction Temperature for Reliability is 125°C.*

b. *The shaded fields provide a recommendation that allows the PEX 8604 to support Industrial Temperature Range (-40 to +85°C).*

c. *The maximum power value listed assumes the conditions listed in Chapter 19, "Electrical Specifications," at Gen 2 (5.0 GT/s).*

d. *Heat Sink Part Number: Alpha Novatech W15-10W.*

e. *Heat Sink Part Number: Alpha Novatech N19-25W.*

20.2 General Package Specifications

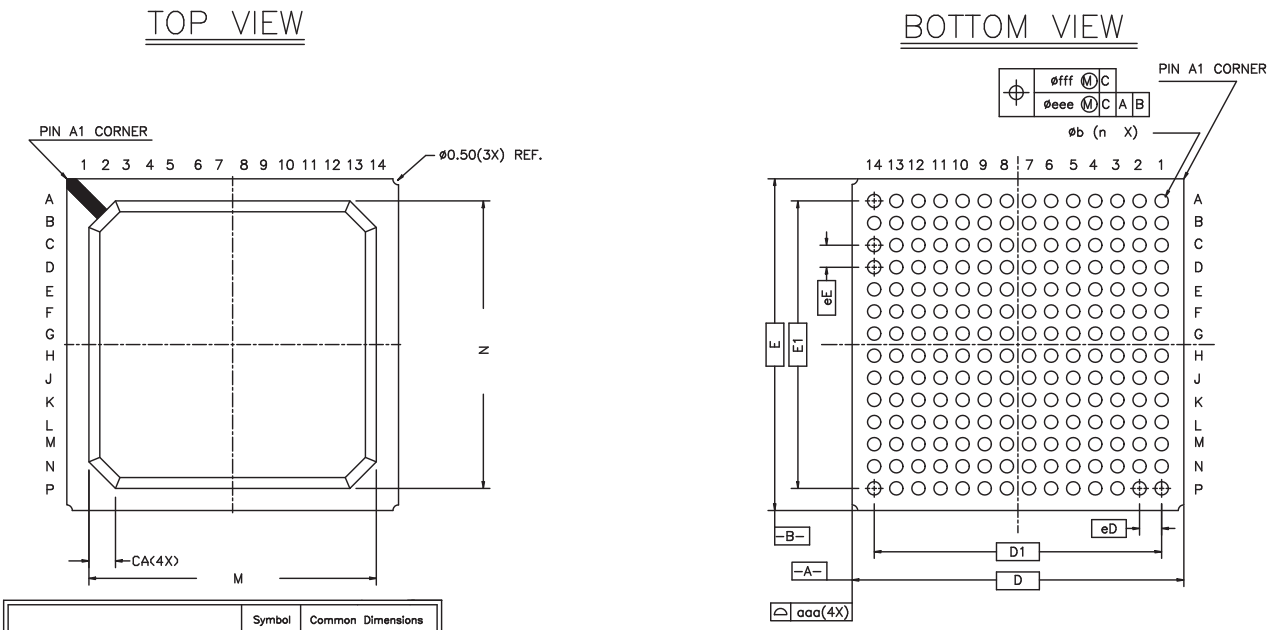
Table 20-2 lists general package specifications. For a more complete list, refer to Figure 20-1.

Table 20-2. General Package Specifications

Parameter	Specification
Package Type	Plastic Ball Grid Array (PBGA)
Quantity of Balls	196
Package Dimensions	15 x 15 mm^2 (approximately 1.71 ±0.19-mm high)
Ball Matrix Pattern	14 x 14 (6 x 6 mm^2 center area ***reserved*** for Ground)
Ball Pitch	1.00 mm
Ball Diameter	0.60 mm
Ball Spacing	0.40 mm

20.3 Mechanical Dimensions

Figure 20-1. Mechanical Dimensions (15 x 15 mm^2 PBGA Package)



		Symbol	Common Dimensions
Package :			PBGA
Body Size:	X	D	15.000
	Y	E	15.000
Ball Pitch :	X	eD	1.000
	Y	eE	1.000
Total Thickness :		A	1.710 +/– 0.190
Mold Thickness :		A3	0.850 Ref.
Substrate Thickness :		A2	0.360 Ref.
Ball Diameter :			0.600
Stand Off :		A1	0.400 ~ 0.600
Ball Width :		b	0.500 ~ 0.700
Mold Area :	X	M	13.000
	Y	N	13.000
Chamfer		CA	1.200 Ref.
Package Edge Tolerance :		aaa	0.200
Substrate Flatness :		bbb	0.250
Mold Flatness :		ccc	0.350
Coplanarity:		ddd	0.150
Ball Offset (Package) :		eee	0.250
Ball Offset (Ball) :		fff	0.100
Ball Count :		n	196
Edge Ball Center to Center :	X	D1	13.000
	Y	E1	13.000

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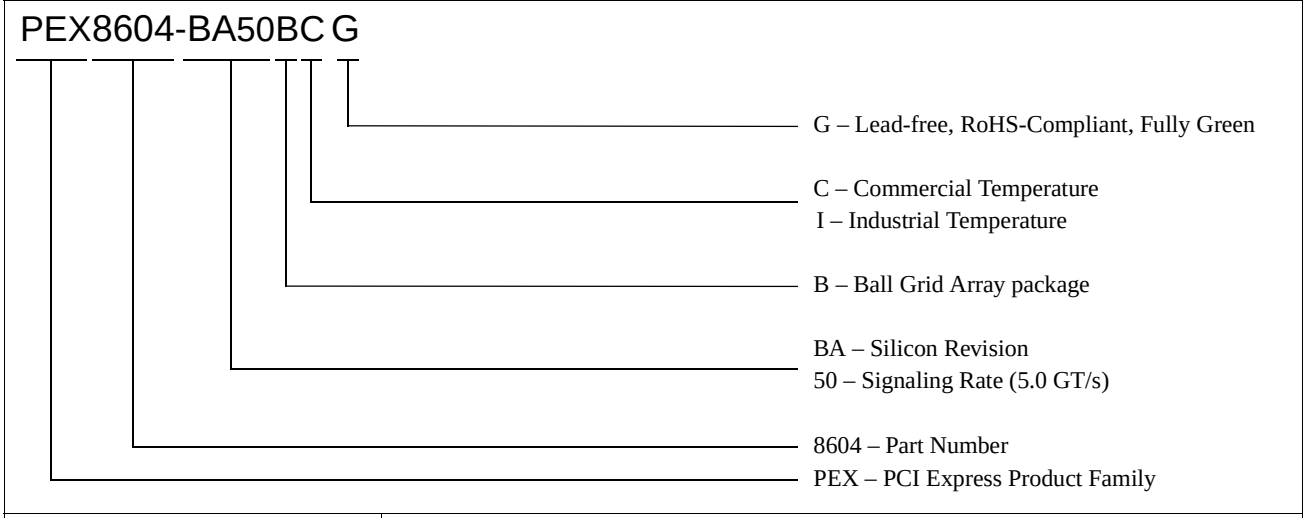
Appendix A General Information

A.1 Product Ordering Information

Contact your local PLX Sales Representative for ordering information.

Table A-1. Product Ordering Information

Part Numbers	Description
PEX8604-BA50BC	PEX 8604 4-Lane, 4-Port PCI Express Gen 2 Switch PBGA Leaded Package (15 x 15 mm^2, 196-ball)
PEX8604-BA50BC G	PEX 8604 4-Lane, 4-Port PCI Express Gen 2 Switch PBGA Lead-Free Package (15 x 15 mm^2, 196-ball)
PEX8604-BA50BI G	PEX 8604 4-Lane, 4-Port PCI Express Gen 2 Switch PBGA Lead-Free Package (15 x 15 mm^2, 196-ball) with Industrial Temperature Support
	
PEX 8604BA-AIC1U1D Kit	PEX 8604 Rapid Development Kit with x1 Upstream Port and Three x1 Downstream Ports

A.2 United States and International Representatives and Distributors

PLX Technology, Inc., representatives and distributors are listed at www.plxtech.com.

A.3 Technical Support

PLX Technology, Inc., technical support information is listed at www.plxtech.com/support, or call 800 759-3735 (domestic only) or 408 774-9060.