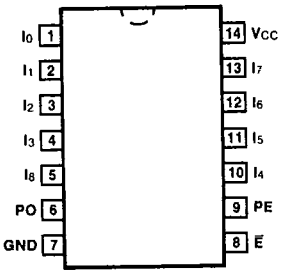
93S62

9-INPUT PARITY CHECKER/GENERATOR

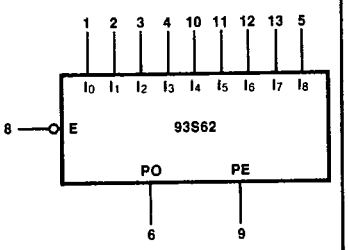
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '62 is a very high speed 9-input parity checker/generator for use in error detection and error correction applications. The '62 provides odd and even parity for up to nine data bits. The even parity output (PE) is HIGH if an even number of inputs are HIGH and $\overline{E}$ is LOW. The odd parity output (PO) will be HIGH if an odd number of inputs are HIGH and $\overline{E}$ is LOW. A HIGH level on the Enable ($\overline{E}$) input forces both outputs LOW.

- **INPUT-TO-OUTPUT DELAY 16 ns**
- **OUTPUT ENABLE TERMINAL**
- **BOTH ODD AND EVEN PARITY OUTPUTS PROVIDED**
- **GENERATES A PARITY BIT FOR UP TO NINE BITS**
- **CHECKS FOR PARITY ON UP TO NINE BITS**
- **EASILY EXPANDABLE**

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	93S62PC		9A
Ceramic DIP (D)	A	93S62DC	93S62DM	6A
Flatpak (F)	A	93S62FC	93S62FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93S (U.L.) HIGH/LOW
$I_0 - I_8$	Data Inputs	1.25/1.0
$\overline{E}$	Output Enable (Active LOW)	2.5/2.0
PO	Odd Parity Output	25/12.5
PE	Even Parity Output	25/12.5

FUNCTIONAL DESCRIPTION — The '62 is a very high speed 9-input parity checker or generator. It is intended primarily for error detection in systems which transmit data in 8-bit bytes, but it can be expanded to any number of data inputs. Both even and odd parity outputs are available to allow maximum flexibility for both parity generation and parity checking. When the device is enabled ($\overline{E}$ = LOW), the Even Parity output (PE) is HIGH when an even number of inputs is HIGH, and the Odd Parity output (PO) is HIGH when an odd number of inputs is HIGH. The active LOW Enable ($\overline{E}$) controls the state of both outputs; when the Enable ($\overline{E}$) is HIGH, both outputs will be LOW. The Enable may be used to strobe the outputs at very high speeds to synchronize or inhibit the parity data.

The '62 has been designed with two sections using Exclusive-NOR comparison techniques. Eight data inputs I_0 thru I_7 represent one section which will generate a parity bit in 16 to 20 ns. The ninth input (I_8) bypasses three levels of logic and switches the outputs in 6.0 ns to 9.0 ns. This feature may be used to compensate for delayed arrival of the parity bit, allowing faster system cycle times *(Figure a)*. The fast I_8 input is also useful when more than nine bits are to be checked. The output of one '62 drives the I_8 input of a second '62 providing a 17-bit parity check in 29 ns (typ).

When some inputs of the '62 are not used, such as for words of less than nine bits or when using parallel expansion techniques, there is an optimum delay scheme for termination of the unused inputs (see Table II). In essence, if one of the inputs of any Exclusive-NOR stays HIGH, the delay from the other input to the output is minimized.

TRUTH TABLE
($\overline{E}$ = LOW)

Number of Inputs I_0 — I_8 that are HIGH	OUTPUTS	
	PO	PE
1, 3, 5, 7, 9	H	L
0, 2, 4, 6, 8	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

TABLE II — Termination Recommendations for Less Than Nine Bits

Number of Data Inputs	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8
3	D_0	L	D_1	L	D_2	L	L	L	L
4	D_0	L	D_1	L	D_2	L	D_3	L	L
5	D_0	L	D_1	L	D_2	L	D_3	L	D_4
6	D_0	D_1	D_2	D_3	D_4	L	D_5	L	L
7	D_0	D_1	D_2	D_3	D_4	L	D_5	L	D_6
8	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L

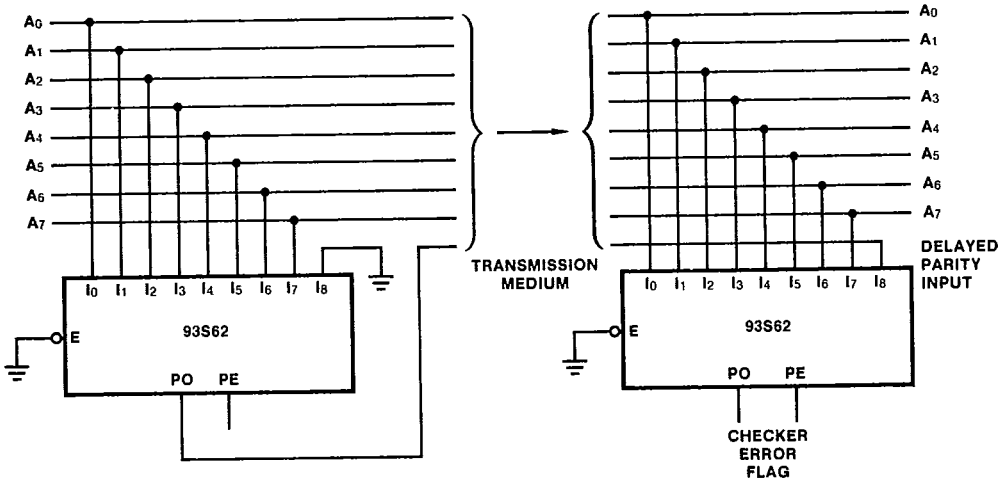
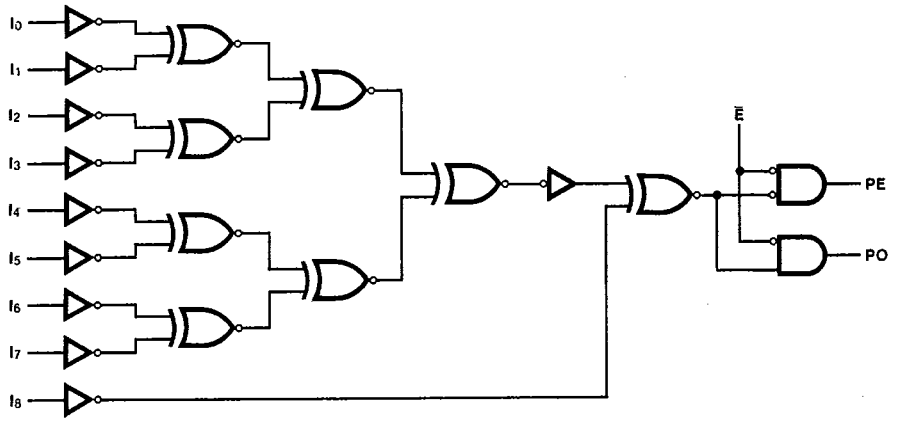


Fig. a Fast Input I_8 Allows Higher System Speed

LOGIC DIAGRAM



$PO = (I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8) \cdot \overline{E}$

$PE = \overline{(I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8)} \cdot \overline{E}$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93S Min	93S Max	UNITS	CONDITIONS
I_{IL}	Input LOW Current	$I_0 - I_8$		-1.6	mA	V_{CC} = Max, V_{IN} = 0.5 V
		$\overline{E}$		-3.2		
I_{CC}	Power Supply Current			65	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93S C_L = 15 pF Min	93S C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay $I_0 - I_7$ to PE		26 22	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_8 to PE		12 9.0	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $I_0 - I_7$ to PO		26 26	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_8 to PO		13 13	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to PE		7.0 7.0	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to PO		7.0 7.0	ns	Figs. 3-1, 3-4