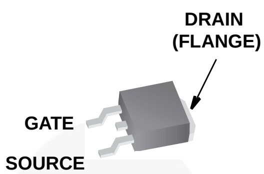
Data Sheet **October 2013**

N-Channel Logic Level UltraFET Power MOSFET
100 V, 20 A, 54 mΩ

Packaging

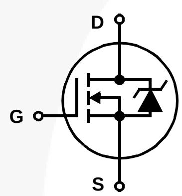
JEDEC TO-252AA



Features

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.052\Omega$, $V_{GS} = 10V$
  - $r_{DS(ON)} = 0.054\Omega$, $V_{GS} = 5V$
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electriecal Models
  - Spice and SABER Thermal Impedance Models
  - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Symbol



Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF76629D3ST	TO-252AA	76629D

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HUF76629D3ST	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	100	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current			
Continuous ($T_C = 25^oC$, $V_{GS} = 5V$)	I_D	20	A
Continuous ($T_C = 25^oC$, $V_{GS} = 10V$) (Figure 2)	I_D	20	A
Continuous ($T_C = 100^oC$, $V_{GS} = 5V$)	I_D	20	A
Continuous ($T_C = 100^oC$, $V_{GS} = 4.5V$) (Figure 2)	I_D	20	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	UIS	Figures 6, 17, 18	
Power Dissipation	P_D	110	W
Derate Above 25^oC		0.74	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief TB334	T_{pkg}	260	^oC

NOTES:

1. $T_J = 25^oC$ to 150^oC.

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Product reliability information can be found at http://www.fairchildsemi.com/products/discrete/reliability/index.html
For severe environments, see our Automotive HUFA series.
All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 12)		100	-	-	V
		I_D = 250µA, V_{GS} = 0V , T_C = -40^{o}C (Figure 12)		90	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 95V, V_{GS} = 0V		-	-	1	µA
		V_{DS} = 90V, V_{GS} = 0V, T_C = 150^{o}C		-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16V		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA (Figure 11)		1	-	3	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 20A, V_{GS} = 10V (Figures 9, 10)		-	0.0415	0.052	Ω
		I_D = 20A, V_{GS} = 5V (Figure 9)		-	0.046	0.054	Ω
		I_D = 20A, V_{GS} = 4.5V (Figure 9)		-	0.047	0.055	Ω
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-252AA		-	-	1.36	^{o}C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	100	^{o}C/W
SWITCHING SPECIFICATIONS (V_{GS} = 4.5V)							
Turn-On Time	t_{ON}	V_{DD} = 50V, I_D = 20A V_{GS} = 4.5V, R_{GS} = 6.8Ω (Figures 15, 21, 22)		-	-	190	ns
Turn-On Delay Time	$t_{d(ON)}$			-	11	-	ns
Rise Time	t_r			-	114	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	38	-	ns
Fall Time	t_f			-	60	-	ns
Turn-Off Time	t_{OFF}			-	-	145	ns
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 50V, I_D = 20A V_{GS} = 10V,R_{GS} = 8.2Ω (Figures 16, 21, 22)		-	-	50	ns
Turn-On Delay Time	$t_{d(ON)}$			-	6.8	-	ns
Rise Time	t_r			-	28	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	67	-	ns
Fall Time	t_f			-	60	-	ns
Turn-Off Time	t_{OFF}			-	-	190	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 50V, I_D = 20A, $I_{g(REF)}$ = 1.0mA (Figures 14, 19, 20)	-	38	46	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	21	25	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	1.2	1.6	nC
Gate to Source Gate Charge	Q_{gs}			-	3.3	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	10	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 13)		-	1285	-	pF
Output Capacitance	C_{OSS}			-	270	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	65	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 20A	-	-	1.25	V
		I_{SD} = 10A	-	-	1.00	V
Reverse Recovery Time	t_{rr}	I_{SD} = 20A, dI_{SD}/dt = 100A/µs	-	-	110	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 20A, dI_{SD}/dt = 100A/µs	-	-	370	nC

Typical Performance Curves

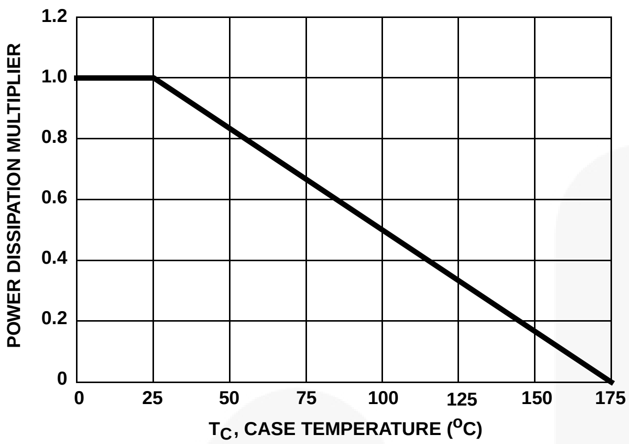


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

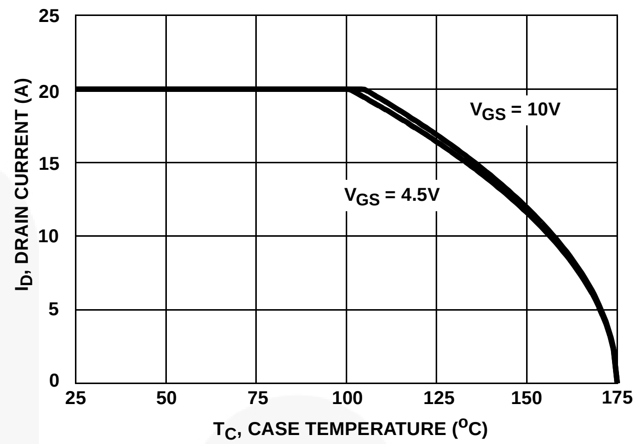


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

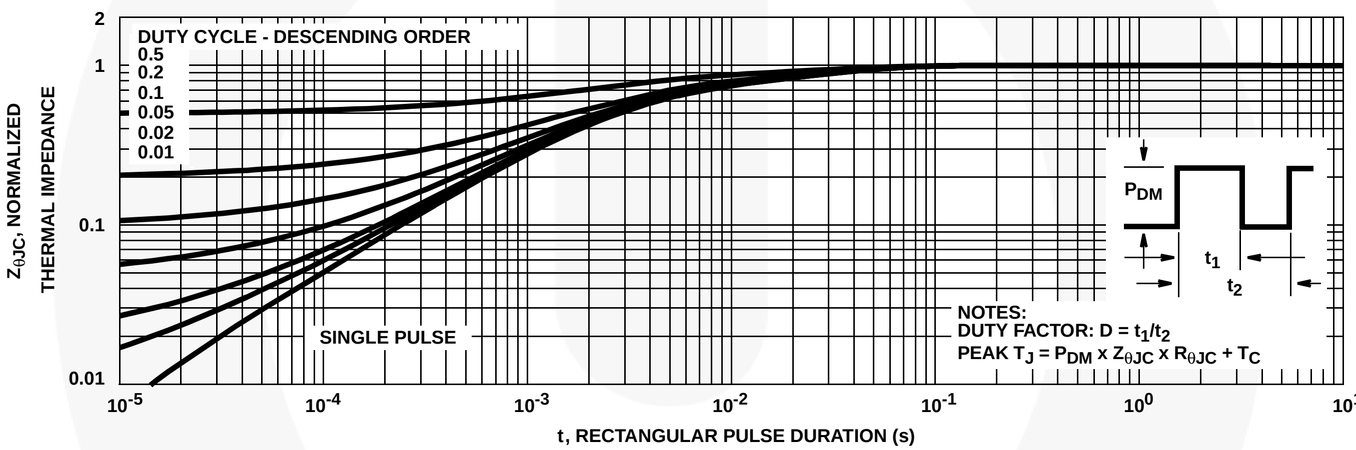


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

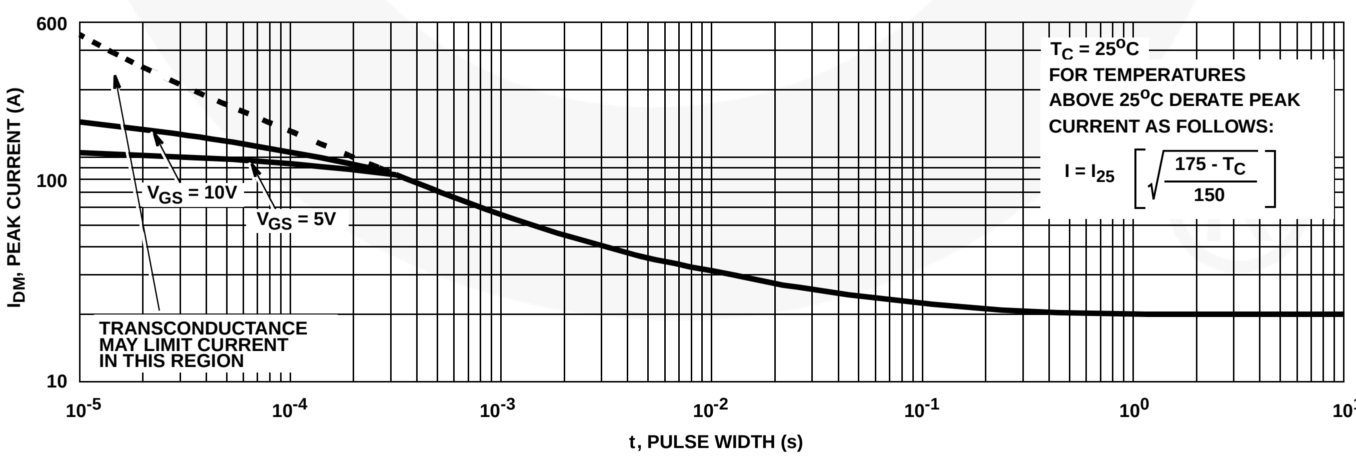


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

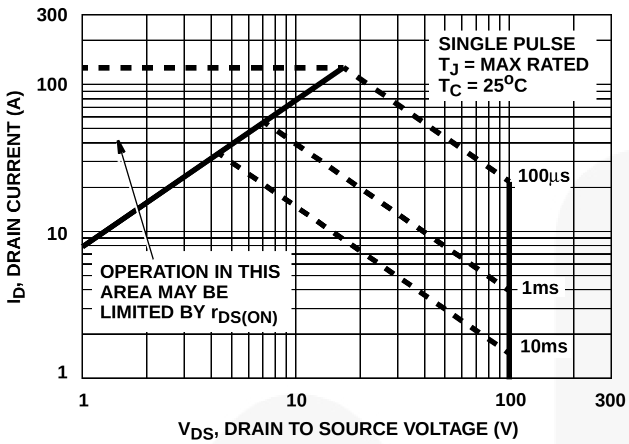
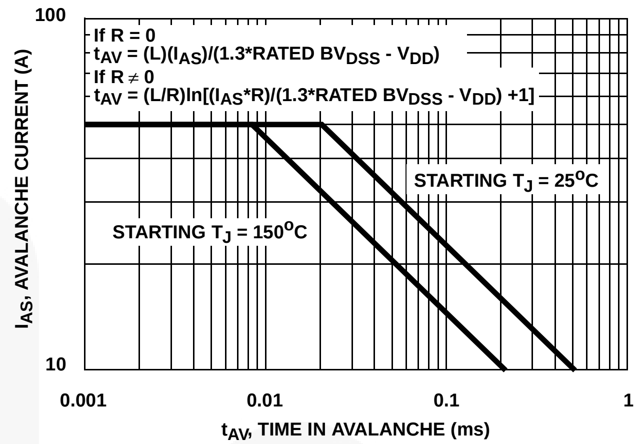


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

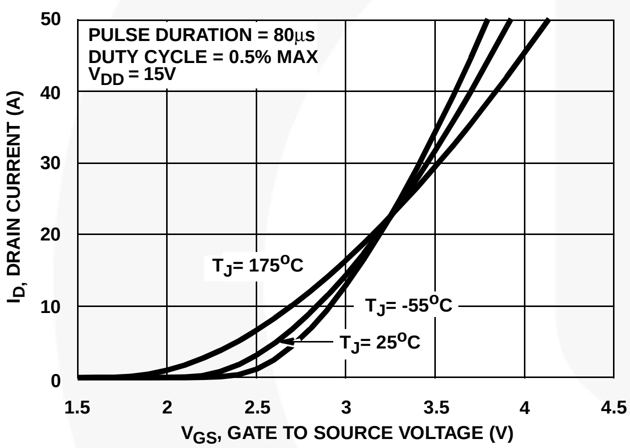


FIGURE 7. TRANSFER CHARACTERISTICS

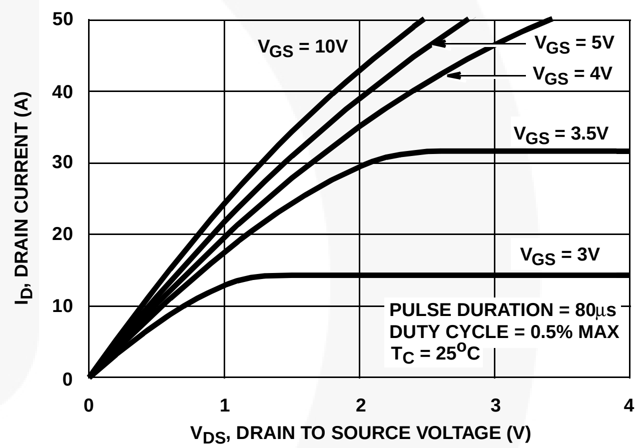


FIGURE 8. SATURATION CHARACTERISTICS

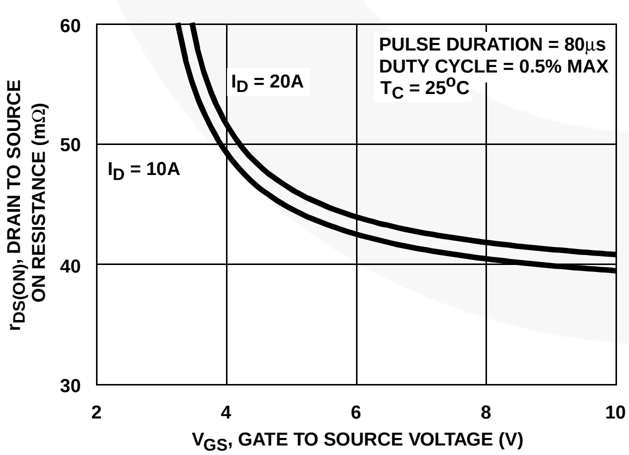


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

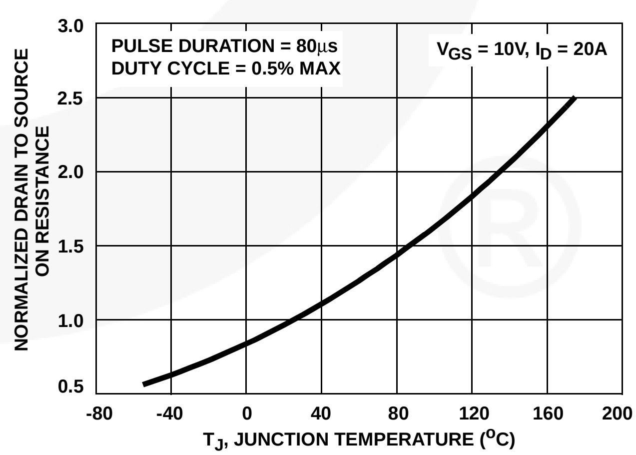


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

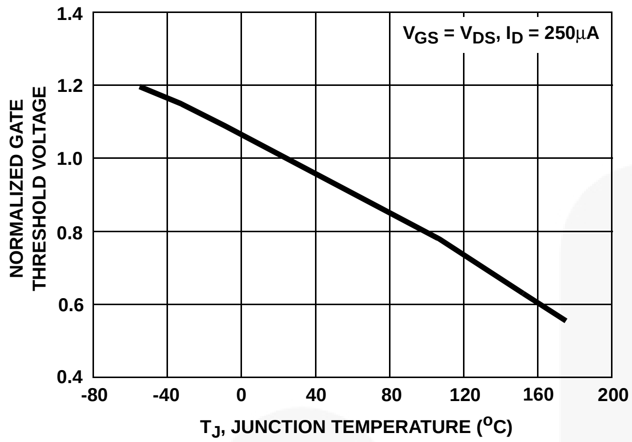


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

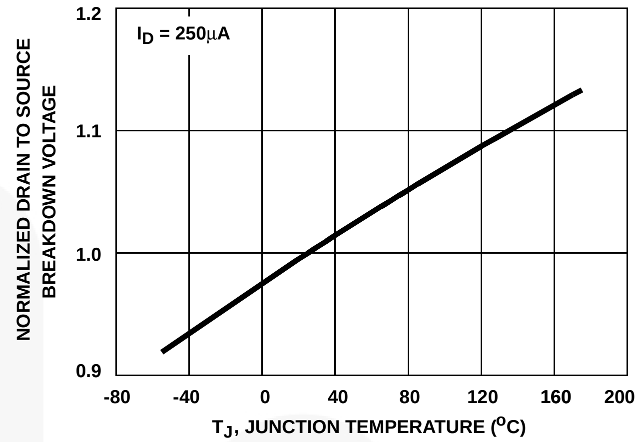


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

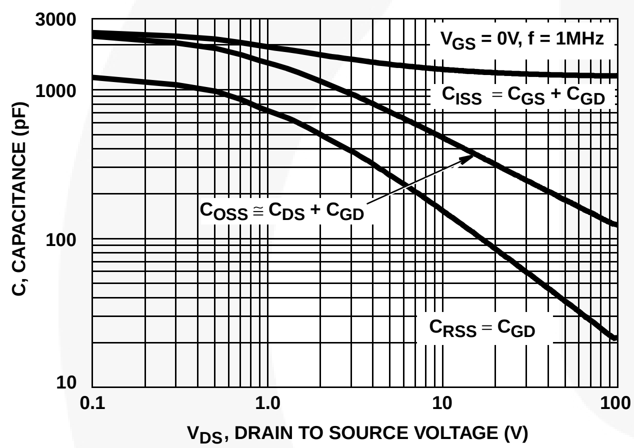
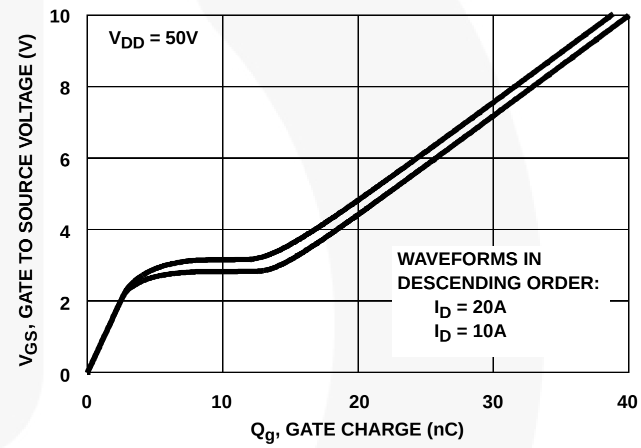


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

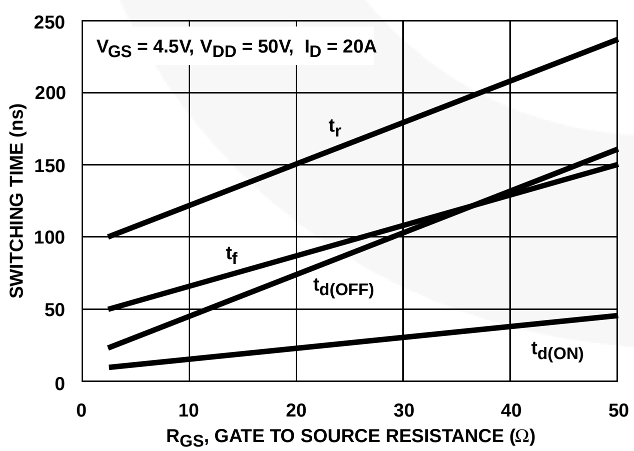


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

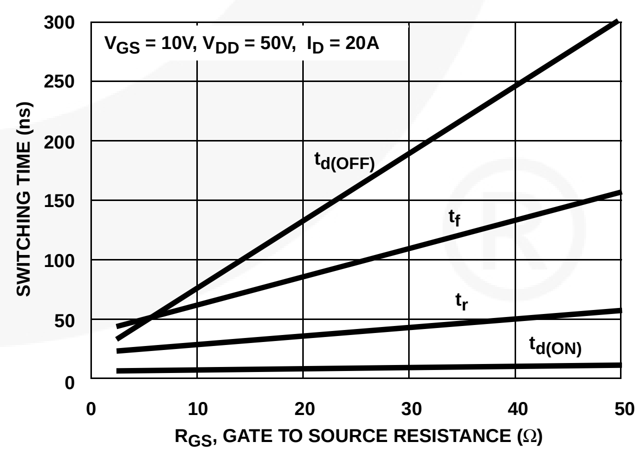


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

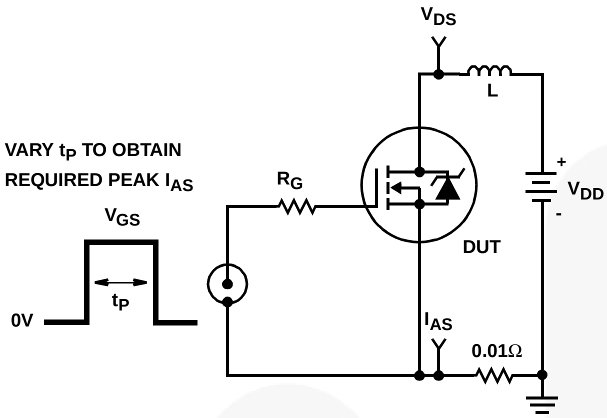


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

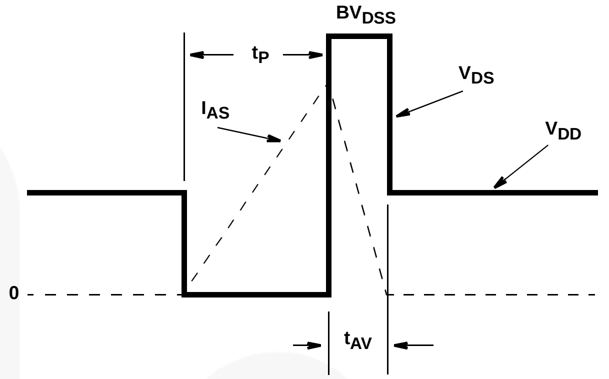


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

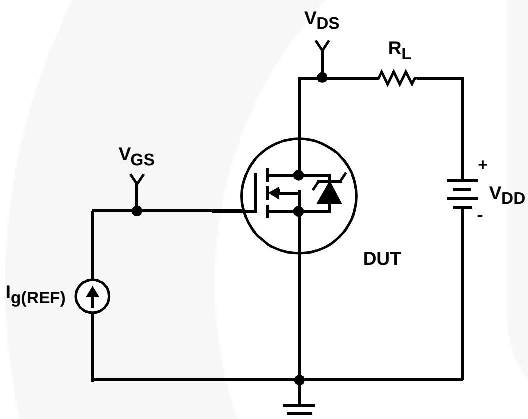


FIGURE 19. GATE CHARGE TEST CIRCUIT

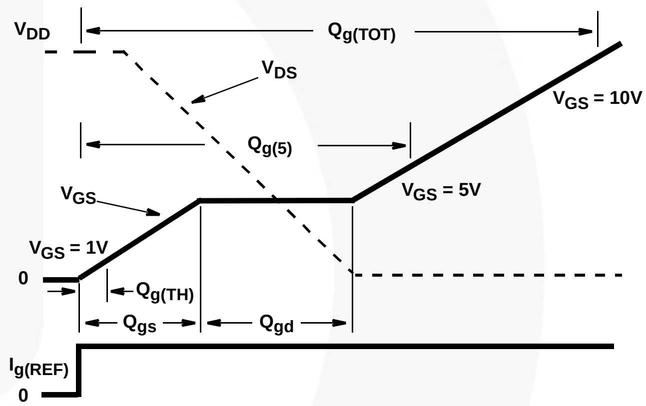


FIGURE 20. GATE CHARGE WAVEFORMS

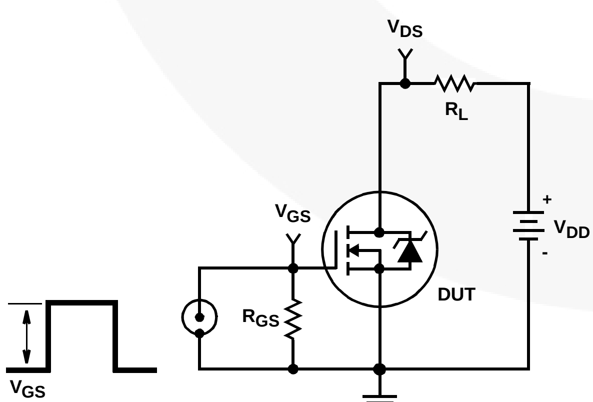


FIGURE 21. SWITCHING TIME TEST CIRCUIT

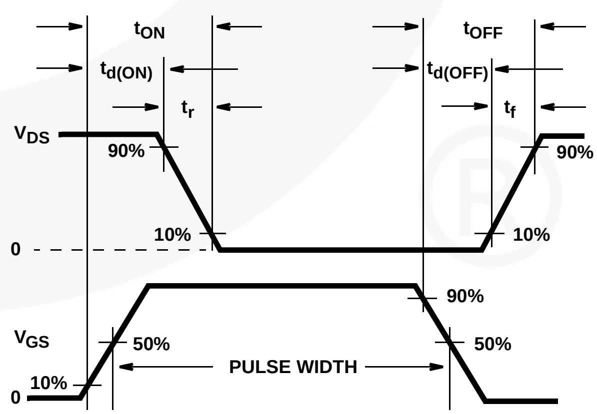


FIGURE 22. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT HUF76629D3 2 1 3 ;   rev 30 July 1999

CA 12 8 2.32e-9
CB 15 14 2.32e-9
CIN 6 8 1.22e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 117.89
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

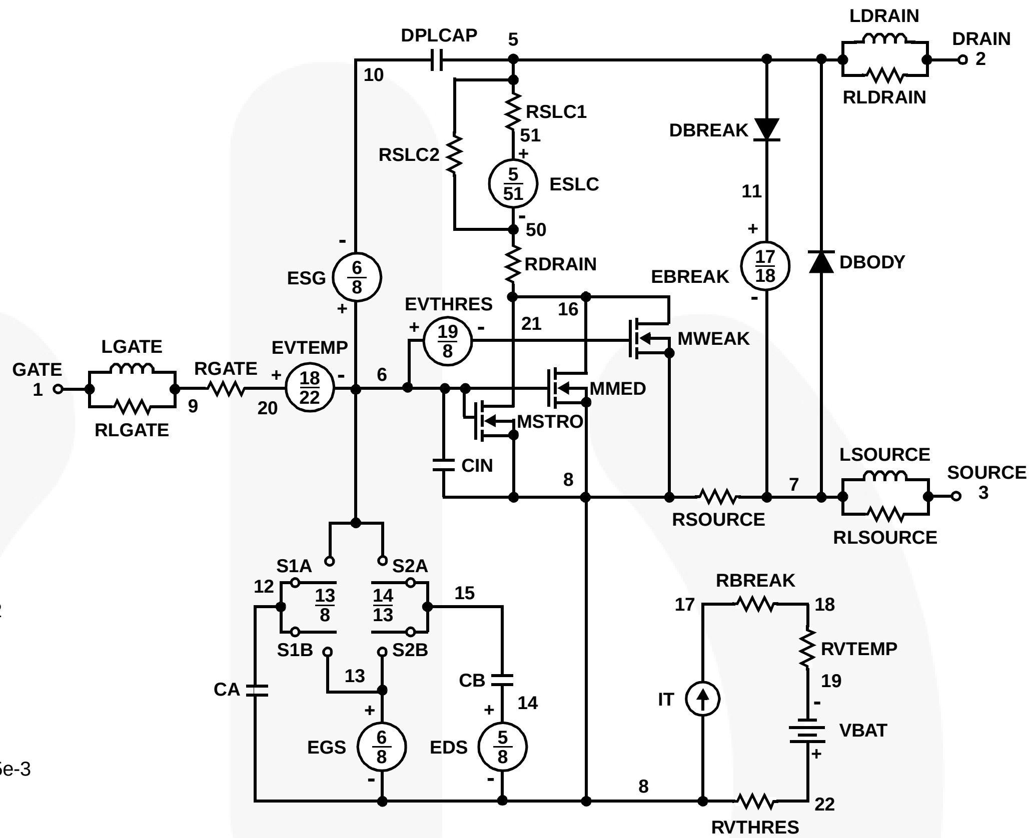
LDRAIN 2 5 1e-9
LGATE 1 9 3.11e-9
LSOURCE 3 7 3.72e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 2.97e-2
RGATE 9 20 2.81
RLDRAIN 2 5 10
RLGATE 1 9 54.2
RLSOURCE 3 7 41.6
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 6.5e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1



ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*61),3))}

.MODEL DBODYMOD D (IS = 1.15e-12 IKF = 4.3 RS = 7.45e-3 TRS1 = 2.40e-3 TRS2 = 5.15e-7 CJO = 1.14e-9 TT = 5.86e-8 M = 0.52 XTI = 3.65)
.MODEL DBREAKMOD D (RS = 3.78e- 1TRS1 = 1e- 3TRS2 = -1e-6)
.MODEL DPLCAPMOD D (CJO = 1.37e- 9IS = 1e-3 0N = 10 M = 0.94)
.MODEL MMEDMOD NMOS (VTO = 1.84 KP = 2.6 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.81)
.MODEL MSTROMOD NMOS (VTO = 2.13 KP = 42.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.58 KP = 0.07 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 28.1 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.88e- 4TC2 = -5.40e-7)
.MODEL RDRAINMOD RES (TC1 = 7.85e-3 TC2 = 1.95e-5)
.MODEL RSLCMOD RES (TC1 = 4.97e-3 TC2 = 5.05e-6)
.MODEL RSOURCEMOD RES (TC1 = 1.5e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -1.85e-3 TC2 = -4.48e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.72e- 3TC2 = 6.00e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.5 VOFF= -2.2)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.2 VOFF= -5.5)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.1 VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF= -1.1)

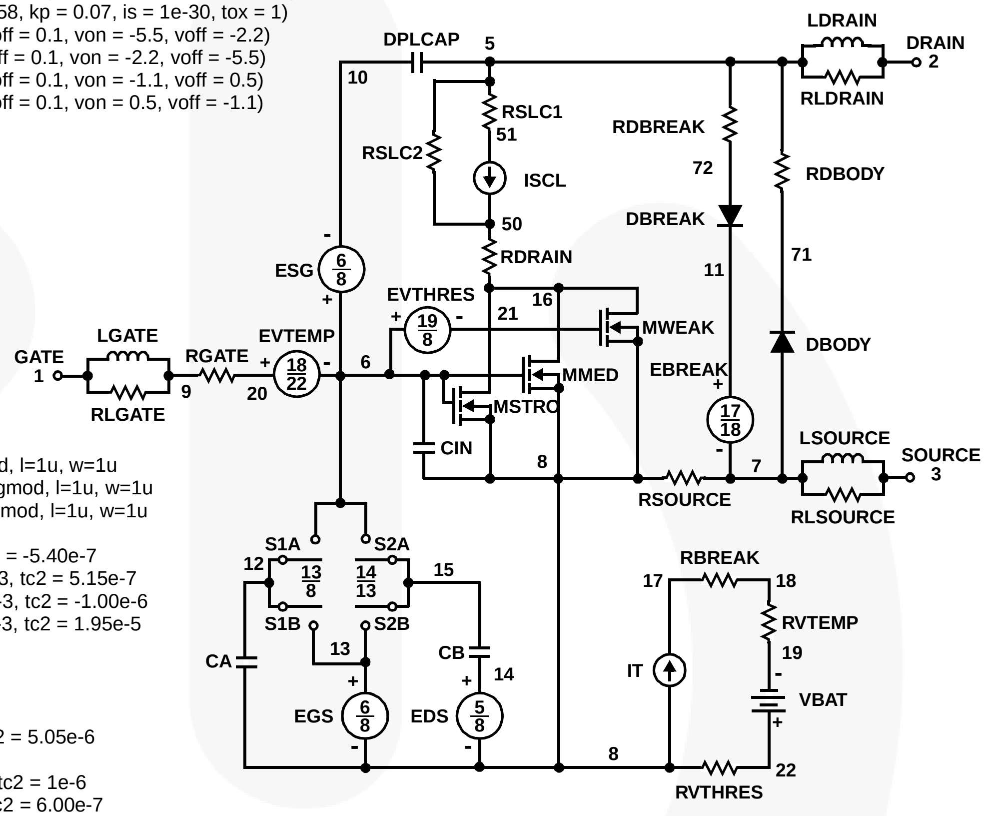
.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV 30 July 1999

```
template huf76629d3 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod = (is = 1.15e-12, cjo = 1.14e-9, tt = 5.86e-8, xti = 3.65, m = 0.52)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 1.37e-9, is = 1e-30, n = 10, m = 0.94)
m..model mmedmod = (type=_n, vto = 1.84, kp = 2.6, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.13, kp = 42.5, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.58, kp = 0.07, is = 1e-30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -5.5, voff = -2.2)
sw_vcsp..model s1bmod = (ron =1e-5, roff = 0.1, von = -2.2, voff = -5.5)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -1.1, voff = 0.5)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.5, voff = -1.1)

c.ca n12 n8 = 2.32e-9
c.cb n15 n14 = 2.32e-9
c.cin n6 n8 = 1.22e-9

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 3.11e-9
l.lsource n3 n7 = 3.72e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1 = 9.88e-4, tc2 = -5.40e-7
res.rdbody n71 n5 = 7.45e-3, tc1 = 2.40e-3, tc2 = 5.15e-7
res.rdbreak n72 n5 = 3.78e-1, tc1 = 1.00e-3, tc2 = -1.00e-6
res.rdrain n50 n16 = 2.97e-2, tc1 = 7.85e-3, tc2 = 1.95e-5
res.rgate n9 n20 = 2.81
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 54.2
res.rlsource n3 n7 = 41.6
res.rslc1 n5 n51 = 1e-6, tc1 = 4.97e-3, tc2 = 5.05e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 6.5e-3, tc1 = 1.5e-3, tc2 = 1e-6
res.rvtemp n18 n19 = 1, tc1 = -1.72e-3, tc2 = 6.00e-7
res.rvthres n22 n8 = 1, tc1 = -1.85e-3, tc2 = -4.48e-6

spe.ebreak n11 n7 n17 n18 = 117.89
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/61))** 3))
}
}
```



SPICE Thermal Model

REV 26 July 1999

HUF76629D3

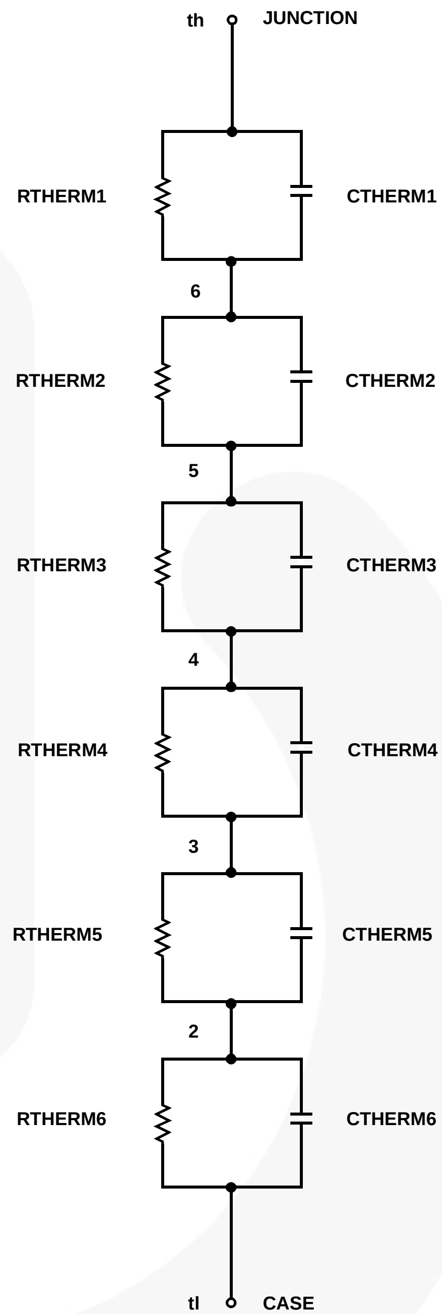
CTHERM1 th 6 2.45e-3
CTHERM2 6 5 8.15e-3
CTHERM3 5 4 7.40e-3
CTHERM4 4 3 7.45e-3
CTHERM5 3 2 1.01e-2
CTHERM6 2 tl 7.49e-2

RTHERM1 th 6 9.00e-3
RTHERM2 6 5 1.80e-2
RTHERM3 5 4 9.15e-2
RTHERM4 4 3 2.43e-1
RTHERM5 3 2 3.50e-1
RTHERM6 2 tl 3.62e-1

SABER Thermal Model

SABER thermal model HUF76629D3

```
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 2.45e-3
ctherm.ctherm2 6 5 = 8.15e-3
ctherm.ctherm3 5 4 = 7.40e-3
ctherm.ctherm4 4 3 = 7.45e-3
ctherm.ctherm5 3 2 = 1.01e-2
ctherm.ctherm6 2 tl = 7.49e-2

rtherm.rtherm1 th 6 = 9.00e-3
rtherm.rtherm2 6 5 = 1.80e-2
rtherm.rtherm3 5 4 = 9.15e-2
rtherm.rtherm4 4 3 = 2.43e-1
rtherm.rtherm5 3 2 = 3.50e-1
rtherm.rtherm6 2 tl = 3.62e-1
}
```



FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficentMax™
ESBC™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource^SM^
GreenBridge™
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
Marking Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
mWSaver®
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
µSerDes™
SerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used here in:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handing and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66

