



Integrated Device Technology, Inc.

# FAST CMOS OCTAL TRANSCEIVER/REGISTERS (3-STATE)

IDT54/74FCT646T/AT/CT/DT - 2646T/AT/CT  
IDT54/74FCT648T/AT/CT  
IDT54/74FCT652T/AT/CT/DT - 2652T/AT/CT

## FEATURES:

- **Common features:**
  - Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - $V_{OH} = 3.3\text{V}$  (typ.)
    - $V_{OL} = 0.3\text{V}$  (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT646T/648T/652T:**
  - Std., A, C and D speed grades
  - High drive outputs (-15mA IOH, 64mA IOL)
  - Power off disable outputs permit "live insertion"
- **Features for FCT2646T/2652T:**
  - Std., A, and C speed grades
  - Resistor outputs (-15mA IOH, 12mA IOL Com.) (-12mA IOH, 12mA IOL Mil.)
  - Reduced system switching noise

## DESCRIPTION:

The FCT646T/FCT2646T/FCT648T/FCT652T/2652T consist of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

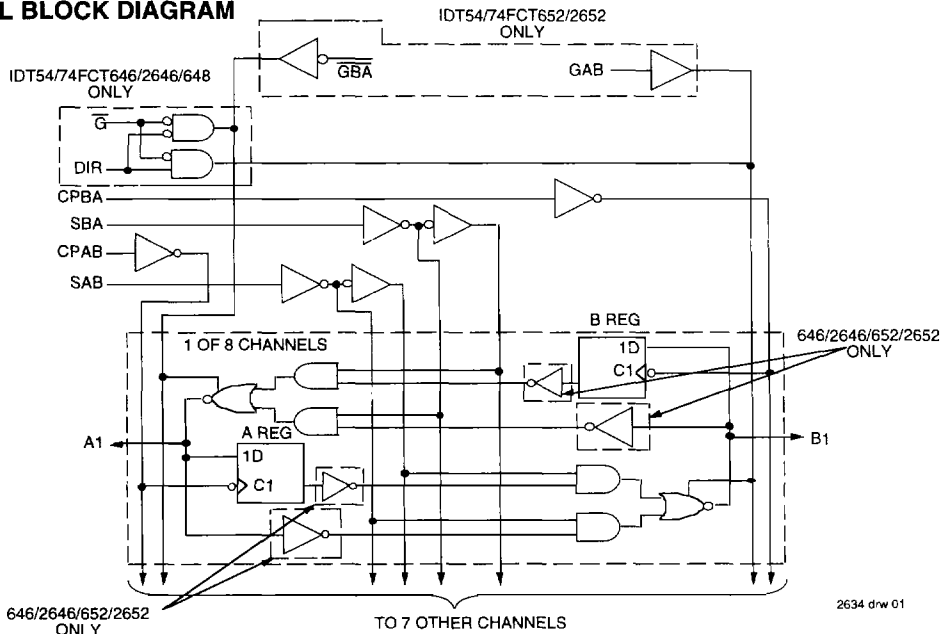
The FCT652T/FCT2652T utilize GAB and  $\overline{\text{GBA}}$  signals to control the transceiver functions. The FCT646T/FCT2646T/FCT648T utilize the enable control ( $\overline{\text{G}}$ ) and direction (DIR) pins to control the transceiver functions.

SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

The FCT26xxT have balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

## FUNCTIONAL BLOCK DIAGRAM



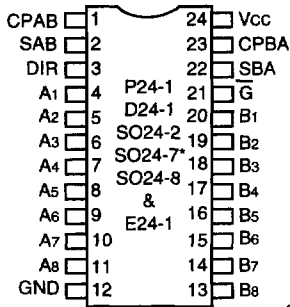
2634 drw 01

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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**JUNE 1996**

**PIN CONFIGURATIONS**

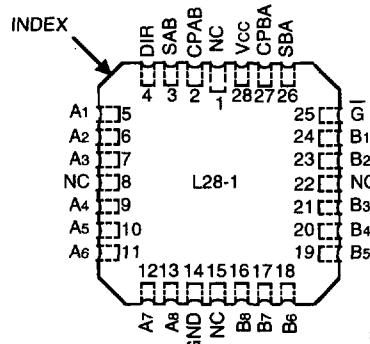


2634 drw 02

**DIP/SOIC/SSOP/QSOP/CERPACK  
TOP VIEW**

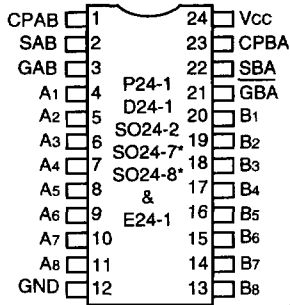
\* FCT646/2646T/AT/CT/DT only

**FCT646/FCT2646T  
FCT648**



2634 drw 03

**LCC  
TOP VIEW**

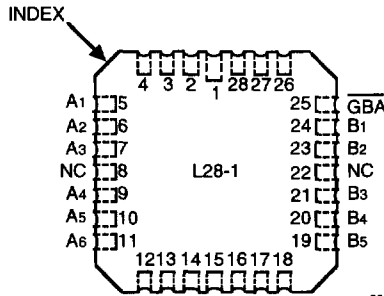


2634 drw 04

**DIP/SOIC/SSOP/QSOP/CERPACK  
TOP VIEW**

\* FCT652/2652T/AT/CT/DT only

**FCT652/FCT2652T**



2634 drw 05

**LCC  
TOP VIEW**



**PIN DESCRIPTION**

Pin Names	Description
A1 - A8	Data Register A Inputs Data Register B Outputs
B1 - B8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\bar{G}$	Output Enable Inputs (646/648)
GAB, $\bar{G}A$	Output Enable Inputs (652)

2634 tbl 01

**FUNCTION TABLE (646/648)**

Inputs						Data I/O <sup>(1)</sup>		Operation or Function	
$\bar{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>1</sub> - A <sub>8</sub>	B <sub>1</sub> - B <sub>8</sub>	FCT646T/FCT2646T	FCT648T
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\bar{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\bar{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\bar{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\bar{A}$ Data to B Bus

2634 tbl 02

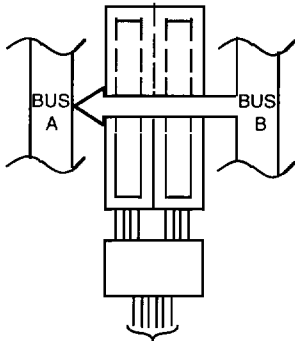
**FUNCTION TABLE (652)**

Inputs						Data I/O		Operation or Function	
GAB	$\bar{G}BA$	CPAB	CPBA	SAB	SBA	A <sub>1</sub> - A <sub>8</sub>	B <sub>1</sub> - B <sub>8</sub>	FCT652T/FCT2652T	
L	H	H or L	H or L	X	X	Input	Input	Isolation	
L	H	↑	↑	X	X			Store A and B Data	
X	H	↑	H or L	X	X	Input	Unspecified <sup>(1)</sup>	Store A, Hold B	
H	H	↑	↑	X <sup>(2)</sup>	X	Input	Output	Store A in Both Registers	
L	X	H or L	↑	X	X	Unspecified <sup>(1)</sup>	Input	Hold A, Store B	
L	L	↑	↑	X	X <sup>(2)</sup>	Output	Input	Store B in Both Registers	
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	
L	L	X	H or L	X	H			Stored B Data to A Bus	
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	
H	H	H or L	X	H	X			Stored A Data to B Bus	
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus	

**NOTES:**

- The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.  
 Select control = H: clocks must be staggered in order to load both registers.  
 H = HIGH, L = LOW, X = Don't Care, ↑ = LOW-to-HIGH transition.
- $\bar{A}$  in B Register.
- $\bar{B}$  in A Register.

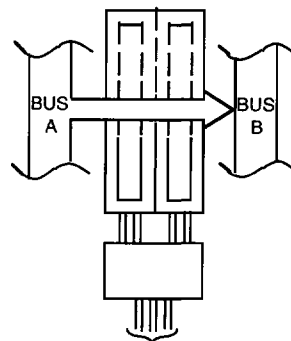
2634 tbl 03



652/2652	GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
646/2646/ 648	DIR	$\overline{\text{G}}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

REAL-TIME TRANSFER  
BUS B TO A

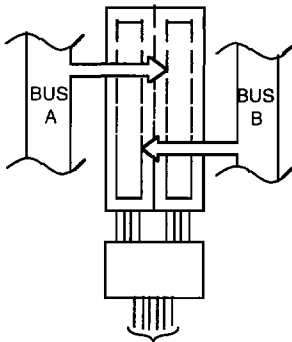
2634 drw 06



652/2652	GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X
646/2646/ 648	DIR	$\overline{\text{G}}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X

REAL-TIME TRANSFER  
BUS A TO B

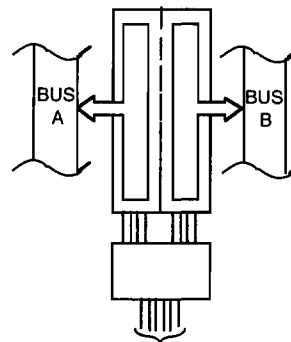
2634 drw 07



652/2652	GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X
646/2646/ 648	DIR	$\overline{\text{G}}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X

STORAGE FROM  
A AND/OR B

2634 drw 08



652/2652	GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA
	H	L	H or	H or	H	H
646/2646/ <sup>(1)</sup> 648	DIR	$\overline{\text{G}}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or	X	H
	H	L	H or	X	H	X

TRANSFER STORES  
DATA TO A AND/OR B

2634 drw 09

**NOTE:**

- 646/2646/648 cannot transfer data to A bus and B bus simultaneously.

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**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	-0.5 to V <sub>CC</sub> +0.5	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Input and V<sub>CC</sub> terminals only.
- Outputs and I/O terminals only.

**CAPACITANCE (TA = +25°C, f = 1.0MHz)**

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
COU	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

**NOTE:**

- This parameter is measured at characterization but not tested.

2634 Ink 05

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, V<sub>CC</sub> = 5.0V ± 5%; Military: TA = -55°C to +125°C, V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V <sub>IL</sub>	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I <sub>IH</sub>	Input HIGH Current <sup>(4)</sup>	V <sub>CC</sub> = Max. V <sub>I</sub> = 2.7V	—	—	±1	μA
I <sub>IL</sub>	Input LOW Current <sup>(4)</sup>		V <sub>I</sub> = 0.5V	—	—	±1
I <sub>OZH</sub>	High Impedance Output Current (3-State Output pins) <sup>(4)</sup>	V <sub>CC</sub> = Max. V <sub>O</sub> = 2.7V	—	—	±1	μA
I <sub>OZL</sub>			V <sub>O</sub> = 0.5V	—	—	±1
I <sub>I</sub>	Input HIGH Current <sup>(4)</sup>	V <sub>CC</sub> = Max., V <sub>I</sub> = V <sub>CC</sub> (Max.)	—	—	±1	μA
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18mA	—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	—	—	200	—	mV
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub>	—	0.01	1	mA

2634 Ink 05

**OUTPUT DRIVE CHARACTERISTICS FOR FCT646T/648T/652T**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -6mA MIL.	2.4	3.3	—	V
			I <sub>OH</sub> = -8mA COM'L.	—	—	—	—
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -12mA MIL.	2.0	3.0	—	V
			I <sub>OH</sub> = -15mA COM'L.	—	—	—	—
I <sub>OL</sub>	Output LOW Current	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 48mA MIL.	—	0.3	0.55	V
			I <sub>OL</sub> = 64mA COM'L.	—	—	—	—
I <sub>OS</sub>	Short Circuit Current	V <sub>CC</sub> = Max., V <sub>O</sub> = GND <sup>(3)</sup>	-60	-120	-225	mA	
I <sub>OFF</sub>	Input/Output Power Off Leakage <sup>(5)</sup>	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> ≤ 4.5V	—	—	±1	μA	

2634 Ink 06

**OUTPUT DRIVE CHARACTERISTICS FOR FCT2646T/2652T**

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
IODL	Output LOW Current	VCC = 5V, VIN = VIH or VIL, VOUT = 1.5V <sup>(3)</sup>		16	48	—	mA
IODH	Output HIGH Current	VCC = 5V, VIN = VIH or VIL, VOUT = 1.5V <sup>(3)</sup>		-16	-48	—	mA
VOH	Output HIGH Voltage	VCC = Min. VIN = VIH or VIL	IOH = -12mA MIL. IOH = -15mA COM'L.	2.4	3.3	—	V
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL	IOL = 12mA	—	0.3	0.50	V

**NOTES:**

2634 Ink 07

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is ±5µA at TA = -55°C.
- This parameter is guaranteed but not tested.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit	
ΔIcc	Quiescent Power Supply Current TTL Inputs HIGH	VCC = Max. VIN = 3.4V <sup>(3)</sup>		—	0.5	2.0	mA	
IcCD	Dynamic Power Supply Current <sup>(4)</sup>	VCC = Max. Outputs Open GAB = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Input Toggling 50% Duty Cycle	VIN = VCC VIN = GND	FCTxxxT FCT2xxxT	— —	0.15 0.06	0.25 0.12	mA/ MHz
Ic	Total Power Supply Current <sup>(6)</sup>	VCC = Max. Outputs Open fCP = 10MHz 50% Duty Cycle GAB = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Bit Toggling at fi = 5MHz 50% Duty Cycle	VIN = VCC VIN = GND VIN = 3.4 VIN = GND	FCTxxxT FCT2xxxT FCTxxxT FCT2xxxT	— — — —	1.5 0.6 2.0 1.1	3.5 2.2 5.5 4.2	mA
		VCC = Max. Outputs Open fCP = 10MHz 50% Duty Cycle GAB = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND Eight Bits Toggling at fi = 2.5MHz 50% Duty Cycle	VIN = VCC VIN = GND VIN = 3.4 VIN = GND	FCTxxxT FCT2xxxT FCTxxxT FCT2xxxT	— — — —	3.8 1.5 6.0 3.8	7.3 <sup>(5)</sup> 4.0 <sup>(5)</sup> 16.3 <sup>(5)</sup> 13.0 <sup>(5)</sup>	

**NOTES:**

2634 Ibl 08

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient.
- Per TTL driven input (VIN = 3.4V). All other inputs at VCC or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.

6.  $I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_c = I_{CC} + \Delta I_{CC} \cdot D_{HNT} + I_{CDD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (VIN = 3.4V)}$   
 $D_{HNT} = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CDD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$   
 All currents are in milliamps and all frequencies are in megahertz.



**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Condition <sup>(1)</sup>	646/648/652T 2646/2652T				646/648/652AT 2646/2652AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time, $\overline{G}$ , DIR to Bus <sup>(3)</sup>		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time, $\overline{G}$ , DIR to Bus <sup>(3)</sup>		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SBA or SAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
tsu	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width, HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns

2634 tbl 09

Symbol	Parameter	Condition <sup>(1)</sup>	646/648/652CT 2646/2652CT				646/652DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	1.5	5.4	1.5	6.0	1.5	4.4	—	—	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time, $\overline{G}$ , DIR to Bus <sup>(3)</sup>		1.5	7.8	1.5	8.9	1.5	5.0	—	—	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time, $\overline{G}$ , DIR to Bus <sup>(3)</sup>		1.5	6.3	1.5	7.7	1.5	4.3	—	—	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	4.4	—	—	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SBA or SAB to Bus		1.5	6.2	1.5	7.0	1.5	5.0	—	—	ns
tsu	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	—	—	ns
th	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	1.0	—	—	—	ns
tw	Clock Pulse Width, HIGH or LOW <sup>(4)</sup>		5.0	—	5.0	—	3.0	—	—	—	ns

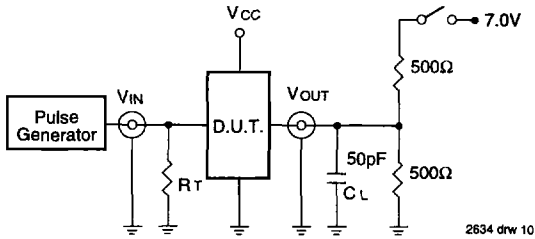
2634 tbl 10

**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. GAB, GBA to Bus for 652.
4. This parameter is guaranteed but not tested.

**TEST CIRCUITS AND WAVEFORMS**

**TEST CIRCUITS FOR ALL OUTPUTS**



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**SWITCH POSITION**

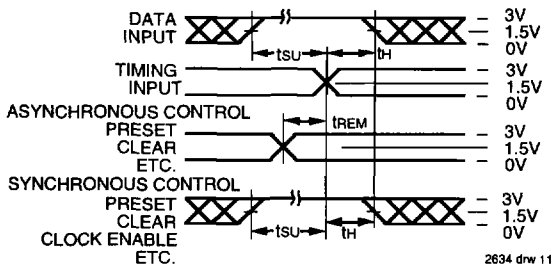
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

**DEFINITIONS:**

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to Z<sub>out</sub> of the Pulse Generator.

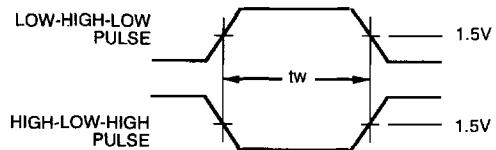
2634 Ink 11

**SET-UP, HOLD AND RELEASE TIMES**



2634 drw 11

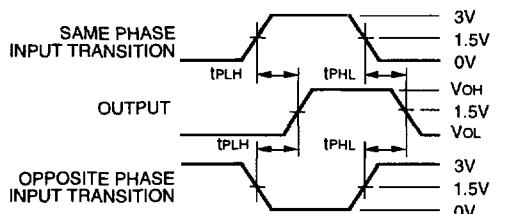
**PULSE WIDTH**



2634 drw 12

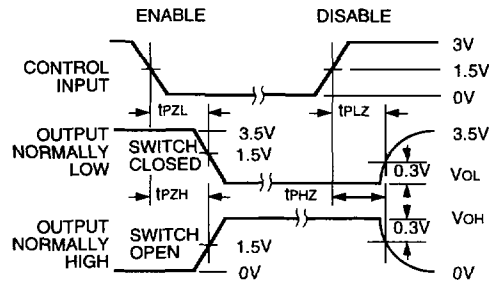


**PROPAGATION DELAY**



2634 drw 13

**ENABLE AND DISABLE TIMES**



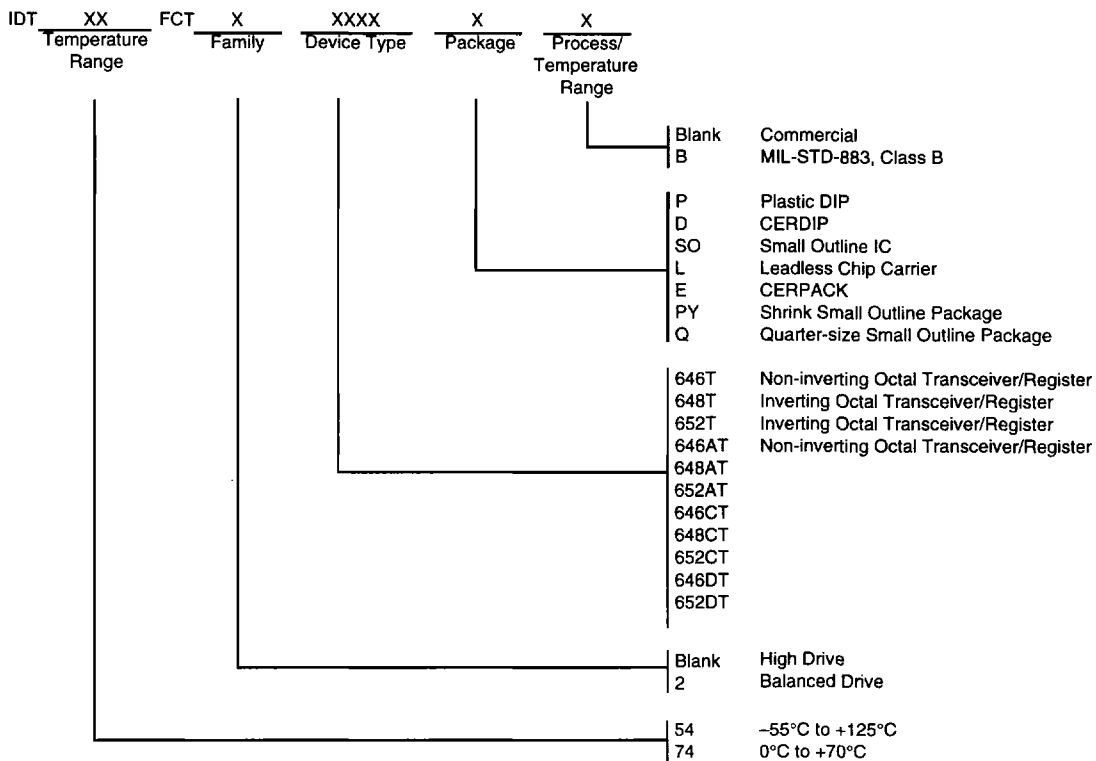
2634 drw 14

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tf ≤ 2.5ns



**ORDERING INFORMATION**



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