OctalFALC™

Octal E1/T1/J1 Framer and Line Interface Component for Long- and Short-Haul Applications

PEF 22558 E, Version 1.1

Wireline Communications

Never stop thinking.

Edition 2005-05-03

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
81669 München, Germany

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Revision History:	**2005-05-03**	Rev. 2.0
Previous Version:	**Rev. 1.0**	

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46	Transmit Line Monitor

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Abstract

This document describes the differences of PEF 22558 E, OctalFALC™, Version v1.1, relative to the QuadFALC® , Version 2.1. QuadFALC is a registered brand.

1 General

The number of receive and transmit channels has been increased from four to eight. All channels can be configured and used independently.

To enable a seamless transition from QuadFALC® designs to OctalFALC™ applications, a compatibility mode is provided. This mode allows software written for the QuadFALC® to be used with the OctalFALC™ without changes.

For new applications, a number of additional features and enhancements are provided.

2 Compatibility

2.1 Hardware Compatibility

The OctalFALC™ always requires two supply voltages, 1.8 V and 3.3 V. The 3.3 V-only mode usable with QuadFALC® (V1.3 and V2.1) is *not* supported.

To enable use of PG-LBGA-256-1 package the number of multifunction ports is reduced to three in receive and two in transmit direction per channel. Furthermore RCLK signals are provided on multifunction ports instead of separate pins.

To ensure software compatibility unused registers (for example PC4) still exists but are not used. **Figure 1** shows the Logical Symbol of the OctalFALC™.

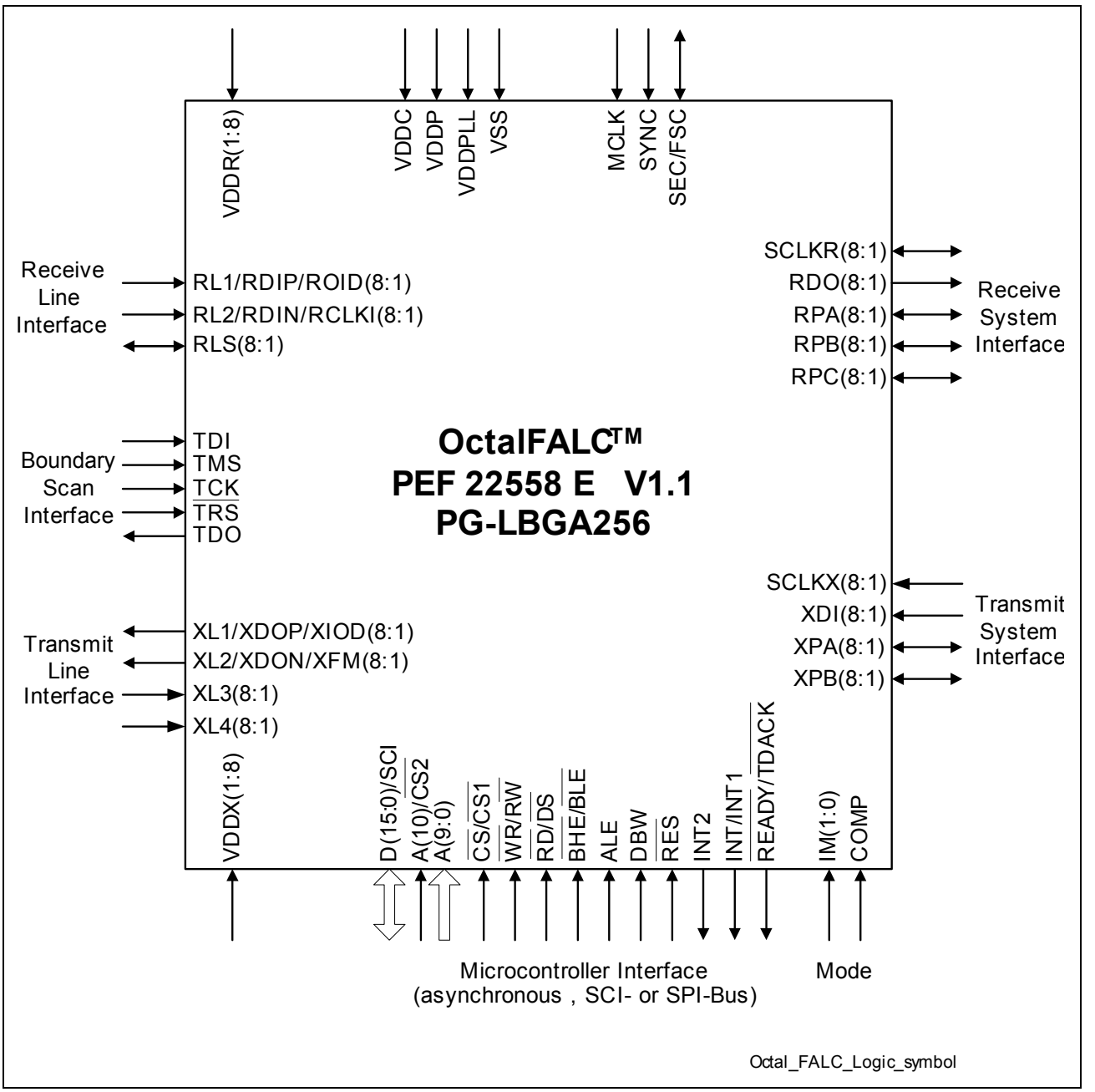

Figure 1 Logic Symbol

2.2 Software Compatibility

The OctalFALC™ can be used in two basic modes. The “QuadFALC® Compatibility Mode” allows to use the device like two separate QuadFALC®s while the “OctalFALC™ Generic Mode” handles the device as a single entity. The “Compatibility Mode” option allows an easy migration of designs from QuadFALC® to OctalFALC™ without the need for *software* changes. As for the QuadFALC® the register addresses are 10 bits wide.

In the “OctalFALC™ Generic Mode” the register addresses are 11 bit wide.

An overview is given in **Table 1**.

Additional features are available also in compatibility mode, but are disabled by default and must be activated by software.

If compatibility mode is selected, the version status register VSTR shows the same value as in QuadFALC® V2.1 while the JTAG boundary scan ID is always the OctalFALC™ number and not affected by the mode selection. In compatibility mode the behavior of the clocking system is the same as in the QuadFALC®. So the eigenfrequencies and attunation factors of all PLLs, especially of the DCO-R and DCO-X must be in the near of the QuadFALC® values with the equivalent register programing. Also the multi function pin RPC must have the function RCLK after reset (Register bits PC1.RPC(3:0)).

*Note: In compatibility mode and if microcontroller mode is selected, A(10) - active high - is used as second chip select signal ($\overline{CS2}$) - active low - for the second pseudo QuadFALC®, see **Figure 2** and **Table 1**. The first pseudo QuadFALC® is selected by $\overline{CS1}$. Activation of both chip selects simultaneous is not allowed.*

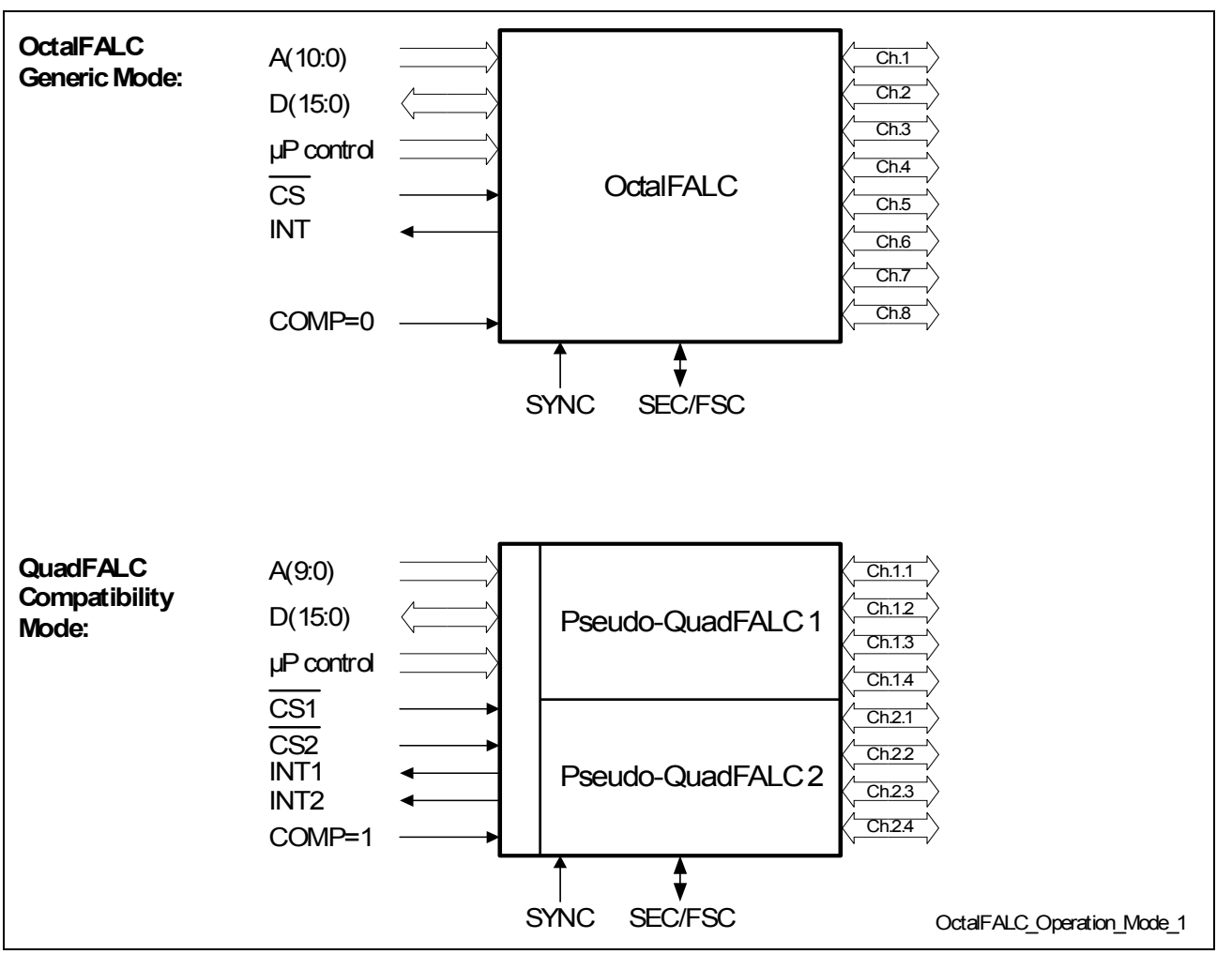

Figure 2 Basic Operation Modes for Microcontroller interface

Table 1 Overview Interface- and Basic Operation-Modes

Interface Mode	IM(1:0)	COMP	$\overline{CS}$	A(10)	A(9:0)	Basic Operation Modes
Intel or Motorola micro processor mode	0x	1	$\overline{CS1}$, for pseudo QuadFALC1	$\overline{CS2}$, for pseudo QuadFALC 2	10-bit parallel address	“Compatibility Mode”
		0	CS	11-bit parallel address		“Generic Mode”
SPI	10	Not valid	CS	Not valid; serial addresses are always 11 bit		
SCI	11					

In compatibility mode every global register exists one times in both of the pseudo QuadFALC®s : CIS, GPC(1:6), IPC, VSTR, GIS, GCM(1:8), GIMR, GIS2, GLC1, INBLDTR, DSTR and PRBSTS(1:4).

In compatibility mode (COMP = ´1´) the registers regarding the central clock PLL, GCM(1:8), exists one times in both of the pseudo QuadFALC®s, but the registers of the pseudo QuadFALC®2 are “dummys”: Writing and reading is possible but their values are not taken for any configuration of the PLL and writing on register GCM5 or GCM6 causes NO reset of the PLL. Only the registers GCM(1:8) of the pseudo QuadFALC®1 are taken for configuration of the PLL and writing on register GCM5 or GCM6 causes a reset of the PLL as in QuadFALC® or FALC56v2.1

In compatibility mode (COMP = ´1´) the status registers regarding the central clock PLL, GIS2 and GIMR, exists one times in both of the pseudo QuadFALC®s: The status of the one PLL is “doubled” and can be masked individually in every of the both pseudo QuadFALC®s.

In generic mode (COMP = ´0´) the registers GIMR, GIS2 and GCM(1:8) exist only one times in the whole device.

If compatibility mode is selected, the version status register VSTR shows the same value as in QuadFALC® V2.1 while the JTAG boundary scan ID is always the OctalFALC™ number and not affected by the compatibility mode selection.

3 Microcontroller Interface

The microcontroller interface is selected if IM(1:0) is strapped to ´00_B´ (Intel mode) or ´01_B´ (Motorola mode).

It is based on the existing QuadFALC® interface. An additional handshake signal (data acknowledge $\overline{\text{DTACK}}$ for Motorola- and $\overline{\text{READY}}$ for Intel-mode) is provided indicating successful read or write cycle. By using $\overline{\text{DTACK}}$ or $\overline{\text{READY}}$ respectively no counter is necessary in the microcontroller to finish the access.

The generation of $\overline{\text{READY}}$ is asynchronous:

In Intel mode read access $\overline{\text{READY}}$ will be set to low by the OctalFALC™ after the data output is stable at the OctalFALC™. After the rising edge of $\overline{\text{RD}}$ (which is driven by the micro controller), $\overline{\text{READY}}$ is low for a “hold time”, before it will be set to high by the OctalFALC™.

In the Intel mode write acces $\overline{\text{READY}}$ will be set to low by the OctalFALC™ after the falling edge of $\overline{\text{WR}}$ (which is driven by the micro controller). After $\overline{\text{WR}}$ is high and data are written successfully into the registers of the OctalFALC™, $\overline{\text{READY}}$ will be set to high by the OctalFALC™.

The general timing diagrams are shown in **Figure 3** to **Figure 7**:

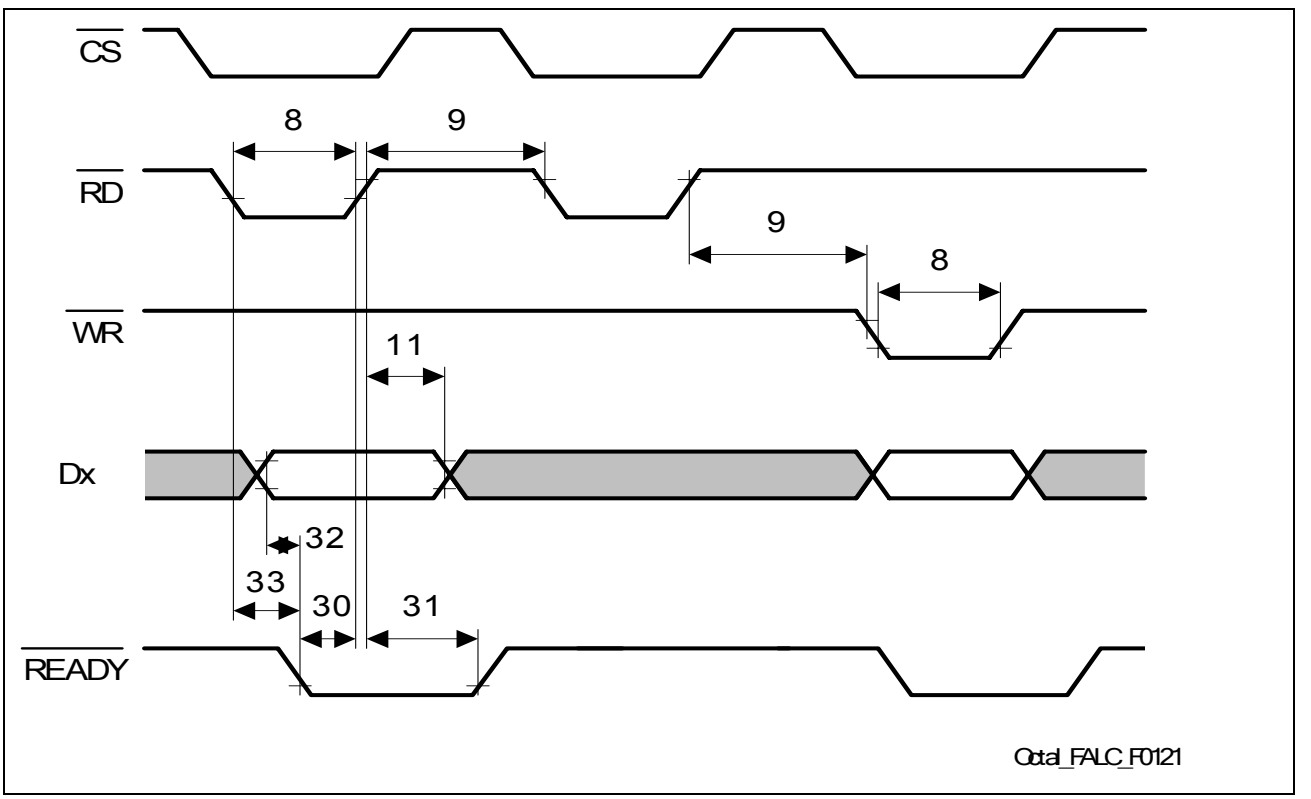

Figure 3 Intel Read Cycle Timing

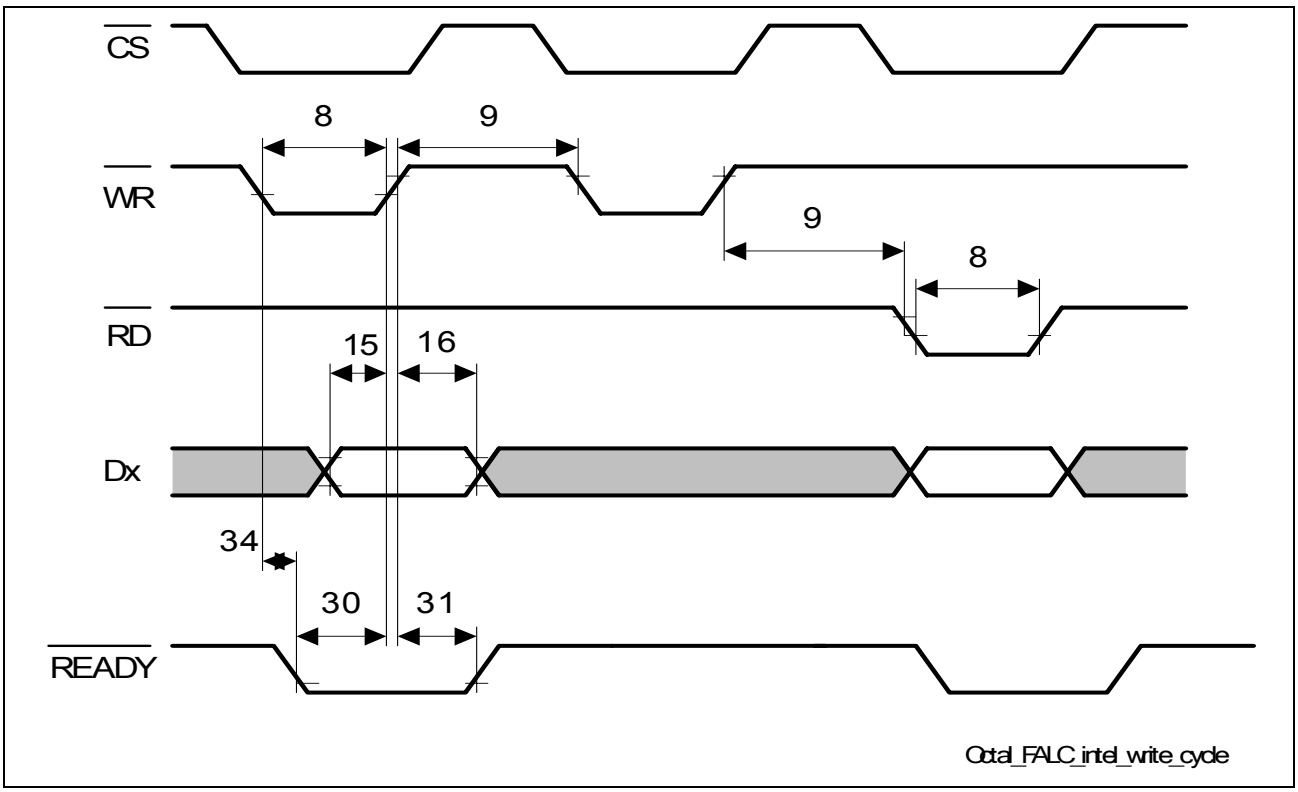

Figure 4 Intel Write Cycle Timing

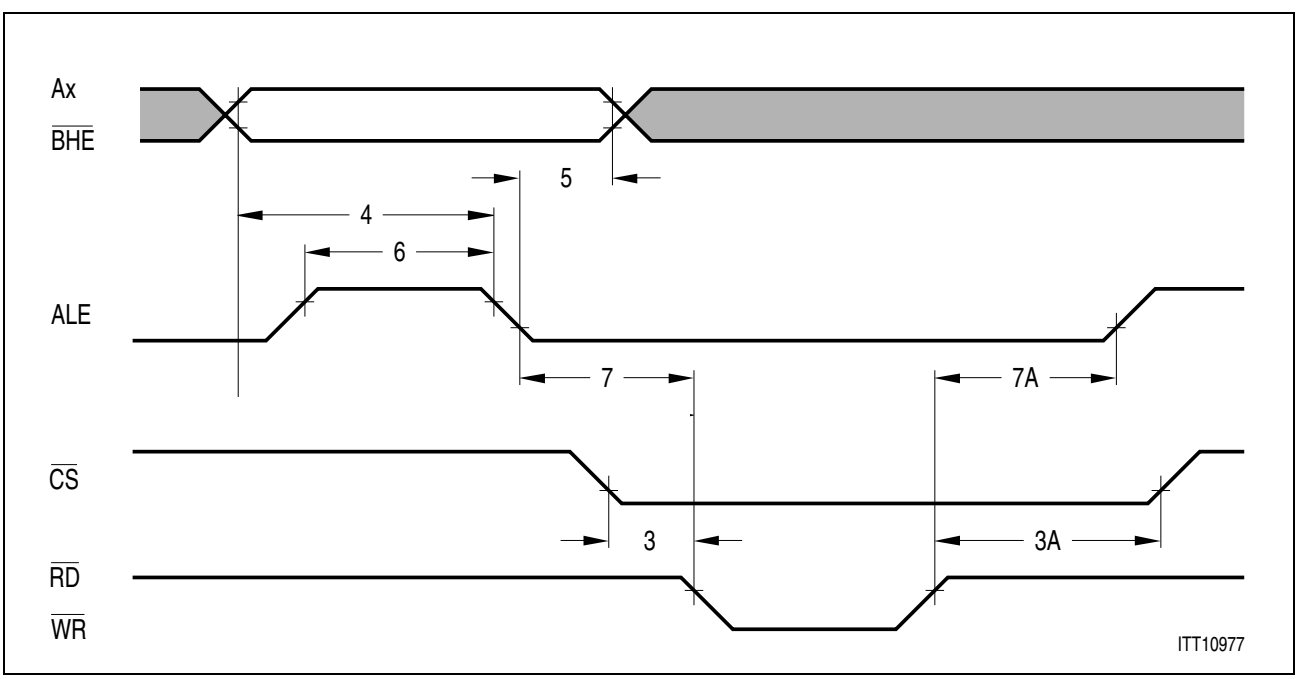

Figure 5 Intel Multiplexed Address Timing

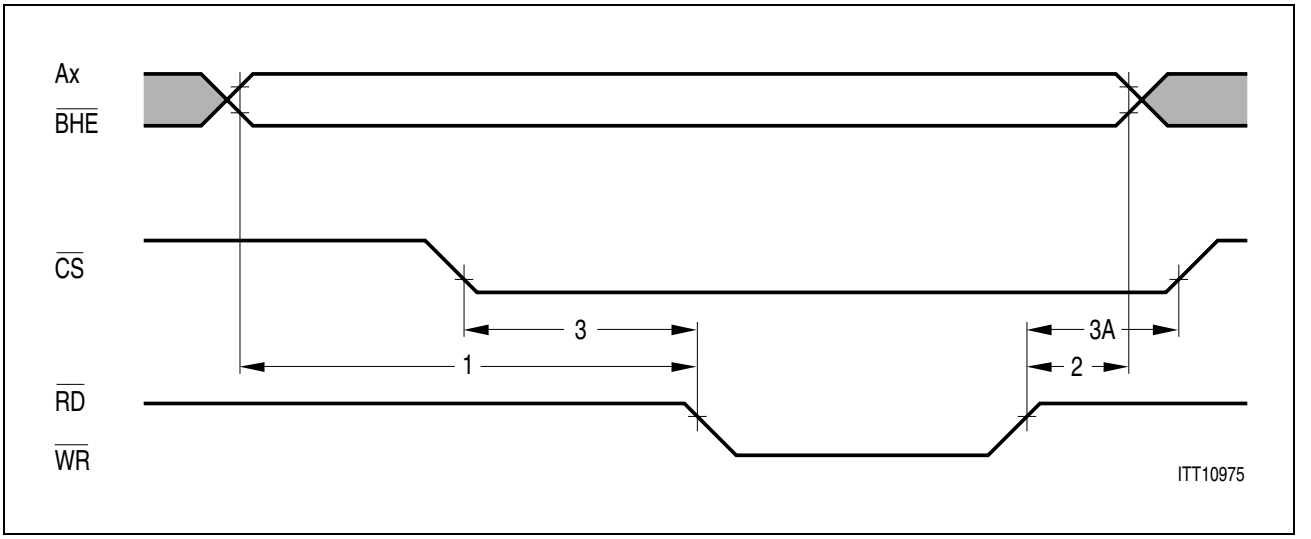

Figure 6 Intel Non Multiplexed Address Timing

Table 2 Intel Bus Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		Min.	Max.	
1	Address, $\overline{BHE}$ setup time	5		ns
2	Address, $\overline{BHE}$ hold time	0		ns
3	$\overline{CS}$ setup time	0		ns
3A	$\overline{CS}$ hold time	0		ns
4	Address, $\overline{BHE}$ stable before ALE inactive	20		ns
5	Address, $\overline{BHE}$ hold after ALE inactive	10		ns
6	ALE pulse width	30		ns
7	ALE setup time before $\overline{RD}$ or $\overline{WR}$	0		ns
7A	ALE hold time after $\overline{RD}$ or $\overline{WR}$	30		ns
8	$\overline{RD}$, $\overline{WR}$ pulse width	80		ns
9	$\overline{RD}$, $\overline{WR}$ control interval	70		ns
11	Data hold after $\overline{RD}$ inactive	10	30	ns
15	Data stable before $\overline{WR}$ inactive	30		ns
16	Data hold after $\overline{WR}$ inactive	10		ns

Table 2 Intel Bus Interface Timing Parameter Values (cont'd)

No.	Parameter	Limit Values		Unit
		Min.	Max.	
30	$\overline{WR}$ or $\overline{RD}$ delay after $\overline{READY}$	t.b.d.		ns
31	$\overline{READY}$ hold time after $\overline{RD}$ or $\overline{WR}$			ns
32	Data stable before $\overline{READY}$			ns
33	$\overline{RD}$ to $\overline{READY}$ delay			ns
34	$\overline{WR}$ to $\overline{READY}$ delay			ns

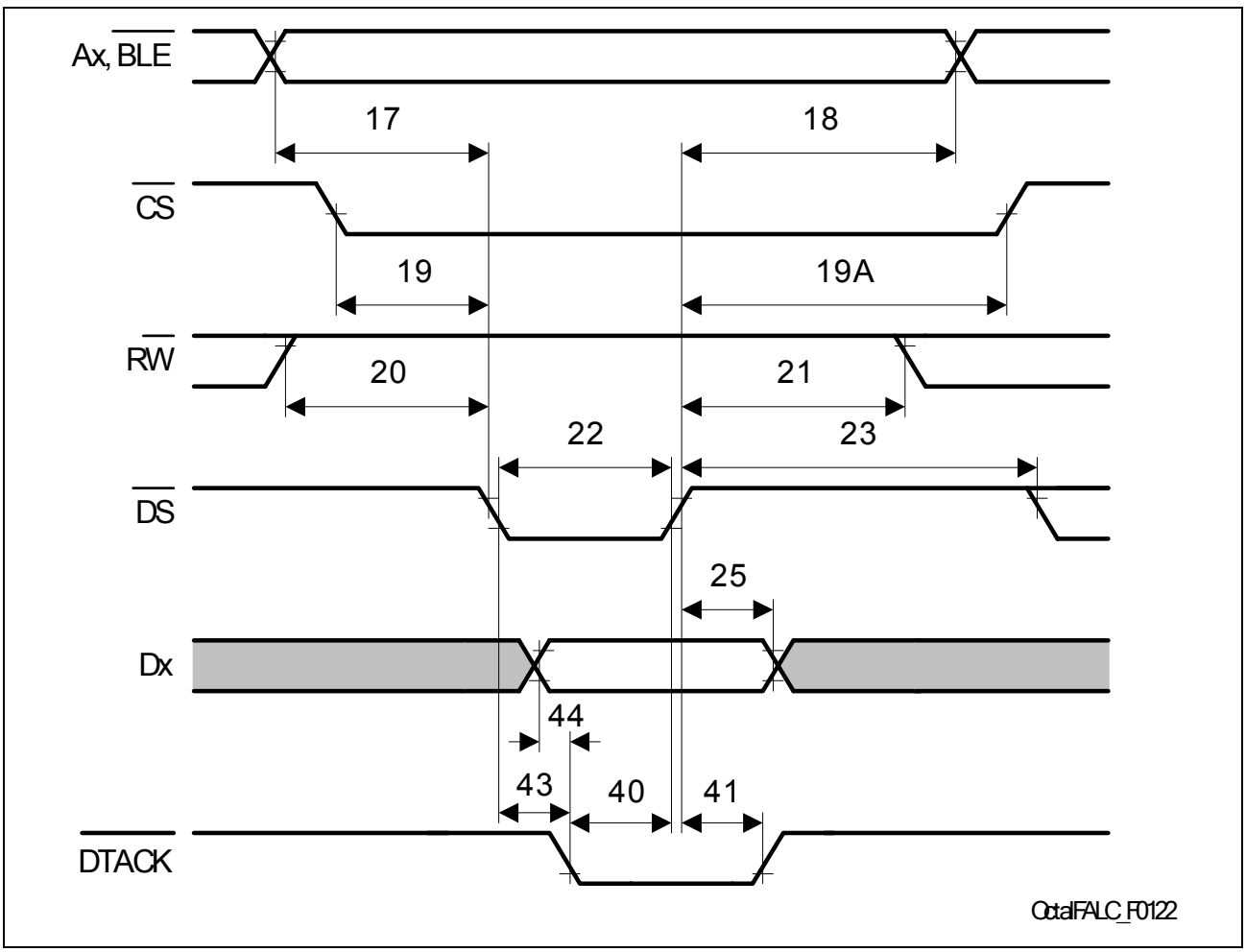

Figure 7 Motorola Read Cycle Timing

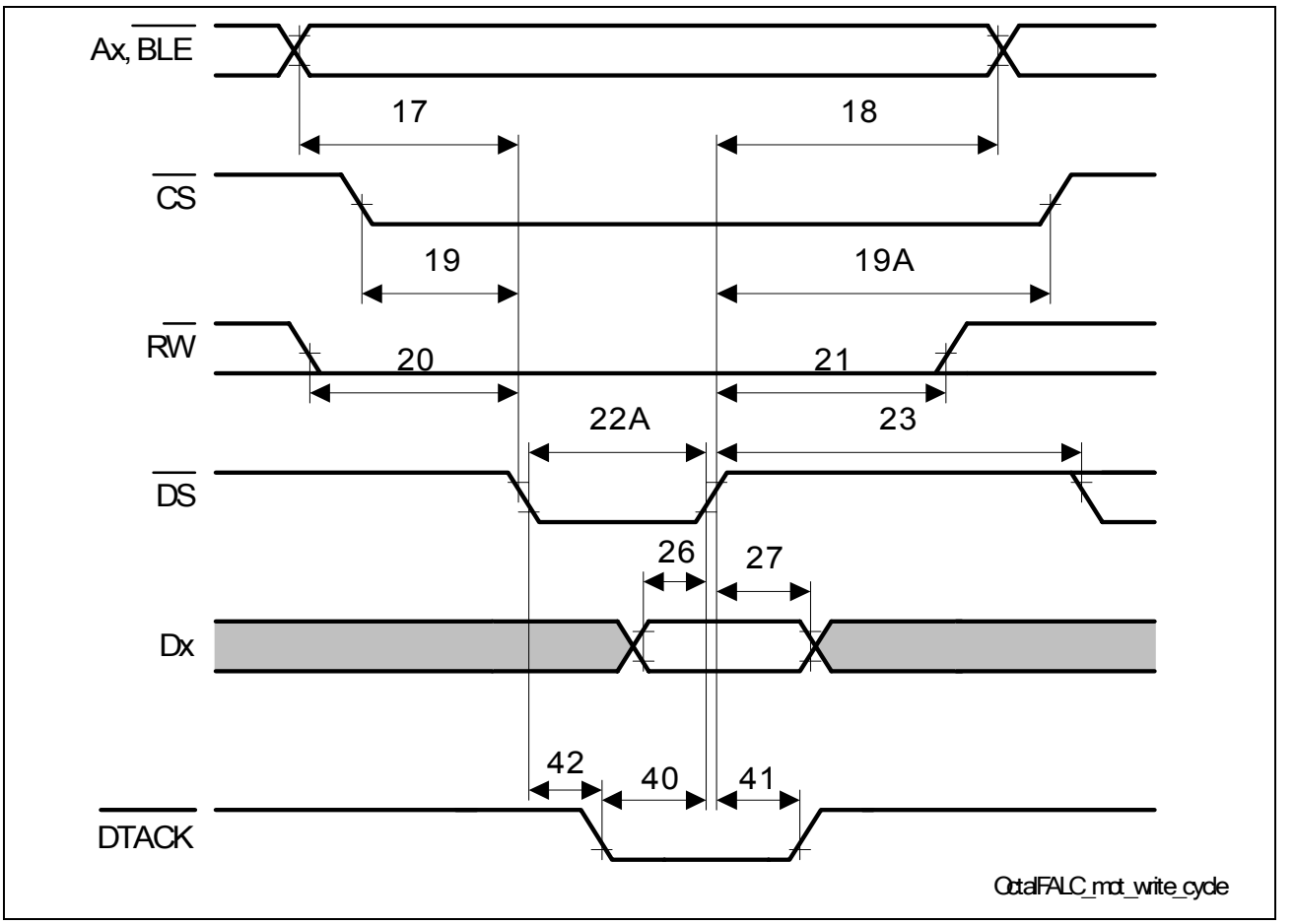

Figure 8 Motorola Write Cycle Timing

Table 3 Motorola Bus Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		Min.	Max.	
17	Address, BLE setup time before $\overline{DS}$ active	15		ns
18	Address, $\overline{BLE}$ hold after $\overline{DS}$ inactive	0		ns
19	$\overline{CS}$ active before $\overline{DS}$ active	0		ns
19A	$\overline{CS}$ hold after $\overline{DS}$ inactive	0		ns
20	R$\overline{W}$ stable before $\overline{DS}$ active	10		ns
21	R$\overline{W}$ hold after $\overline{DS}$ inactive	0		ns
22	$\overline{DS}$ pulse width (read access)	80		ns
22A	$\overline{DS}$ pulse width (write access)	70		ns
23	$\overline{DS}$ control interval	70		ns
24	Data valid after $\overline{DS}$ active (read access)		75	ns

Table 3 Motorola Bus Interface Timing Parameter Values (cont'd)

No.	Parameter	Limit Values		Unit
		Min.	Max.	
25	Data hold after $\overline{DS}$ inactive (read access)		30	ns
26	Data stable before $\overline{DS}$ active (write access)	30		ns
27	Data hold after $\overline{DS}$ inactive (write access)	10		ns
40	$\overline{DS}$ delay after $\overline{DTACK}$	t.b.d.		ns
41	$\overline{DTACK}$ hold time after $\overline{DS}$ inactive			ns
42	$\overline{DS}$ to $\overline{DTACK}$ delay for write			ns
43	$\overline{DS}$ to $\overline{DTACK}$ delay for read			ns
44	data stable before $\overline{DTACK}$			ns

4 Serial Interfaces

Two additional serial interfaces are included to enable device programming and controlling:

- Slave Serial Control Interface (SCI)
- Slave Serial Peripheral Interface (SPI)

By using the SCI Interface, the OctalFALC™ can be easily connected to Infineon interworking devices like the SDC16. The SCI is used as interface also in the Infineon SHDSL- and ADSL-PHYs so that implementation of different line transmission technologies on the same line card easily is possible. The SCI interface is a three-wire bus and optionally replaces the parallel processor interface to reduce wiring overhead on the PCB, especially if multiple devices are used on a single board. Data on the bus is HDLC encapsulated and uses a message-based communication protocol. The OctalFALC™ SCI interface is always a slave.

If SCI interface with multipoint to multipoint configuration is used, address pins A(5:0) are used for SCI source (slave) address pin strapping.

In compatibility mode (pin COMP = 1) these both new interfaces are also supported.

The four possible interface modes - two microconroller modes and two serial interface modes - are selected by using the interface mode selection pins IM(1:0). This selection is valid immediately after reset becomes inactive.

After changing of the interface mode by IM(1:0), a hardware reset must be applied.

Note that after a reset writing into or reading from OctalFALC™ registers using the SCI- or SPI-Interface is not possible until the PLL is locked: If the SCI-Interface is used no acknowledge message will be send by the OctalFALC™. If the SPI-Interface is used pin SDO has high impedance (SDO is pulled up by external resistor). To trace if the SPI

interface is accessible, the micro controller should poll for example the register DSTR so long as it read no longer the value ´F_H‘.

4.1 SCI Interface

The Serial Control Interface (SCI) is selected if IM(1:0) is strapped to ´11_H´.

The SCI interface of the OctalFALC™ is always a slave.

Figure 9 shows a first application using the SCI interfaces of some OctalFALC™s were point to point full duplex connections are realized between every OctalFALC™ and the microcontroller. Here the data out pins of the SCI interfaces (SCI_TXD) of the OctalFALC™s must be configured as push-pull (PP), see configuration registerbit PP in **Table 5**.

Figure 10 shows an application with Multipoint to multipoint connections between the OctalFALC™s and the microcontroller (half duplex). Here the data out pin of the SCI interfaces (SCI_TXD) of all OctalFALC™s must be configured as an open Drain (oD), see configuration registerbit PP in **Table 5**. Data out and data in pin (SCI_RXD) of every OctalFALC™ are connected together and build the common data line. Together with a common pull up resistor for the data line, all open Drain data out pins are building a wired And.

The IFX propritary Daisy-Chain approach is not supported.

The group address of the SCI interface after reset is ´00_H´. (Recommendation: set group address to ´$C4_H$´ by a configuration message, than it is disjunct to that of other infineon devices.)

In case of multipoint to multipoint applications the 6 MSBs of the SCI source address will be defined by pinstrapping of the address pins A5 to A0. The two LSBs of the SCI source address are constant ´10_B´, see **Table 5**. The SCI source address can be overwritten by a write command into the SCI configuration register. For applications with point to point connections for the SCI interface the source address is not valid.

Because 14 bits are used for the register addresses in the SCI interface macro the two MSBs of the 16 bit wide register addresses are set fixed to zero. (Because the MSBs for global addresses are ´00_H´ and the MSBs for local addresses exceeds not the 14-bit range, there is no problem.)

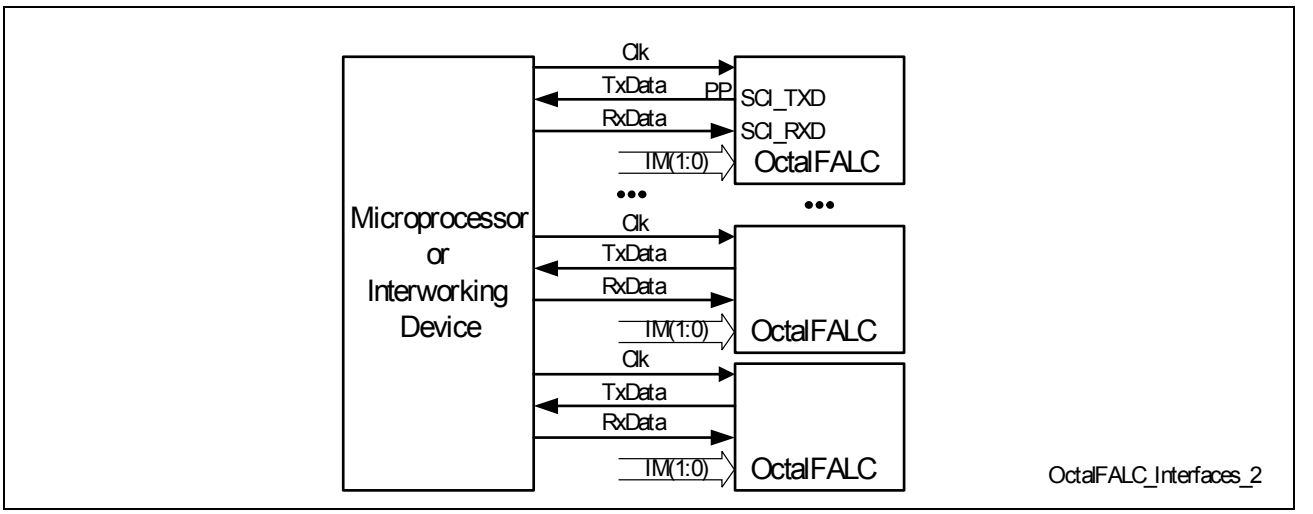

Figure 9 SCI interface Application with Point to Point Connections

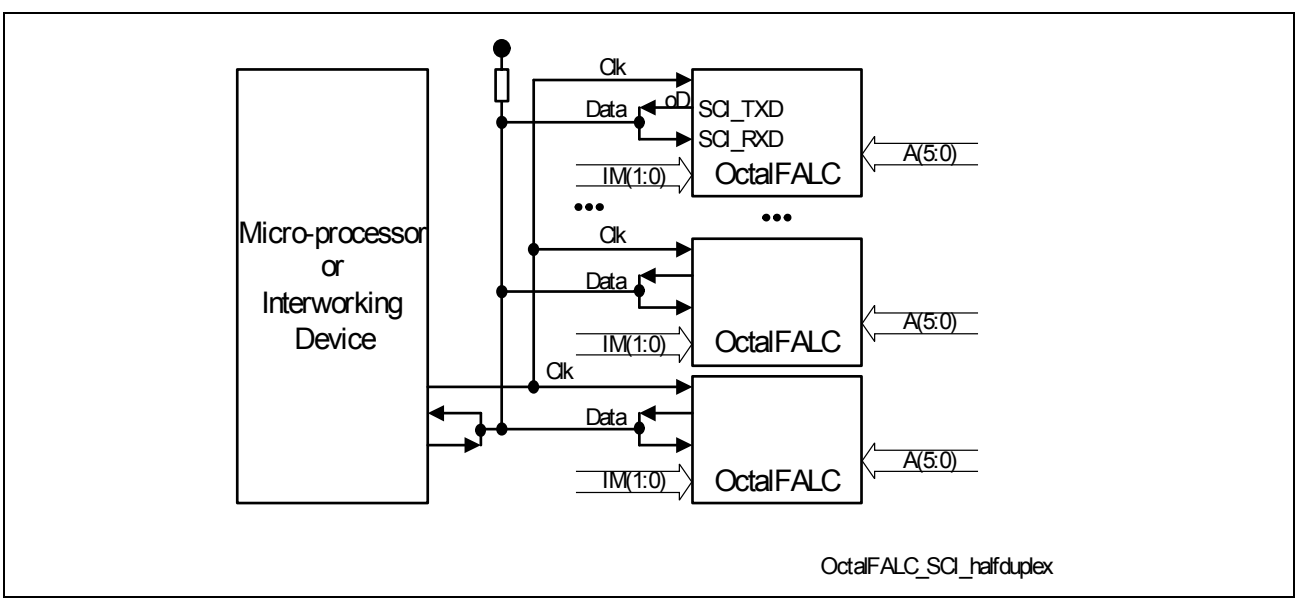

Figure 10 SCI interface Application with Multipoint to Multipoint Connection

The following configurations of the SCI interface of the OctalFALC™ can be set by the microcontroller by a write command into the SCI configuration register (control bits ´10_B´, see **Table 4**, SCI register address is ´0000_H´, see **Table 5** and **Figure 12**):

- Half duplex/full duplex (reset value: Half duplex), bit DUP
- OpenDrain/push-pull (configuration of output pin to openDrain/push-pull is in general independent of the duplex mode and must be set appropriately in application) (reset value: open Drain), bit PP
- CRC for transmit and receive on/off (reset value: off), bit CRC_EN
- Automatic acknowledgement of CMD messages on/off (reset value: off), bit ACK_EN
- Clock edge rising/falling (reset value: falling), bit CLK_POL
- Clockgating (reset value: off), bit CLK_GAT

The following SCI configurations are fixed and cannot be set by the microcontroller:

- Interrupt feature is disabled, bit INT_EN = ´0_B´
- Arbitration always made with LAPD (only SCI applications like in **Figure 9** and **Figure 10** are possible), bit ARB = ´0_B´

Recommendation for configuring: Set CRC, automatic acknowledgement and clock gating to ´on´.

The maximum possible SCI clock frequency is 6 MHz for point to point applications (full duplex) and about 2 MHz for multipoint to multipoint applications, dependent on the electrical capacity of the bus lines of the PCB.

Figure 11 shows the message structure of the OctalFALC™.

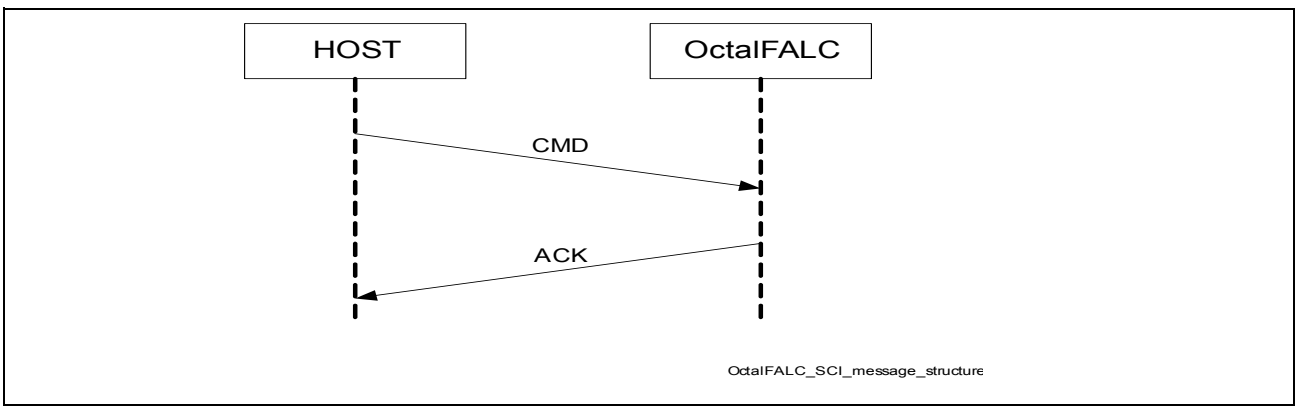

Figure 11 SCI Message Structure of OctalFALC™

Every write into or read from a register of the OctalFALC™ is initiated by a command message CMD from the Host (microconroller) and is then confirmed by an acknowledge message ACK from the OctalFALC™ if in the SCI configuration automatic acknowledgement is set (bit ACK_EN, see **Table 5**).

The frame structure of this messages are shown in **Figure 12**.

In general the LSB of every byte is transmitted first and lower bytes are transmitted before higher bytes (regarding the register address).

The HDLC flags mark beginning and end of all messages.

Source and destination addresses are 8 bits long. Only the first 6 bits are really used for addressing. The bit C/R (Command/Response) distinguishes between a command and a response. The bit MS (Master/Slave) is ´0_B´ for all Slaves and ´1_B´ for all masters, see **Table 5** and **Figure 12**.

The source address is defined by pinstrapping of A5 to A0 after reset, but other values can be configured by programming of the SCI configuration register.

The payload of the write CMD includes two control bits (MSBs of the payload), which distinguish between the different kind of commands, see **Table 4**, the 14 bit wide register address and the 8 bit wide data whereas the read CMD payload includes only the control bits and the register address. Register addresses can be either OctalFALC™ register

addresses or SCI configuration register addresses. Because of the address space of the OctalFALC™, really 11 LSBs of the 14 bit address are used in the OctalFALC™. The 3 MSBs are ignored.

The Frame Check Sequence FCS has16 bits.

The Read Status Byte RSTA of the acknowledge message shows the status of the received message and is built by the SCI interface of the OctalFALC™, see **Figure 13** and **Read Status Byte (RSTA) of the Acknowledge (ACK)**.

The destination address in the ACK message is always the source address of the corresponding CMD (the address of the microcontroller), see **Figure 13**, because no CMD messages will be sent by the OctalFALC™ SCI interface.

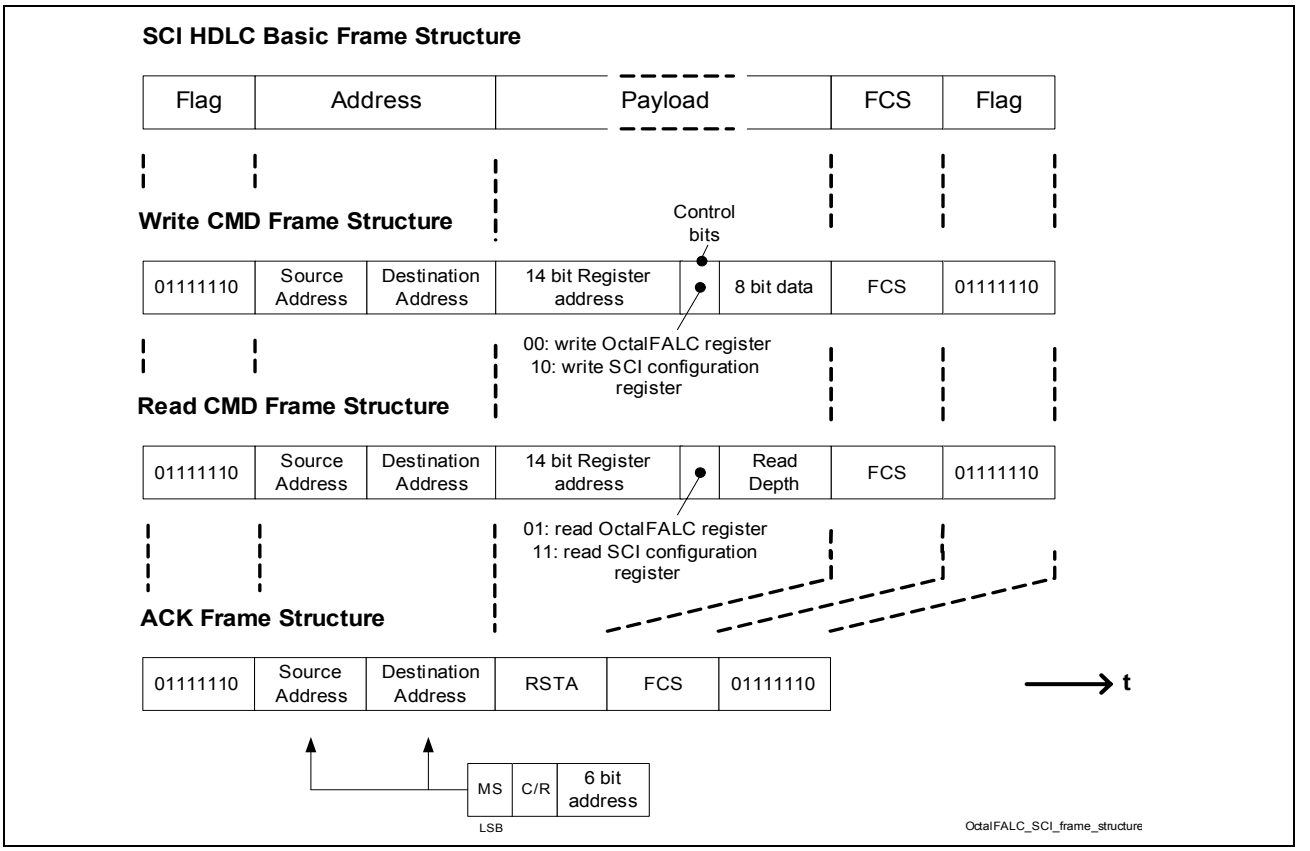

Figure 12 Frame Structure of OctalFALC™ SCI Messages

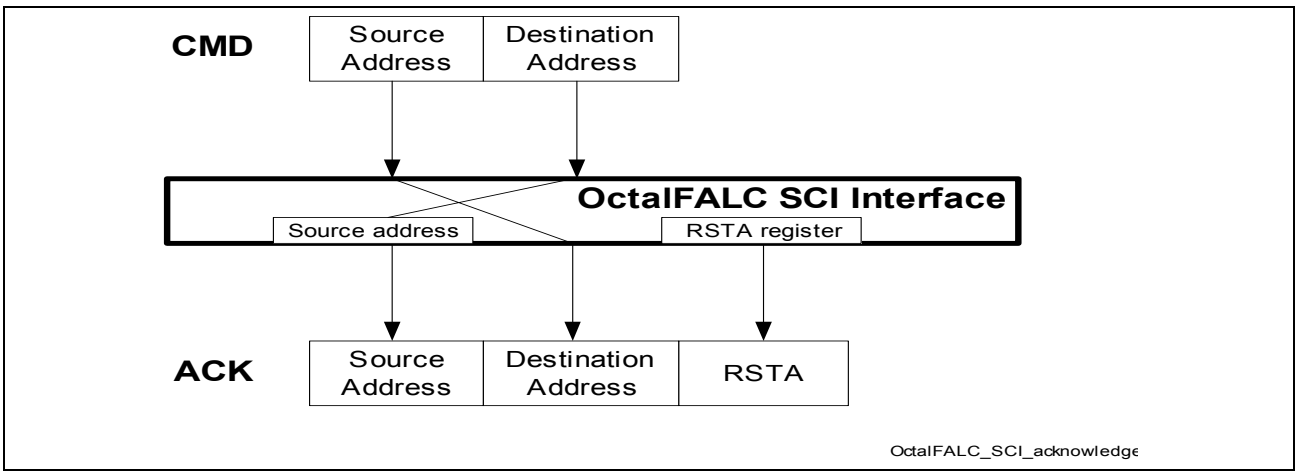

Figure 13 Principle of Building of Addresses and RSTA Bytes in the SCI ACK Message

Read Status Byte (RSTA) of the Acknowledge (ACK)

7 (MSB)	6	5	4	3	2	1	0 (LSB)
VFR	**RDO**	**CRC**	**RAB**	**SA(1:0)**		**C/R**	**TA**

Field	Bits	Description
VFR	7	**Valid Frame** Indicates whether a valid frame has been received. 0_B **VFR_0**, received frame is invalid. 1_B **VFR_1**, received frame is valid.
RDO	6	**Reserved**
CRC	5	**CRC Compare/Check** Indicates wether a CRC check is failed or not 0_B **CRC_0**, CRC error check failed on the received frame. 1_B **CRC_1**, received frame is free of CRC errors.
RAB	4	**Receive Message Aborted** CMD Message abortion is declared. The receive message was aborted by the Host. A sequence of seven consecutive ´1´was detected before closing the flag. 0_B **RAB_0**, data reception is in progress. 1_B **RAB_1**, data reception has been aborted. *Note: ACK message and therefore RAB will be send not before destination address was received.*

Field	Bits	Description
SA(1:0), C/R, TA	[3:0]	**Reserved**

Table 4 Definition of Control Bits in Commands (CMD)

Control Bits (MSB LSB)	Command Type
01	Read OctalFALC™ register
00	Write OctalFALC™ register
10	Write SCI configuration register
11	Read SCI configuration register

Table 5 SCI Configuration Register Content

Address	bit 7 (MSB)	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0 (LSB)
´0000$_H$´	PP	CLK_POL	CLK_GAT	ACK_EN	INT_EN	CRC_EN	ARB	DUP
´0001$_H$´	Source Address						1 (= C/R)	0 (= MS)
´0002$_H$´	Group Address						1 (= C/R)	0 (= MS)

Figure 14 shows the timing of the SCI interface and **Table 6** the appropriate timing parameter values.

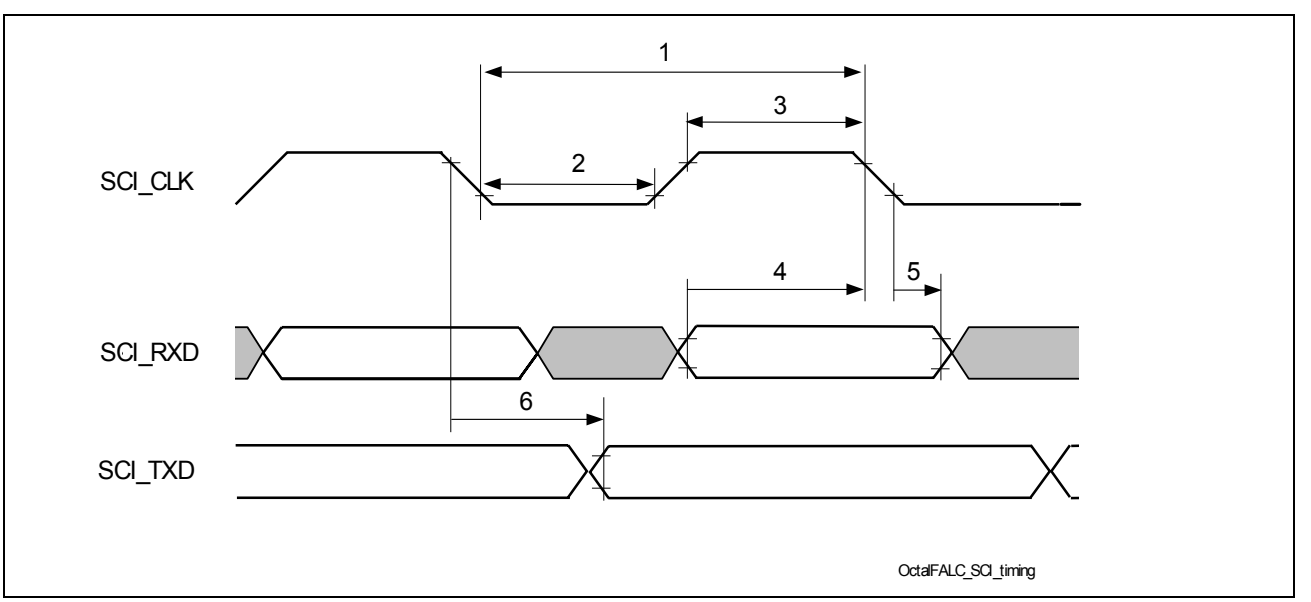

Figure 14 SCI Interface Timing

Table 6 SCI Timing Parameter Values

No	Parameter	Limit Values		Unit
		Min.	Max.	
1	SCI_CLK cycle time full duplex mode	170		ns
1	SCI_CLK cycle time half duplex mode	500		ns
2	SCI_CLK low time	t.b.d.		ns
3	SCI_CLK high time	t.b.d.		ns
4	SCI_RXD setup time before SCI_CLK	t.b.d.		ns
5	SCI_RXD hold time after SCI_CLK	0		ns
6	SCI_TXD delay time after SCI_CLK		t.b.d.	ns

4.2 SPI Interface

The Serial Peripheral Interface (SPI) is selected if IM(1:0) is strapped to ´10_H´.

The SPI interface of the OctalFALC™ is always a slave.

Figure 15 and **Figure 16** show the read and the write operation respectively. The start of a read or write operation is marked by the falling edge of the chip select signal $\overline{CS}$ whereas the end of the operations is marked by the rising edge of $\overline{CS}$. Because of $\overline{CS}$ the SPI interface has no slave address.

The first bit of the serial data in (SDI) is ´1_B´ for a read operation and ´0_B´ for a write operation. The first four bits of the 15 bit address are not valid for the OctalFALC™.

In read operation the OctalFALC™ delivers the 8 bit wide content of the addressed register at the serial data out (SDO).

In general SPI data are driven with the negative edge of the serial clock (SCLK) and sampled with the positive edge of SCLK. **Figure 17** shows the timing of the SPI interface and **Table** the appropriate timing parameter values.

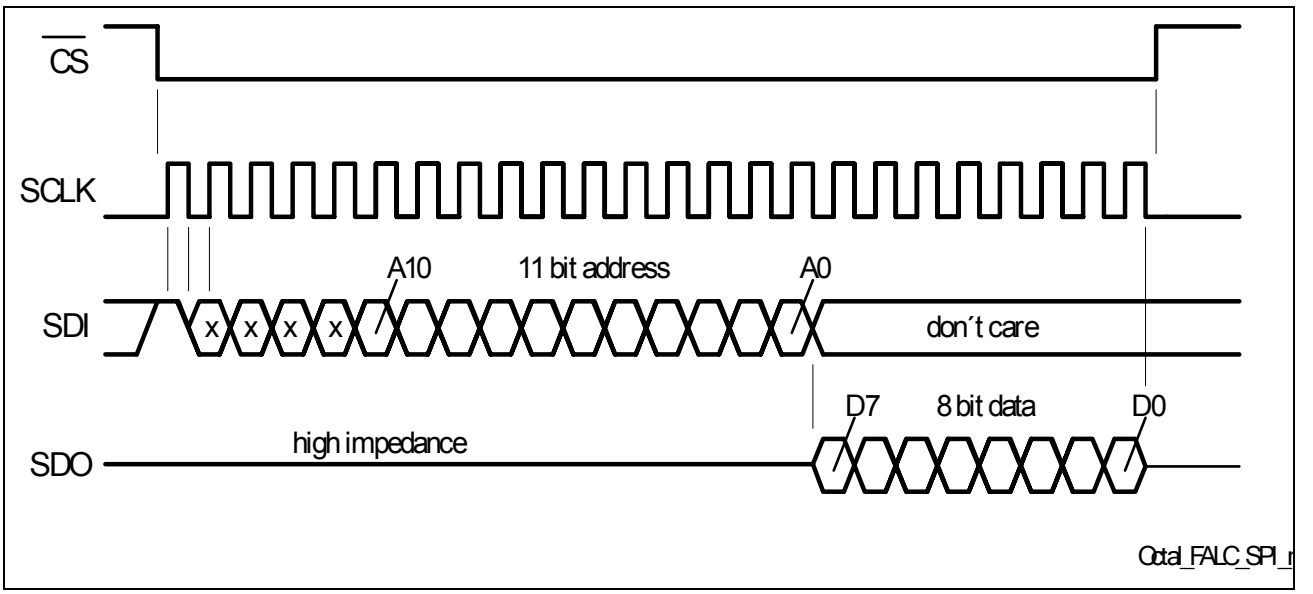

Figure 15 SPI Read Operation

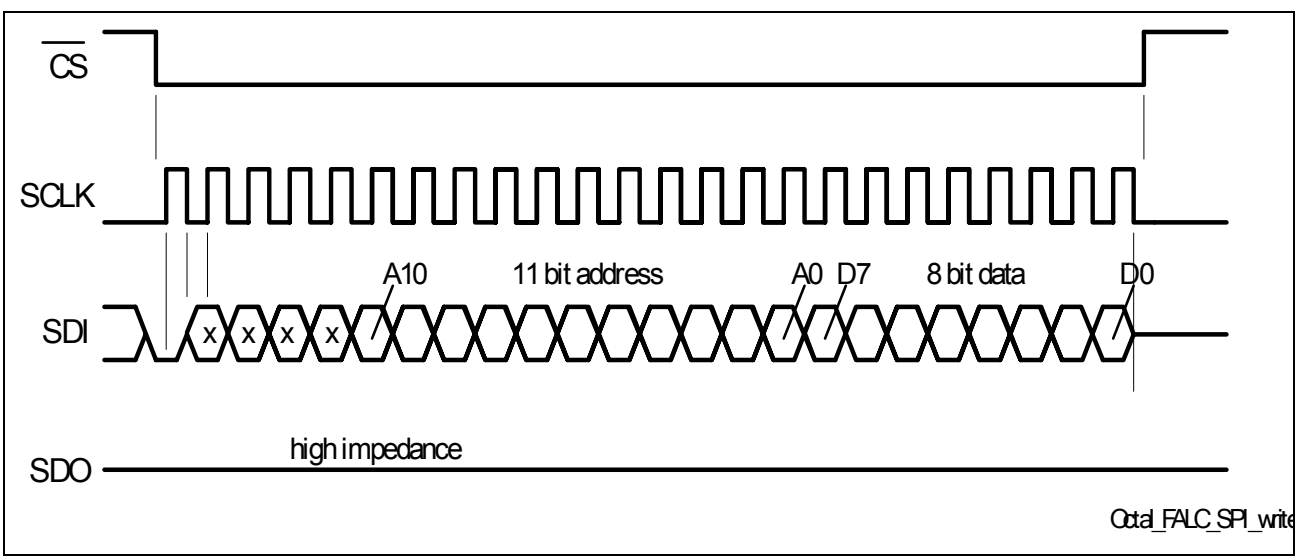

Figure 16 SPI Write Operation

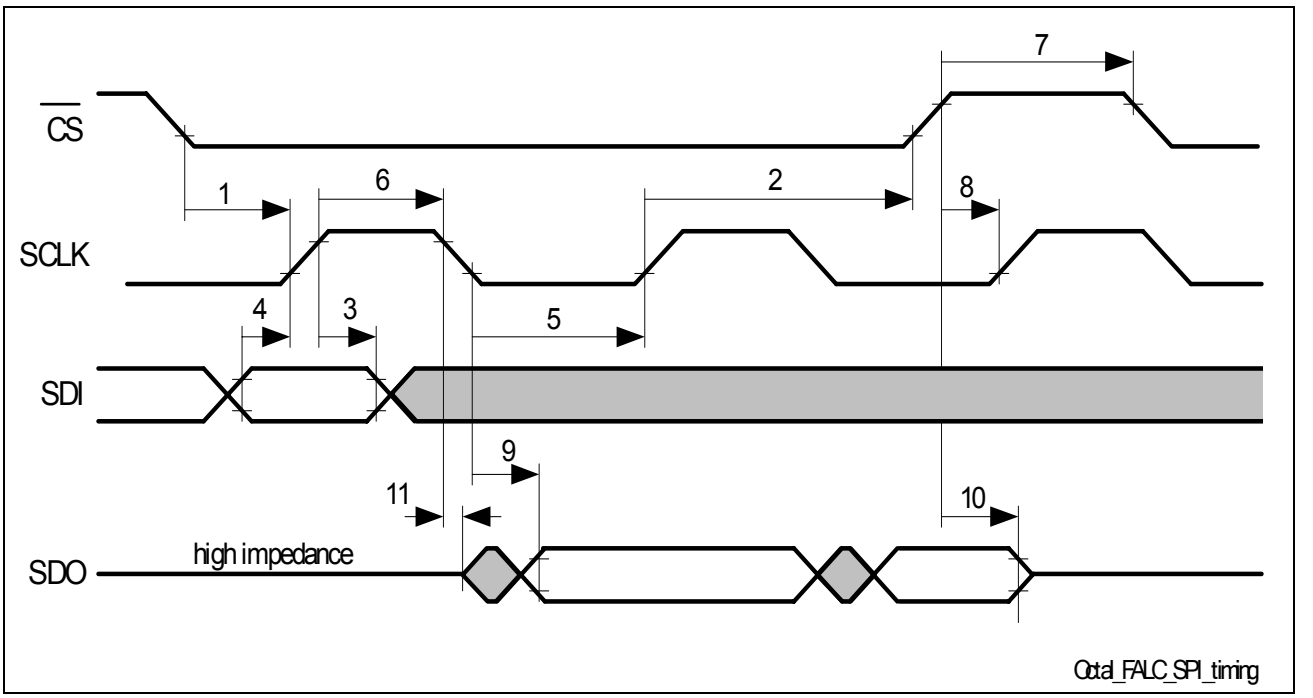

Figure 17 SPI Interface Timing

Table 7 SPI Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		Min.	Max.	
-	SCLK frequency		t.b.d.	MHz
1	$\overline{CS}$ setup time before SCLK	50		ns
2	$\overline{CS}$ hold time after SCLK	100		ns
3	SDI hold time after SCLK	150		ns
4	SDI setup time before SCLK	50		ns
5	SCLK low time	205		ns
6	SCLK high time	205		ns
7	$\overline{CS}$ high time	100		ns
8	Clock disable time before SCLK	50		ns
9	SDO output stable after SCLK		150	ns
10	SDO output hold after $\overline{CS}$ disable		50	ns
11	SDO output High Impedance after SCLK	0		

5 Clock Modes

5.1 Individual Receive Clock Selection

The source of every of the eight receive clocks (RCLK(8:1)) can be independently selected out of every of the eight channels. The additional registers GPC2 to GPC6 are used for controlling. GPC2 to GPC6 are not valid if COMP = ´1´. For COMP = ´1´ only the source of RCLK1 can be selected by the register GPC1 of the pseudo QuadFALC®1, RCLK2,3,4 sources are the appropriate channels. Equivalent, the RCLK5 source can be selected by the register GPC1 of the pseudo QuadFALC®2 and the sources of RCLK6,7,8 are the appropriate channels. For the principle see also **Figure 18**. After reset RCLK1 is sourced by channel 1 and RCLK5 is sourced by channel 5 and switched to the multi function ports RPC.

Note that in CT mode the DCO-R is always on.

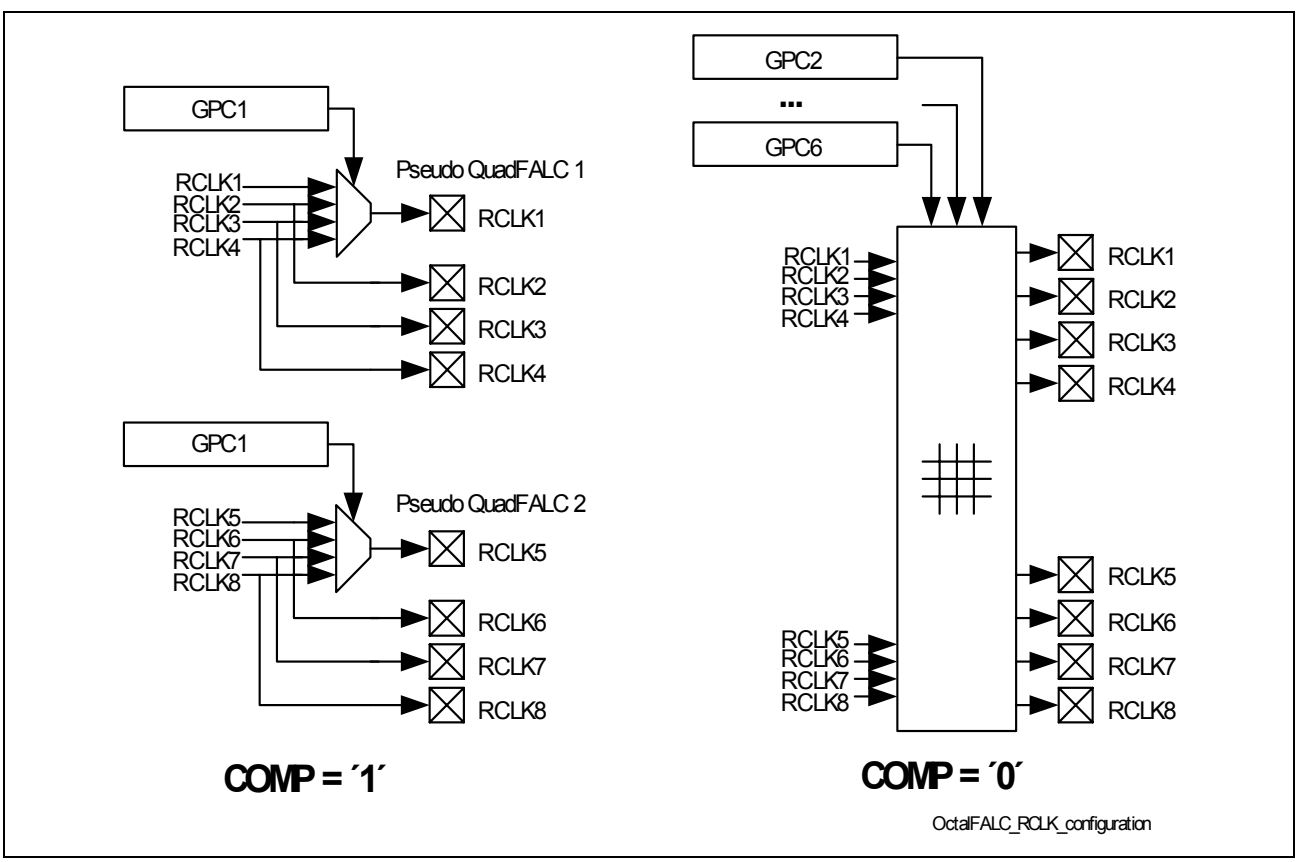

Figure 18 Receive Clock Selection

5.2 Transmit Clock Switching

The transmit clock can be automatically switched between TCLK and SCLKX. This enables an automatic switch over between different clock sources within the system in case the original clock source is lost. In general the clock switching is glitch free.

TCLK loss is detected if the transmit clock derived from TCLK failed to occur.

Automatic transmit clock switching is controlled by the register bit CMR4.ATCS.

If the TCLK input is used directly as transmit clock XCLK, the output of the DCO-X (CU-ADPLL-X) is not used. The DCO-X reference clock is SCLKX. If loss of TCLK is detected, the transmit clock will be switched automatically to the DCO-X output which is synchronous to SCLKX if CMR4.ATCS = ´1´. This switching is shown in the interrupt status bit ISR7.XCLKSS0 which is masked by IMR7.XCLKSS0. This switching cannot be done in general without occuring of phase jumps or spikes in the transmit clock XCLK. Additionally after loss of TCLK the transmit clock XCLK is also lossed during the “detection time” for loss of TCLK,

If the transmit clock XCLK is sourced by the DCO-X output and the DCO-X reference clock is TCLK, the DCO-X reference will be switched to SCLK after a loss of TCLK was detected if CMR4.ATCS = ´1´. This switching is shown in the interrupt status bit ISR7.XCLKSS1 which is masked by IMR7.XCLKSS1.

In that case, the transmit clock XCLK fullfils the jitter-, wander- and frequency deviation-requiements as specified for E1/T1 after the clock source of the DCO-X was changed. Slipping of the (active) transmit buffer should be avoided.

Comment: TCLK is sourced by RCLK in normal application, so loss of TCLK happens because of loss of RCLK.

5.3 TCLK Frequency

TCLK supports 1.544, 3.088, 6.176, 12.352 and 24.704 MHz in T1/J1 mode and 2.048, 4.096, 8.192, 16.384 and 32.768 MHz in E1 mode and in T1/J1 channel translation mode. If COMP = ´0´controlling is done by the register CMR5, bits STF(2:0), if COMP = ´1´ controlling is done by the register CMR1, bit STF.

5.4 RCLK Frequency

RCLK supports 1.544, 3.088, 6.176, and 12.352 in T1/J1 mode and 2.048, 4.096, 8.192, and 16.384 MHz in E1 mode and in T1/J1 channel translation mode. If COMP = ´0´controlling is done by the register CMR4, bits RS(1:0), if COMP = ´1´ controlling is done by the register CMR1, bits RS(1:0). If the recovered clock out (of the clock data recovery) is the source of RCLK then only 2.048 MHz (1.544,) is possible. If the DCO-R is the source of RCLK all above described frequencies are possible.

5.5 DCO-R/DCO-X Characteristics

The corner frequencies of DCO-R and DCO-X can be adjusted in a wider range. Proposal: The DCO-X and the DCO-R (2nd order PLLs) must have eigenfrequencies in the range 8 Hz to 0.2 Hz, for example 8 Hz, 4 Hz, 2 Hz, 1 Hz, 0.5 Hz, 0.25 Hz, 0.125 Hz

and should have an attunation factor of about 1.1 (minimum of equivalent noise bandwidth) for minimum jitter at the output. The appropriate P- and I- factors of the PLL loop filter and registerbits of CMR3 and CMR6 are to be defined.

The corner frequencies after reset are 2 Hz and can be switched to 0.2 Hz with the register bit LIM2.SCF for the receive direction (DCO-R) and with the register bit CMR5.SCFX for the transmit direction (DCO-X) if corner frequency adjust is not enabled by the register bit CMR2.ECFAX or CMR2.ECFAR respectively.

If corner frequency adjust is enabled it can be individually configured by using the registers CMR3, CMR4 and CMR5.

The adaption speed can be adjusted..

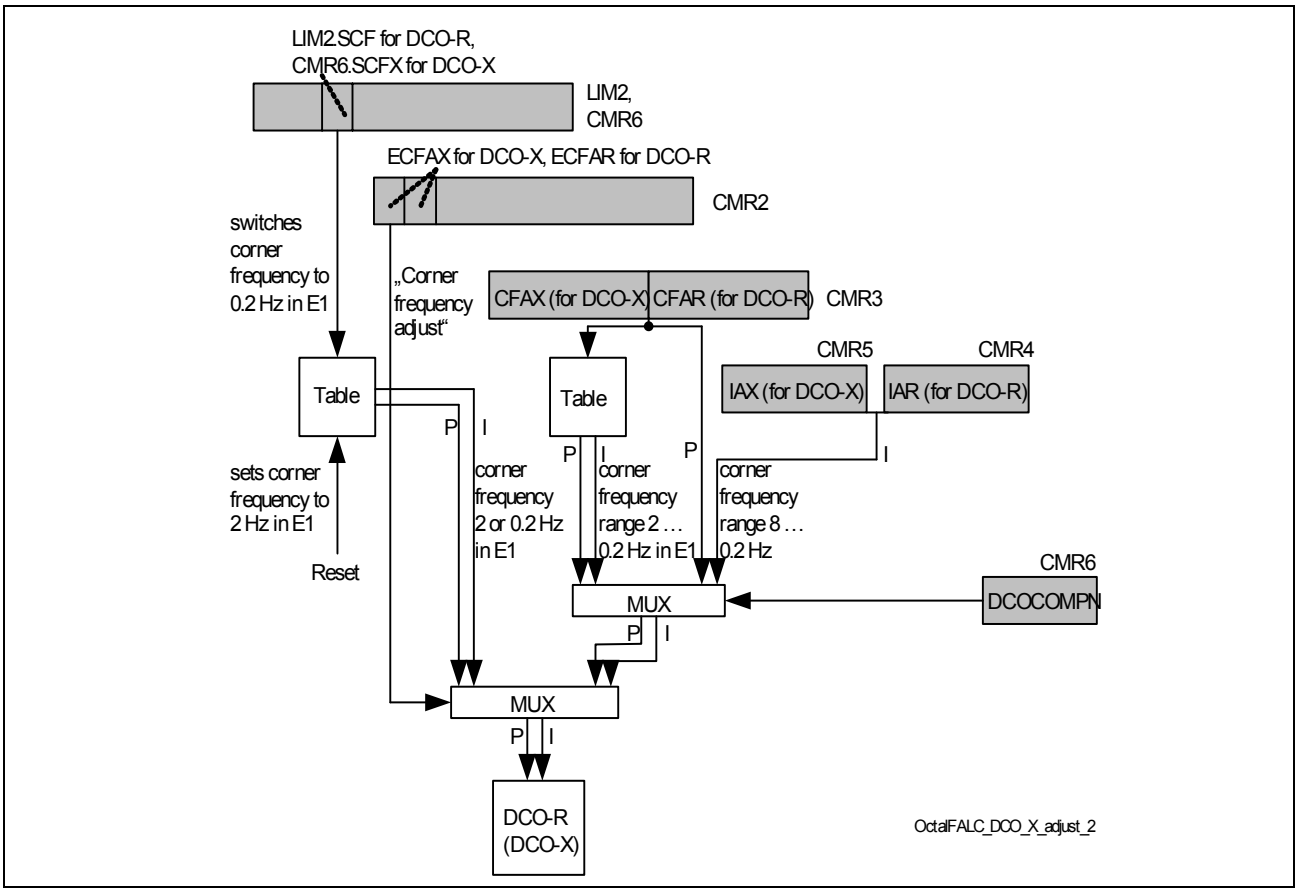

Figure 19 Principle of Setting Parameters of the DCO-X and DCO-R

5.6 PLL Reset and Configuring

The OctalFALC™ provides a flexible clocking unit, which references to any clock in the range of 1.02 to 20 MHz supplied on pin MCLK, see **Figure 20**.

The clocking unit has two different modes:

- In the “flexible master clocking mode” (GCM2.VFREQ_EN = ´1´) the clocking unit has to be tuned to the selected reference frequency by setting the global clock mode

registers GCM(8:1) accordingly, see formulas in GCM6 description. All eight ports can work in E1 or T1 mode individually. After reset the clocking unit is in “flexible master clocking mode”.

- In the “clocking fixed mode” (GCM2.VFREQ_EN = ´0´) the tuning of the clocking unit is done internally so that no setting of the global clock mode registers GCM(8:1) is necessary. All eight ports must work together either in E1 or in T1 mode.

For the calculation for the appropriate register settings the “flexible Master Clock Calculator” can be used which is part of the software support of the OctalFALC™.

All required clocks for E1 or T1/J1 operation are generated by the device internally. The global setting depends only on the selected master clock frequency and is the same for E1 and T1/J1 because both clock rates are provided simultaneously.

To meet the E1 requirements the MCLK reference clock must have an accuracy of better than ± 32 ppm. The synthesized clock can be controlled on pins RCLK, SCLKR and XCLK.

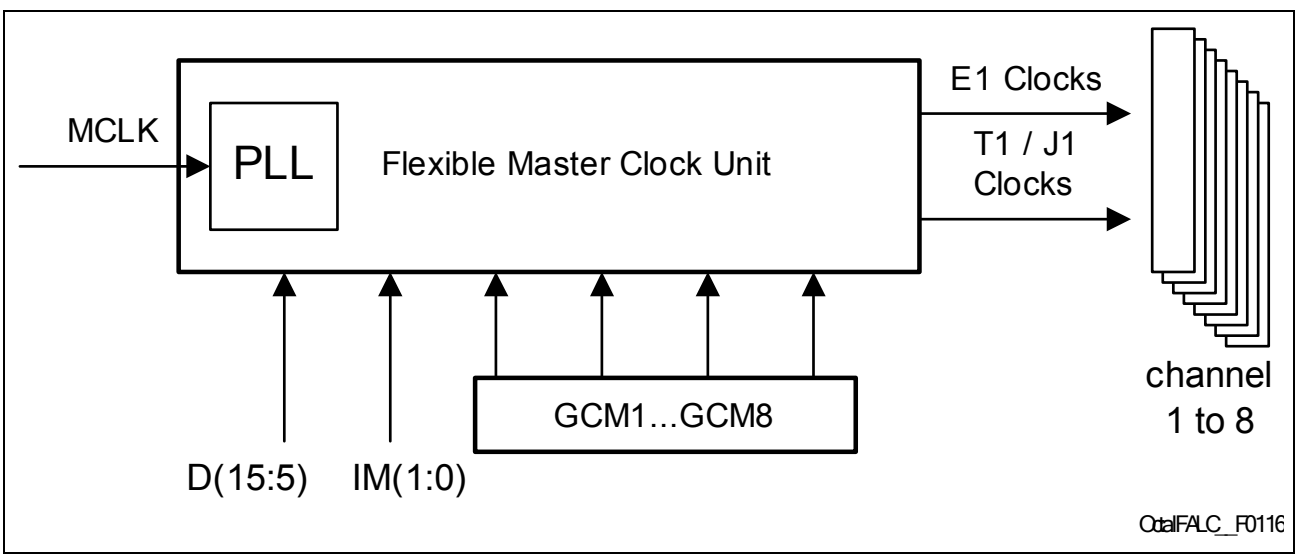

Figure 20 Flexible Master Clock Unit

If the (asynchronous) microcontroller interface mode is selected by IM(1:0) the PLL must be configured either

- By programming of the registers GCM5 and GCM6 in “flexible master clocking mode”. Every change of the contents of these registers - the divider factors N and M of the PLL - causes a reset of the PLL. Switching between E1 and T1 modes in arbitrary channels causes a reset of the clock unit but not of the PLL itself.
- Or by enabling of the ” fixed mode”: GCM2.VFREQ_EN = ´0´. Programming of registers GCM5 and GCM6 is not necessary. Any programming of GCM5 and GCM6 does NOT cause a reset of the PLL. Switching between E1 and T1 modes (for all channels) causes a reset of the clock unit but not of the PLL itself.

The SPI and SCI are synchronous interfaces and therefore need defined clocks immediately after reset, before any device configuration is done. To enable access to

serial interfaces, the clock MCLK must be active and must have a defined frequency before reset becomes inactive. Depending on the supplied MCLK frequency the internal PLL must be configured if the SCI- or SPI-Interface mode is selected by IM(1:0). This can be performed either

- By strapping of the pins D(15:5) if “flexible master clocking mode” is enabled (GCM2.VFREQ_EN = ´1´). Because the “flexible master clocking mode” is enabled after reset, pinstrapping at D(15:5) is always necessary! Every status change of the signals at these pins causes a reset of the PLL. Configuring by the registers GCM5 and GCM6 has no effect and does not cause a reset of the main PLL
- Or by usage of the ”clocking fixed mode” (GCM2.VFREQ_EN = ´0´). **This is only allowed if the values of N and M defined by pinstrapping are identical to that values which are internally used for the “clocking fixed mode”.** This avoids changing of N and M by switching into the ”clocking fixed mode” and therefore a new reset of the PLL. (A reset of the PLL can cause a reset of the hole transceiver! Clock and data processing will be interrupted.) The used values of N and M in “clocking fixed mode” are: N = ´33_{10}´, M = ´0_{10}´. This requires the pinstrapping configuration to be: D(10:5) = ´HLLLLH´, D(15:11) = ´LLLLL´. In ”clocking fixed mode” further programming of the registers GCM1 to GCM8 is no longer necessary. The pinstrapping configuration at the pins D(15:5) do not have any effect. Changing of these values does NOT cause a reset of the PLL. Switching between E1 and T1 modes causes a reset of the clock unit but not of the main PLL itself.

The configuration of the PLL by pinstrapping in case of serial interface modes is done in the same way as by using the registers GCM5 and GCM6 if asynchronous micro controller interface mode (Intel or Motorola) is selected. Calculation of the values to be configured by pinstrapping can be done also by using the formulas described for the registers GCM6 or by using the “flexible Master Clock Calculator” which is part of the software support of the OctalFALC™. If the serial interfaces are selected, pinstrapping of D(15:5) configures the PLL directly, so changes causes a direct reset of the PLL.

The conditions to trigger a reset of the central clock PLL are listed in **Table 8**. Every reset of the PLL causes a reset of the clock system.

Table 8 Conditions for a PLL Reset

Reset Pin	GCM2.VFREQ_EN	Used controller interface	A PLL reset is made...
active	x (will be set to ´1´by reset	x	always

Table 8 Conditions for a PLL Reset (cont'd)

Reset Pin	GCM2.VFREQ_EN	Used controller interface	A PLL reset is made...
inactive	1	asynchron (Motorola or Intel)	if GCM5 or GCM6 are written and their values N or M changes
		SCI or SPI	if pinstrappng values change
	0	asynchron (Motorola or Intel)	never
		SCI or SPI	if pinstrappng values change
	0 -> 1 or 1 -> 0	asynchron (Motorola or Intel)	if actual values of N or M in GCM5 in GCM6 are different to internal settings of the "fixed mode"
		SCI or SPI	if pinstrap values in are different to internal settings of the "fixed mode". **That is not allowed**

5.7 PLL Interrupt Status Bits

If the central clock PLL status indication bit GIS2.PLLLS *changes*, an interrupt is generated. An additional bit GIS2.PLLLC is provided to indicate the change. Masking can be made by GIMR.PLLL. The visibility of PLLLC can be set by the register bit IPC.VISPLL.

For COMP = ´1´ both of the pseudo QuadFALC®s have its own (interrupt) status register GIS2 and mask register GIMR. The status of the one PLL is "doubled" for the two status registers . So masking or setting of the visibility can be made Individulally in both of the pseudo QuadFALC®s.

The status bit PLLLS is only available for COMP = ´1´, but the status of the PLL is shown in GIS2.PLLLS independent on the value of COMP.

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6 Framer Features

6.1 Remote Defect Indication (E1 only)

In E1 mode, Remote Defect Indication (RDI) is implemented in compliance with ITU-T G.775 (chapter 6):

Criteria for detection and clearance of a Remote Defect Indication (RDI) defect, chapter 6.1 and 6.2:

“A Remote Defect Indication (RDI) defect at 2048 kbit/s TS-16 path termination functions is detected (status register bit FRS1.RDI) when the incoming signal has the "alarm indication to the remote" bit set to binary ONE ("1") for z consecutive CAS multiframe periods, where z = 1 ...5. z is not provisionable.

The RDI defect is cleared when the incoming signal has the "alarm indication to the remote end" bit set to binary ZERO ("0") for z consecutive CAS multiframe periods.

Note: The alarm indication to the remote end bit is the "y bit" in TS-16´s frame 0 of the CAS multiframe defined in 5.1.3.2.2/G.704.”

“A Remote Defect Indication (RDI) defect at 2048 kbit/s path termination functions is detected when the incoming signal has the "Remote alarm indication" bit set to binary ONE ("1") for z consecutive double frame periods, where z = 2,...5. z is not provisionable.

The RDI defect is cleared when the incoming signal has the "Remote alarm indication" bit set to binary ZERO ("0") for z consecutive double frame periods.

Note: The Remote alarm indication bit is the "A bit" in the 2048 kbit/s frame defined in Recommendation G.704.”

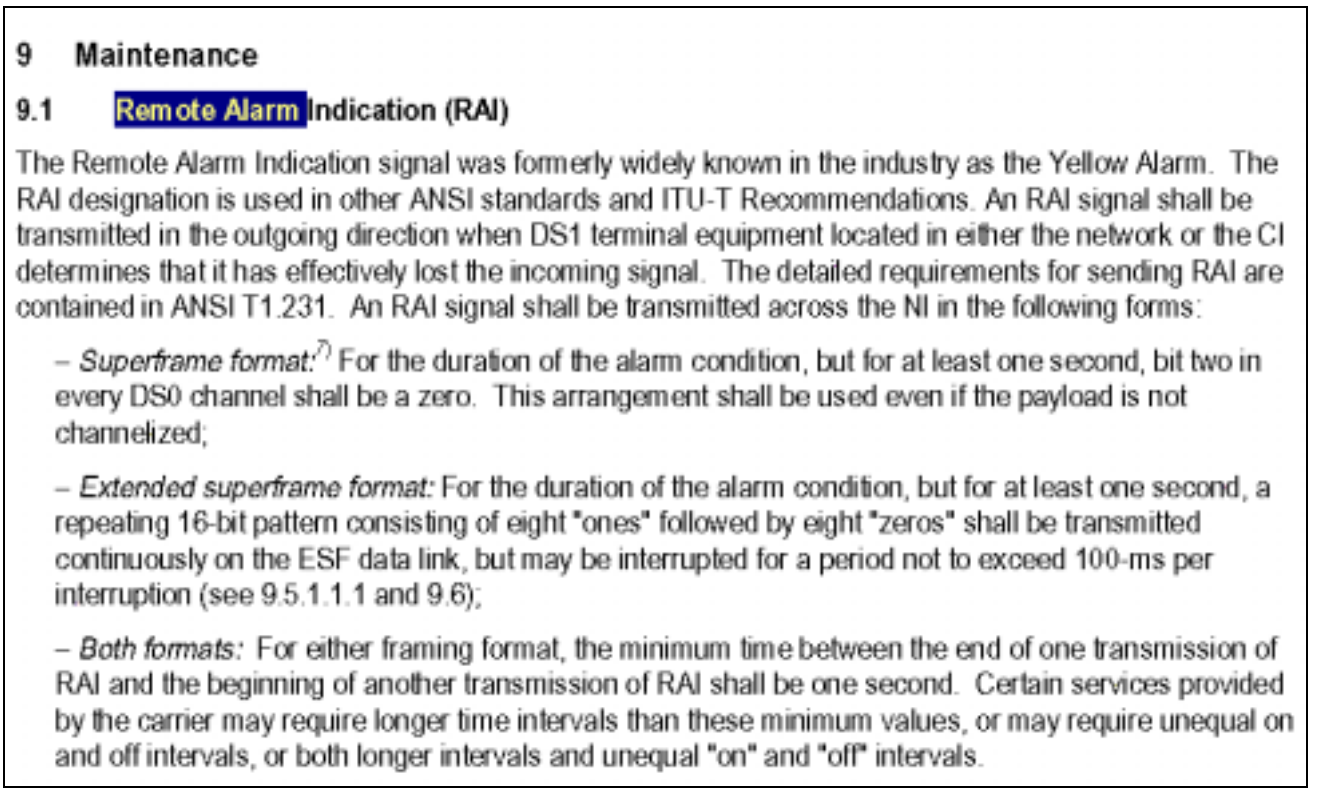
Implementation:

Controlling of the number (z) of multiframe periods or double frame periods is performed by the register bits FMR4.RDIS(1:0) and FMR4.RDIC(1:0). The RDI bit FRS1.RDI is a status bit, not an interrupt status bit.

6.2 Automatic Sending of Transmit Remote Alarm (T1/J1 only)

Note: As in FALC56 V2

In T1/J1 mode, the Automatic Remote Alarm feature (AXRA) is now compliant with ANSI T1.403-1999 (see **Figure 21**).(The one-second requirement for on/off must be fulfilled.)



9 Maintenance

9.1 Remote Alarm Indication (RAI)

The Remote Alarm Indication signal was formerly widely known in the industry as the Yellow Alarm. The RAI designation is used in other ANSI standards and ITU-T Recommendations. An RAI signal shall be transmitted in the outgoing direction when DS1 terminal equipment located in either the network or the CI determines that it has effectively lost the incoming signal. The detailed requirements for sending RAI are contained in ANSI T1.231. An RAI signal shall be transmitted across the NI in the following forms:

– *Superframe format:*7) For the duration of the alarm condition, but for at least one second, bit two in every DS0 channel shall be a zero. This arrangement shall be used even if the payload is not channelized;

– *Extended superframe format:* For the duration of the alarm condition, but for at least one second, a repeating 16-bit pattern consisting of eight "ones" followed by eight "zeros" shall be transmitted continuously on the ESF data link, but may be interrupted for a period not to exceed 100-ms per interruption (see 9.5.1.1.1 and 9.6);

– *Both formats:* For either framing format, the minimum time between the end of one transmission of RAI and the beginning of another transmission of RAI shall be one second. Certain services provided by the carrier may require longer time intervals than these minimum values, or may require unequal on and off intervals, or both longer intervals and unequal "on" and "off" intervals.

Figure 21 AXRA Requirements

6.3 RSC Interrupt (T1/J1 only)

The RSC interrupt can be suppressed for cleared channels to reduce the interrupt load. Suppression mode is selected by CCR1.RSCC = 1.

6.4 DL-Bit Access (T1/J1 only)

In T1/J1 ESF mode the DL-bit access is improved to reduce the number of required register accesses by 25%. For details see **Figure 22** and **Figure 23**. The optional mode is selected by the new register bit FMR5.DLM. The transmit direction works accordingly.

BOM-Codes can be inserted continuously without additional microcontroller access every multiframe.

The BOM code has the following format: 11111111 0xxxxxx0 were the left bit here of every byte is the MSB and the right one is the LSB. (11111111 is the BOM flag, xxxxxx is the BOM code) That´s another ordering as in ANSI T1.403, 1999, table 4 !!. Sending is done as for HDLC: LSB first. That´s consistent to the note 1) in the ANSI: “rightmost bit transmitted first”.

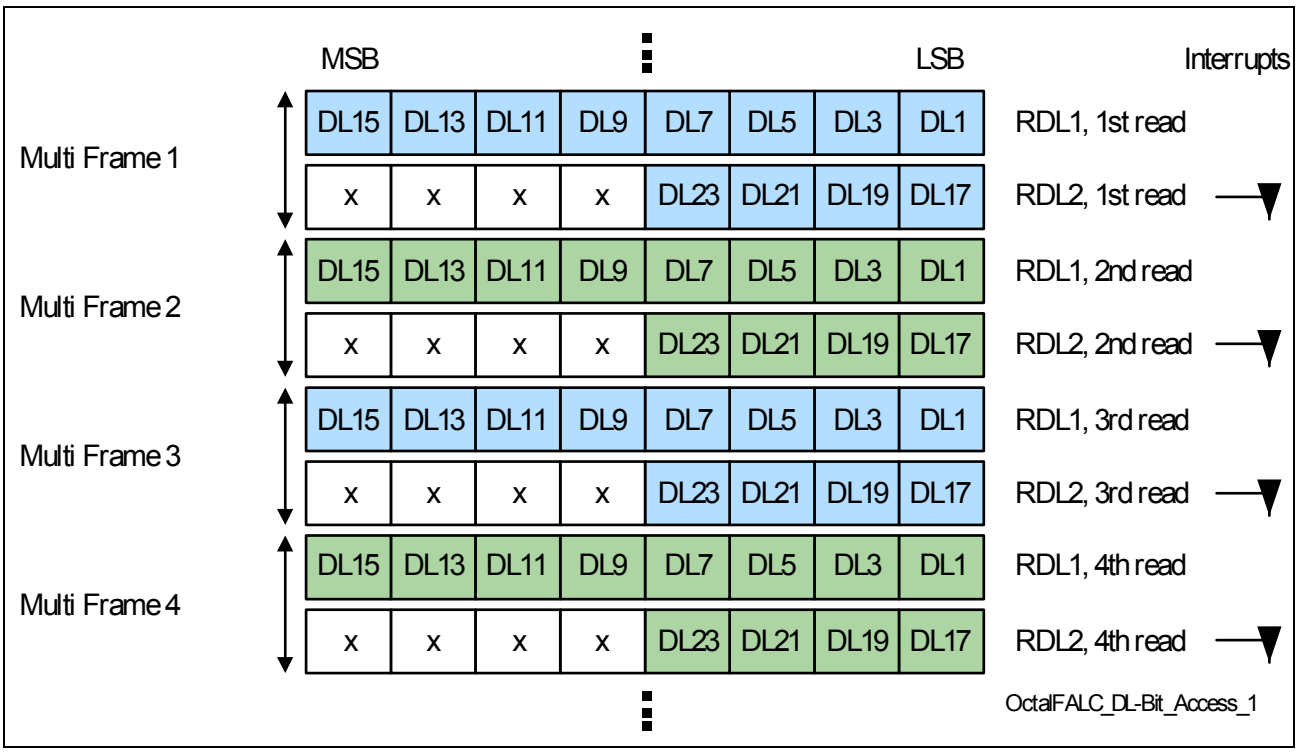


Figure 22 Standard DL-Bit Access in ESF Mode

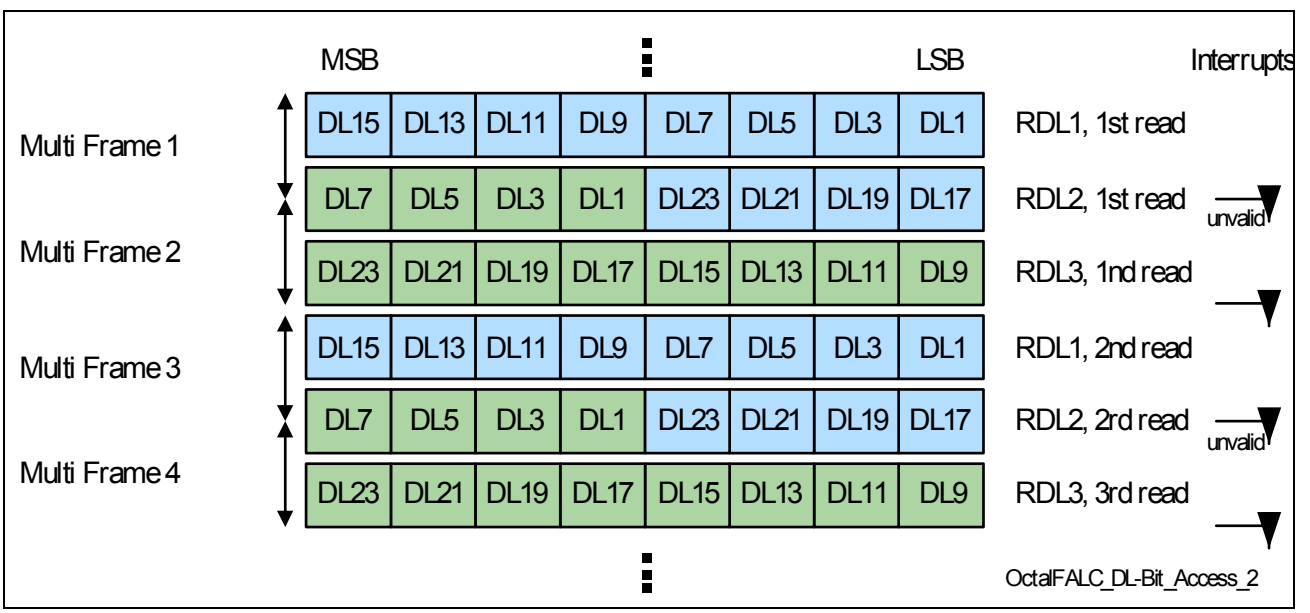


Figure 23 Optional DL-Bit Access in ESF Mode

7 CAS Features

7.1 Basic CAS Operation Mode

The basic operation mode (serial or register based) can be selected individually for receive and transmit direction.

If RSIG is configured on one of the RX multifunction ports RPA...RPC, serial RX-CAS data on RSIG are used automatically. If XSIG is configured on one of the TX multifunction ports XPA, RPB, serial TX-CAS data on XSIG are used automatically and XS1...16 registers are ignored.

7.2 Bit Robbing Force One in Cleared Channels (T1/J1 only)

In T1 mode the function to force all robbed bits to “one” can be selected to be not performed in CAS cleared channels. This mode is selected by setting register bit XC0.BRFO1 = 1.

7.3 Bit Robbing Idle (T1/J1 only)

In T1 mode the bit robbing idle function is selectable by register bit XC0.BRIF. If this bit is set, bit robbing information is not overwritten by the idle code in idle channels.

8 HDLC/BOM Controllers

Each of the eight ports provides three HDLC/BOM Controllers. Each of these units can be attached to either the line side (“standard”) or the system side (“inverse”). Inverse HDLC mode is selected by setting MODE.HDLCI = 1, MODE2.HDLCI2 = 1, or MODE3.HDLCI3 = 1 (for each of the three HDLC controllers and each of the eight E1/T1/J1 ports individually). Note that a detection of a Out-Band loop message (BOM code) on the line side is only possible if the HDLC controller is attached to the line side; a detection of a BOM code on the system side is only ossible in the “inverse” mode of the HDLC controller.

Each HDLC/BOM controller can be reset individually without disturbing the transmission on the remaining channels. Use CMDR.SRES for HDLC channel 1, CMDR3.RRES and CMDR3.SRES for HDLC channel 2, and CMDR4.RRES and CMDR4.SRES for HDLC channel 3, respectively.

Each of the eight ports provides one signalling controller for SS7 signaling.

The signalling controller has an interrupt status bit ISR1.SUEX which shows exceeding of the error threshold in SS7 mode. These interrupt status bit is masked by the bit IMR1.SUEX .

The error counter for SS7 mode can be reset by setting the register bit CMDR2.RSUC.

The error threshold for SS7 mode can be configured by setting the register bit CCR5.SUET.

After an RDO interrupt on one HDLC controller, the receive HDLC controller needs no reset. So a receive HDLC controller reset per channel is not necessary.

Note: CMDR.RRES resets the whole RX path and therefor all HDLC channels.

The FIFO depth is doubled to 128 byte in RX, see **Table 9**, and 128 byte in TX (by setting register bit CCR2.TFTS) per HDLC/BOM controller (64 byte user and 64 byte shadow RAM).

As in the FALC56 version V2.1 the total length of the received frame can be always read directly in registers RBCL and RBCH after a RPF interrupt, except when the threshold is increased during reception of that frame, but additionally to the FALC56 version V2.1 bit RBC5 will be taken into account if the FIFO depth is 64 bytes, see **Table 9** as example for the HDLC channel 1. The register bits CCR3.RFT(2:0)2 and CCR4.RFT(2:0)3 set the FIFO depth in the same way for the HDLC channel 2 and 3 respectively.

If a HDLC frame was completely received the content of the register RSIS (HDLC channel1, RSIS2 andRSIS3 for HDLC channel 2 and 3) will be written as last byte into the receive FIFO.

Table 9 Receive FIFO User Depth (HDLC channel 1) and Bit Positions in Register RBCL

# bytes	CCR1.RFT(1:0)	MODE.RFT2	Bit Positions in RBCL Reset by a CMDR.RMC Command
32	00	0	RBC(4:0)
16	01	0	RBC(3:0)
4	10	0	RBC(1:0)
2	11	0	RBC0
64	xx	1	RBC(5:0)

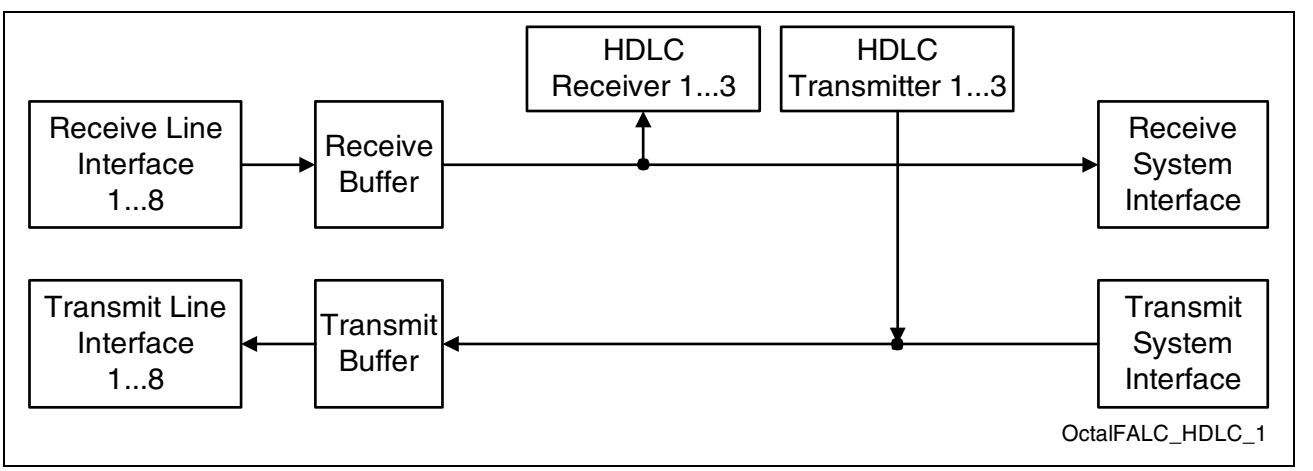


Figure 24 HDLC Controller Standard Configuration for all three HDLC Channels

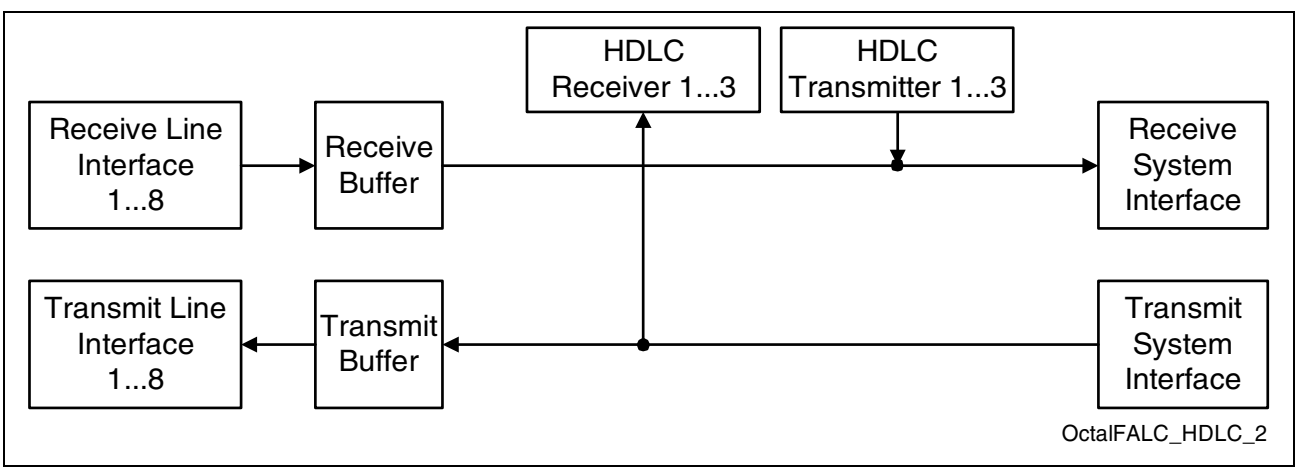


Figure 25 HDLC Controller Inverse Configuration for All Three HDLC Channels

Switchin between HDLC and BOM (if both MODE.BRAC and MODE.HRAC are set) will be done in the following way:

- After reset the HDLC/BOM controller is in HDLC mode
- After eight consecutive ones (´FF_H´) were received: switching to BOM mode (note that eight consecutive ones are also an HDLC abort)
- After one HDLC flag (´$7E_H$´) was received: switching to HDLC mode (directly, additionalHDLC flags are not necessary)
- Asequence ´FF_H´, ´$7E_H$´ are seen also as HDLC start flag

The status bit SIS.BOM reflects the actual mode of the HDLC/BOM controller.

Note that BOM codes ´$7E_H$‘ should be avoid.

If a BOM message occurs “inside” of a HDLC protocoll, the HDLC protocoll (frame) is corrupted.

9 System Interface

9.1 System Multiplex Mode

The following multiplex modes are supported, see **Figure 26**, were only pins RDO of the ports are shown, and **Table 10**:

- 8-to-1 Multiplex Mode at 16 Mbit/s. Multiplexing is done on port 1. Output pins of the other ports are set to tristate input pins of the other ports are unused.
- Dual 4-to-1 Multiplex Mode at 8 Mbit/s. Multiplexing is done on port 1 and port 5. Output pins of the other ports are set to tristate , input pins of the other ports are unused.
- Dual 4-to-1 Multiplex Mode at 16 Mbit/s. Multiplexing is done on port 1 and port 5 were four phases are unused on every port. Disjunct phases must be used on both ports. 16 Mbit/s multiplexing is done by external logical or on the PCB. Output RDO is driven to low level for inactive phases. Output pins of the other ports are undefined, input pins of the other ports are unused.

Switching between 8-to-1 Multiplex Mode (using only one port) and QuadFALC® compatible 4:1 Multiplex Modes (using two or more ports) is done by the register bit GPC6.SSI16, see **Table 10**.

Multiplexing of RSIG is done in the same way as shown for RDO in **Figure 26**. Demultiplexing of XDI and XSIG is done vice versa.

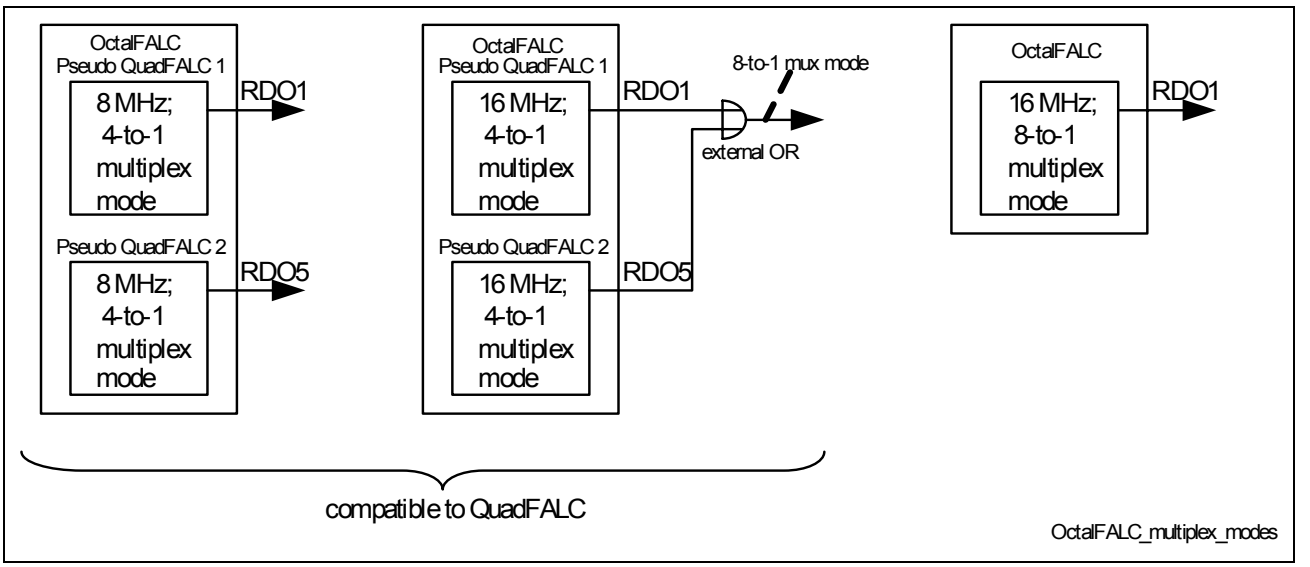


Figure 26 Principle of System Interface Multiplex Modes, shown for RDO

Table 10 System Multiplex Modes

GPC1.SMM	GPC6:SSI16	Mode
0	0	No multiplexing
0	1	Not defined
1	0	4:1 multiplexing; 8Mbit/s or 16Mbit/s dependent on SIC1.SSD1 and SIC1.SSC(1:0). For COMP = ´1´ setting of 4:1 multiplexing can be done individually in both pseudo QuadFALC® s; for COMP=´0´ 4:1 multiplexing is done in both of the pseudo QuadFALC® s
1	1	8:1 multiplexing; 16Mbit/s. For COMP = ´1´ the register bit GPC1.SMM must be set to ´1´in both of the pseudo QuadFALC® s. (For COMP = ´0´ only one register bit GPC1.SMM exists.)

To perform the system interface mode the following configuration of the multi function ports must be identical for all channels:

- SYPR has to be provided on RPA
- SYPX1 or XMFS has to be provided on XPA
- XSIG has to be provided on XPB
- RSIG must be output on RPB

All other assumptions to perform the system interface mode are the same as described in the data sheet of the QuadFALC®.

9.2 Clock Edge Selection

The active clock edge of $\overline{\text{SYPX}}$ can be selected related to that of the other interface transmit data and marker. Also selection of the clock edge for $\overline{\text{SYPR}}$ is possible related to that of the other interface receive data and marker. Use register bits SIC4.SYPRCE, or SIC4.SYPXCE. Note that the clock selection of the transmit data and marker with exception of $\overline{\text{SYPX}}$ is done by SIC3.RESX and that of the receive data and marker with exception of $\overline{\text{SYPR}}$ is done by SIC3.RESR.

9.3 Tristate Modes

- FSC can be switched into tristate mode by setting SIC3.FSCT = 1.
- RDO and RSIG can be switched into tristate mode for unused time slots by setting SIC3.RTRI = ´1´.
- RDO, RSIG, SCLKR and RFM can be set into tristate mode constantly (for redundancy applications) using the registerbit SIC3.RRTRI and - if the RTDMT function is selected on one of the multi fuction port - by RTDMT. If the RTDMT function is selected the values of RTDMT and SIC3.RRTRI are logically exored. This enables an easy redundance application using only one signal for switching between two devices, see the next chapter. If the RTDMT function is not selected SIC3.RRTRI = ´1´ set the pins into tristate mode constantly. In this mode “tristate” means high impedance against V_{DD} and V_{SS}: No pull up or pull down resistor is active.

Table 11 Tristate Configurations for the RDO, RSIG, SCLKR and RFM Pins

- RRTRI / - RRTRI exor RTDMT if RTDMT is selected on MFP	RTRI	RDO, RSIG	SCLKR, RFM
1	x	Constant tristate (without pull up and pull down resistor)	Constant tristate (without pull up and pull down resistor)
0	0	Never tristate	Never tristate
0	1	Tristate during inactive channel phases (with pull up resistor)	

9.4 Redundancy Mode

In redundancy mode the data inputs XDI are connected together. The outputs RDO and the signaling outputs RSIG (if used) of two channels can be connect together in the OctalFALC™ also, because one of them is set constantly into tristate respectively while the other is active. **Figure 27** shows the application.

Both channels must be configured identically and must be supplied with the same clocks and (transmit) data and signaling.

Switching between both channels can be done on the line side in transmit direction by a hardware signal if the multi function pin XPA is configured as tristate input XLT by the register bits PC1.XPC1 = ´1000b´. If one pin XPA is programmed as low active (PC1.XPC1 = ´1110b´) and the one of the other channel as high active (PC1.XPC1 = ´1000b´), no external inverter is necessary as shown in **Figure 27**. So switching between both channels on line side is possible using only one signal.

Switching can also be done on the line side in transmit direction by software, if setting the register bit XPM2.XLT. The register bit value XPM2.XLT and the pin value of XPA are logically ored. (That means if XPA is configured as low active then

tristate = XPM2.XLT or not($\overline{\text{XPA}}$).)

Because the register bit XPM2.XLT and the multi function pin XPA exist individually for every channel, switching on the line side in transmit direction can be done between channels of different or of the same OctalFALC™ device.

Switching between both channels can be done on the system side in receive direction by using the registerbit SIC3.RRTRI and with or without selection of the multi function port as RTDMT. If the RTDMT function is selected the values of RTDMT and SIC3.RRTRI are logically exored. If in one of the both channels SIC3.RRTRI is set, RTDMT is low active because of the logical exor, and if in the other channel SIC3.RRTRI is cleared, RTDMT is low active because of the logical exor. So switching between both channels on system side in receive direction is possible using only one signal.

By using the XLT, $\overline{\text{XLT}}$ and RTDMT function of the multi function ports and do the appropriate programming of the bits SIC3.RRTRI, switching between both channels can be done on the system and the line side together with only one common signal, as shown in **Figure 27** and **Table 12**.

Table 12 Redundancy Application Using RLM Mode

Configuration	Register Bits	Channel 1 (active/stand-by)	Channel 2 (stand-by/active)
XLT, $\overline{\text{XLT}}$	PC1.XPC1(3:0)	1000	1110
RTDMT	PC1.RPC1(3:0)	1101	1101

Table 12 Redundancy Application Using RLM Mode (cont'd)

Configuration	Register Bits	Channel 1 (active/stand-by)	Channel 2 (stand-by/active)
Receive system interface	SIC3.RRTRI	0	1
RLM mode	LIM0.RLM	0	1

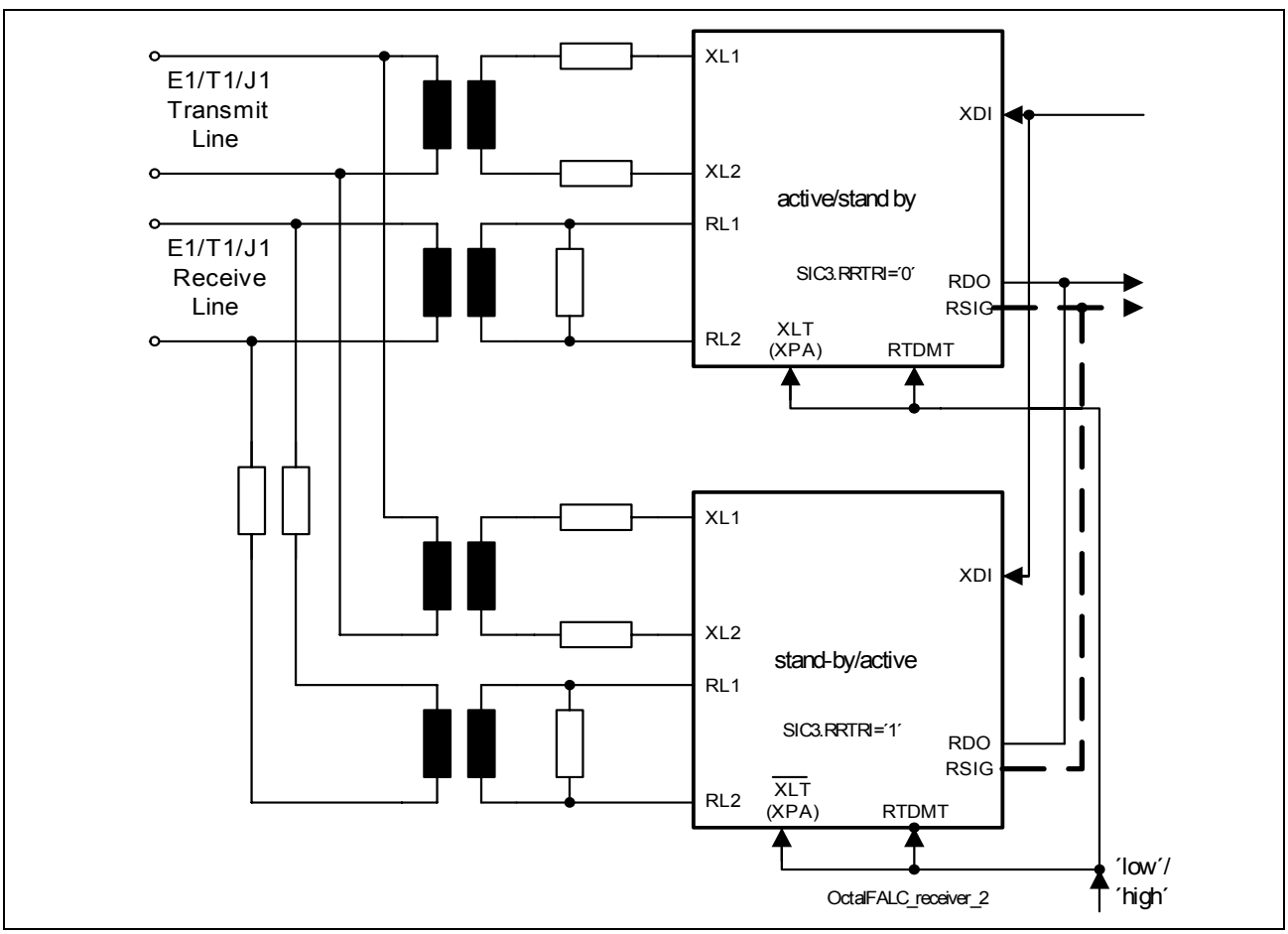


Figure 27 Redundancy Application (shown for one channel and using RLM)

To fulfill these requirements the RX- and TX-pathes of the two channels must be work synchronous to another.

Figure 28 shows a redundancy application for long haul mode using the internal analog switch. With the configuration shown in **Table 13**, switching between both channels is possible using only one board signal which is connected to XLT, XLT, RLT and RTDMT. Because the OctalFALC™ builds the logical equivalence out of RLT and LIM0.RTRS, the analog switches of both channels are controlled by these signal.

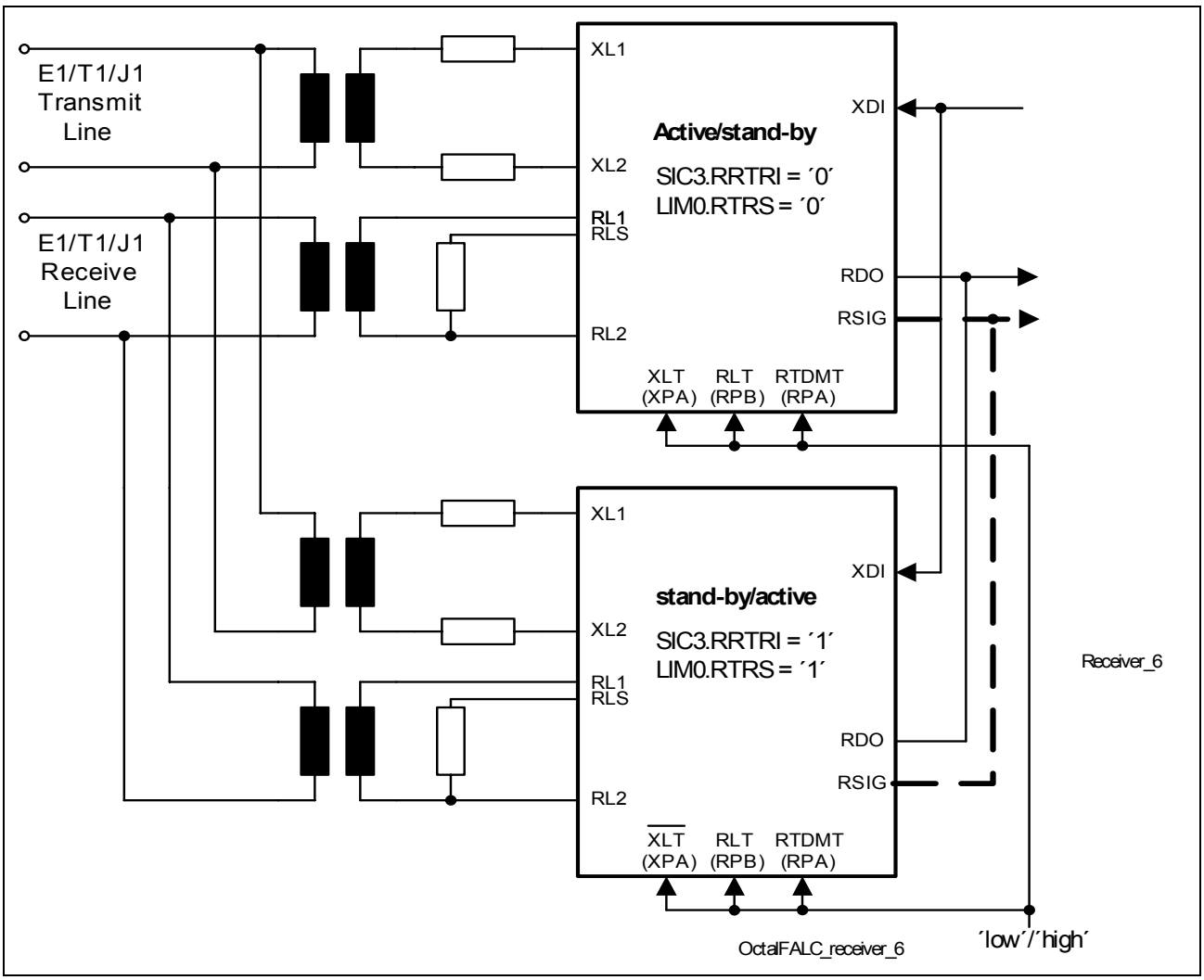


Figure 28 Long Haul Redundancy Application using the Analog Switch (shown for one line)

Table 13 Redundancy Application Using the Analog Switch, Switching with only one Board Signal

Configuration	Register Bits	Channel 1 (active/stand-by)	Channel 2 (stand-by/active)
XLT, $\overline{\text{XLT}}$	PC1.XPC1(3:0)	1000	1110
RTDMT	PC1.RPC1(3:0)	1101	1101
Receive system interface	SIC3.RRTRI	0	1
RLT	PC2.RPC2(3:0)	1000	1000
Receive line termination	LIM0.RTRS	0	1

10 Line Interface

10.1 Tunable Transmit Line Output Resistance

For optimized return loss the transmit output resistance can be configured by using the pins XL3 and XL4 as shown in **Figure 29**.

Generic E1/T1/J1 applications can be built where the operation mode is selected by software without the need for external hardware changes. Note that shorts between XL1 and XL2 are not detected by the transmit line monitor, see chapter 10.2.

The principle transmitter circuit diagram is shown in **Figure 29**. For non-generic applications pins XL3 and XL4 can be left open. The serial resistance can be selected by register programming as shown in **Table 14**.

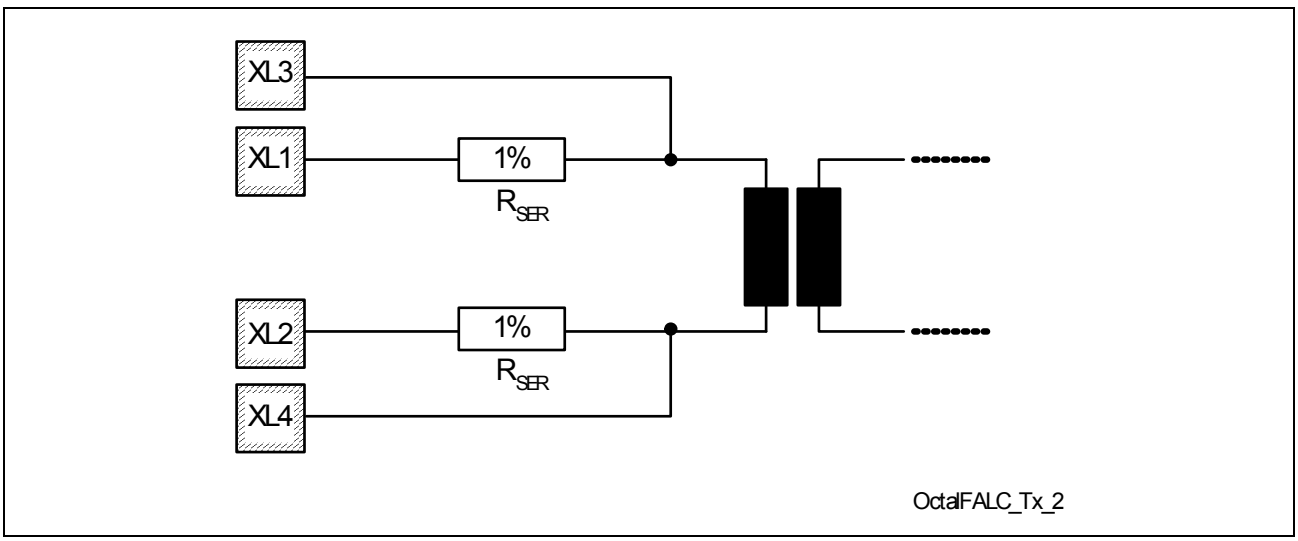


Figure 29 Transmit Impedances

Table 14 Serial Impedance Values

Parameter	Symbol	Values	Unit	Note/Test Condition
Serial Resistance, accuracy ± 1%	R_{SER}	2[1)]	Ω	Generic E1/T1/J1 PC6.TSRE = 1 (E1)
				PC6.TSRE = 0 (T1/J1)
		2[1)]		Non generic T1/J1 PC6.TSRE = 0
		7.5[1)]		Non generic E1 PC6.TSRE = 0

1) This value refers to an ideal transformer without any parasitics. Any transformer resistance or other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

10.2 Transmit Line Monitor

Shorts between XL1 and XL2 cannot be detected. A short between XL1 and XL2 will not ham the device.

10.3 Programmable Pulse Shaper and Line Build-Out

The transmitter includes a programmable pulse shaper to generate transmit pulse masks according to:

- For T1: FCC68; ANSI T1. 403 1999, figure 4; ITU-T G703 11/2001, figure 10 (for different cable lengths), for measurement configuration were R_{load} = 100 Ω
- For E1: ITU-T G703 11/2001, figure 15 (for 0 m cable length) ; ITU-T G703 11/2001, figure 20 (for DCIM mode), for measurement configuration were R_{load} = 120 Ω or R_{load} = 75 Ω

The transmit pulse shape (U_{PULSE}) is programmed either

- By the registers XMP(2:0) compatible to the QuadFALC®, if the register bit XPM2.XPDIS is cleared,
- or by the registers TXP(16:1), if the register bit XPM2.XPDIS is set.

To reduce the crosstalk on the received signals in long haul applications the OctalFALC™ offers the ability to place a transmit attenuator (Line Build-Out, LBO) in the data path. This is used only in T1 mode. LBO attenuation is selectable with the values 0, -7.5, -15 or -22.5 dB (register bits LIM2.LBO(2:1)). ANSI T1. 403 defines only 0 to -15 dB.

10.3.1 QuadFALC® Compatible Programming

After reset XPM2.XPDIS is zero so that QuadFALC® compatible programming is selected. The default setting after reset for the registers XMP(2:0) generates the E1 pulse shape, see **Table 16**, but with an unreduced amplitude. No reset value for T1 mode exists. So after switching into T1 mode, an explicit new programming as described in **Table 15** is necessary.

If LBO attenuation is selected, the programming of XPM(2:0) will be ignored. Instead the pulse shape programming is handled internally: The generated pulse shape before LBO filtering is the same as for T1 0 to 40 m.

The given values are optimized for transformer ratio: 1 : 2.4 and cable type AWG24 using transmitter configurations listed in **Table 14**. The standardized measurement configurations with R_{load} = 120 Ω and with R_{load} = 100 Ω are used.

Table 15 Recommended Pulse Shaper Programming for T1/J1 with registers XPM(2:0) (Compatible to QuadFALC®)

LBO	Range	Range	XPM0	XPM1	XPM2
[dB]	[m]	[ft]	hexadecimal		
0	0 to 40	0 to 133	D7	22	1
0	40 to 81	133 to 266	FA	26	1
0	81 to 122	266 to 399	3D	37	1
0	122 to 162	399 to 533	5F	3F	1
0	162 to 200	533 to 655	3F	CB	1
7.5	---		are not taken into account: Pulse shape generation is handled internally.		
15	---				
22.5	---				

Table 16 Recommended Pulse Shaper Programming for E1 with Registers XPM(2:0) (Compatible to QuadFALC®)

R_{SER}	Z_0	Transmit Line Interface Mode	XPM0	XPM1	XPM2
[Ω]	[Ω]		hexadecimal		
7.5[1)]	120	non generic	9C	03	00
7.5	75	non generic	BD	03	00
---	reset values		7B	03	40
7.5	DCIM Mode	non generic	EF	BD	07

1) The values in this row refers to an ideal application without any parasitics. Any other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

10.3.2 Programming with TXP(16:1) Registers

By setting of register bit XPM2.XPDIS the pulse shape will be configured by the registers TXP(16:1) . Each of these registers define the amplitude value of one sampling point in the symbol. A symbol is formed by 16 sampling points.

The default setting after reset for the registers TXP(16:1) generates also the E1 pulse shape (0m), but with an unreduced amplitude. (TXP(9:16) = ´00_H´; TXP(1:8) = ´38_H´= 56_D´) No reset value for T1 mode exists. So after switching into T1 mode, an explicit new programming like **Table 17** is necessary.

The pulse shape configuration will be done also by the registers TXP(16:1) if LBO attenuation is selected. The pulse shape is then determined by both the values of TXP(16:1) and the LBO filtering.

The given values in the following tables are optimized for transformer ratio: 1 : 2.4; cable: AWG24 and configurations listed in **Table 14**.

Table 17 Recommended Pulse Shaper Programming for T1 with Registers TXP(16:1)

LBO	Range	Range	TXP values, decimal															
[dB]	[m]	[ft]	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0 to 40	0 to 133	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
0	40 to 81	133 to 266	48	50	48	46	46	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
0	81 to 122	266 to 399	48	50	46	44	44	44	44	44	16	-25	-17	-14	-4	-4	-4	-4
0	122 to 162	399 to 533	63	55	46	46	44	44	44	44	16	-30	-17	-17	-4	-4	-4	-4
0	162 to 200	533 to 655	63	63	63	58	50	50	50	50	50	-60	-26	-20	-12	-8	-6	-4
7.5	--	--	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
155	--	--	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
22.5	--	--	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4

Table 18 Recommended Pulse Shaper Programming for E1 with Registers TXP(16:1)

R_{SER}	Z_0	Transmit Line Interface Mode	TXP values, decimal															
[Ω]	[Ω]		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
2[1)]	120	generic	42	40	40	40	40	40	40	42	0	0	0	0	0	0	0	0
7.5	120	non generic	63	57	57	57	57	57	57	57	-4	0	0	0	0	0	0	0
2	75	generic	42	40	40	40	40	40	40	40	0	0	0	0	0	0	0	0
7.5	75	non generic	60	58	58	58	58	58	58	58	0	0	0	0	0	0	0	0
--	reset values		56	56	56	56	56	56	56	56	0	0	0	0	0	0	0	0
2	DCIM Mode	generic	20	20	20	20	20	20	20	20	-20	-20	-20	-20	-20	-20	-20	-20
7.5	DCIM mode	non generic	28	28	28	28	28	28	28	28	-28	-28	-28	-28	-28	-28	-28	-28

1) The values in this row refers to an ideal application without any parasitics. Any other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

10.4 Receive Line Termination

In general the E1 line impedance operating modes with 75 Ω (used with coaxial cable) or with 120 Ω (used with twisted pair cable) line termination are selectable by switching resistors in parallel or using special transformers with different transfer ratios in one package (using center tap). These two options both provide only one analog front end circuitry for both transmission media types.

The OctalFALC™ supports a software selectable generic E1/T1/J1 solution without the need for external hardware changes by using the integrated analog switch and two external resistors for line impedance matching, see application example in **Figure 30**. By default the analog switch is off.

This allows, for example, to switch between 100 Ω (T1/E1 twisted pair) and 75 Ω (E1 coax) termination resistance using the external resistors R_{E1} = 100 Ω and R_{E2} = 300 Ω, see **Table 19**. The analog switch can be controlled by access to the register bit LIM0.RTRS and by hardware using the receive Multi Function Ports. For that, only one (but not more) of the receive Multi Function Ports must be configured as Receive Line Termination (RLT) input. For controlling of the analog switch a logical equivalence is build out of RLT and the register bit LIM0.RTRS if RLT is configured at one multi function port.

If the analog switched is not used in an application, the pin RLS can be left open.

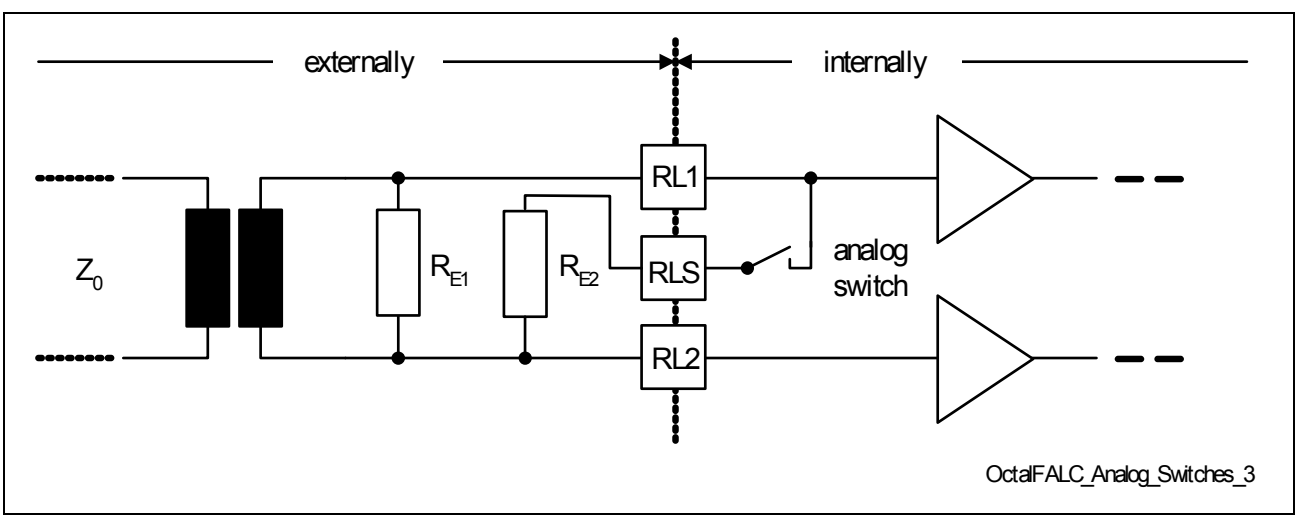


Figure 30 Receiver Configuration with Integrated Analog Switch for Receive Impedance Matching

Table 19 Receiver Configuration Examples

Line Impeance Z_0	External Resistor R_{E1}	External Resistor R_{E2}	Inter-nal Ana-log Switc h	LIM0.RTRS; RLT
120 Ω	100 Ω (for common E1/T1/J1 applications)	300 Ω (for common E1/T1/J1 applications)	**off**	if RLT is configured: (LIM0.RTRS equivalent RLT) = ´0´ if RLT is not configured: LIM0.RTRS = ´0´
100 Ω			**off**	
75Ω			**on**	if RLT is configured: (LIM0.RTRS equivalent RLT) = ´1´ if RLT is not configured: LIM0.RTRS = ´1´

11 Multi Function Port Features

Several additional functions are available on the multi function ports, see **Table 20**. Old features known from QuadFALC® are shown in *italic*. After reset, input function is selected ($\overline{SYPR}$ or $\overline{SYPX}$) with exception of the ports RPC were RCLK output is selected: The register bits PC3.RPC2 have the reset value F_H. (Note that PC5.CRP must be set to ´1´ for an active RCLK output. After reset PC5.CRP is ´0´ and RCLK is pulled up.)

Three multi function ports (MFP) for RX - so called as RPA, RPB, RPC - and two MFPs for TX - so called as XPA, XPB - are implemented for every channel. The port levels are reflected in the appropriate bits of the register MFPI.

The actual logical state of the 5 multifunction ports can be read out using the register MFPI. This function together with static output signal optins in **Table 20** offers general purpose I/O functionality on unused multi function port pins.

If a port is configured as GPOH or GPOL the port level is set fix to high or low level respectively.

Each of the input functions may only be selected once. No input function must be selected twice or more.

Table 20 Multi Function Port Selection

Selection	RFP Signal	Avail.	RFP Function	XFP Signal	Avail.	XFP Function
0000	*$\overline{SYPR}$*	ABC	*Synchronous pulse receive input*	*$\overline{SYPX}$*	AB	*Synchronous pulse transmit input*
0001	*RFM*	ABC	*Receive frame marker output*	*XMFS*	AB	*Transmit multiframe synchronization input*
0010	*RMFB*	ABC	*Receive multiframe begin marker output*	*XSIG*	AB	*Transmit signaling data input*
0011	*RSIGM*	ABC	*Receive signaling marker output*	*TCLK*	AB	*Transmit clock input*
0100	*RSIG*	ABC	*Receive signaling data output*	*XMFB*	AB	*Transmit multiframe begin marker output*

Table 20 Multi Function Port Selection (cont'd)

Selection	RFP Signal	Avail.	RFP Function	XFP Signal	Avail.	XFP Function
0101	*DLR*	ABC	*Data link bit receive output*	*XSIGM*	AB	*Transmit signaling marker output*
0110	*FREEZE*	ABC	*Freeze signaling output*	*DLX*	AB	*Data link bit transmit marker output*
0111	*$\overline{RFSP}$*	ABC	*Frame synchronous pulse output*	*XCLK*	AB	*Transmit clock output*
1000	RLT	ABC	*Receive line termination*	*XLT*	AB	*Transmit line tristate control high active*
1001	GPI	ABC	*General purpose input*	GPI	AB	*General purpose input*
1010	GPOH	ABC	*General purpose output high*	GPOH	AB	*General purpose output high*
1011	GPOL	ABC	*General purpose output low*	GPOL	AB	*General purpose output low*
1100	LOS	ABC	*loss of signal indication output*	reserved	AB	*reserved*
1101	RTDMT	ABC	*Receive TDM I/F tristate for pins RDO,RSIG, SCLKR, RFM; logically exored with SIC3.RRTRI*	XDIN	AB	*transmit data negative input*
1110	RDON	ABC	*receive data negative output / bipolar violation output*	$\overline{XLT}$	AB	*Transmit line tristate control low active*
1111	RCLK	ABC	*RCLK output*	reserved	AB	

12 Test and Maintenance

12.1 PRBS Test Signal

Different PRBS modes which are using different bits and time slots in a E1/T1/J1 frame can be selected, see **Table 22**.

In the so called “unframed” mode all bits of all slots in a E1/T1/J1 frame are used for PRBS.

In the so called “framed” mode the frame byte (time slot 0) of an E1 frame or the frame bit in a T1/J1 frame is not used for PRBS respectively.

Selection of the PRBS modes “unframed” and “framed”is done by TPC0.PRM = ´00b´ and TPC0.FRA.

For TPC0.PRM not ´00b´, each time slot of an E1/T1/J1 signal can be selected indiviually to send and receive a PRBS signal. Selection is done by the registers PRBSTS1 to PRBSTS4. Here the used time slot numbers are the same as used normally for numbering of the time slots:

-In E1 frames time slot 0 (TS0) up to time slot 31 (TS31), were TS0 is the frame byte (time slot number 0 indicates the frame byte).

-In T1/J1 frames the time slot number 0 indicates the frame bit and the time slot numbers 1 up to 24 indicates the TS1 up to TS24.

If a time slot is used or not for PRBS sending and reception is controlled by the registers PRBSTS1..4. The number of used time slots for PRBS is so called as “N”. The range of N is 1, ..., 32 for E1 and 1, ..., 25 for T1/J1 (if no channel translation mode is selected) because of the frame bit. The time slot selection 0 up to 31 for E1 or 0 up to 24 for T1/J1 (if no channel translation mode is selected) by PBBSTS(1:4) is common for all eight ports respectively.

If channel translation mode is selected, the time slot numbers are the same as used in the ordering of the active time slots at the system interface (0, ..., 31), see also table 31 of QuadFALC® data sheet.

The N multiple time slots are selected arbitrarily for PRBS. The PRBS data stream has to be written into or read from the time slots consecutive respectively.

The selected time slot numbers are related to the mapping used on the system interface.

Note that deselection of time slot 0 (PRBSTS1.TS0 = ´0´) perfomes a “framed” mode for E1/T1/J1.

For TPC0.PRM not ´00b´, normally all eight bits of the time slots are used for PRBS (“N × 64 kbit/s”). To allow CAS-BR in T1 mode, only 7 MSBs of the all time slots which are selected for PRBS can be optionally used for PRBS to avoid CAS disturbance (“N × 56 kbit/s”), the eight´s bit of all time slots (which is the CAS bit in T1) is not used for PRBS. Setting of this mode is performed by setting the register bits TPC0.PRM(1:0)

to´11b´. Note that this mode can be used also in E1 mode, but makes no sense: In E1 CAS disturbance can be avoided by deselection of the appropriate time slot 16.

Note that the “N × 56 kbit/s” mode is automatically a “framed” mode in T1 because the frame bit in TS0 is identical to the “robbed” CAS bit.

Note that for “N × 64 kbit/s” selection and selection af all time slots by PRBSTS(1:4) all bits in the frame are used for PRBS (that is an “unframed” mode).

The kind of PRBS patterns (polynoms) can be selected to be 2^{11}-1, 2^{15}-1, 2^{20}-1or 2^{23}-1 by the register bits TPC0.PRP(1:0) and LCR1.LLBP, see **Table 22**. For definition of this polynoms see the Standards ITU-T O.150, O.151. and TR62441. New against FALC56v2.1 are the patterns 2^{11}-1 and 2^{23}-1 which can be selected only if TPC0.PRM not ´00b´.

The transmit of PRBS pattern is enabled by register bit LCR1.XPRBS. With the register bit LCR1.FLLB switching between not inverted and inverted transmit pattern can be done.

The receive monitoring of PRBS patterns is enabled by register bit LCR1.EPRM. In general, dependend on bit LCR1.EPRM the source of the interrupt status bit ISR1.LLBSC changed, see register description. The kind of detected PRBS pattern in the receiver is shown in the status register bits PRBSSTA.PRS. Every change of the bits PRS in PRBSSTA sets the interrupt bit ISR1.LLBSC if register bit LCR1.EPRM is set. No pattern is also detected if signal “alarm simulation” is active.

The detection of all_zero or all_ones is done over 12, 16, 21 or 24 consecutive bits, dependent on the choosed PRBS polynom (11, 15, 20 or 23). The detection of all_zero or all_ones is independent on LCR1.FLLB. Note that if the information about the first reached PRBS status after the monitor was enabled (“PRBS pattern detected” or “inverted PRBS pattern detected”) is combined with the status information “all-zero pattern detected” or “all-ones pattern detected”, the controller can conclude the real polarity of the all-ones or all-zeros pattern.

Because every bit error in the PRBSequence increments the bit error counter BEC, no special status information like “PRBS detected with errors” is given here.

Table 21 Supported PRBS Polynomials (pattern)

TPC0.PRP	TPC0.PRM	LCR1.LLBP	Kind of polynomial	Comment
00	01 or 11	x	2^{11}-1	
01	01 or 11	x	2^{15}-1	
10	01 or 11	x	2^{20}-1	
11	01 or 11	x	2^{23}-1	

Table 21 Supported PRBS Polynomials (pattern) (cont'd)

TPC0.PRP	TPC0.PRM	LCR1.LLBP	Kind of polynomial	Comment
xx	00	0	2^{15}-1	SW compatibel to QuadFALC®
xx	00	1	2^{20}-1	

Table 22 Bit/Timeslot Selection of PRBS Pattern

TPC0.PRM	TPC0.FRA	kind of selection	comment
00	0	Unframed	PRBSTS settings are not valid; SW compatibel to QuadFALC®
00	1	Framed	
01	x	N x 64 kbit/s	"Framed" mode if TS0 is deselected; CAS in E1 not disturbed if TS 16 is deselected
10	x	Reserved	
11	x	N x 56 kbit/s	Implies a "framed" mode

12.2 PPR Enhancement (T1/J1 only)

The PPR (Periodical Performance Report, see ANSI T1.403) status which is sent out in the data link channel of the extended superframe format (ESF/F24 only) automatically (dependent on the bit CCR5.EPR) or manually (if setting CMDR2.XPPR to ´1´; then last PPR is sent once; CMDR2.XPPR bit is cleared automatically after sending was finished) can additionally be read from registers PPR0 and PPR1, too. Performance data is updated once every second. Only the actual performance parameters (for t_0) are accessible via registers. New data is available immediately after the one second interrupt is triggered and must be read before the next one-second interrupt occurs.

12.3 In-Band Loop Switching

Automatic loop switching (activation and deactivation) based on detected In-Band Loop codes can be done.

Detection and generation of In-Band Loop code is supported on line and system side independent from another.

Detection, generation and loop switching is possible on all eight channels, independent from another.

Framed and unframed In-Band loop code can be generated and detected.

Automatic loop switching must be enabled through configuration register bits ALS.SILS for the In-Band Loop codes coming from the system side and ALS.LILS for the In-Band Loop codes coming from the line side respecively.

Automatic loop switching is logically ored with the appropriate loop switching by register bits.

If a remote loop is activated by an automatic loop switching the register bit LIM0.JATT controls also if the jitter attunator is active or not.

If ALS.LILS is set, the remote loop is activated after an activation In-Band loop code (see ANSI T1 404, chapter 9.4.1.1.) was detected from the line side and if the local loop is not activated by LIM0.LL = ´1´. The remote loop is deactivated after a deactivation In-Band loop code (see ANSI T1 404, chapter 9.4.1.2.) was detected from the line side. (But if the remote loop is addtionally activated by LIM0.RL = ´1´ the remote loop is still active, because automatic loop switching is logically ored with the appropriate loop switching by register bits.)

If ALS.SILS is set, the local loop is activated after an activation In-Band loop code (see ANSI T1 404, chapter 9.4.1.1.) was detected from the system side. The local loop is deactivated after a deactivation In-Band loop code (see ANSI T1 404, chapter 9.4.1.2.) was detected from the system side. (But if the local loop is addtionally activated by LIM0.LL = ´1´ the local loop is still active, because automatic loop switching is logically ored with the appropriate loop switching by register bits.)

ALS.SILS and ALS.LILS both must not be set to ´1´ simultaneous.

If ALS.SILS or ALS.LILS are set after an In-Band loop code was detected, no automatic loop switching is performed.

If ALS.LILS is cleared, an automatic activated remote loop is deactivated.

If ALS.SILS is cleared, an automatic activated local loop is deactivated.

The type of detected In-Band loop codes is shown in the interrupt status register bits ISR6.(3:0)

The bits ISR6.(3:0) will be set to ´1´ if an appropriate In-Band code were detected, independent if automatic loop switching is enabled or not . (Because the controller knows if automatic loop switching is enabled, it knows if a loop is activated or not.) Code detection status only for the line side is displayed in status register bits RSP. LLBBD and RSP.LLBAD . Masking of ISR6.(3:0) for interrupt can be done by register bits IMR6.(3:0).

Sending of In-Band loop codes is done by the OctalFALC™ lasting for at least 5 seconds. Detection of received In-Band loop codes and automatic switching into the loopback (activaton or deactivation) will be done after the code is lasting for at least 16 or 32 patterns or 4 or 5 seconds, dependend on the setting of the register bits INBLDTR.INBLDT(1:0).

Note:

1. *For SF format the protocoll currently used by the carriers for network access to the customer installation (CI) is an in-band control code. Note that E1/T1repeaters are in general transparent, so they have not any influence on the in-band signaling.*
2. *If In Band Signaling is enabled in transmit direction, all data bits of all 24 time slots of a frame are overwritten by signaling information (code). In Band Signaling is an unchannelized signaling method. If the 1. bit of a frame (frame bit) will be also overwritten it is the so called “unframed” signaling, otherwise it is called “framed” signaling. This configuration can be done by the register bit LCR1.FLLB.*
3. *If the signaling code is used for line loop back switching it is so called as” LLB code” (line loop back). Two kinds of codes exist: “LLB down code” for deactivation of the loop and “LLB up code” for activation. The codes are defined in ANSI-T1.403, 1999 in chapter 9.4.1.1 and 9.4.1.2. respectively.*
4. *An In-Band loop pattern has a minimum length of about 51200 symbols (100 double frames).*

12.4 Out-Band Loop Switching (T1/J1 only)

Note: For the ESF format activation and deactivation of loopbacks are performed by using Out-Band messages (BOM) described in ANSI-T1.403, 1999 in chapter 9.4.2.The BOM code has the following format: 11111111 0xxxxxx0 were the first bit of every byte is the MSB and the last is the LSB. (11111111 is the BOM flag.) That´s another ordering as in the ANSI table!!. Sending is done as for HDLC: LSB first, ´11111111´ first. That´s consistent to the note 1) in the ANSI: “rightmost bit transmitted first”.

The OctalFALC™ performes the following functionalities regarding the Out-band loop codes (bit oriented messages, BOM) on all eight channels independent from each other:

- Detection of Out-band loop codes (BOM).
- Generation of Out-band loop codes (BOM) by setting of the appropriate DL-bits by the micro controller.
- Automatic loop switching (activation and deactivation, for remote loop and payload loop based on detected Out-band loop codes.

Loop switching (“Out-band loop switching”) is possible by enabling of the BOM

receiver 1 signaling (MODE.BRAC = ´1´ and CCR1.EITS = ´1´) and detection of the following Out-Band loop messages related to ANSI-T1.403, 1999, table4.

Table 23 Out-Band Loop (BOM) Messages

Function	Message
line loopback activate	00001110 11111111
line loopback deactivate	00111000 11111111
payload loopback activate	00010100 11111111
payload loopback deactivate	00110010 11111111
universal loopback deactivate	00100100 11111111

12.4.1 Bit Oriented Messages (BOM): Generation, Detection and Loop Switching (T1/J1)

The OctalFALC™ performes the following functionalities regarding the Out-band loop codes (bit oriented messages, BOM) on all eight channels independent from each other:

- Detection of Out-band loop codes (BOM).
- Generation of Out-band loop codes (BOM) by setting of the appropriate DL-bits by the micro controller.
- Automatic loop switching (activation and deactivation, for remote loop and payload loop) based on detected Out-band loop codes.

Loop switching (“Out-band loop switching”) is possible by enabling of the BOM receiver 1 signaling (MODE.BRAC = ´1´ and CCR1.EITS = ´1´) and detection of the following Out-Band loop messages related to ANSI-T1.403, 1999, table4:

Table 24 Out-band Loop Messages for Loop Switching (T1/J1)

Function	Message (BOM Code)
Line loopback activate	´00001110 11111111_b´
Line loopback deactivate	´00111000 11111111_b´
Payload loopback activate	´00010100 11111111_b´
Payload loopback deactivate	´00110010 11111111_b´
Universal loopback deactivate	´00100100 11111111_b´

If the register bit CCR2.RBFE is set, BOM messages are accepted if at least seven consecutive and identical BOM messages were received.

Dependent on the BOM mode (configured by register bits CCR1.BRM and CCR2.RBFE) the content of register RSIS will be written as last byte into the receive FIFO.

Automatic loop switching by BOM messages is logically ored with the appropriate loop switching by register bits.

If ALS.SOLS is set, the payload loop is activated after the “payload loopback activate“ code was detected from the line side or the system side and if the local loop is not activated by LIM0.LL = ´1´. The payload loop is deactivated after an appropriate deactivation Out-Band loop code was detected from the line side or the system side. (But if the payload loop is additionally activated by FMR2.PLB = ´1´ the payload loop is still active, because automatic loop switching is logically ored with the appropriate loop switching by register bits.)

If ALS.LOLS is set, the remote loop is activated after the “line loopback activate” code was detected from the line side or the system side and if the local loop is not activated by LIM0.LL = ´1´. The remote loop is deactivated after the “line loopback deactivate” code was detected from the line side or the system side. (But if the remote loop is additionally activated by LIM0.RL = ´1´ the remote loop is still active, because automatic loop switching is logically ored with the appropriate loop switching by register bits.)

If the remote loop is activated by an automatic loop switching the register bit LIM0.JATT controls also if the jitter attenuator is active or not.

ALS.SOLS and ALS.LOLS both can be set to ´1´ simultaneous.

Because BOM messages coming from the system side are not included in the E1/T1/J1 standards, receive of these BOM messages and the possibility of automatic loop switching (ALS.SOLS) are features of the OctalFALC™. It has to be handle carefully to avoid deadlocks.

If ALS.SOLS or ALS.LOLS are set after an Out-Band loop code was detected, no automatic loop switching is performed.

If ALS.LOLS is cleared, an automatic activated remote loop is deactivated.

If ALS.SOLS is cleared, an automatic activated payload loop is deactivated.

The kind of performed automatic loop switching caused by the appropriate detected Out-band message is shown in the register bits ISR6.(7:4). Masking of ISR6.(7:4) for controlling of the interrupt can be done by register bits IMR6.(7:4). If an Out-band message were detected, the appropriate register bits ISR6.(7:4) will be set to ´1´, independent if automatic loop switching has been enabled. (Because the micro controller knows if automatic loop switching is enabled, it knows if a loop is activated or not.)

A detection of an Out-band loop message (BOM) “universal loopback deactivate” sets both bits ISR6.SOLSD and ISR6.LOLSD, independent if a loop is active (switched) or not. Dependent on ALS.LOLS or ALS.SOLS the remote or the payload loopback is switched off respectively.

A received BOM message causes setting of the interrupt bit ISR0.RME and is stored in the receive FIFO, marked with a BOM frame.

Note that detection of Out-band Loop messages (BOM codes) is only possible either on the line side or the system side, dependent on the configuration of the HDLC controller: If the HDLC/BOM controller 1 is attached to the line side (MODE.HDLCI = ´0´) only BOM messages coming from the line side can be detected. If the HDLC/BOM controller is

attached to the system side (MODE.HDLCI = ´1´), so called “inverse configuration”) only BOM messages coming from the system side can be detected. BOM messages coming from the system side are not included in (ANSI-)standards, but can be handled by the OctalFALC™.

12.5 FEC Count Up Behaviour

The kind of count up behaviour of the frame error counter FEC can be controlled by the register bit DEC.FECC because there are differences in the ANSI standard T1-403 between 1995 and 1999:

-FEC count up will be done also if a severely error occurs as it is described in ANSI-T1-403 1995: DEC.FECC = ´0´.

-FEC count up is not done if a simultaneous severely error occurs as described in ANSI-T1-403 1999: DEC.FECC = ´1´.

Note that the FEC status is stored in the registers FECH and FECL.

12.6 SEF Error Indication

An SEF interrupt statusbit ISR7.SEFEI and an appropriate mask register bit IMR7.SEFEI is provided, which shows SEF errors according to ANSI-T1.231:

6.1.2.2.2: “An SEF defect is determined by examining contiguous time windows for frame bit errors. For SF, the window size is 0.75 ms, and only the F_t-bits are examined. For ESF, the window size is 3 ms, and only the frame pattern sequence (FPS) bits are examined.

An SEF defect occurs when two or more frame bit errors in a window are detected. An SEF defect is terminated when the signal is in-frame and there are less than two frame bit errors in a window.

Note that an AIS-CI and an AIS signal (alarm indication signal), or a signal that is OOF (out of frame), will typically cause an SEF defect.

12.7 Test Access Port and Boundary Scan

The TAP (Test Access Port) is conform to the IEEE standard 1149.1-2001.

Complete Boundary Scan Number: (MSB...LSB) = 0001 0000 0000 1101 1110 0000 1000 0011_B. It consists on:

Version Number (1^{st} 4 bits) = 0001_B

Part Number (next 16 bits) = 0000 0000 1101 1110_B

Manufacturer ID (next 11 bits) = 0000 1000 001_B

LSB = 1_B

13 Supported Standards

The following international standards are supported additionally by this device:

- ANSI T1.231
- ITU-T G.812
- ITU-T G.733
- ITU-T JG.733
- JEDECJ-STD-020A-1999-04
- JEDECJ-STD-020B-1999-07

14 Development Support

14.1 IBIS Model

A new IBIS model is supplied, compliant with IBIS version t.b.d.

14.2 Development Tools

An EASY22558 evaluation board will be provided for device demonstration and testing.

15 Register Functions

After reset or if COMP = ´1´, the behavior is the same as for QuadFALC® V2.1. and any new functions are not valid. Full software compatibility is realized. Any new function to be used must be enabled explicitly.

The higher address part of all global registers is ´00_H´, that of the port (channel) specific ones include the channel number 1 to 8 and is marked in the following tables with´xx_H´.

For the description of the registers see the datasheet of the OctalFALC™ (User's Manual).

15.1 Global Register Compatibility Handling

The following global registers require specific handling, depending on the compatibility mode selection. See **Figure 31** to **Figure 32** for more detail.

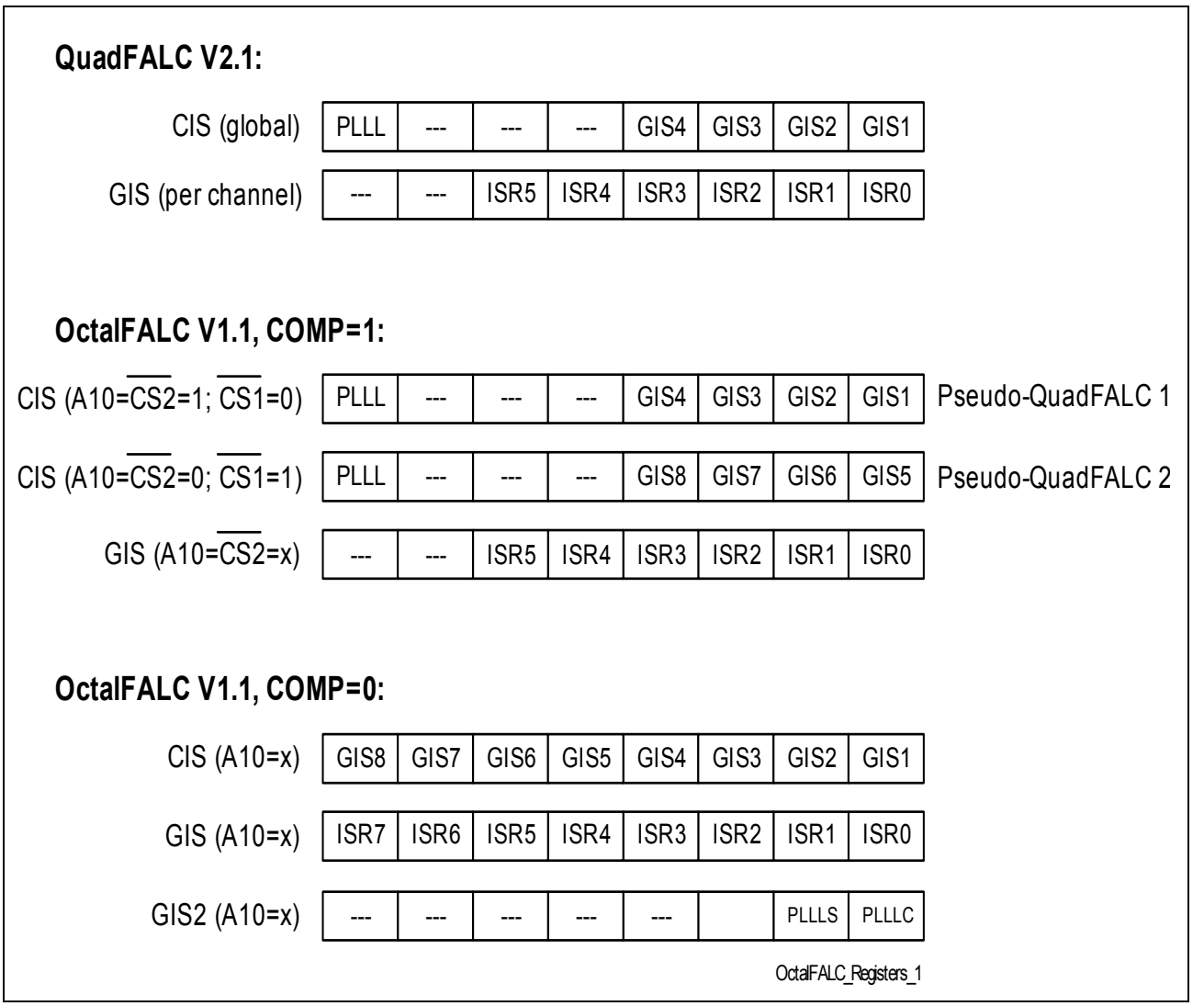


Figure 31 GIS Register Compatibility

For the OctalFALC™ in compatibility mode (pin COMP = 1) the nomenclature for the register bits of CIS for A10 = ´0´ (pseudo-QuadFALC 2, GIS8 to GIS5) is taken to declare the apropriate channels 8 to 5, but the name of the bits is also GIS4 to GIS1 as for A10 = ´1´.

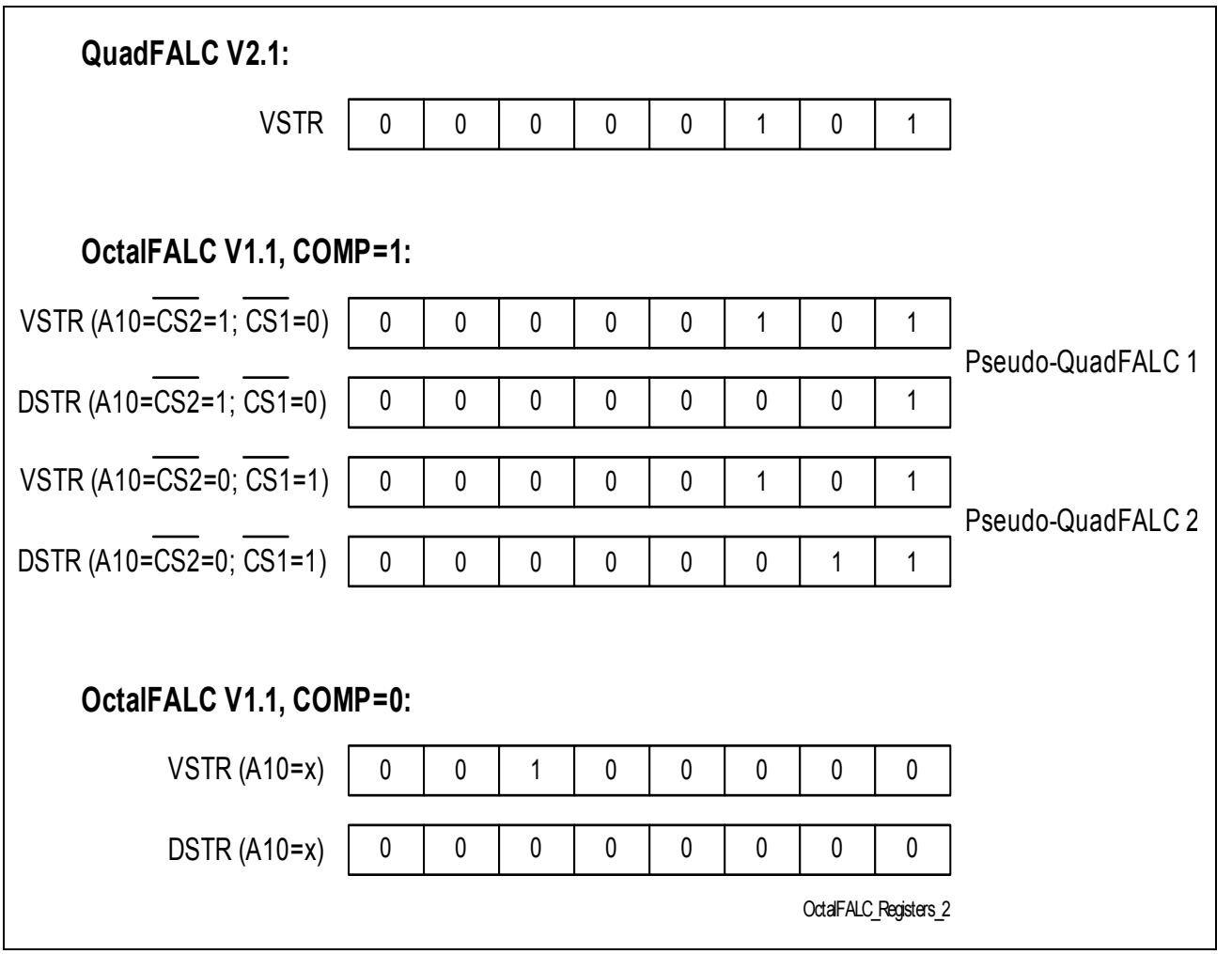


Figure 32 VSTR and DSTR Register Compatibility

15.2 Pseudo QuadFALC® Register GPC1

The register GPC1 (global port configuration register 1) is used in the QuadFALC® to configure the sources of FSC out of the 4 channels. In compatibility mode of the OctalFALC™ (pin COMP = ´1´) this register must have the same function. That means one GPC1 register exists in every of the both pseudo QuadFALC®s. So with these one GPC1register its only possible to control a 4:1 multiplexer. But really eight channels exists in the OctalFALC™ and therefor 8:1 multiplexing must be performed, because only one FSC/SEC pin exists in the OctalFALC™. **Figure 33** shows the principle of the solution using an additional 2:1 multiplexer.

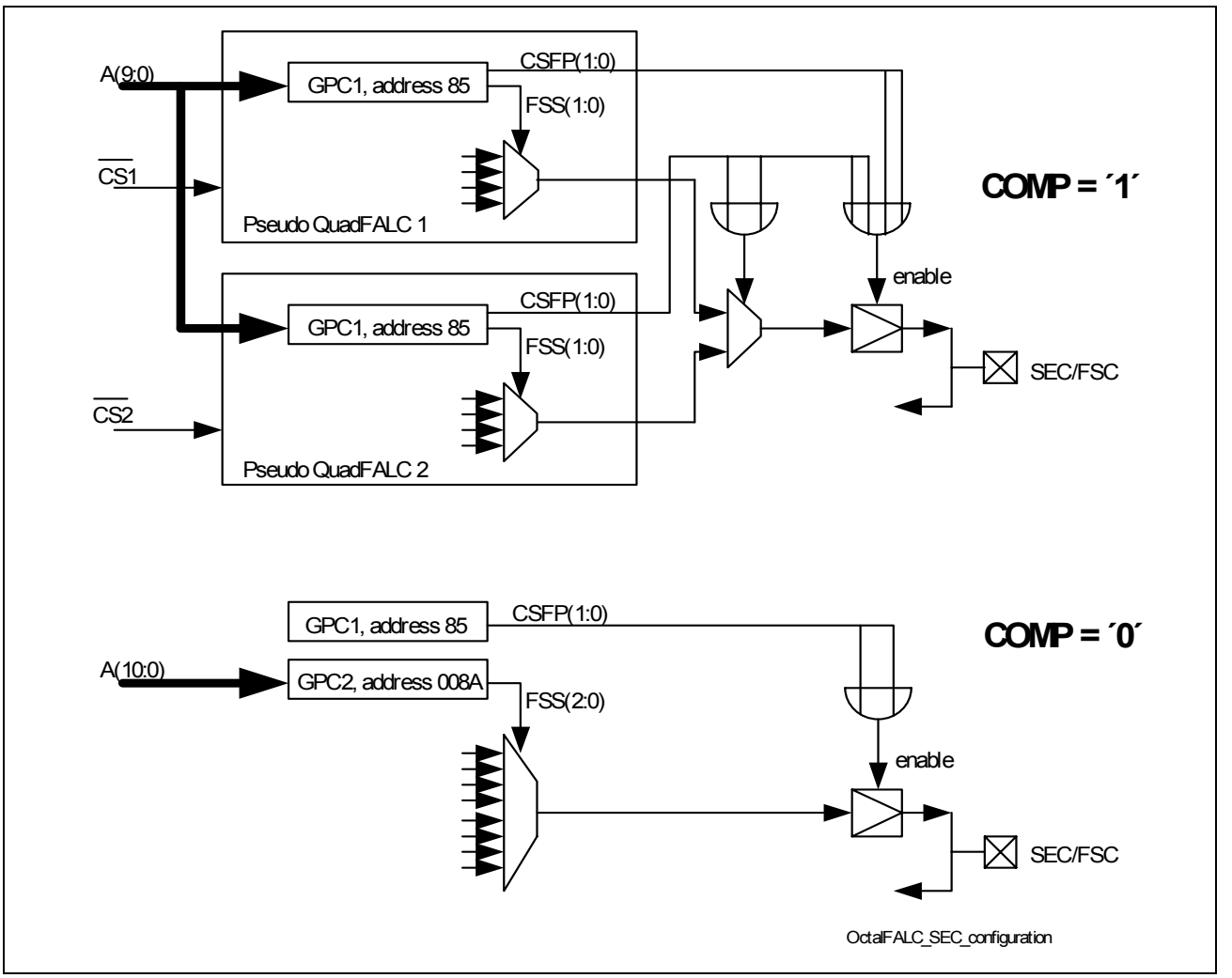


Figure 33 Principle of configuration of SEC/FSC Output

The 2:1 multiplexer is controlled by the register bits GPC1.CSFP(1:0) of the second Pseudo QuadFALC®. Enable of the SEC/FSC pin as output is performed by the register bits GPC1.CSFP(1:0) of the first and the second Pseudo QuadFALC® were all are logical ored.

In not compatibility mode the one global GPC2 register is used instead of the both GPC1 registers in compatibility mode.

15.3 Additional Registers or Register Bits

Only the additional registers or registers with additional bits compared to the QuadFALC® V2.1 are listed below. For detailed register description see the datasheet of the OctalFALC™ (User's Manual).

Table 25 Overview of Additional Control Register Functions for E1 Mode

Register Short Name	Register Long Name	Offset Address
MODE_E	Mode Register	03_H
IPC_E	Interrupt Port Configuration	08_H
CCR2_E	Common Configuration Register 2	$0A_H$
RDICR_E	RDI Clear Condition Register	$0B_H$
IMR3_E	Interrupt Mask Register 3	17_H
IMR4_E	Interrupt Mask Register 4	18_H
IMR5_E	Interrupt Mask Register 5	19_H
IMR6_E	Interrupt Mask Register 6	$1A_H$
XPM2_E	Transmit Pulse Mask2	28_H
SIC4_E	System Interface Control 4	$2A_H$
LIM0_E	Line Interface Mode 0	36_H
SIC3_E	System Interface Control 3	40_H
CMR4_E	Clock Mode Register 4	41_H
CMR5_E	Clock Mode Register 5	42_H
CMR6_E	Clock Mode Register 6	43_H
CMR1_E	Clock Mode Register 1	44_H
CMR2_E	Clock Mode Register 2	45_H
CMR3_E	Clock Mode Register 3	48_H
PC1_E	Port Configuration Register 1	80_H
PC2_E	Port Configuration Register 2	81_H
PC3_E	Port Configuration Register 3	82_H
PC5_E	Port Configuration 5	84_H
GPC1_E	Global Port Configuration 1	85_H
PC6_E	Port Configuration 6	86_H
CMDR3_E	Command Register 3	88_H
CMDR4_E	Command Register 4	89_H
GPC2_E	Global Port Configuration 2	$8A_H$
CCR3_E	Common Configuration Register 3	$8B_H$
CCR4_E	Common Configuration Register 4	$8C_H$
CCR5_E	Common Configuration Register 5	$8D_H$

Table 25 Overview of Additional Control Register Functions for E1 Mode

Register Short Name	Register Long Name	Offset Address
MODE2_E	Mode Register 2	$8E_H$
MODE3_E	Mode Register 3	$8F_H$
GCM2_E	Global Clock Mode Register 2	93_H
GCM4_E	Global Clock Mode Register 4	95_H
XFIFO2L_E	Transmit FIFO 2 Lower Byte	$9C_H$
XFIFO2H_E	Transmit FIFO 2 Higher Byte	$9D_H$
XFIFO3L_E	Transmit FIFO 3 Lower Byte	$9E_H$
XFIFO3H_E	Transmit FIFO 3 Higher Byte	$9F_H$
TSE0_E	Time Slot Even/Odd Select	$A0_H$
TSBS2_E	Time Slot Bit Select 2	$A2_H$
TSBS3_E	Time Slot Bit Select 3	$A3_H$
TSS2_E	Time Slot Select 2	$A4_H$
TSS3_E	Time Slot Select 3	$A5_H$
GIMR_E	Global Interrupt Mask Register	$A7_H$
TPC0_E	Test Pattern Control Register 0	$A8_H$
TXP1_E	TX Pulse Template 1	$C1_H$
TXP2_E	TX Pulse Template 2	$C2_H$
TXP3_E	TX Pulse Template 3	$C3_H$
TXP4_E	TX Pulse Template 4	$C4_H$
TXP5_E	TX Pulse Template 5	$C5_H$
TXP6_E	TX Pulse Template 6	$C6_H$
TXP7_E	TX Pulse Template 7	$C7_H$
TXP8_E	TX Pulse Template 8	$C8_H$
TXP9_E	TX Pulse Template 9	$C9_H$
TXP10_E	TX Pulse Template 10	CA_H
TXP11_E	TX Pulse Template 11	CB_H
TXP12_E	TX Pulse Template 12	CC_H
TXP13_E	TX Pulse Template 13	CD_H
TXP14_E	TX Pulse Template 14	CE_H
TXP15_E	TX Pulse Template 15	CF_H

Table 25 Overview of Additional Control Register Functions for E1 Mode

Register Short Name	Register Long Name	Offset Address
TXP16_E	TX Pulse Template 16	$D0_H$
GPC3_E	Global Port Configuration Register 3	$D3_H$
GPC4_E	Global Port Configuration Register 4	$D4_H$
GPC5_E	Global Port Configuration Register 5	$D5_H$
GPC6_E	Global Port Configuration Register 6	$D6_H$
INBLDTR_E	In Band Loop Detection Time Register	$D7_H$
ALS_E	Automatic Loop Switching	$D9_H$
PRBSTS1_E	PRBS Time Slot Register 1	DB_H
PRBSTS2_E	PRBS Time Slot Register 2	DC_H
PRBSTS3_E	PRBS Time Slot Register 3	DD_H
PRBSTS4_E	PRBS Time Slot Register 4	DE_H
IMR7_E	Interrupt Mask Register 7	DF_H

Table 26 Overview of Additional Status Register Functions for E1 Mode

Offset Address	Register Short Name	Register Long Name
4A	VSTR_E	Version Status Register
6E	GIS_E	Global Interrupt Status
6F	CIS_E	Channel Interrupt Status
90	RBC2_E	Receive Bytecount Register 2
91	RBC3_E	Receive Bytecount Register 3
9A	SIS3_E	Signaling Status Register 3
9B	RSIS3_E	Receive Signaling Status Register 3
A9	SIS2_E	Signaling Status Register 2
AA	RSIS2_E	Receive Signaling Status Register 2
AB	MFPI_E	Multi Function Port Input Status Register
AC	ISR6_E	Interrupt Status Register 6
AD	GIS2_E	Global Interrupt Status 2
D8	ISR7_E	Interrupt Status Register 7
DA	PRBSTA_E	PRBS Status Register

Table 26 Overview of Additional Status Register Functions for E1 Mode

Offset Address	Register Short Name	Register Long Name
E7	DSTR_E	Device Status Register
FE	CLKSTAT_E	Clock Status Register

Table 27 Overview of Additional Control Register Functions for T1/J1

Register Short Name	Register Long Name	Offset Address
MODE_T	Mode Register	03_H
IPC_T	Interrupt Port Configuration	08_H
CCR1_T	Common Configuration Register 1	09_H
CCR2_T	Common Configuration Register 2	$0A_H$
IMR3_T	Interrupt Mask Register 3	17_H
IMR4_T	Interrupt Mask Register 4	18_H
IMR5_T	Interrupt Mask Register 5	19_H
IMR6_T	Interrupt Mask Register 6	$1A_H$
FMR5_T	Framer Mode Register 5	21_H
XC0_T	Transmit Control 0	22_H
XPM2_T	Transmit Pulse-Mask Register 2	28_H
SIC4_T	System Interface Control 4	$2A_H$
LIM0_T	Line Interface Mode 0	36_H
SIC3_T	System Interface Control 3	40_H
CMR4_T	Clock Mode Register 4	41_H
CMR5_T	Clock Mode Register 5	42_H
CMR6_T	Clock Mode Register 6	43_H
CMR1_T	Clock Mode Register 1	44_H
CMR2_T	Clock Mode Register 2	45_H
CMR3_T	Clock Mode Register 3	48_H
DEC_T	Disable Error Counter	60_H
PC1_T	Port Configuration 1	80_H
PC2_T	Port Configuration 2	81_H
PC3_T	Port Configuration 3	82_H

Table 27 Overview of Additional Control Register Functions for T1/J1 (cont'd)

Register Short Name	Register Long Name	Offset Address
PC4_T	Port Configuration 4	83_H
PC5_T	Port Configuration 5	84_H
GPC1_T	Global Port Configuration 1	85_H
PC6_T	Port Configuration 6	86_H
CMDR3_T	Command Register 3	88_H
CMDR4_T	Command Register 4	89_H
GPC2_T	Global Port Configuration 2	$8A_H$
CCR3_T	Common Configuration Register 3	$8B_H$
CCR4_T	Common Configuration Register 4	$8C_H$
MODE2_T	Mode Register 2	$8E_H$
MODE3_T	Mode Register 3	$8F_H$
GCM2_T	Global Clock Mode Register 2	93_H
GCM4_T	Global Clock Mode Register 4	95_H
XFIFO2L_T	Transmit FIFO 2 Lower Byte	$9C_H$
XFIFO2H_T	Transmit FIFO 2 Higher Byte	$9D_H$
XFIFO3L_T	Transmit FIFO 3 Lower Byte	$9E_H$
XFIFO3H_T	Transmit FIFO 3 Higher Byte	$9F_H$
TSE0_T	Time Slot Even/Odd Select	$A0_H$
TSBS2_T	Time Slot Bit Select 2	$A2_H$
TSBS3_T	Time Slot Bit Select 3	$A3_H$
TSS2_T	Time Slot Select 2	$A4_H$
TSS3_T	Time Slot Select 3	$A5_H$
GIMR_T	Global Interrupt Mask Register	$A7_H$
TPC0_T	Test Pattern Control Register 0	$A8_H$
TXP1_T	TX Pulse Template 1	$C1_H$
TXP2_T	TX Pulse Template 2	$C2_H$
TXP3_T	TX Pulse Template 3	$C3_H$
TXP4_T	TX Pulse Template 4	$C4_H$
TXP5_T	TX Pulse Template 5	$C5_H$
TXP6_T	TX Pulse Template 6	$C6_H$

Table 27 Overview of Additional Control Register Functions for T1/J1 (cont'd)

Register Short Name	Register Long Name	Offset Address
TXP7_T	TX Pulse Template 7	$C7_H$
TXP8_T	TX Pulse Template 8	$C8_H$
TXP9_T	TX Pulse Template 9	$C9_H$
TXP10_T	TX Pulse Template 10	CA_H
TXP11_T	TX Pulse Template 11	CB_H
TXP12_T	TX Pulse Template 12	CC_H
TXP13_T	TX Pulse Template 13	CD_H
TXP14_T	TX Pulse Template 14	CE_H
TXP15_T	TX Pulse Template 15	CF_H
TXP16_T	TX Pulse Template 16	$D0_H$
GPC3_T	Global Port Configuration Register 3	$D3_H$
GPC4_T	Global Port Configuration Register 4	$D4_H$
GPC5_T	Global Port Configuration Register 5	$D5_H$
GPC6_T	Global Port Configuration Register 6	$D6_H$
INBLDTR_T	In Band Loop Detection Time Register	$D7_H$
ALS_T	Automatic Loop Switching	$D9_H$
PRBSTS1_T	PRBS Time Slot Register 1	DB_H
PRBSTS2_T	PRBS Time Slot Register 2	DC_H
PRBSTS3_T	PRBS Time Slot Register 3	DD_H
PRBSTS4_T	PRBS Time Slot Register 4	DE_H
IIMR7_T	Interrupt Mask Register 7	DF_H

Table 28 Overview of Additional Status Register Functions for T1/J1s

Register Short Name	Register Long Name	Offset Address
VSTR_T	Version Status Register	$4A_H$
GIS_T	Global Interrupt Status Register	$6E_H$
CIS_T	Channel Interrupt Status Register	$6F_H$
RBC2_T	Receive Byte Count Register 2	90_H
RBC3_T	Receive Byte Count Register 3	91_H

Table 28 Overview of Additional Status Register Functions for T1/J1s (cont'd)

Register Short Name	Register Long Name	Offset Address
SIS3_T	Signaling Status Register 3	$9A_H$
RSIS3_T	Receive Signaling Status Register 3	$9B_H$
RFIFO2L_T	Receive FIFO 2 Lower Byte	$9C_H$
RFIFO2H_T	Receive FIFO 2 Higher Byte	$9D_H$
RFIFO3L_T	Receive FIFO 3 Lower Byte	$9E_H$
RFIFO3H_T	Receive FIFO 3 Higher Byte	$9F_H$
SIS2_T	Signaling Status Register 2	$A9_H$
RSIS2_T	Receive Signaling Status Register 2	AA_H
MFPI_T	Multi Function Port Input Status Register 2	AB_H
ISR6_T	Interrupt Status Register 6	AC_H
GIS2_T	Global Interrupt Status 2	AD_H
PPR0_T	PPR Data Register 0	$D1_H$
PPR1_T	PPR Data Register 1	$D2_H$
ISR7_T	Interrupt Status Register 7	$D8_H$
PRBSTA_T	PRBS Status Register	DA_H
DSTR_T	Device Status Register	$E7_H$
CLKSTAT_T	Clock Status Register	FE_H

16 External Signals

In addition to the signals known from QuadFALC®, several add-on functions are provided.

The logic symbol is shown in **Figure 1**.

A signal list is given in **Table 29**.

Only additional signals or signals with extended functions against the QuadFALC® V2.1 are listed. For functional description of the other signals see the QuadFALC® V2.1 Data Sheet (User's Manual) or OctalFALC™ Data Sheet (User's Manual).

If a pin function is controlled by a register (e.g. multi function pins) the reset configuration of this pin like I/O, tristate, PD and PU is given by the reset value of the appropriate register.

Table 29 I/O Signals

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
Analog Line Interface					
-	7A	**RLS21**	IO	-	**Receive Line Switch, Port 1**
-	3A	**RLS22**	IO	-	**Receive Line Switch, Port 2**
-	3T	**RLS23**	IO	-	**Receive Line Switch, Port 3**
-	7R	**RLS24**	IO	-	**Receive Line Switch, Port 4**
-	11T	**RL1.5**	I	-	**Line Receiver, Port 5** Analog input 1
		RDIP5	I	-	**Receive Digital Input Positive 5**
		ROID5	I	-	**Receive Optical Interface Data 5**
-	9T	**RL2.5**	I	-	**Line Receiver, Port 5** Analog input 2
		RDIN5	I	-	**Receive Digital Input Negative 5**
		RCLKI5	I	-	**Receive Clock 5**
-	10T	**RLS25**	IO	-	**Receive Line Switch, Port 5**
-	13T	**RL1.6**	I	-	**Line Receiver, Port 6** Analog input 1
		RDIP6	I	-	**Receive Digital Input Positive 6**
		ROID6	I	-	**Receive Optical Interface Data 6**

Table 29 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
-	15T	**RL2.6**	I	-	**Line Receiver, Port 6** Analog input 2
		RDIN6	I	-	**Receive Digital Input Negative 6**
		RCLKI6	I	-	**Receive Clock 6**
-	14T	**RLS26**	IO	-	**Receive Line Switch, Port 6**
-	13A	**RL1.7**	I	-	**Line Receiver, Port 7** Analog input 1
		RDIP7	I	-	**Receive Digital Input Positive 7**
		ROID7	I	-	**Receive Optical Interface Data 7**
-	15A	**RL2.7**	I	-	**Line Receiver, Port 7** Analog input
		RDIN7	I	-	**Receive Digital Input Negative 7**
		RCLKI7	I	-	**Receive Clock 7**
-	14A	**RLS27**	IO	-	**Receive Line Switch, Port 7**
-	11A	**RL1.8**	I	-	**Line Receiver, Port 8** Analog input 1
		RDIP8	I	-	**Receive Digital Input Positive 8**
		ROID8	I	-	**Receive Optical Interface Data 8**
-	10A	**RL2.8**	I	-	**Line Receiver, Port 8** Analog input 2
		RDIN8	I	-	**Receive Digital Input Negative 8**
		RCLKI8	I	-	**Receive Clock 8**
-	10B	**RLS28**	IO	-	**Receive Line Switch, Port 8**
-	7C	**XL3.1**	I	-	**Line Transmitter, Port 1** Analog input1
-	6C	**XL4.1**	I	-	**Line Transmitter, Port 1** Analog input2
-	4C	**XL3.2**	I	-	**Line Transmitter, Port 2** Analog input1
-	3C	**XL4.2**	I	-	**Line Transmitter, Port 2** Analog input2

Table 29 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
-	4P	**XL3.3**	I	-	**Line Transmitter, Port 3** Analog input1
-	3P	**XL4.3**	I	-	**Line Transmitter, Port 3** Analog input2
-	7N	**XL3.4**	I	-	**Line Transmitter, Port 4** Analog input1
-	6N	**XL4.4**	I	-	**Line Transmitter, Port 4** Analog input2
-	11N	**XL1.5**	O	-	**Line Transmitter, Port 5** Analog output1
		XDOP5	O	-	**Transmit Digital Output Positive 5**
		XOID5	O	-	**Transmit Optical Interface Data 5**
-	10N	**XL2.5**	O	-	**Line Transmitter, Port 5** Analog output2
		XDON5	O	-	**Transmit Digital Output Negative 5**
		XFM5	O	-	**Transmit Frame Marker 5**
-	11P	**XL3.5**	I	-	**Line Transmitter, Port 5** Analog input1
-	10P	**XL4.5**	I	-	**Line Transmitter, Port 5** Analog input2
-	14N	**XL1.6**	O	-	**Line Transmitter, Port 6** Analog output1
		XDOP6	O	-	**Transmit Digital Output Positive 6**
		XOID6	O	-	**Transmit Optical Interface Data 6**
-	13N	**XL2.6**	O	-	**Line Transmitter, Port 6** Analog output2
		XDON6	O	-	**Transmit Digital Output Negative 6**
		XFM6	O	-	**Transmit Frame Marker 6**
-	14P	**XL3.6**	I	-	**Line Transmitter, Port 6** Analog input1
-	13P	**XL4.6**	I	-	**Line Transmitter, Port 6** Analog input2

Table 29 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
-	14D	**XL1.7**	O	-	**Line Transmitter, Port 7** Analog output1
		XDOP7	O	-	**Transmit Digital Output Positive 7**
		XOID7	O	-	**Transmit Optical Interface Data 7**
-	13D	XL2.7	O	-	**Line Transmitter, Port 7** Analog output2
		XDON7	O	-	**Transmit Digital Output Negative 7**
		XFM7	O	-	**Transmit Frame Marker 7**
-	14C	**XL3.7**	I	-	**Line Transmitter, Port 7** Analog input1
-	13C	**XL4.7**	I	-	**Line Transmitter, Port 7** Analog input2
-	11E	**XL1.8**	O	-	**Line Transmitter, Port 8** Analog output1
		XDOP8	O	-	**Transmit Digital Output Positive 8**
		XOID8	O	-	**Transmit Optical Interface Data 8**
-	10E	**XL2.8**	O	-	**Line Transmitter, Port 8** Analog output2
		XDON8	O	-	**Transmit Digital Output Negative 8**
		XFM8	O	-	**Transmit Frame Marker 8**
-	11D	**XL3.8**	I	-	**Line Transmitter, Port 8** Analog input1
-	10D	**XL4.8**	I	-	**Line Transmitter, Port 8** Analog input
Operation Mode Selection and Device Initialization					

Table 29 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
-	8B	**COMP**	I	PU	**Software Compatibility Mode** 1_B **QuadFALC® Mode** ("Compatibility Mode") is selected: OctalFALC™ can be used as it consists on two separate "pseudo" QuadFALCs. 0_B **OctalFALC™ Mode** ("Generic Mode") is selected. COMP is only valid if Motorola or Intel bus interface mode is selected by IM(1:0). If SPI or SCI slave mode is selected for the interface, COMP is not valid and the OctalFALC™ is in "Generic Mode", see Table 1.
-	6B	**IM1**	I	PU	**Interface Mode Selection** 00_B **Intel Bus Mode, async.** 01_B **Motorola Bus Mode, async.** 10_B **SPI Bus Slave Mode** 11_B **SCI Bus Slave Mode** Two parallel (Intel, Motorola) and two serial (SPI, SCI) interface modes can be selected.
-	4B	**IM0**	I	PU	

Table 29 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
Microprocessor and Serial Interfaces					
-	K12	**A10**	I	PU	**Address Bus, Line 10** MSB of address if COMP = 0_B and if microcontroller mode (Intel, Motorola) is selected, see **Table 1** and **Table 30**
		$\overline{CS2}$	I	PU	**Chip Select 2** Low active chip select for second "pseudo" QuadFALC® if COMP = 1_B and if microcontroller mode (Intel, Motorola) is selected, see **Table 1** and **Table 30**
-	J12	**A5**	I	PU	**Address Bus, Line 5**
		A5	I	PU	**SCI source address bit 5 (MSB)**, only used if SCI interface mode is selected, see **Table 30** and **Table 5**
-	J15	**A4**	I	PU	**Address Bus, Line 4**
		A4	I	PU	**SCI source address bit 4**, only used if SCI interface mode is selected, see **Table 30** and **Table 5**
-	J16	**A3**	I	PU	**Address Bus, Line 3**
		A3	I	PU	**SCI source address bit 3**, only used if SCI interface mode is selected, see **Table 30** and **Table 5**
-	J14	**A2**	I	PU	**Address Bus, Line 2**
		A2	I	PU	**SCI source address bit 2**, only used if SCI interface mode is selected, see **Table 30** and **Table 5**
-	J13	**A1**	I	PU	**Address Bus, Line 1**
		A1	I	PU	**SCI source address bit 1**, only used if SCI interface mode is selected, see **Table 30** and **Table 5**

Table 29 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
-	G16	**A0**	I	PU	**Address Bus, Line 0 (LSB)**
		A0	I	PU	**SCI source address bit 0**, only used if SCI interface mode is selected, see Table 30 and Table 5
-	1F	**D15**	IO	PU	**Data Bus, Line 15**
		PLL10	I	PU	**PLL programming bit 10**, only used if SCI or SPI interface mode is selected, see Table 30
-	2F	**D14**	IO	PU	**Data Bus, Line 14**
		PLL9	I	PU	**PLL programming bit 9**, only used if SCI or SPI interface mode is selected, see Table 30
-	3F	**D13**	IO	PU	**Data Bus, Line 13**
		PLL8	I	PU	**PLL programming bit 8**, only used if SCI or SPI interface mode is selected, see Table 30
-	4F	**D12**	IO	PU	**Data Bus, Line 12**
		PLL7	I	PU	**PLL programming bit 7**, only used if SCI or SPI interface mode is selected, see Table 30
-	1G	**D11**	IO	PU	**Data Bus, Line 11**
		PLL6	I	PU	**PLL programming bit 6**, only used if SCI or SPI interface mode is selected, see Table 30
-	2G	**D10**	IO	PU	**Data Bus, Line 10**
		PLL5	I	PU	**PLL programming bit 5**, only used if SCI or SPI interface mode is selected, see Table 30
-	3G	**D9**	IO	PU	**Data Bus, Line 9**
		PLL4	I	PU	**PLL programming bit 4**, only used if SCI or SPI interface mode is selected, see Table 30

Table 29 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
-	1H	**D8**	IO	PU	**Data Bus, Line 8**
		PLL3	I	PU	**PLL programming bit 3**, only used if SCI or SPI interface mode is selected, see **Table 30**
-	2H	**D7**	IO	PU	**Data Bus, Line 7**
		PLL2	I	PU	**PLL programming bit 2**, only used if SCI or SPI interface mode is selected, see **Table 30**
-	1J	**D6**	IO	PU	**Data Bus, Line 6**
		PLL1	I	PU	**PLL programming bit 1**, only used if SCI or SPI interface mode is selected, see **Table 30**
-	3H	**D5**	IO	PU	**Data Bus, Line 5**
		PLL0	I	PU	**PLL programming bit 0**, only used if SCI or SPI interface mode is selected, see **Table 30**
-	3K	**D2**	IO	PU	**Data Bus, Line 2**
		SCI_CLK	I	-	**SCI Bus clock**, if SCI interface mode is selected
		SCLK	I	-	**SPI Bus Clock**, if SPI interface mode is selected
-	1K	**D1**	IO	PU	**Data Bus, Line 1**
		SCI_RXD	I	PU	**SCI bus Serial Data In**, if SCI interface mode is selected
		SDI	I	PU	**SPI bus Serial Data In**, if SPI interface mode is selected
-	2K	**D0**	IO	PU	**Data Bus, Line 0**
		SCI_TXD	O	PP or oD	**SCI bus Serial Data Out**, if SCI interface mode is selected
		SDO	O	PU	**SPI bus Serial Data Out**, if SPI interface mode is selected

Table 29 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
-	12H	**$\overline{CS}$**	I	PU	**Chip Select** Low active chip select if SPI or SCI interface mode is selected or if COMP = ´0_B´ and microcontroller mode (Intel, Motorola) is selected, see **Table 1**
		$\overline{CS1}$	I	PU	**Chip Select 1** Low active chip select for first "pseudo" QuadFALC® if COMP = ´1_B´ and if microcontroller mode (Intel, Motorola) is selected, see **Table 1** and **Table 30**.
-	11H	**INT**	O	-	**Interrupt Output** if COMP = ´0_B´
		INT1	O	-	**Interrupt Output 1** Interrupt output of first "pseudo" QuadFALC ® if COMP = ´1_B´
-	14H	**INT2**	O	-	**Interrupt Output 2** Interrupt output of second "pseudo" QuadFALC® if COMP = ´1_B´
	14G	**$\overline{READY}$**	O	-	**Data Ready** (Intel Bus Mode)
		$\overline{DTACK}$	O	-	**Data Acknowledge** (Motorola Bus Mode)
Clock Signals					
-	16P	**SCLKR5**	IO	PU	**System Clock Receive, Port 5**
-	16M	**SCLKR6**	IO	PU	**System Clock Receive, Port 6**
-	13F	**SCLKR7**	IO	PU	**System Clock Receive, Port 7**
-	16E	**SCLKR8**	IO	PU	**System Clock Receive, Port 8**
-	12M	**SCLKX5**	IO	PU	**System Clock Transmit, Port 5**
-	16L	**SCLKX6**	IO	PU	**System Clock Transmit, Port 6**
-	12F	**SCLKX7**	IO	PU	**System Clock Transmit, Port 7**
-	16D	**SCLKX8**	IO	PU	**System Clock Transmit, Port 8**
System Interface					
-	15P	**RDO5**	O	-	**Receive Data Out, Port 5**

Table 29 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
-	10M	**RDO6**	O	-	**Receive Data Out, Port 6**
-	15F	**RDO7**	O	-	**Receive Data Out, Port 7**
-	13E	**RDO8**	O	-	**Receive Data Out, Port 8**
-	11M	**XDI5**	I	-	**Transmit Data In, Port 5**
-	14L	**XDI6**	I	-	**Transmit Data In, Port 6**
-	9F	**XDI7**	I	-	**Transmit Data In, Port 7**
-	15C	**XDI8**	I	-	**Transmit Data In, Port 8**
Multifunction Ports					
-	1B	**RPA1**	IO	PU/-	**Receive Multifunction Port A, Port 1**
-	2D	**RPB1**	IO	PU/-	**Receive Multifunction Port B, Port 1**
-	7E	**RPC1**	IO	PU/-	**Receive Multifunction Port C, Port 1**
-	6E	**RPA2**	IO	PU/-	**Receive Multifunction Port A, Port 2**
-	8E	**RPB2**	IO	PU/-	**Receive Multifunction Port B, Port 2**
-	9E	**RPC2**	IO	PU/-	**Receive Multifunction Port C, Port 2**
-	4L	**RPA3**	IO	PU/-	**Receive Multifunction Port A, Port 3**
-	2L	**RPB3**	IO	PU/-	**Receive Multifunction Port B, Port 3**
-	1L	**RPC3**	IO	PU/-	**Receive Multifunction Port C, Port 3**
-	4M	**RPA4**	IO	PU/-	**Receive Multifunction Port A, Port 4**
-	5M	**RPB4**	IO	PU/-	**Receive Multifunction Port B, Port 4**
-	2N	**RPC4**	IO	PU/-	**Receive Multifunction Port C, Port 4**
-	16R	**RPA5**	IO	PU/-	**Receive Multifunction Port A, Port 5**
-	15N	**RPB5**	IO	PU/-	**Receive Multifunction Port B, Port 5**
-	16N	**RPC5**	IO	PU/-	**Receive Multifunction Port C, Port 5**
-	13M	**RPA6**	IO	PU/-	**Receive Multifunction Port A, Port 6**
-	13L	**RPB6**	IO	PU/-	**Receive Multifunction Port B, Port 6**
-	15L	**RPC6**	IO	PU/-	**Receive Multifunction Port C, Port 6**
-	16F	**RPA7**	IO	PU/-	**Receive Multifunction Port A, Port 7**
-	14F	**RPB7**	IO	PU/-	**Receive Multifunction Port B, Port 7**
-	10F	**RPC7**	IO	PU/-	**Receive Multifunction Port C, Port 7**
-	12E	**RPA8**	IO	PU/-	**Receive Multifunction Port A, Port 8**

Table 29 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
-	15D	**RPB8**	IO	PU/-	**Receive Multifunction Port B, Port 8**
-	11F	**RPC8**	IO	PU/-	**Receive Multifunction Port C, Port 8**
-	3E	**XPA1**	IO	PU/-	**Transmit Multifunction Port A, Port 1**
-	2E	**XPB1**	IO	PU/-	**Transmit Multifunction Port B, Port 1**
-	5F	**XPA2**	IO	PU/-	**Transmit Multifunction Port A, Port 2**
-	6F	**XPB2**	IO	PU/-	**Transmit Multifunction Port B, Port 2**
-	7L	**XPA3**	IO	PU/-	**Transmit Multifunction Port A, Port 3**
-	2M	**XPB3**	IO	PU/-	**Transmit Multifunction Port B, Port 3**
-	1P	**XPA4**	IO	PU/-	**Transmit Multifunction Port A, Port 4**
-	1R	**XPB4**	IO	PU/-	**Transmit Multifunction Port B, Port 4**
-	14M	**XPA5**	IO	PU/-	**Transmit Multifunction Port A, Port 5**
-	15M	**XPB5**	IO	PU/-	**Transmit Multifunction Port B, Port 5**
-	12L	**XPA6**	IO	PU/-	**Transmit Multifunction Port A, Port 6**
-	11L	**XPB6**	IO	PU/-	**Transmit Multifunction Port B, Port 6**
-	14E	**XPA7**	IO	PU/-	**Transmit Multifunction Port A, Port 7**
-	15E	**XPB7**	IO	PU/-	**Transmit Multifunction Port B, Port 7**
-	16C	**XPA8**	IO	PU/-	**Transmit Multifunction Port A, Port 8**
-	16B	**XPB8**	IO	PU/-	**Transmit Multifunction Port B, Port 8**

A pinstrapping overview is given in **Table 30**.

Table 30 Pinstrapping Overview

Pin	Used	Pinstrapping Function
COMP	always	defines the compatibility mode if microcontroller interface mode (Intel or Motorola) is selected by IM(1:0). If serial interface modes (SPI, SCI) are selected, COMP is not valid, see **Table 1**
IM(1:0)	always	defines the interface mode, see **Table 1**

Table 30 Pinstrapping Overview (cont'd)

Pin	Used	Pinstrapping Function
A(10)	only in micro controller interface modes	Used as second chip select signal in compatibility mode, see **Table 1**
A(5:0)	only in SCI interface mode	Defines the 6 MSBs of the SCI source address, if SCI interface mode is selected by IM(1:0), see **Chapter 4.1** A5 is MSB
D(15:5)	only in SCI or SPI interface mode	Programs PLL if SPI- or SCI-Interface is used instead of registers GCM5 and GCM6, see **Chapter 4**. If SPI- or SCI-Interface is selected - D(15:11) values programs PLL dividing factor M, - D(10:5) values programs PLL dividing factor N equivalent to programming by register bits GCM5.PLL_M(4:0) or GCM6.PLL_N(5:0) as it is if microcontroller mode (Intel or Motorola) is selected

17 Package

Due to the increased number of signals, a PG-LBGA-256-1 package is used. It uses a 16 × 16 full matrix (256 balls at 1 mm ball pitch), with an overall package size of 17 mm × 17 mm. See **Figure 34** for mechanical details. The package uses "green" package materials only (halogen-free, lead-free solder balls, etc.). Solder balls with lead are available on request.

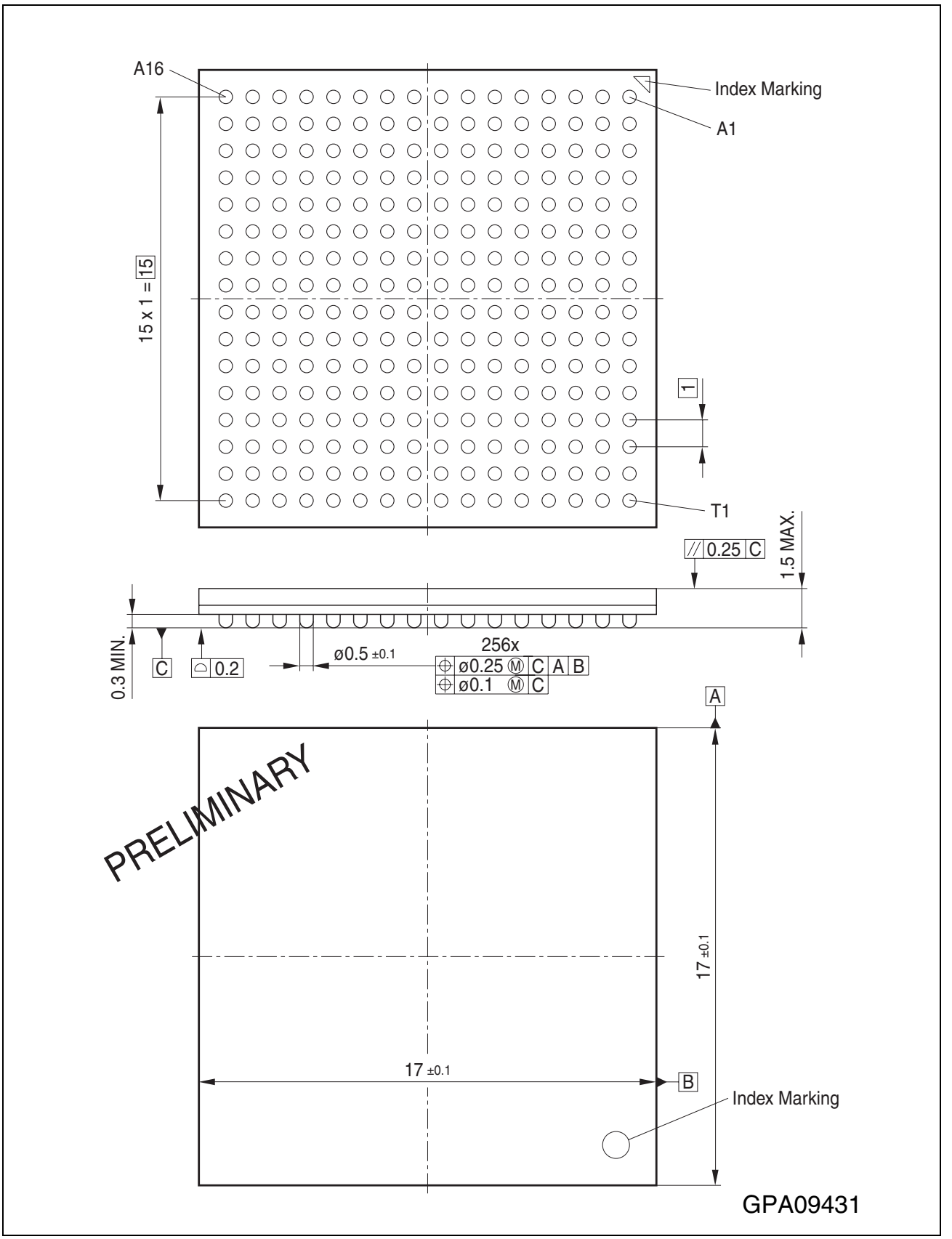


Figure 34 **PG-LBGA-256-1** (Plastic Green Low Profile Ball Grid Array Package)

18 Electrical Characteristics

This chapter describes operating conditions and DC characteristics and limits.

18.1 Absolute Maximum Ratings

Table 31 defines the maximum voltages and temperature which may be applied to the device without damage.

Table 31 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Ambient temperature under bias	T_A	-40	–	+85	°C	–
Storage temperature	T_{STG}	-65	–	+125	°C	–
Moisture Level 3 temperature	T_{ML3}	–	–	+225	°C	According to IPS J-STD 020
				+245	°C	According to Infineon internal standard
Supply voltage (pads, digital)	V_{DD}	-0.5	3.30	4.50	V	–
Supply voltage (core, digital)	V_{DDC}	-0.5	1.80	2.40	V	–
Supply voltage (PLL, analog)	V_{DDP}	-0.4	3.30	4.50	V	–
Supply voltage (receiver, analog)	V_{DDR}	-0.4	3.30	4.50	V	–
Supply voltage (transmitter, analog)	V_{DDX}	-0.4	3.30	4.50	V	–
Receiver input signal with respect to ground	V_{RLmax}	-0.8	–	4.50	V	RL1/RL2
Voltage on any pin with respect to ground	V_{max}	-0.4	–	4.50	V	except V_{DDC}, RL1/RL2

Table 31 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
ESD robustness HBM	$V_{ESD,HBM}$	–	–	2000	V	1.5 kΩ, 100 pF; according to EIA/JESD22-A114-B
ESD robustness CDM	$V_{ESD,CDM}$	–	–	500	V	According to ESD Association Standard DS5.3.1 - 1999

Attention: Absolute Maximum Ratings are stress ratings only, and functional operation and reliability under conditions beyond those defined in the normal operating conditions is not guaranteed. Stresses above the maximum ratings are likely to cause permanent damage to the chip.

18.2 Operating Range

Table 32 defines the maximum voltages and temperature which may be applied to guarantee proper operation.

Table 32 Operating Range

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Ambient temperature	T_A	-40	–	+85	°C	–
Supply voltage (pads, digital)	V_{DD}	3.13	3.30	3.46	V	3.3 V ±5%
Supply voltage (core, digital)	V_{DDC}	1.62	1.80	1.98	V	1.8 V ±10%
Supply voltage (PLL, analog)	V_{DDP}	3.13	3.30	3.46	V	3.3 V ±5%
Supply voltage (receiver, analog)	V_{DDR}	3.13	3.30	3.46	V	3.3 V ±5% 1)
Supply voltage (transmitter, analog)	V_{DDX}	3.13	3.30	3.46	V	3.3 V ±5%
Analog input voltages on RL1/2	V_{RL}	0	–	V_{DDR} +0.3V	V	RL1, RL2

Table 32 Operating Range (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Digital input voltages	V_{ID}	-0.4	–	3.46	V	3.3 V ±5%
Ground	V_{SS} V_{SSR} V_{SSX}	0	0	0	V	

1) Voltage ripple on analog supply less than 50 mV

Note: V_{DD}, V_{DDR} and V_{DDX} have to be connected to the same voltage level.

18.3 DC Characteristics

Table 33 DC Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input low voltage	V_{IL}	– 0.4	–	0.8	V	1)
Input high voltage	V_{IH}	2.0	–	3.46	V	1)
Output low voltage	V_{OL}	V_{SS}	–	0.45	V	I_{OL} = + 2 mA 2)
Output high voltage	V_{OH}	2.4	–	V_{DD}	V	I_{OH} = - 2 mA2)
Average power supply current (analog line interface mode, single power supply)	I_{DDE1}	–	t.b.d.	t.b.d.	mA	E1 application LIM1.DRS = 0_B VSEL = $1_{B;}$ PRBS pattern
	I_{DDT1}	–	t.b.d.	t.b.d.	mA	T1 application LIM1.DRS = 0_B VSEL = 1_B PRBS pattern
Average power supply current (analog line interface mode, single power supply)	I_{DDE1}	–	t.b.d.	t.b.d.	mA	E1 application LIM1.DRS = 0_B VSEL = 1_B All-One pattern
	I_{DDT1}	–	t.b.d.	t.b.d.	mA	T1 application LIM1.DRS = 0_B VSEL = 1_B All-One pattern

Table 33 DC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Average power supply current (digital line interface mode, single power supply)	I_{DD}	–	t.b.d.	t.b.d.	mA	LIM1.DRS = 1_B [3] VSEL = 1_B
Input leakage current	I_{L11}	–	–	1	µA	V_{IN} =V_{DD} [4]
Input leakage current	I_{IL12}	–	–	1	µA	V_{IN} =V_{SS} [4]
Input pullup current	I_P	2	–	15	µA	V_{IN} =V_{SS}
Output leakage current	I_{OZ1}	–	–	1	µA	V_{OUT} = *tristate* $V_{SS} < V_{meas} < V_{DD}$ measured against V_{DD} and V_{SS}; all except XL1/2
Transmitter leakage current	I_{TL}	–	–	30	µA	XL1/2 = V_{DDX}; XPM2.XLT = 1
		–	–	30	µA	XL1/2 = V_{SSX}; XPM2.XLT = 1
Transmitter output impedance	R_X	–	–	3	Ω	applies to XL1and XL2 [5]
Transmitter output current	I_X	–	–	105	mA	XL1, XL2
Differential peak voltage of a mark	V_X	–	–	2.15	V	Voltage between XL1 and XL2
Receiver peak voltage of a mark (at RL1 or RL2)	V_{R12}	-0.45	–	3.8	V	RL1, RL2
		-0.75	–	4.1	V	RZ signals, during T1 pulse over-/undershoot only
Receiver differential peak voltage of a mark (between RL1 and RL2)	V_{RL12}	–	–	4.00	V	RL1, RL2
		–	–	4.63	V	RZ signals, during T1 pulse over-/undershoot only

Table 33 DC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Receiver input impedance	Z_R	–	50	–	kΩ	5)
Receiver sensitivity	S_{RLH}	-43	–	0	dB	RL1, RL2 E1 mode
		-36	–	0		RL1, RL2 T1 mode

1) Applies to all input pins except analog pins RLx
2) Applies to all output pins except pins XLx
3) System interface at 16 MHz; all-ones data.
4) Pin leakage is measured in a test mode with all internal pullups disabled.
5) Parameter not tested in production

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