an Intel company

2.5 Gbit/s Laser Driver GD16573A

Preliminary

General Description

The GD16573A is a high performance low power 2.5 Gbit/s Laser Driver.

The GD16573A is designed to meet and exceed ITU-T STM-16 or SONET OC-48 fiberoptic communication systems requirements.

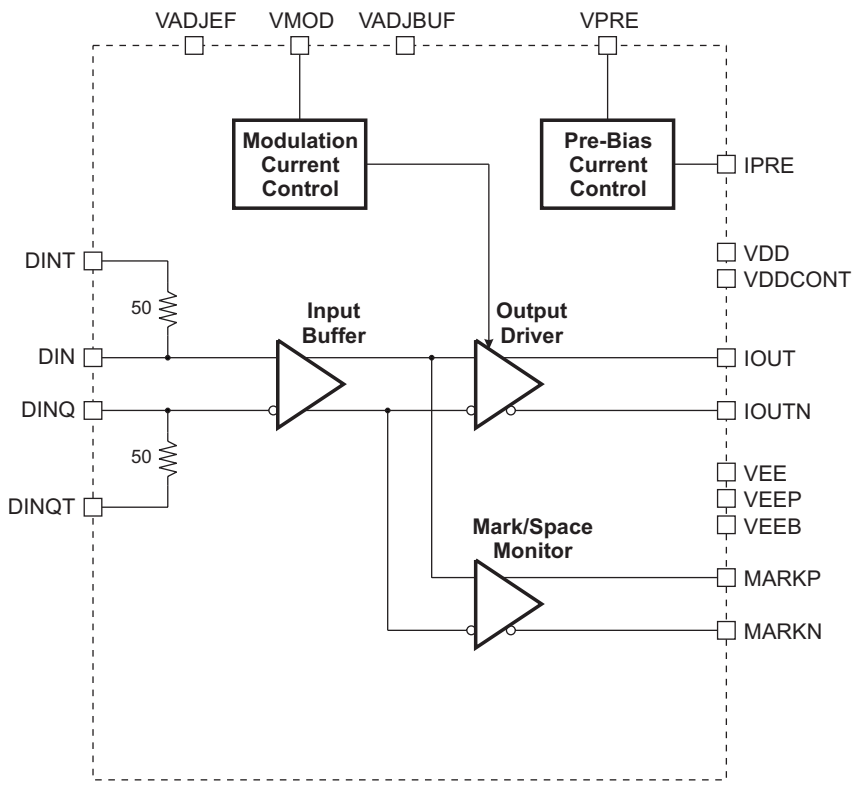
The GD16573A is designed to sink a Modulation Current into the IOUT pin and a Pre-Bias Current into the IPRE pin. The Modulation Current is adjustable up to 70 mA by means of the pin VMOD. The Pre-Bias Current may be adjusted up to 50 mA by means of the VPRE pin.

A Mark-Space monitor is available on the pins MARKP and MARKN.

The GD16573A is implemented in a Silicon Bipolar process.

The GD16573A requires a single +5 V supply or a single -5.2 V supply.

The circuit is available in a thermally enhanced 32-pin TQFP plastic package.



Features

- Complies with ITU-T STM-16 and SONET OC-48 standards.
- Intended for driving a 25 Ω load, e.g. a laser diode with 25 Ω input impedance.
- Large modulation current adjustment range from 5 mA to 70 mA.
- Output voltage over / under shoot less than ±2 % respectively ±5 %.
- Rise / fall times less than 100 ps.
- Laser diode pre-bias adjustable up to 50 mA.
- Mark-Space monitor.
- Internal 50 Ω termination of data and clock inputs.
- Operates up to 3.5 Gbit/s.
- Power dissipation: 0.38 W. Excluding Modulation Current and Pre-bias Current.
- Silicon Bipolar process.
- 32 pin thermally enhanced TQFP plastic package.

Applications

- Tele Communication:
  - SDH STM-16
  - SONET OC-48
- Datacom up to 3.125 Gbit/s.
- Electro Absorption laser driver.
- Direct Modulation laser driver.

Functional Details

GD16573A is a 2.5 Gbit/s laser driver. It is capable of driving high power laser diodes, typically having input impedance of 25 Ω, at a maximum modulation current of 70 mA and a maximum pre-bias current of 50 mA.

The differential data inputs (DINT and DINQT) are internally terminated to the DINT and DINQT respectively with 50 Ω resistors. This allows loop-through termination on both inputs and ensures optimum jitter performance. The input sensitivity when driven with a single ended signal is better than 150 mV.

The output pin (IOUT) is an open collector output designed for driving external loads with 25 Ω characteristic impedance. Because of the nature of an open collector the output therefore may be regarded as a current switch, with infinite output impedance. The characteristic impedance through the package is approximately 25 Ω. Optimum performance of GD16573A therefore is achieved if the output is terminated into a 25 Ω impedance.

The output modulation current is controlled by the pin VMOD and can be controlled in the range from 0 mA to 70 mA, however the specifications is only valid in the range from 5 mA to 70 mA.

The output voltage swing across the external load may be varied accordingly. The modulation current control on pin VMOD is implemented as a current mirror and therefore sinks a current proportional to the modulation current. The current sink into the VMOD pin is approximately 3/80 of the modulation current.

Two additional pins (VADJBUF and VADJEF) are available in order to optimise the performance of the output signal quality, specifically with respect to overshoot and undershoot. Typically best performance is obtained if these pins are connected to VMOD.

The pre-bias current is controlled by the pin VPRE and can be controlled from 0 mA to 50 mA. The pre-bias current control on pin VPRE is implemented as a current mirror and therefore sinks a current proportional to the pre-bias current. The current sink into the VPRE pin is approximately 3/500 of the pre-bias current.

An important parameter for laser drivers is voltage overshoot on the output pin (IOUT), because it determines the extinction ratio. GD16573A has been designed with special emphasis on achieving a very small voltage overshoot. For GD16573A the voltage overshoot is less than 2 % across the full modulation current range, when driving a 25 Ω load. Similarly the voltage undershoot is less than 5 %.

A mark-space monitor is provided through the pins MARKP and MARKN. These may be connected as shown in the application diagram below, with a capacitor across the two outputs and a comparator (or Op-amp) to determine the mark density.

AC Coupled Output

When DC coupled the output swing will be limited by IOUT output voltage specified to -2 V. For maximum output voltage swing the output should be AC coupled.

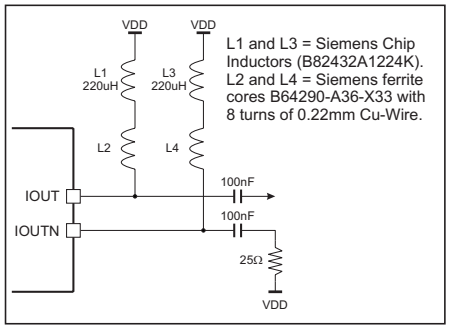


Figure 2. *AC Coupled Output*

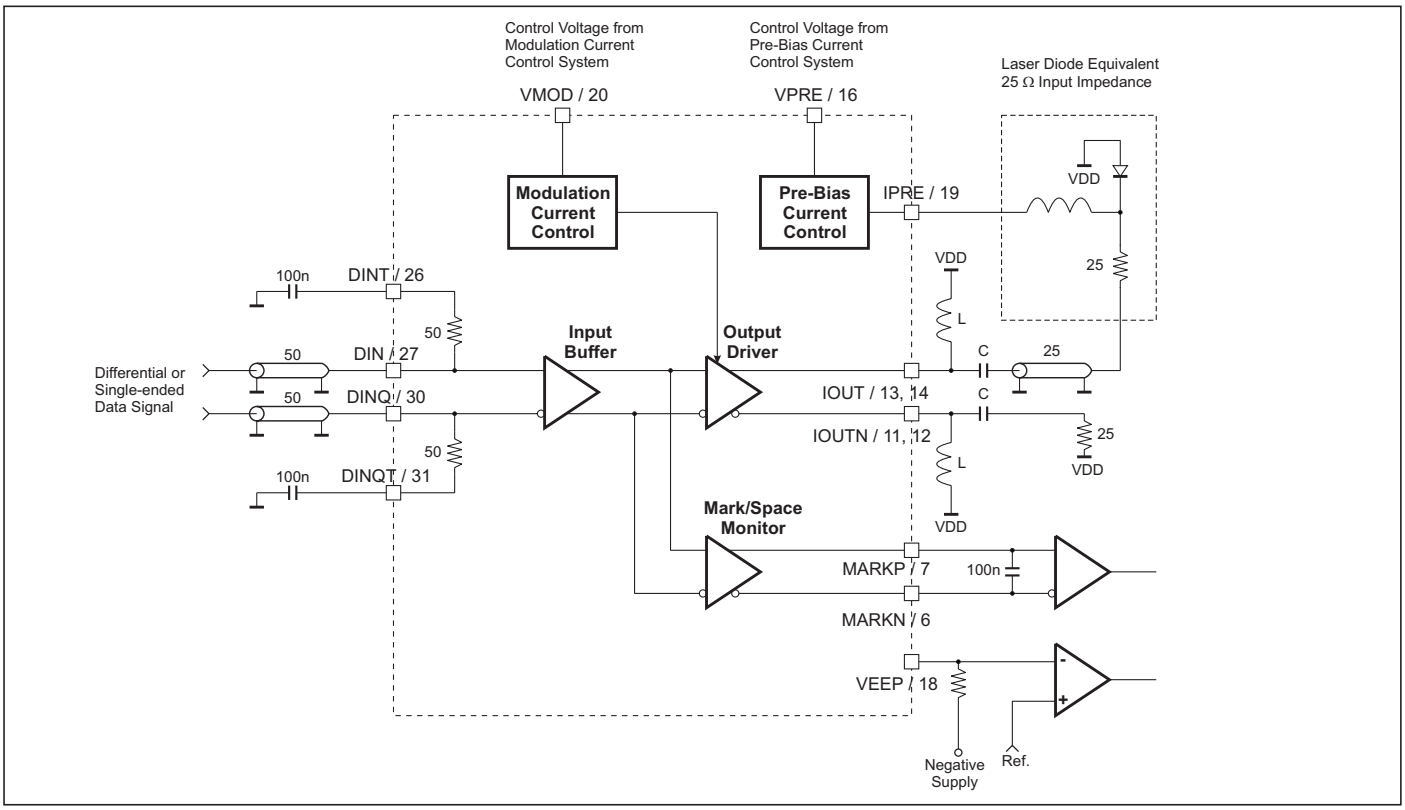


Figure 1. *Application Diagram*

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
DIN, DINQ	27, 30	AC IN	Data inputs. Internally terminated in 50 Ω to DINT and DINQT respectively.
DINT, DINQT	26, 31	ANL IN	Termination voltages for DIN and DINQ.
IOUT IOUTN	13, 14 11, 12	OPEN COLLECTOR	Laser Driver Output (2.5 Gbit/s). IOUT and IOUTN sink a modulation current, which is controlled by the pin VMOD. The current into IOUT is low when data is high on DIN.
IPRE	19	OPEN COLLECTOR	Pre-bias current output. IPRE sinks a current, which is controlled by the pin VPRE.
VMOD	20	ANL IN	Modulation current control input. The control system is made as a current mirror. VMOD sinks a current proportional to the modulation current. This current is approximately 3/80 times “The modulation current”.
VPRE	16	ANL IN	Pre-bias current control input. The control system is made as a current mirror. VPRE sinks a current proportional to the pre-bias current. This current is approximately 3/500 times “The pre-bias current”.
MARKP MARKN	7 6	ANL OUT	Mark-space monitor outputs. High impedance CML outputs. The output voltage of the MARKP pin is the same polarity as the voltage on the DIN input.
VADJBUF VADJEF	22 21	ANL IN	Pins used to optimise the performance of the output in terms of overshoot and undershoot. Typically optimum performance will be achieved when shorted to VMOD.
VDD	2, 4, 9, 10, 15, 24, 28, 29	PWR	Ground pins for laser driver part. (Package back).
VDDCONT	3	PWR	Ground pin for modulation current control system.
VEE	1, 5, 8, 23, 25, 32	PWR	Negative supply pins for laser driver part.
VEEP	18	PWR	Negative supply pin for output driver.
VEEB	17	PWR	Negative supply pin for pre-bias circuitry.
Heat sink	Package back		Connected to VDD

Package Pinout

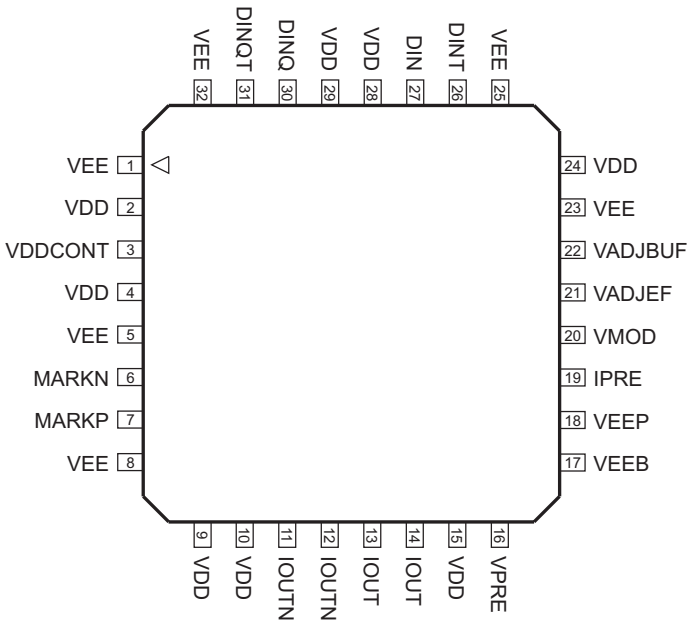


Figure 3. *Package 32 TQFP, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VDD.
All currents in table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Power Supply		-6		0	V
V_O	Applied Voltage (All Outputs)		V_{EE} -0.5		2	V
V_I	Applied Voltage (All Inputs)		V_{EE} -0.5		0.5	V
$I_{I\ AC\ IN}$	Input Current (AC IN)		-1		1	mA
$I_{I\ VMOD}$	Input Current (VMOD)		-4		1	mA
$I_{I\ VPRE}$	Input Current (VPRE, VADJBUF and VADJEF)	Note 1	-1		1	mA
T_O	Operating Temperature	Base	-55		+125	°C
T_S	Storage Temperature		-65		+150	°C

Note 1: Voltage and/or current should be externally limited to specified range.

DC Characteristics

T_{CASE} = -40 °C to 85 °C.
All voltages in table are referred to VDD.
All currents in table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Power Supply		–5.5	–5.2	-4.7	V
I_{EE}	Negative Supply Current	I_{OUT} = 0 A		75		mA
P_{DISS}	Power Dissipation	V_{EE} = –5.0 V, I_{OUT} = 0 A, I_{PRE} = 0 A		0.38	0.5	W
$V_{pp\ AN\ IN}$	Peak–peak Voltage when Input is Driven Single ended.	V_{VTH} = –1.3 V	150		800	mV
V_{VMOD}	Voltage Range for VMOD		V_{EE}		V_{DD}	V
I_{VMOD}	Sink Current into pin VMOD		–4		0	mA
$V_{IN\ NN}$	Input Voltage Range for VPRE, VADJBUF, and VADJEF		V_{EE}		V_{DD}	V
$I_{SINK\ NN}$	Sink Current into pin VPRE, VADJBUF, and VADJEF		–1		0	mA
$V_{LO\ MARK}$	Low Output Voltage for Mark-Space Monitor			–2.0		V
$R_{O\ MARK}$	Output Impedance for Mark-Space Monitor			4.0		kΩ
$V_{O\ IPRE}$	IPRE Output Voltage		–2.0			V
I_{IPRE}	IPRE Current		–50		0	mA
$V_{O\ IOUT}$	IOUT Output Voltage	Note 1	–2.0			V
$I_{Mod,HI\ IOUT}$	IOUT High Modulation Current	Note 1, 2	–70		0	mA
$I_{Mod,LO\ IOUT}$	IOUT Low Modulation Current	Note 1, 3	–3		1	mA

Note 1: R_{LOAD} = 25 Ω to *VDD* connected to pin IOUT. Sink current is controlled by the VMOD pin, and may be adjusted in the range as specified. Notice that high modulation current means that the output voltage level is low.
Note 2: The AC parameters are only specified in the range from -70 mA to -5 mA. However at T_{CASE} = 0 ° to 70 °C AC parameters are specified from -80 mA to -5 mA.
Note 3: This is a leakage current. Maximum leakage current is present at max modulation current (i.e. at 70 mA modulation current). The leakage current decreases for smaller modulation currents.

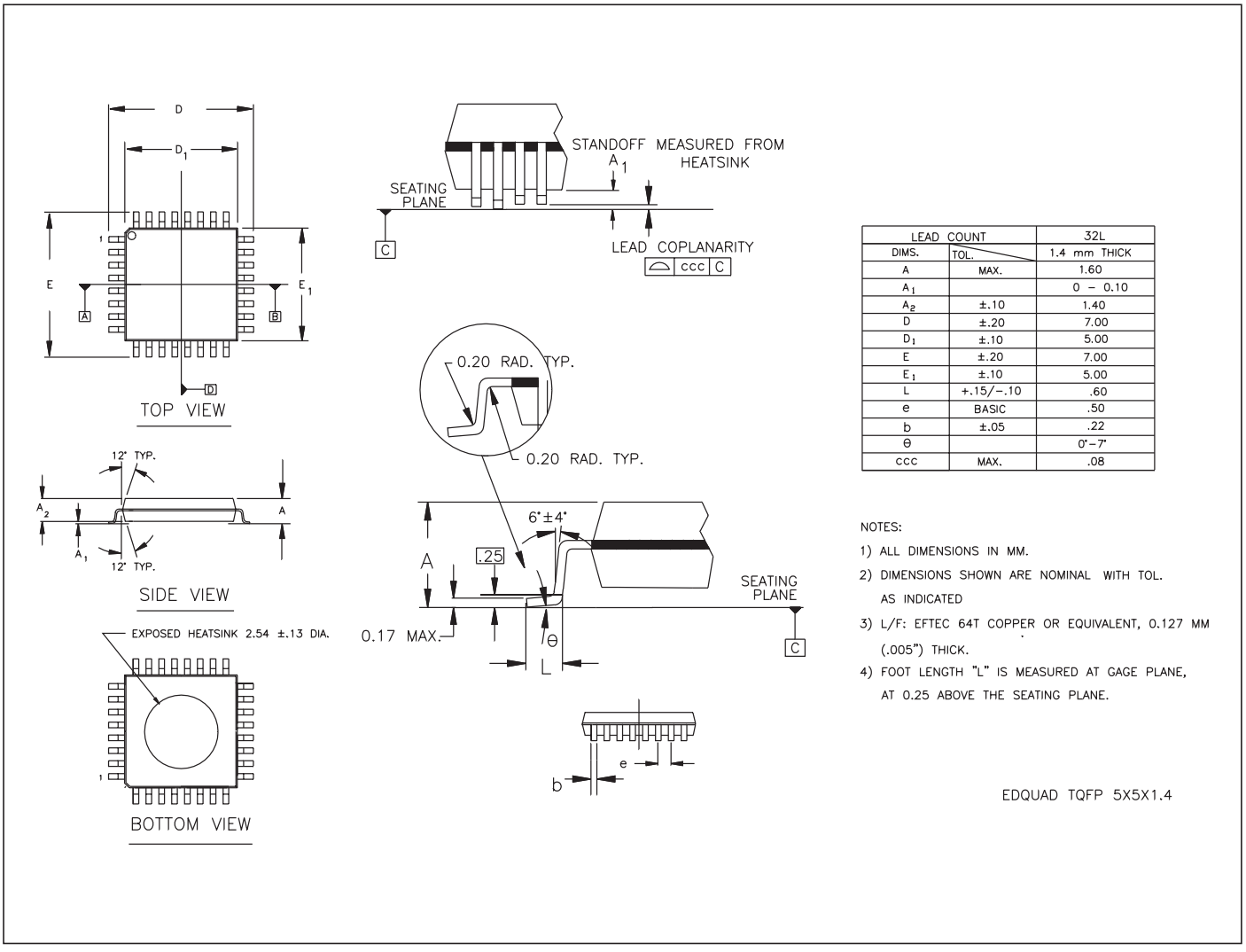
AC Characteristics

T_{CASE} = -40 °C to +85 °C.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$f_{MAX\ OUT}$	Data Output Frequency		2500			Mbit/s
$J_{pp\ OUT}$	Added Output Jitter	Note 1			20	ps
$t_{RISE\ OUT}$	Output Rise Time	Note 1			100	ps
$t_{FALL\ OUT}$	Output Fall Time	Note 1			100	ps

Note 1: R_{LOAD} = 25 Ω to *VDD* connected to pin IOUT. I_{LD} = 70 mA. Rise/Fall times at 20 – 80 % of HI/LO voltage levels.

Package Outline



LEAD COUNT		32L
DIMS.	TOL.	1.4 mm THICK
A	MAX.	1.60
A_1		0 – 0.10
A_2	±.10	1.40
D	±.20	7.00
D_1	±.10	5.00
E	±.20	7.00
E_1	±.10	5.00
L	+.15/−.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°–7°
ccc	MAX.	.08

NOTES:
1) ALL DIMENSIONS IN MM.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED
3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") THICK.
4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.

EDQUAD TQFP 5X5X1.4

Figure 4. *Package 32L TQFP (5 x 5 x 1.4 mm)*

Device Marking

Figure 5. *Device Marking, 32 pin Package - Top View*

Ordering Information

To order, please specify as shown below:

Product Name:	**Intel Order Number**:	**Package Type:**	**Case Temperature Range:**
GD16573A-32BA	**FAGD16573A32BA** MM#: 836126	32L TQFP EDQUAD	-40..85 °C

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