



Intel[®] Advanced Boot Block Flash Memory (B3)

28F008/800B3, 28F016/160B3, 28F320B3, 28F640B3

Datasheet

Product Features

- Flexible SmartVoltage Technology
 - 2.7 V – 3.6 V read/program/erase
 - 12 V V_{PP} fast production programming
- 1.65 V – .5 V or 2.7 V – 3.6 V I/O option
 - Reduces overall system power
- High Performance
 - 2.7 V – 3.6 V: 70 ns max access time
- Optimized Block Sizes
 - Eight 8-KB blocks for data, top or bottom locations
 - Up to 127 x 64-KB blocks for code
- Block Locking
 - V_{CC} -level control through Write Protect WP#
- Low Power Consumption
 - 9 mA typical read current
- Absolute Hardware-Protection
 - V_{PP} = GND option
 - V_{CC} lockout voltage
- Extended Temperature Operation
 - -40 °C to +85 °C
- Automated Program and Block Erase
 - Status registers
- Intel[®] Flash Data Integrator Software
 - Flash Memory Manager
 - System Interrupt Manager
 - Supports parameter storage, streaming data (for example, voice)
- Extended Cycling Capability
 - Minimum 100,000 block erase cycles
- Automatic Power Savings Feature
 - Typical I_{CCS} after bus inactivity
- Standard Surface Mount Packaging
 - 48-Ball CSP packages
 - 40-Lead and 48-Lead TSOP packages
- Density and Footprint Upgradeable for common package
 - 8-, 16-, 32-, and 64-Mbit densities
- ETOX[™] VIII (0.13 μ m) Flash Technology
 - 16-Mbit and 32-Mbit densities
- ETOX[™] VII (0.18 μ m) Flash Technology
 - 16-, 32-, and 64-Mbit densities
- ETOX[™] VI (0.25 μ m) Flash Technology
 - 8-, 16-, and 32-Mbit densities
- Do not use the x8 option for new designs

The Intel[®] Advanced Boot Block Flash Memory (B3) device, manufactured on the Intel 0.13 μ m and 0.18 μ m technologies, is a feature-rich solution at a low system cost. The B3 device in x16 is available in 48-lead TSOP and 48-ball CSP packages. The x8 option of this product family is available only in 40-lead TSOP and 48-ball μ BGA* packages. For additional information about this product family, see the Intel website: <http://www.intel.com/design/flash>.

Notice: This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 290580, Revision: 020
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Revision History

Revision Number	Description
-001	Original version
-002	<p>Section 3.4, <i>V_{PP} Program and Erase Voltages</i>, added</p> <p>Updated Figure 9: <i>Automated Block Erase Flowchart</i></p> <p>Updated Figure 10: <i>Erase Suspend/Resume Flowchart</i> (added program to table)</p> <p>Updated Figure 16: <i>AC Waveform: Program and Erase Operations</i> (updated notes)</p> <p><i>I_{PPR}</i> maximum specification change from $\pm 25 \mu\text{A}$ to $\pm 50 \mu\text{A}$</p> <p>Program and Erase Suspend Latency specification change</p> <p>Updated Appendix A: <i>Ordering Information</i> (included 8 M and 4 M information)</p> <p>Updated Figure, Appendix D: <i>Architecture Block Diagram</i> (Block info. in words not bytes)</p> <p>Minor wording changes</p>
-003	<p>Combined byte-wide specification (previously 290605) with this document</p> <p>Improved speed specification to 80 ns (3.0 V) and 90 ns (2.7 V)</p> <p>Improved 1.8 V I/O option to minimum 1.65 V (Section 3.4)</p> <p>Improved several DC characteristics (Section 4.4)</p> <p>Improved several AC characteristics (Sections 4.5 and 4.6)</p> <p>Combined 2.7 V and 1.8 V DC characteristics (Section 4.4)</p> <p>Added 5 V <i>V_{PP}</i> read specification (Section 3.4)</p> <p>Removed 120 ns and 150 ns speed offerings</p> <p>Moved <i>Ordering Information</i> from Appendix to Section 6.0; updated information</p> <p>Moved <i>Additional Information</i> from Appendix to Section 7.0</p> <p>Updated figure Appendix B, <i>Access Time vs. Capacitive Load</i></p> <p>Updated figure Appendix C, <i>Architecture Block Diagram</i></p> <p>Moved Program and Erase Flowcharts to Appendix E</p> <p>Updated <i>Program Flowchart</i></p> <p>Updated <i>Program Suspend/Resume Flowchart</i></p> <p>Minor text edits throughout</p>
-004	<p>Added 32-Mbit density</p> <p>Added 98H as a reserved command (Table 4)</p> <p>$A_1-A_{20} = 0$ when in read identifier mode (Section 3.2.2)</p> <p>Status register clarification for SR3 (Table 7)</p> <p><i>V_{CC}</i> and <i>V_{CCQ}</i> absolute maximum specification = 3.7 V (Section 4.1)</p> <p>Combined <i>I_{PPW}</i> and <i>I_{CCW}</i> into one specification (Section 4.4)</p> <p>Combined <i>I_{PPE}</i> and <i>I_{CCE}</i> into one specification (Section 4.4)</p> <p>Max Parameter Block Erase Time ($t_{\text{WHQV2}}/t_{\text{EHQV2}}$) reduced to 4 sec (Section 4.7)</p> <p>Max Main Block Erase Time ($t_{\text{WHQV3}}/t_{\text{EHQV3}}$) reduced to 5 sec (Section 4.7)</p> <p>Erase suspend time @ 12 V ($t_{\text{WHRH2}}/t_{\text{EHRH2}}$) changed to 5 μs typical and 20 μs maximum (Section 4.7)</p> <p><i>Ordering Information</i> updated (Section 6.0)</p> <p>Write State Machine Current/Next States Table updated (Appendix A)</p> <p>Program Suspend/Resume Flowchart updated (Appendix F)</p> <p>Erase Suspend/Resume Flowchart updated (Appendix F)</p> <p>Text clarifications throughout</p>
-005	<p>μBGA package diagrams corrected (Figures 3 and 4)</p> <p><i>I_{PPD}</i> test conditions corrected (Section 4.4)</p> <p>32-Mbit ordering information corrected (Section 6)</p> <p>μBGA package top side mark information added (Section 6)</p>
-006	<p><i>V_{IH}</i> and <i>V_{IL}</i> Specification change (Section 4.4)</p> <p><i>I_{CCS}</i> test conditions clarification (Section 4.4)</p> <p>Added Command Sequence Error Note (Table 7)</p> <p>Data sheet renamed from <i>Smart 3 Advanced Boot Block 4-Mbit, 8-Mbit, 16-Mbit Flash Memory Family</i>.</p> <p>Added device ID information for 4-Mbit x8 device</p> <p>Removed 32-Mbit x8 to reflect product offerings</p> <p>Minor text changes</p>

Revision Number	Description
-007	Corrected RP# pin description in Table 2, 3 Volt Advanced Boot Block Pin Descriptions Corrected typographical error fixed in <i>Ordering Information</i>
-008	4-Mbit packaging and addressing information corrected throughout document
-009	Corrected 4-Mbit memory addressing tables in Appendices D and E
-010	Max I _{CCD} changed to 25 μ A V _{CC} Max on 32 M (28F320B3) changed to 3.3 V
-011	Added 64-Mbit density and faster speed offerings Removed access time vs. capacitance load curve
-012	Changed references of 32Mbit 80ns devices to 70ns devices to reflect the faster product offering. Changed V _{CC} Max=3.3V reference to indicate the affected product is the 0.25 μ m 32Mbit device. Minor text edits throughout document.
-013	Added New Pin-1 indicator information on 40 and 48Lead TSOP packages. Minor text edits throughout document.
-014	Added specifications for 0.13 micron product offerings throughout document
-015	Minor text edits throughout document.
-016	Adjusted ordering information. Adjusted specifications for 0.13 micron product offerings. Revised and corrected DC Characteristics Table. Adjusted package diagram information. Minor text edits throughout document.
-017	Updated ordering information. Adjusted specifications for 0.13 micron product offerings. Updated AC/DC Characteristics Table. Added TSOP and μ BGA* package diagram information. Minor text edits throughout document.
-018	Updated the layout of the datasheet.
-019	Added line items to Table 34 "Ordering Information: Valid Combinations" on page 70.
-020	Removed all x8 products from ordering information, page 70

1.0 Introduction

This datasheet describes the specifications for the Intel[®] Advanced Boot Block Flash Memory (B3) device (hereafter referred to as the B3 flash memory device).

The B3 flash memory device is optimized for portable, low-power, systems. This family of products features 1.65 V to 2.5 V or 2.7 V to 3.6 V I/Os, and a low V_{CC}/V_{PP} operating range of 2.7 V to 3.6 V for Read, Program, and Erase operations. The B3 device is also capable of fast programming at 12 V.

Throughout this document:

- 2.7 V refers to the full voltage range 2.7 V to 3.6 V (except where noted otherwise).
- $V_{PP} = 12\text{ V}$ refers to $12\text{ V} \pm 5\%$.

1.1 Nomenclature

Table 1. Nomenclature

Term	Definition
0x	Hexadecimal prefix
0b	Binary prefix
Byte	8 bits
Word	16 bits
KW or Kword	1024 words
Mword	1,048,576 words
Kb	1024 bits
KB	1024 bytes
Mb	1,048,576 bits
MB	1,048,576 bytes
APS	Automatic Power Savings
CSP	Chip Scale Package
CUI	Command User Interface
OTP	One Time Programmable
PR	Protection Register
PRD	Protection Register Data
PLR	Protection Lock Register
RFU	Reserved for Future Use
SR	Status Register
SRD	Status Register Data
WSM	Write State Machine

1.2 Conventions

Table 2. Conventions

Convention	Description
Pin or signal	Used interchangeably to refer to the external signal connections on the package. Note: For a chip scale package (CSP), the term <i>ball</i> is used in place of <i>pin</i> .
Group Membership Brackets	Square brackets designate group membership or define a group of signals with similar function (for example, A[21:1], SR[4:1])
Set	When referring to registers, the term <i>set</i> means the bit is a logical 1.
Clear:	When referring to registers, the term <i>clear</i> means the bit is a logical 0.
Block	A group of bits (or words) that erase simultaneously using one block erase instruction.
Main Block	A block that contains 32 Kwords.
Parameter Block	A block that contains 4 Kwords.

2.0 Functional Overview

The B3 flash memory device features the following:

- Enhanced blocking for easy segmentation of code and data or additional design flexibility.
- Program Suspend to Read command.
- V_{CCQ} input of 1.65 V to 2.5 V or 2.7 V to 3.6 V on all I/Os. See [Figure 1](#) through [Figure 4](#) for pinout diagrams and V_{CCQ} location.
- Maximum program and erase time specification for improved data storage.

Table 3. B3 Device Feature Summary (Sheet 1 of 2)

Feature	28F008B3, 28F016B3	28F800B3, 28F160B3, 28F320B3 ⁽³⁾ , 28F640B3	Reference
V_{CC} Read Voltage	2.7 V– 3.6 V		Section 6.2 , Section 7.2
V_{CCQ} I/O Voltage	1.65 V–2.5 V or 2.7 V– 3.6 V		Section 4.2 , 4.4
V_{PP} Program/Erase Voltage	2.7 V– 3.6 V or 11.4 V– 12.6 V		Section 4.2 , 4.4
Bus Width	8 bit	16 bit	Table 27
Speed	70 ns, 80 ns, 90 ns, 100 ns, 110 ns		Section 8.1
Memory Arrangement	1024 Kbit x 8 (8 Mbit), 2048 Kbit x 8 (16 Mbit)	512 Kbit x 16 (8 Mbit), 1024 Kbit x 16 (16 Mbit), 2048 Kbit x 16 (32 Mbit), 4096 Kbit x 16 (64 Mbit)	Section 3.2

Table 3. B3 Device Feature Summary (Sheet 2 of 2)

Feature	28F008B3, 28F016B3	28F800B3, 28F160B3, 28F320B3 ⁽³⁾ , 28F640B3	Reference
Blocking (top or bottom)	Eight 8-Kbyte parameter blocks and Fifteen 64-Kbyte blocks (8 Mbit) or Thirty-one 64-Kbyte main blocks (16 Mbit) Sixty-three 64-Kbyte main blocks (32 Mbit) One hundred twenty-seven 64-Kbyte main blocks (64 Mbit)		Section 3.2, "Memory Maps and Block Organization" on page 11
Locking	WP# locks/unlocks parameter blocks All other blocks protected using V _{PP}		Section 12.0 Table 32
Operating Temperature	Extended: -40 °C to +85 °C		Section 6.2, Section 7.2
Program/Erase Cycling	100,000 cycles		Section 6.2, Section 7.2
Packages	40-lead TSOP ⁽¹⁾ , 48-Ball μBGA* CSP ⁽²⁾	48-Lead TSOP, 48-Ball μBGA CSP ⁽²⁾ , 48-Ball VF BGA	Figure 8, Figure 9

Notes:

- 32-Mbit and 64-Mbit densities not available in 40-lead TSOP.
- 8-Mbit densities not available in μBGA* CSP.
- V_{CC}Max is 3.3 V on 0.25μm 32-Mbit devices.

3.0 Functional Overview

Intel provides the most flexible voltage solution in the flash industry, providing three discrete voltage supply pins:

- V_{CC} for Read operation
- V_{CCQ} for output swing
- V_{PP} for Program and Erase operation.

All B3 flash memory devices provide program/erase capability at 2.7 V or 12 V (for fast production programming), and read with V_{CC} at 2.7 V. Because many designs read from the flash memory a large percentage of the time, 2.7 V V_{CC} operation can provide substantial power savings.

The B3 flash memory device family is available in either x8 or x16 packages in the following densities (see [Appendix C, "Ordering Information,"](#) for availability):

- 8-Mbit (8, 388, 608-bit) flash memory organized as 512 Kwords of 16 bits each or 1024 Kbytes of 8-bits each.
- 16-Mbit (16, 777, 216-bit) flash memory organized as 1024 Kwords of 16 bits each or 2048 Kbytes of 8-bits each.
- 32-Mbit (33, 554, 432-bit) flash memory organized as 2048 Kwords of 16 bits each.
- 64-Mbit (67, 108, 864-bit) flash memory organized as 4096 Kwords of 16 bits each.

The parameter blocks are located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map, to accommodate different microprocessor protocols for kernel code location. The upper two (or lower two) parameter blocks can be locked to provide complete code security for system initialization code. Locking and unlocking is controlled by Write Protect WP# (see [Section 12.0, "Block Locking" on page 62](#) for details).

- The Command User Interface (CUI) is the interface between the microprocessor or microcontroller and the internal operation of the flash memory.
- The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for Program and Erase operations (including verification), which unburdens the microprocessor or microcontroller.
- To indicate the status of the WSM, the Status Register signifies block erase or word program completion and status.

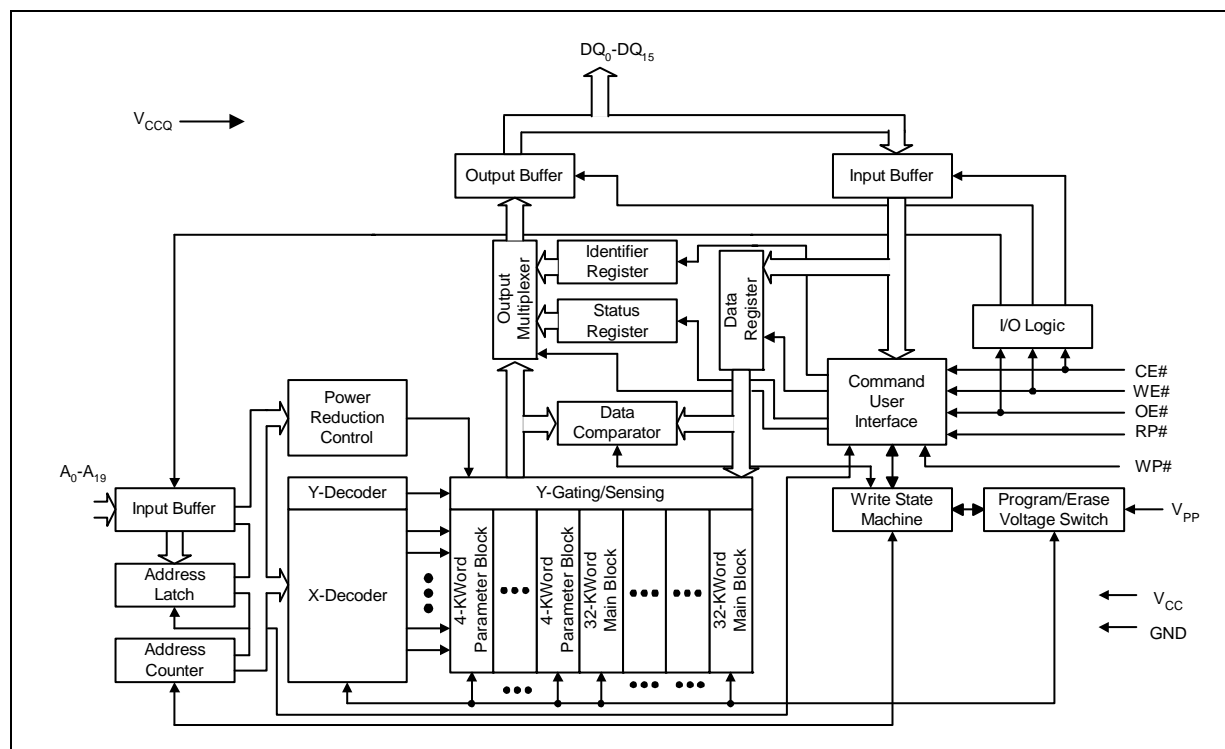
The B3 flash memory device also provides Automatic Power Savings (APS), which minimizes system current drain and allows for very low power designs. This mode is entered following the completion of a read cycle (approximately 300 ns later).

The RP# pin provides additional protection against unwanted command writes that might occur during system reset and power-up/down sequences due to invalid system bus conditions (see “Power and Reset Specifications” on page 47).

- [Section 10.0, “Operations Overview” on page 50](#) explains the different modes of operation.
- [Section 7.0, “Electrical Specifications” on page 34](#) and [Section 8.0, “AC Characteristics” on page 37](#) provide complete current and voltage specifications.
- [Section 8.1, “AC Read Characteristics” on page 37](#) provides read, program, and erase performance specifications.

3.1 Architecture Diagram

Figure 1. B3 Architecture Block Diagram



3.2 Memory Maps and Block Organization

The B3 flash memory device uses an asymmetrically blocked architecture, enabling system integration of code and data within a single flash memory device. Each block can be erased independently of other blocks up to 100,000 times. For the address locations of each block, see the following memory maps:

- Table 4 “16-Mbit and 32-Mbit Word-Wide Memory Addressing Map” on page 11
- Table 5 “4-Mbit and 8-Mbit Word-Wide Memory Addressing Map” on page 14
- Table 6 “16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing Map” on page 15
- Table 7 “8-Mbit and 16-Mbit Byte-Wide Memory Addressing Map” on page 20
- Table 8 “4-Mbit Byte Wide Memory Addressing Map” on page 23

3.2.1 Parameter Blocks

The B3 flash memory device architecture includes parameter blocks to facilitate storing frequently updated small parameters (such as data traditionally stored in an EEPROM). The word-rewrite functionality of EEPROMs can be emulated using software techniques. Each flash memory device contains eight parameter blocks of 8 Kbytes/4 Kwords (8192 bytes/4,096 words) each.

3.2.2 Main Blocks

After the parameter blocks, the remainder of the flash memory array is divided into equal-size main blocks (65,536 bytes/32,768 words) for data or code storage.

- The 8-Mbit flash memory device contains 15 main blocks.
- The 16-Mbit flash memory device contains 31 main blocks.
- The 32-Mbit memory device contains 63 main blocks.
- The 64-Mbit memory device contains 127 main blocks.

3.2.3 4-Mbit, 8-Mbit, 16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Maps

Table 4. 16-Mbit and 32-Mbit Word-Wide Memory Addressing Map (Sheet 1 of 4)

16-Mbit and 32-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)		16 Mbit	32 Mbit	Size (KW)	8 Mbit	16 Mbit	32 Mbit
4		FF000-FFFFF	1FF000-1FFFFFF	32			1F8000-1FFFFFF
4		FE000-FEFFF	1FE000-1FEFFF	32			1F0000-1F7FFF
4		FD000-FDFFF	1FD000-1FDFFF	32			1E8000-1EFFFF
4		FC000-FCFFF	1FC000-1FCFFF	32			1E0000-1E7FFF

Table 4. 16-Mbit and 32-Mbit Word-Wide Memory Addressing Map (Sheet 2 of 4)

16-Mbit and 32-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)		16 Mbit	32 Mbit	Size (KW)	8 Mbit	16 Mbit	32 Mbit
4		FB000-FBFFF	1FB000-1FBFFF	32			1D8000-1DFFFF
4		FA000-FAFFF	1FA000-1FAFFF	32			1D0000-1D7FFF
4		F9000-F9FFF	1F9000-1F9FFF	32			1C8000-1CFFFF
4		F8000-F8FFF	1F8000-1F8FFF	32			1C0000-1C7FFF
32		F0000-F7FFF	1F0000-1F7FFF	32			1B8000-1BFFFF
32		E8000-EFFFF	1E8000-1EFFFF	32			1B0000-1B7FFF
32		E0000-E7FFF	1E0000-1E7FFF	32			1A8000-1AFFFF
32		D8000-DFFFF	1D8000-1DFFFF	32			1A0000-1A7FFF
32		D0000-D7FFF	1D0000-1D7FFF	32			198000-19FFFF
32		C8000-CFFFF	1C8000-1CFFFF	32			190000-197FFF
32		C0000-C7FFF	1C0000-1C7FFF	32			188000-18FFFF
32		B8000-BFFFF	1B8000-1BFFFF	32			180000-187FFF
32		B0000-B7FFF	1B0000-1B7FFF	32			178000-17FFFF
32		A8000-AFFFF	1A8000-1AFFFF	32			170000-177FFF
32		A0000-A7FFF	1A0000-1A7FFF	32			168000-16FFFF
32		98000-9FFFF	198000-19FFFF	32			160000-167FFF
32		90000-97FFF	190000-197FFF	32			158000-15FFFF
32		88000-8FFFF	188000-18FFFF	32			150000-157FFF
32		80000-87FFF	180000-187FFF	32			148000-14FFFF
32		78000-7FFFF	178000-17FFFF	32			140000-147FFF
32		70000-77FFF	170000-177FFF	32			138000-13FFFF
32		68000-6FFFF	168000-16FFFF	32			130000-137FFF
32		60000-67FFF	160000-167FFF	32			128000-12FFFF
32		58000-5FFFF	158000-15FFFF	32			120000-127FFF
32		50000-57FFF	150000-157FFF	32			118000-11FFFF
32		48000-4FFFF	148000-14FFFF	32			110000-117FFF
32		40000-47FFF	140000-147FFF	32			108000-10FFFF
32		38000-3FFFF	138000-13FFFF	32			100000-107FFF
32		30000-37FFF	130000-137FFF	32		F8000-FFFFF	0F8000-0FFFFF
32		28000-2FFFF	128000-12FFFF	32		F0000-F7FFF	0F0000-0F7FFF



Table 4. 16-Mbit and 32-Mbit Word-Wide Memory Addressing Map (Sheet 3 of 4)

16-Mbit and 32-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)		16 Mbit	32 Mbit	Size (KW)	8 Mbit	16 Mbit	32 Mbit
32		20000-27FFF	120000-127FFF	32		E8000-EFFFF	0E8000-0EFFFF
32		18000-1FFFF	118000-11FFFF	32		E0000-E7FFF	0E0000-0E7FFF
32		10000-17FFF	110000-117FFF	32		D8000-DFFFF	0D8000-0DFFFF
32		08000-0FFFF	108000-10FFFF	32		D0000-D7FFF	0D0000-0D7FFF
32		00000-07FFF	100000-107FFF	32		C8000-CFFFF	0C8000-0CFFFF
This column continues on next page				This column continues on next page			
32			0F8000-0FFFFF	32		C0000-C7FFF	0C0000-0C7FFF
32			0F0000-0F7FFF	32		B8000-BFFFF	0B8000-0BFFFF
32			0E8000-0EFFFF	32		B0000-B7FFF	0B0000-0B7FFF
32			0E0000-0E7FFF	32		A8000-AFFFF	0A8000-0AFFFF
32			0D8000-0DFFFF	32		A0000-A7FFF	0A0000-0A7FFF
32			0D0000-0D7FFF	32		98000-9FFFF	098000-09FFFF
32			0C8000-0CFFFF	32		90000-97FFF	090000-097FFF
32			0C0000-0C7FFF	32		88000-8FFFF	088000-08FFFF
32			0B8000-0BFFFF	32		80000-87FFF	080000-087FFF
32			0B0000-0B7FFF	32		78000-7FFFF	78000-7FFFF
32			0A8000-0AFFFF	32		70000-77FFF	70000-77FFF
32			0A0000-0A7FFF	32		68000-6FFFF	68000-6FFFF
32			098000-09FFFF	32		60000-67FFF	60000-67FFF
32			090000-097FFF	32		58000-5FFFF	58000-5FFFF
32			088000-08FFFF	32		50000-57FFF	50000-57FFF
32			080000-087FFF	32		48000-4FFFF	48000-4FFFF
32			078000-07FFFF	32		40000-47FFF	40000-47FFF
32			070000-077FFF	32		38000-3FFFF	38000-3FFFF
32			068000-06FFFF	32		30000-37FFF	30000-37FFF
32			060000-067FFF	32		28000-2FFFF	28000-2FFFF
32			058000-05FFFF	32		20000-27FFF	20000-27FFF
32			050000-057FFF	32		18000-1FFFF	18000-1FFFF
32			048000-04FFFF	32		10000-17FFF	10000-17FFF
32			040000-047FFF	32		08000-0FFFF	08000-0FFFF

4. 16-Mbit and 32-Mbit Word-Wide Memory Addressing Map (Sheet 4 of 4)

16-Mbit and 32-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	16 Mbit	32 Mbit	Size (KW)	8 Mbit	16 Mbit	32 Mbit	
		038000-03FFFF	4		07000-07FFF	07000-07FFF	
		030000-037FFF	4		06000-06FFF	06000-06FFF	
		028000-02FFFF	4		05000-05FFF	05000-05FFF	
		020000-027FFF	4		04000-04FFF	04000-04FFF	
		018000-01FFFF	4		03000-03FFF	03000-03FFF	
		010000-017FFF	4		02000-02FFF	02000-02FFF	
		008000-00FFFF	4		01000-01FFF	01000-01FFF	
		000000-007FFF	4		00000-00FFF	00000-00FFF	

Table 5. 4-Mbit and 8-Mbit Word-Wide Memory Addressing Map (Sheet 1 of 2)

4-Mbit and 8-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	4 Mbit			Size (KW)	4 Mbit	8 Mbit	
	3F000-3FFFF	7F000-7FFFF		32		78000-7FFFF	
	3E000-3EFFF	7E000-7EFFF		32		70000-77FFF	
	3D000-3DFFF	7D000-7DFFF		32		68000-6FFFF	
	3C000-3CFFF	7C000-7CFFF		32		60000-67FFF	
	3B000-3BFFF	7B000-7BFFF		32		58000-5FFFF	
	3A000-3AFFF	7A000-7AFFF		32		50000-57FFF	
	39000-39FFF	79000-79FFF		32		48000-4FFFF	
	38000-38FFF	78000-78FFF		32		40000-47FFF	
4	30000-37FFF	70000-77FFF		32	38000-3FFFF	38000-3FFFF	
4	28000-2FFFF	68000-6FFFF		32	30000-37FFF	30000-37FFF	
4	20000-27FFF	60000-67FFF		32	28000-2FFFF	28000-2FFFF	
4	18000-1FFFF	58000-5FFFF		32	20000-27FFF	20000-27FFF	
4	10000-17FFF	50000-57FFF		32	18000-1FFFF	18000-1FFFF	
4	08000-0FFFF	48000-4FFFF		32	10000-17FFF	10000-17FFF	
4	00000-07FFF	40000-47FFF		32	08000-0FFFF	08000-0FFFF	
4		38000-3FFFF		4	07000-07FFF	07000-07FFF	
32		30000-37FFF		4	06000-06FFF	06000-06FFF	
32		28000-2FFFF		4	05000-05FFF	05000-05FFF	
32		20000-27FFF		4	04000-04FFF	04000-04FFF	
32		18000-1FFFF		4	03000-03FFF	03000-03FFF	



Table 5. 4-Mbit and 8-Mbit Word-Wide Memory Addressing Map (Sheet 2 of 2)

4-Mbit and 8-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	4 Mbit			Size (KW)	4 Mbit	8 Mbit	
32		10000-17FFF		4	02000-02FFF	02000-02FFF	
32		08000-0FFFF		4	01000-01FFF	01000-01FFF	
32		00000-07FFF		4	00000-00FFF	00000-00FFF	

Table 6. 16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 1 of 6)

16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	16 Mbit	32 Mbit	64 Mbit	Size (KW)	16 Mbit	32 Mbit	64 Mbit
4	FF000-FFFFF	1FF000-1FFFFF	3FF000-3FFFFFF	32			3F8000-3FFFFFF
4	FE000-FEFFF	1FE000-1FEFFF	3FE000-3FEFFF	32			3F0000-3F7FFF
4	FD000-FDFFF	1FD000-1FDFFF	3FD000-3FDFFF	32			3E8000-3EFFFF
4	FC000-FCFFF	1FC000-1FCFFF	3FC000-3FCFFF	32			3E0000-3E7FFF
4	FB000-FBFFF	1FB000-1FBFFF	3FB000-3FBFFF	32			3D8000-3DFFFF
4	FA000-FAFFF	1FA000-1FAFFF	3FA000-3FAFFF	32			3D0000-3D7FFF
4	F9000-F9FFF	1F9000-1F9FFF	3F9000-3F9FFF	32			3C8000-3CFFFF
4	F8000-F8FFF	1F8000-1F8FFF	3F8000-3F8FFF	32			3C0000-3C7FFF
32	F0000-F7FFF	1F0000-1F7FFF	3F0000-3F7FFF	32			3B8000-3BFFFF
32	E8000-EFFFF	1E8000-1EFFFF	3E8000-3EFFFF	32			3B0000-3B7FFF
32	E0000-E7FFF	1E0000-1E7FFF	3E0000-3E7FFF	32			3A8000-3AFFFF
32	D8000-DFFFF	1D8000-1DFFFF	3D8000-3DFFFF	32			3A0000-3A7FFF
32	D0000-D7FFF	1D0000-1D7FFF	3D0000-3D7FFF	32			398000-39FFFF
32	C8000-CFFFF	1C8000-1CFFFF	3C8000-3CFFFF	32			390000-397FFF
32	C0000-C7FFF	1C0000-1C7FFF	3C0000-3C7FFF	32			388000-38FFFF
32	B8000-BFFFF	1B8000-1BFFFF	3B8000-3BFFFF	32			380000-387FFF

Table 6. 16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 2 of 6)

16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	16 Mbit	32 Mbit	64 Mbit	Size (KW)	16 Mbit	32 Mbit	64 Mbit
32	B0000-B7FFF	1B0000-1B7FFF	3B0000-3B7FFF	32			378000-37FFFF
32	A8000-AFFFF	1A8000-1AFFFF	3A8000-3AFFFF	32			370000-377FFF
32	A0000-A7FFF	1A0000-1A7FFF	3A0000-3A7FFF	32			368000-36FFFF
32	98000-9FFFF	198000-19FFFF	398000-39FFFF	32			360000-367FFF
32	90000-97FFF	190000-197FFF	390000-397FFF	32			358000-35FFFF
32	88000-8FFFF	188000-18FFFF	388000-38FFFF	32			350000-357FFF
32	80000-87FFF	180000-187FFF	380000-387FFF	32			348000-34FFFF
32	78000-7FFFF	178000-17FFFF	378000-37FFFF	32			340000-347FFF
32	70000-77FFF	170000-177FFF	370000-377FFF	32			338000-33FFFF
32	68000-6FFFF	168000-16FFFF	368000-36FFFF	32			330000-337FFF
32	60000-67FFF	160000-167FFF	360000-367FFF	32			328000-32FFFF
32	58000-5FFFF	158000-15FFFF	358000-35FFFF	32			320000-327FFF
32	50000-57FFF	150000-157FFF	350000-357FFF	32			318000-31FFFF
32	48000-4FFFF	148000-14FFFF	348000-34FFFF	32			310000-317FFF
32	40000-47FFF	140000-147FFF	340000-347FFF	32			308000-30FFFF
32	38000-3FFFF	138000-13FFFF	338000-33FFFF	32			300000-307FFF
32	30000-37FFF	130000-137FFF	330000-337FFF	32			2F8000-2FFFFF
32	28000-2FFFF	128000-12FFFF	328000-32FFFF	32			2F0000-2F7FFF
32	20000-27FFF	120000-127FFF	320000-327FFF	32			2E8000-2EFFFF
32	18000-1FFFF	118000-11FFFF	318000-31FFFF	32			2E0000-2E7FFF
32	10000-17FFF	110000-117FFF	310000-317FFF	32			2D8000-2DFFFF



Table 6. 16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 3 of 6)

16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	16 Mbit	32 Mbit	64 Mbit	Size (KW)	16 Mbit	32 Mbit	64 Mbit
32	08000-0FFFF	108000-10FFFF	308000-30FFFF	32			2D0000-2D7FFF
32	00000-07FFF	100000-107FFF	300000-307FFF	32			2C8000-2CFFFF
32		0F8000-0FFFFF	2F8000-2FFFFF	32			2C0000-2C7FFF
32		0F0000-0F7FFF	2F0000-2F7FFF	32			2B8000-2BFFFF
32		0E8000-0EFFFF	2E8000-2EFFFF	32			2B0000-2B7FFF
32		0E0000-0E7FFF	2E0000-2E7FFF	32			2A8000-2AFFFF
32		0D8000-0DFFFF	2D8000-2DFFFF	32			2A0000-2A7FFF
32		0D0000-0D7FFF	2D0000-2D7FFF	32			298000-29FFFF
32		0C8000-0CFFFF	2C8000-2CFFFF	32			290000-297FFF
32		0C0000-0C7FFF	2C0000-2C7FFF	32			288000-28FFFF
32		0B8000-0BFFFF	2B8000-2BFFFF	32			280000-287FFF
32		0B0000-0B7FFF	2B0000-2B7FFF	32			278000-27FFFF
32		0A8000-0AFFFF	2A8000-2AFFFF	32			270000-277FFF
32		0A0000-0A7FFF	2A0000-2A7FFF	32			268000-26FFFF
32		098000-09FFFF	298000-29FFFF	32			260000-267FFF
32		090000-097FFF	290000-297FFF	32			258000-25FFFF
32		088000-08FFFF	288000-28FFFF	32			250000-257FFF
32		080000-087FFF	280000-287FFF	32			248000-24FFFF
32		078000-07FFFF	278000-27FFFF	32			240000-247FFF
32		070000-077FFF	270000-277FFF	32			238000-23FFFF
32		068000-06FFFF	268000-26FFFF	32			230000-237FFF

Table 6. 16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 4 of 6)

16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	16 Mbit	32 Mbit	64 Mbit	Size (KW)	16 Mbit	32 Mbit	64 Mbit
32		060000-067FFF	260000-267FFF	32			228000-22FFFF
32		058000-05FFFF	258000-25FFFF	32			220000-227FFF
32		050000-057FFF	250000-257FFF	32			218000-21FFFF
32		048000-04FFFF	248000-24FFFF	32			210000-217FFF
32		040000-047FFF	240000-247FFF	32			208000-20FFFF
32		038000-03FFFF	238000-23FFFF	32			200000-207FFF
32		030000-037FFF	230000-237FFF	32		1F8000-1FFFFF	1F8000-1FFFFF
32		028000-02FFFF	228000-22FFFF	32		1F0000-1F7FFF	1F0000-1F7FFF
32		020000-027FFF	220000-227FFF	32		1E8000-1EFFFF	1E8000-1EFFFF
32		018000-01FFFF	218000-21FFFF	32		1E0000-1E7FFF	1E0000-1E7FFF
32		010000-017FFF	210000-217FFF	32		1D8000-1DFFFF	1D8000-1DFFFF
32		008000-00FFFF	208000-21FFFF	32		1D0000-1D7FFF	1D0000-1D7FFF
32		000000-007FFF	200000-207FFF	32		1C8000-1CFFFF	1C8000-1CFFFF
32			1F8000-1FFFFF	32		1C0000-1C7FFF	1C0000-1C7FFF
32			1F0000-1F7FFF	32		1B8000-1BFFFF	1B8000-1BFFFF
32			1E8000-1EFFFF	32		1B0000-1B7FFF	1B0000-1B7FFF
32			1E0000-1E7FFF	32		1A8000-1AFFFF	1A8000-1AFFFF
32			1D8000-1DFFFF	32		1A0000-1A7FFF	1A0000-1A7FFF
32			1D0000-1D7FFF	32		198000-19FFFF	198000-19FFFF
32			1C8000-1CFFFF	32		190000-197FFF	190000-197FFF
32			1C0000-1C7FFF	32		188000-18FFFF	188000-18FFFF
32			1B8000-1BFFFF	32		180000-187FFF	180000-187FFF
32			1B0000-1B7FFF	32		178000-17FFFF	178000-17FFFF
32			1A8000-1AFFFF	32		170000-177FFF	170000-177FFF



Table 6. 16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 5 of 6)

16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	16 Mbit	32 Mbit	64 Mbit	Size (KW)	16 Mbit	32 Mbit	64 Mbit
32			1A0000-1A7FFF	32		168000-16FFFF	168000-16FFFF
32			198000-19FFFF	32		160000-167FFF	160000-167FFF
32			190000-197FFF	32		158000-15FFFF	158000-15FFFF
32			188000-18FFFF	32		150000-157FFF	150000-157FFF
32			180000-187FFF	32		148000-14FFFF	148000-14FFFF
32			178000-17FFFF	32		140000-147FFF	140000-147FFF
32			170000-177FFF	32		138000-13FFFF	138000-13FFFF
32			168000-16FFFF	32		130000-137FFF	130000-137FFF
32			160000-167FFF	32		128000-12FFFF	128000-12FFFF
32			158000-15FFFF	32		120000-127FFF	120000-127FFF
32			150000-157FFF	32		118000-11FFFF	118000-11FFFF
32			148000-14FFFF	32		110000-117FFF	110000-117FFF
32			140000-147FFF	32		108000-10FFFF	108000-10FFFF
32			138000-13FFFF	32		100000-107FFF	100000-107FFF
32			130000-137FFF	32	F8000-FFFFF	F8000-FFFFF	F8000-FFFFF
32			128000-12FFFF	32	F0000-F7FFF	F0000-F7FFF	F0000-F7FFF
32			120000-127FFF	32	E8000-EFFFF	E8000-EFFFF	E8000-EFFFF
32			118000-11FFFF	32	E0000-E7FFF	E0000-E7FFF	E0000-E7FFF
32			110000-117FFF	32	D8000-DFFFF	D8000-DFFFF	D8000-DFFFF
32			108000-10FFFF	32	D0000-D7FFF	D0000-D7FFF	D0000-D7FFF
32			100000-107FFF	32	C8000-CFFFF	C8000-CFFFF	C8000-CFFFF
32			0F8000-0FFFFF	32	C0000-C7FFF	C0000-C7FFF	C0000-C7FFF
32			0F0000-0F7FFF	32	B8000-BFFFF	B8000-BFFFF	B8000-BFFFF
32			0E8000-0EFFFF	32	B0000-B7FFF	B0000-B7FFF	B0000-B7FFF
32			0E0000-0E7FFF	32	A8000-AFFFF	A8000-AFFFF	A8000-AFFFF
32			0D8000-0DFFFF	32	A0000-A7FFF	A0000-A7FFF	A0000-A7FFF
32			0D0000-0D7FFF	32	98000-9FFFF	98000-9FFFF	98000-9FFFF
32			0C8000-0CFFFF	32	90000-97FFF	90000-97FFF	90000-97FFF
32			0C0000-0C7FFF	32	88000-8FFFF	88000-8FFFF	88000-8FFFF
32			0B8000-0BFFFF	32	80000-87FFF	80000-87FFF	80000-87FFF
32			0B0000-0B7FFF	32	78000-7FFFF	78000-7FFFF	78000-7FFFF
32			0A8000-0AFFFF	32	70000-77FFF	70000-77FFF	70000-77FFF
32			0A0000-0A7FFF	32	68000-6FFFF	68000-6FFFF	68000-6FFFF
32			098000-09FFFF	32	60000-67FFF	60000-67FFF	60000-67FFF
32			090000-097FFF	32	58000-5FFFF	58000-5FFFF	58000-5FFFF

Table 6. 16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 6 of 6)
16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	16 Mbit	32 Mbit	64 Mbit	Size (KW)	16 Mbit	32 Mbit	64 Mbit
32			088000-08FFFF	32	50000-57FFF	50000-57FFF	50000-57FFF
32			080000-087FFF	32	48000-4FFFF	48000-4FFFF	48000-4FFFF
32			078000-07FFFF	32	40000-47FFF	40000-47FFF	40000-47FFF
32			070000-077FFF	32	38000-3FFFF	38000-3FFFF	38000-3FFFF
32			068000-06FFFF	32	30000-37FFF	30000-37FFF	30000-37FFF
32			060000-067FFF	32	28000-2FFFF	28000-2FFFF	28000-2FFFF
32			058000-05FFFF	32	20000-27FFF	20000-27FFF	20000-27FFF
32			050000-057FFF	32	18000-1FFFF	18000-1FFFF	18000-1FFFF
32			048000-04FFFF	32	10000-17FFF	10000-17FFF	10000-17FFF
32			040000-047FFF	32	08000-0FFFF	08000-0FFFF	08000-0FFFF
32			038000-03FFFF	4	07000-07FFF	07000-07FFF	07000-07FFF
32			030000-037FFF	4	06000-06FFF	06000-06FFF	06000-06FFF
32			028000-02FFFF	4	05000-05FFF	05000-05FFF	05000-05FFF
32			020000-027FFF	4	04000-04FFF	04000-04FFF	04000-04FFF
32			018000-01FFFF	4	03000-03FFF	03000-03FFF	03000-03FFF
32			010000-017FFF	4	02000-02FFF	02000-02FFF	02000-02FFF
32			008000-00FFFF	4	01000-01FFF	01000-01FFF	01000-01FFF
32			000000-007FFF	4	00000-00FFF	00000-00FFF	00000-00FFF

3.2.4 4-Mbit, 8-Mbit, and 16-Mbit Byte-Wide Memory Maps
Table 7. 8-Mbit and 16-Mbit Byte-Wide Memory Addressing Map (Sheet 1 of 3)
8-Mbit and 16-Mbit Byte-Wide Memory Addressing

Top Boot			Bottom Boot		
Size (KB)	8 Mbit	16 Mbit	Size (KB)	8 Mbit	16 Mbit
8	FE000-FFFFF	1FE000-1FFFFF	64		
8	FC000-FDFFF	1FC000-1FDFFF	64		
8	FA000-FBFFF	1FA000-1FBFFF	64		
8	F8000-F9FFF	1F8000-1F9FFF	64		
8	F6000-F7FFF	1F6000-1F7FFF	64		
8	F4000-F5FFF	1F4000-1F5FFF	64		
8	F2000-F3FFF	1F2000-1F3FFF	64		
8	F0000-F1FFF	1F0000-1F1FFF	64		



Table 7. 8-Mbit and 16-Mbit Byte-Wide Memory Addressing Map (Sheet 2 of 3)

8-Mbit and 16-Mbit Byte-Wide Memory Addressing

Top Boot			Bottom Boot		
Size (KB)	8 Mbit	16 Mbit	Size (KB)	8 Mbit	16 Mbit
64	E0000-EFFFF	1E0000-1EFFFF	64		
64	D0000-DFFFF	1D0000-1DFFFF	64		
64	C0000-CFFFF	1C0000-1CFFFF	64		
64	B0000-BFFFF	1B0000-1BFFFF	64		
64	A0000-AFFFF	1A0000-1AFFFF	64		
64	90000-9FFFF	190000-19FFFF	64		
64	80000-8FFFF	180000-18FFFF	64		
64	70000-7FFFF	170000-17FFFF	64		
64	60000-6FFFF	160000-16FFFF	64		
64	50000-5FFFF	150000-15FFFF	64		
64	40000-4FFFF	140000-14FFFF	64		
64	30000-3FFFF	130000-13FFFF	64		
64	20000-2FFFF	120000-12FFFF	64		
64	10000-1FFFF	110000-11FFFF	64		
64	00000-0FFFF	100000-10FFFF	64		
64		0F0000-0FFFF	64		
64		0E0000-0EFFFF	64		
64		0D0000-0DFFFF	64		
64		0C0000-0CFFFF	64		
64		0B0000-0BFFFF	64		
64		0A0000-0AFFFF	64		
64		090000-09FFFF	64		
64		080000-08FFFF	64		
64		070000-07FFFF	64		
64		060000-06FFFF	64		1F0000-1FFFF
64		050000-05FFFF	64		1E0000-1EFFFF
64		040000-04FFFF	64		1D0000-1DFFFF
64		030000-03FFFF	64		1C0000-1CFFFF
64		020000-02FFFF	64		1B0000-1BFFFF
64		010000-01FFFF	64		1A0000-1AFFFF
64		000000-00FFFF	64		190000-19FFFF
64			64		180000-18FFFF
64			64		170000-17FFFF
64			64		160000-16FFFF
64			64		150000-15FFFF

Table 7. 8-Mbit and 16-Mbit Byte-Wide Memory Addressing Map (Sheet 3 of 3)

8-Mbit and 16-Mbit Byte-Wide Memory Addressing

Top Boot			Bottom Boot		
Size (KB)	8 Mbit	16 Mbit	Size (KB)	8 Mbit	16 Mbit
64			64		140000-14FFFF
64			64		130000-13FFFF
64			64		120000-12FFFF
64			64		110000-11FFFF
64			64		100000-10FFFF
64			64	F0000-FFFFF	0F0000-0FFFFF
64			64	E0000-EFFFF	0E0000-0EFFFF
64			64	D0000-DFFFF	0D0000-0DFFFF
64			64	C0000-CFFFF	0C0000-0CFFFF
64			64	B0000-BFFFF	0B0000-0BFFFF
64			64	A0000-AFFFF	0A0000-0AFFFF
64			64	90000-9FFFF	090000-09FFFF
64			64	80000-8FFFF	080000-08FFFF
64			64	70000-7FFFF	070000-07FFFF
64			64	60000-6FFFF	060000-06FFFF
64			64	50000-5FFFF	050000-05FFFF
64			64	40000-4FFFF	040000-04FFFF
64			64	30000-3FFFF	030000-03FFFF
64			64	20000-2FFFF	020000-02FFFF
64			64	10000-1FFFF	010000-01FFFF
64			8	0E000-0FFFF	00E000-00FFFF
64			8	0C000-0DFFF	00C000-00DFFF
64			8	0A000-0BFFF	00A000-00BFFF
64			8	08000-09FFF	008000-009FFF
64			8	06000-07FFF	006000-007FFF
64			8	04000-05FFF	004000-005FFF
64			8	02000-03FFF	002000-003FFF
64			8	00000-01FFF	000000-001FFF

Table 8. 4-Mbit Byte Wide Memory Addressing Map

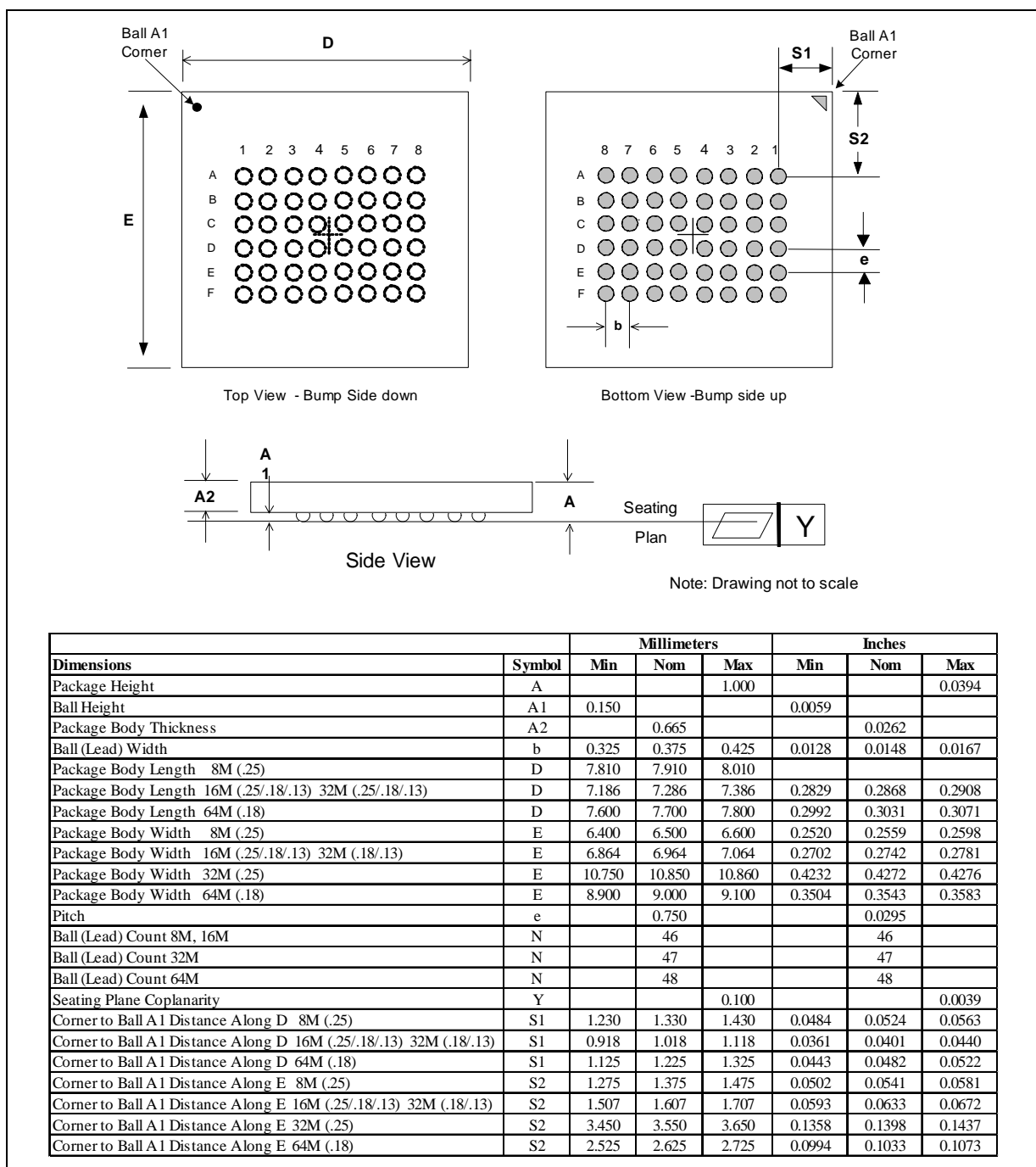
4-Mbit Byte-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KB)	4 Mbit			Size (KB)	4 Mbit		
8	7E000-7FFFF			64	70000-7FFFF		
8	7C000-7DFFF			64	60000-6FFFF		
8	7A000-7BFFF			64	50000-5FFFF		
8	78000-79FFF			64	40000-4FFFF		
8	76000-77FFF			64	30000-3FFFF		
8	74000-75FFF			64	20000-2FFFF		
8	72000-73FFF			64	10000-1FFFF		
8	70000-71FFF			8	0E000-0FFFF		
64	60000-6FFFF			8	0C000-0DFFF		
64	50000-5FFFF			8	0A000-0BFFF		
64	40000-4FFFF			8	08000-09FFF		
64	30000-3FFFF			8	06000-07FFF		
64	20000-2FFFF			8	04000-05FFF		
64	10000-1FFFF			8	02000-03FFF		
64	00000-0FFFF			8	00000-01FFF		

4.0 Package Information

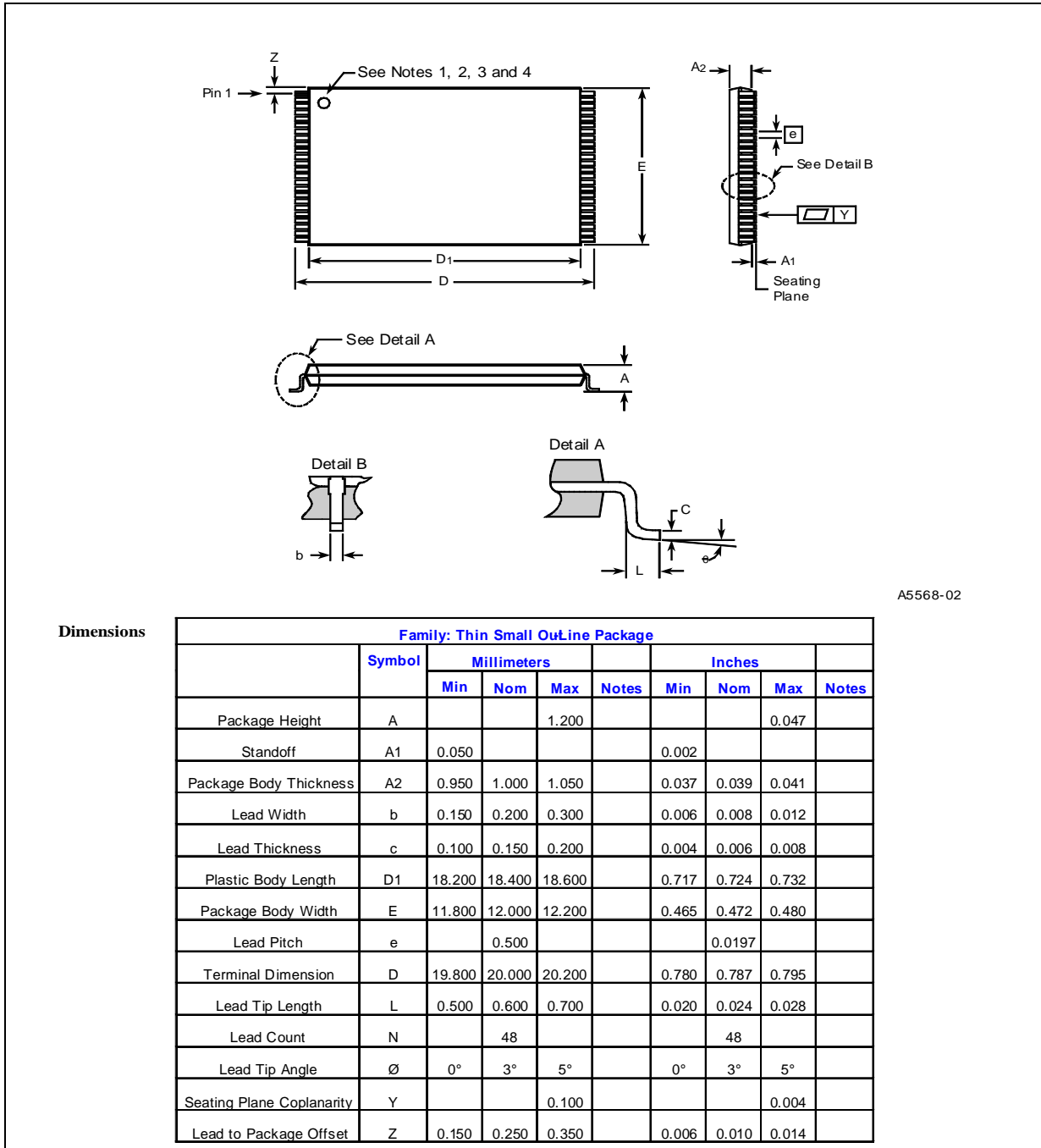
4.1 μ BGA* and Very Thin Profile Fine Pitch Ball Grid Array (VF BGA) Package

Figure 2. μ BGA* and VF BGA Package Drawing



4.2 TSOP Package

Figure 3. TSOP Package Drawing

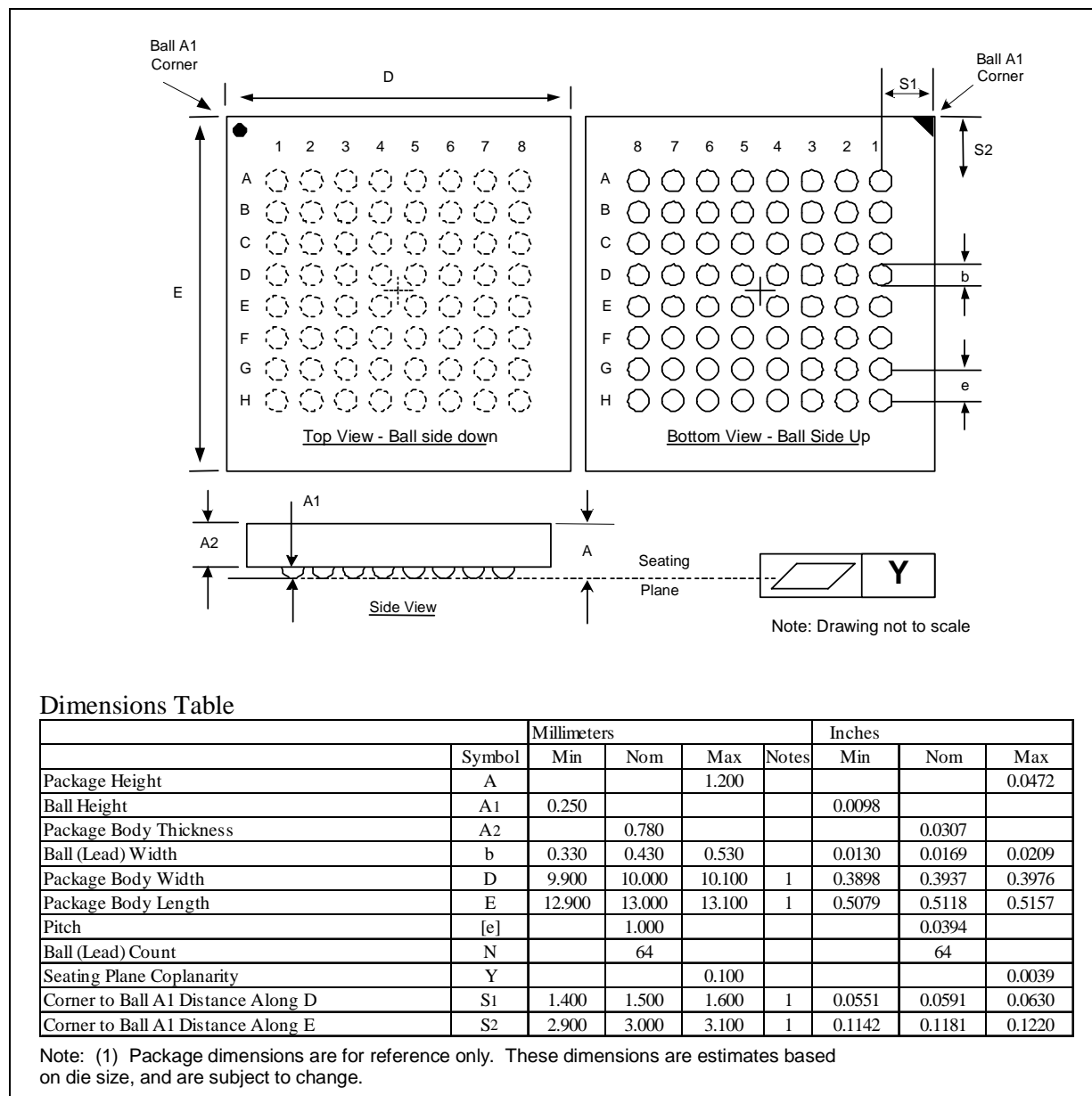


Notes:

1. One dimple on package denotes Pin 1.
2. If two dimples, then the larger dimple denotes Pin 1.
3. Pin 1 is in the upper left corner of the package, in reference to the product mark.

4.3 Easy BGA Package

Figure 4. Easy BGA Package Drawing



5.0 Pinout and Signal Descriptions

This section explains the package pinout and signal descriptions.

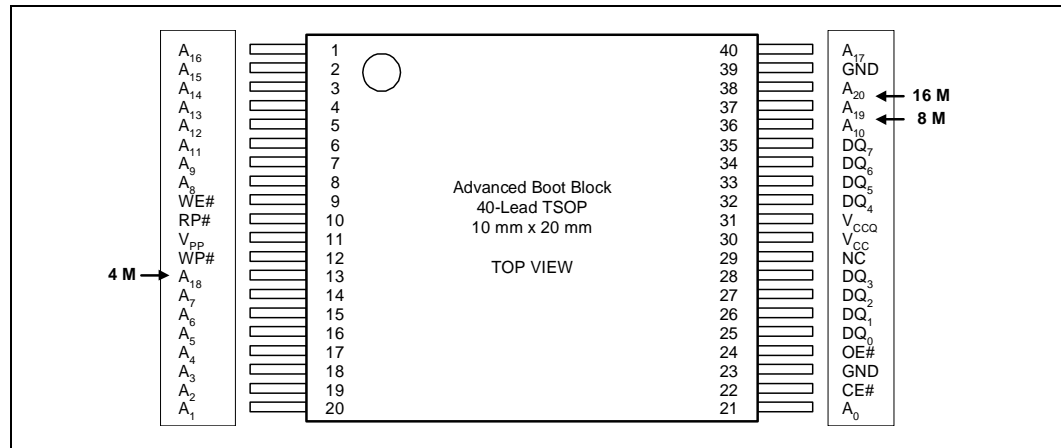
5.1 Signal Pinouts

The B3 flash memory device is available in the following packages:

- 40-lead TSOP (x8, [Figure 5](#)).
- 48-lead TSOP (x16, [Figure 6](#)).
- 48-ball μ BGA (x8 in [Figure 8](#) and x16 in [Figure 9](#)).
- 48-ball VF BGA (x16, [Figure 9](#)).

5.1.1 40-Lead and 48-Lead TSOP Packages

Figure 5. 40-Lead TSOP Package for x8 Configurations



Notes:

1. 40-Lead TSOP available for 8-Mbit and 16-Mbit densities only.
2. Lower densities have NC on the upper address pins. For example, an 8-Mbit device has NC on Pin 38.

Figure 6. 48-Lead TSOP Package for x16 Configurations

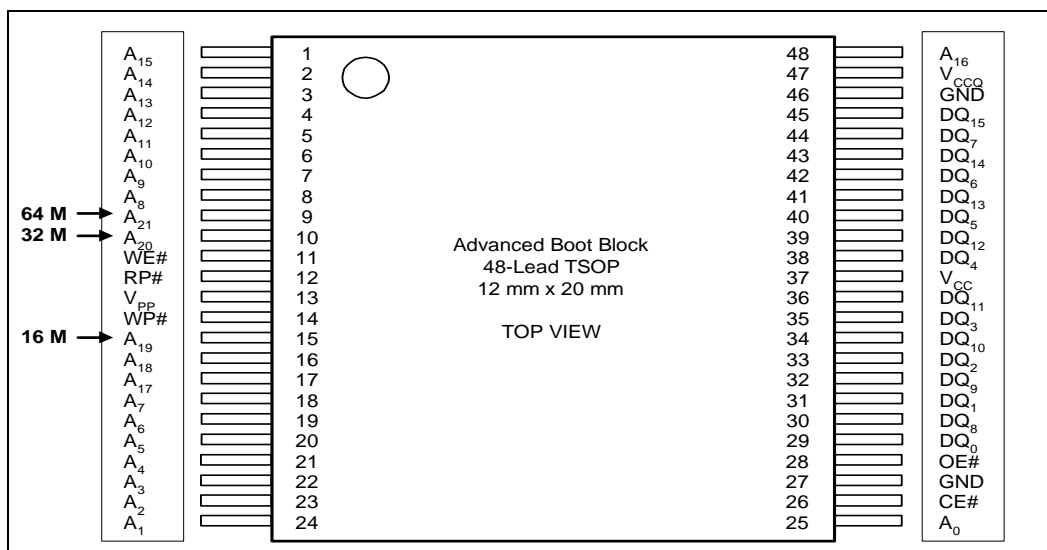
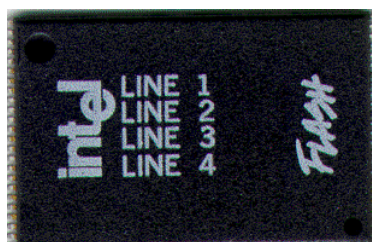
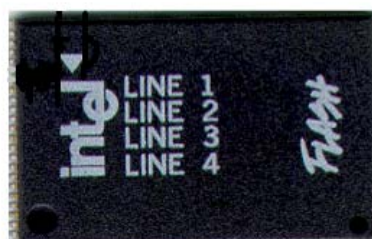


Figure 7. New Mark for Pin-1 Indicator: 40-Lead 8/16 Mb TSOP and 48-Lead 8/16/32 Mb TSOP



New Mark:

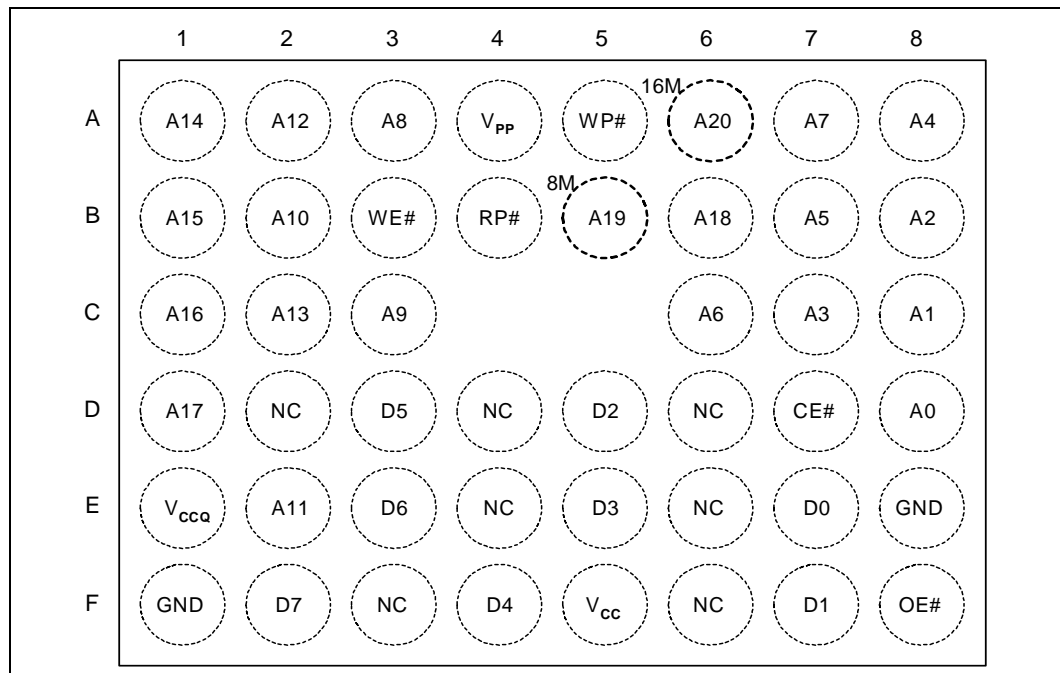


Note: The topside marking on 8-Mb, 16-Mb, and 32-Mb Intel[®] Advanced Boot Block 40L and 48L TSOP products changed to a white ink triangle as a Pin-1 indicator. Products without the white triangle continue to use a dimple as a Pin-1 indicator. No other changes were made in package size, materials, functionality, customer handling, or manufacturability. The product continues to meet stringent Intel quality requirements. [Table 9](#) lists the ordering codes of the affected products. See also [Table 34](#) “Ordering Information: Valid Combinations” on page 70.

Table 9. B3 Flash Memory Device Ordering Information

Ordering Information Valid Combinations				
40-Lead TSOP			48-Lead TSOP	
Ext. Temp. 64 Mbit			TE28F640B3TC70	TE28F640B3BC70
Ext. Temp. 32 Mbit			TE28F320B3TD70 TE28F320B3TC70 TE28F320B3TC90 TE28F320B3TA100 TE28F320B3TA110	TE28F320B3BD70 TE28F320B3BC70 TE28F320B3BC90 TE28F320B3BA100 TE28F320B3BA110
Ext. Temp. 16 Mbit	TE28F016B3TA90 TE28F016B3TA110	TE28F016B3BA90 TE28F016B3BA110	TE28F160B3TC70 TE28F160B3TC80 TE28F160B3TA90 TE28F160B3TA110	TE28F160B3BC70 TE28F160B3BC80 TE28F160B3BA90 TE28F160B3BA110
Ext. Temp. 8 Mbit	TE28F008B3TA90 TE28F008B3TA110	TE28F008B3BA90 TE28F008B3BA110	TE28F800B3TA90 TE28F800B3TA110	TE28F800B3BA90 TE28F800B3BA110

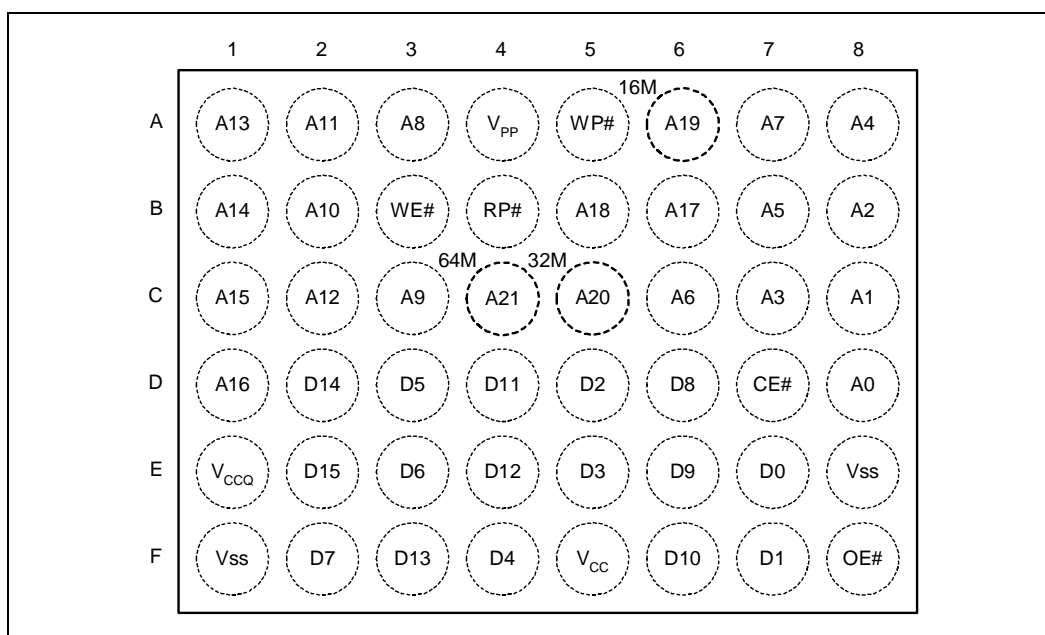
Figure 8. x8 48-Ball μ BGA* Chip Size Package (Top View, Ball Down)



Notes:

1. A19 and A20 indicate the upgrade address connections. Lower density devices do not have the upper address solder balls. Do not route is not done in this area. A₂₀ is the upgrade address for the 16-Mbit device.

Figure 9. x16 48-Ball VF BGA and µBGA* Chip Size Package (Top View, Ball Down)

**Notes:**

1. A19, A20, and A21 indicate the upgrade address connections. Lower density devices do not have the upper address solder balls. Do not route in this area.
 - A₁₉ is the upgrade address for the 16-Mbit device.
 - A₂₀ is the upgrade address for the 32-Mbit device.
 - A₂₁ is the upgrade address for the 64-Mbit device.
2. [Table 10 “B3 Flash memory Device Signal Descriptions” on page 31](#) details the usage of each device pin.

5.2 Signal Descriptions

Table 10 describes the active signals.

Table 10. B3 Flash memory Device Signal Descriptions (Sheet 1 of 2)

Symbol	Type	Description
A ₀ –A ₂₁	Input	ADDRESS INPUTS for memory addresses. Addresses are internally latched during a program or erase cycle. 28F008B3: A[0-19], 28F016B3: A[0-20], 28F800B3: A[0-18], 28F160B3: A[0-19], 28F320B3: A[0-20], 28F640B3: A[0-21]
DQ ₀ –DQ ₇	Input/ Output	DATA INPUTS/OUTPUTS: Inputs array data on the second CE# and WE# cycle during a Program command. <ul style="list-style-type: none"> Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched. Outputs array, identifier and Status Register data. The data pins float to tristate when the chip is deselected or the outputs are disabled.
DQ ₈ –DQ ₁₅	Input/ Output	DATA INPUTS/OUTPUTS: <ul style="list-style-type: none"> Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched. Outputs array and identifier data. The data pins float to tristate when the chip is de-selected. Not included on x8 products.
CE#	Input	CHIP ENABLE: Activates the internal control logic, input buffers, decoders, and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels.
OE#	Input	OUTPUT ENABLE: Enables the flash memory device outputs through the data buffers during a Read operation. OE# is active low.
WE#	Input	WRITE ENABLE: Controls writes to the Command Register and memory array. WE# is active low. Addresses and data are latched on the rising edge of the second WE# pulse.
RP#	Input	RESET/DEEP POWER-DOWN: Uses two voltage levels (V_{IL} , V_{IH}) to control reset/deep power-down mode. <ul style="list-style-type: none"> When RP# is at logic low, the flash memory device is in reset/deep power-down mode, which drives the outputs to High-Z, resets the Write State Machine, and minimizes current levels (I_{CCD}). When RP# is at logic high, the flash memory device is in standard operation. When RP# transitions from logic-low to logic-high, the flash memory device defaults to the read array mode.
WP#	Input	WRITE PROTECT: Locks and unlocks the two lockable parameter blocks. <ul style="list-style-type: none"> When WP# is at logic low, the lockable blocks are locked, preventing Program and Erase operations to those blocks. If a Program or Erase operation is attempted on a locked block, SR.1 and either SR.4 [program] or SR.5 [erase] are set to indicate the operation failed. When WP# is at logic high, the lockable blocks are unlocked and can be programmed or erased. See Section 12.0, "Block Locking" on page 62 for details on write protection.
V _{CCQ}	Input	OUTPUT V_{CC}: Enables all outputs to be driven to 1.8 V to 2.5 V while the V _{CC} is at 2.7 V to 3.3 V. If the V _{CC} is regulated to 2.7 V to 2.85 V, V _{CCQ} can be driven at 1.65 V to 2.5 V to achieve lowest power operation (see Section 7.2, "DC Voltage Characteristics" on page 36). This input can be tied directly to V _{CC} (2.7 V to 3.6 V).
V _{CC}	Power	DEVICE Power Supply: 2.7 V to 3.6 V

Table 10. B3 Flash memory Device Signal Descriptions (Sheet 2 of 2)

Symbol	Type	Description
V_{PP}	Power	PROGRAM/ERASE Power Supply: Supplies power for Program and Erase operations. V_{PP} can be the same as V_{CC} (2.7 V to 3.6 V) for single supply voltage operation. For fast programming at manufacturing, 11.4 V to 12.6 V can be supplied to V_{PP} . This pin cannot be left floating. 11.4 V to 12.6 V can be applied to V_{PP} only for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} can be connected to 12 V for a total of 80 hours maximum (see Section 13.0, “ V_{PP} Program and Erase Voltages” on page 63 for details). $V_{PP} < V_{PPLK}$ protects memory contents against inadvertent or unintended program and erase commands.
GND	—	Ground: For all internal circuitry. All ground inputs must be connected.
NC	—	No Connect: Pin can be driven or left floating.

6.0 Maximum Ratings and Operating Conditions

6.1 Absolute Maximum Ratings

Warning: Stressing the flash memory device beyond the Absolute Maximum Ratings in Table 11 can cause permanent damage. These ratings are stress ratings only.

NOTICE: Specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

Table 11. Absolute Maximum Ratings

Parameter	Maximum Rating	Notes
Extended Operating Temperature	-40 °C to +85 °C	
During Read		
During Block Erase and Program		
Temperature under Bias	-40 °C to +85 °C	
Storage Temperature	-65 °C to +125 °C	
Voltage On Any Pin (except V_{CC} and V_{PP}) with Respect to GND	-0.5 V to +3.7 V	1
V_{PP} Voltage (for Block Erase and Program) with Respect to GND	-0.5 V to +13.5 V	1,2,3
V_{CC} and V_{CCQ} Supply Voltage with Respect to GND	-0.2 V to +3.6 V	
Output Short Circuit Current	100 mA	4

Notes:

- Minimum DC voltage is -0.5 V on input/output pins. During transitions, this level might undershoot to -2.0 V for periods <20 ns. Maximum DC voltage on input/output pins is $V_{CC} + 0.5$ V which, during transitions, might overshoot to $V_{CC} + 2.0$ V for periods <20 ns.
- Maximum DC voltage on V_{PP} might overshoot to +14.0 V for periods <20 ns.
- V_{PP} Program voltage is typically 1.65 V to 3.6 V. Connection to a 11.4 V to 12.6 V supply can be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase. V_{PP} can be connected to 12 V for a total of 80 hours maximum.
- Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Do not operate the flash memory device beyond the Operating Conditions in Table 12. Extended exposure beyond the Operating Conditions can affect device reliability.

Table 12. Temperature and Voltage Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
T_A	Operating Temperature	-40	+85	°C	
V_{CC1}	V_{CC} Supply Voltage	2.7	3.6	Volts	1, 2
V_{CC2}		3.0	3.6		1, 2
V_{CCQ1}	I/O Supply Voltage	2.7	3.6	Volts	1
V_{CCQ2}		1.65	2.5		
V_{CCQ3}		1.8	2.5		
V_{PP1}	Supply Voltage	1.65	3.6	Volts	1
V_{PP2}		11.4	12.6	Volts	1, 3
Cycling	Block Erase Cycling	100,000		Cycles	3

Notes:

- V_{CC} and V_{CCQ} must share the same supply when they are in the V_{CC1} range.
- $V_{CCMax} = 3.3$ V for 0.25 μ m 32-Mbit devices.
- $V_{PP} = 11.4$ V–12.6 V can be applied during a program/erase only for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} can be connected to 12 V for a total of 80 hours maximum.

7.0 Electrical Specifications

7.1 DC Current Characteristics

Table 13. DC Current Characteristics (Sheet 1 of 2)

Sym	Parameter	V _{CC}	2.7 V–3.6 V		2.7 V–2.85 V		2.7 V–3.3 V		Unit	Test Conditions
		V _{CCQ}	2.7 V–3.6 V		1.65 V–2.5 V		1.8 V–2.5 V			
		Note	Typ	Max	Typ	Max	Typ	Max		
I _{LI}	Input Load Current	1,2		± 1		± 1		± 1	μA	V _{CC} = V _{CC} Max V _{CCQ} = V _{CCQ} Max V _{IN} = V _{CCQ} or GND
I _{LO}	Output Leakage Current	1,2		± 10		± 10		± 10	μA	V _{CC} = V _{CC} Max V _{CCQ} = V _{CCQ} Max V _{IN} = V _{CCQ} or GND
I _{CCS}	V _{CC} Standby Current for 0.13 and 0.18 Micron Product	1	7	15	20	50	150	250	μA	V _{CC} = V _{CC} Max CE# = RP# = V _{CCQ} or during Program/ Erase Suspend
	V _{CC} Standby Current for 0.25 Micron Product	1	10	25	20	50	150	250	μA	WP# = V _{CCQ} or GND
I _{CCD}	V _{CC} Power-Down Current for 0.13 and 0.18 Micron Product	1,2	7	15	7	20	7	20	μA	V _{CC} = V _{CC} Max V _{CCQ} = V _{CCQ} Max V _{IN} = V _{CCQ} or GND
	V _{CC} Power-Down Current for 0.25 Product	1,2	7	25	7	25	7	25	μA	RP# = GND ± 0.2 V
I _{CCR}	V _{CC} Read Current for 0.13 and 0.18 Micron Product	1,2,3	9	18	8	15	9	15	mA	V _{CC} = V _{CC} Max V _{CCQ} = V _{CCQ} Max OE# = V _{IH} , CE# = V _{IL} f = 5 MHz, I _{OUT} = 0 mA
	V _{CC} Read Current for 0.25 Micron Product	1,2,3	10	18	8	15	9	15	mA	Inputs = V _{IL} or V _{IH}
I _{PPD}	V _{PP} Deep Power-Down Current	1	0.2	5	0.2	5	0.2	5	μA	RP# = GND ± 0.2 V V _{PP} ≤ V _{CC}
I _{CCW}	V _{CC} Program Current	1,4	18	55	18	55	18	55	mA	V _{PP} = V _{PP1} , Program in Progress
			8	22	10	30	10	30	mA	V _{PP} = V _{PP2} (12v), Program in Progress
I _{CCE}	V _{CC} Erase Current	1,4	16	45	21	45	21	45	mA	V _{PP} = V _{PP1} , Erase in Progress
			8	15	16	45	16	45	mA	V _{PP} = V _{PP2} (12v), Erase in Progress
I _{CCES} / I _{CCWS}	V _{CC} Erase Suspend Current for 0.13 and 0.18 Micron Product	1,4,5	7	15	50	200	50	200	μA	CE# = V _{IH} , Erase Suspend in Progress
	V _{CC} Erase Suspend Current for 0.25 Micron Product		10	25	50	200	50	200	μA	
I _{PPR}	V _{PP} Read Current	1,4	2	±15	2	±15	2	±15	μA	V _{PP} ≤ V _{CC}
			50	200	50	200	50	200	μA	V _{PP} > V _{CC}

Table 13. DC Current Characteristics (Sheet 2 of 2)

Sym	Parameter	V _{CC}	2.7 V–3.6 V		2.7 V–2.85 V		2.7 V–3.3 V		Unit	Test Conditions
		V _{CCQ}	2.7 V–3.6 V		1.65 V–2.5 V		1.8 V–2.5 V			
		Note	Typ	Max	Typ	Max	Typ	Max		
I _{PPW}	V _{PP} Program Current	1,4	0.05	0.1	0.05	0.1	0.05	0.1	mA	V _{PP} = V _{PP1} , Program in Progress
			8	22	8	22	8	22	mA	V _{PP} = V _{PP2} (12V), Program in Progress
I _{PPE}	V _{PP} Erase Current	1,4	0.05	0.1	0.05	0.1	0.05	0.1	mA	V _{PP} = V _{PP1} , Erase in Progress
			8	22	16	45	16	45	mA	V _{PP} = V _{PP2} (12V), Erase in Progress
I _{PPES} / I _{PPWS}	V _{CC} Erase Suspend Current	1,4	0.2	5	0.2	5	0.2	5	μA	V _{PP} = V _{PP1} , Program or Erase Suspend in Progress
			50	200	50	200	50	200	μA	V _{PP} = V _{PP2} (12V), Program or Erase Suspend in Progress

Notes:

- All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC}, T_A = +25 °C.
- The test conditions V_{CC}Max, V_{CCQ}Max, V_{CC}Min, and V_{CCQ}Min refer to the maximum or minimum V_{CC} or V_{CCQ} voltage listed at the top of each column. V_{CC}Max = 3.3 V for 0.25μm 32-Mbit devices.
- Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels in static operation (CMOS inputs).
- Sampled, not 100% tested.
- I_{CCES} or I_{CCWS} is specified with the flash memory device deselected.
 - If the device is read while in erase suspend, the current draw is the sum of I_{CCES} and I_{CCR}.
 - If the device is read while in program suspend, the current draw is the sum of I_{CCWS} and I_{CCR}.

7.2 DC Voltage Characteristics

Table 14. DC Voltage Characteristics

Symbol	Parameter	V _{CC}	2.7 V–3.6 V		2.7 V–2.85 V		2.7 V–3.3 V		Unit	Test Conditions
		V _{CCQ}	2.7 V–3.6 V		1.65 V–2.5 V		1.8 V–2.5 V			
		Note	Min	Max	Min	Max	Min	Max		
V _{IL}	Input Low Voltage		-0.4	V _{CC} * 0.22 V	-0.4	0.4	-0.4	0.4	V	
V _{IH}	Input High Voltage		2.0	V _{CCQ} +0.3V	V _{CCQ} - 0.4V	V _{CCQ} +0.3V	V _{CCQ} - 0.4V	V _{CCQ} +0.3V	V	
V _{OL}	Output Low Voltage		-0.1	0.1	-0.1	0.1	-0.1	0.1	V	V _{CC} = V _{CCMin} V _{CCQ} = V _{CCQMin} I _{OL} = 100 μA
V _{OH}	Output High Voltage		V _{CCQ} -0.1V		V _{CCQ} - 0.1V		V _{CCQ} - 0.1V		V	V _{CC} = V _{CCMin} V _{CCQ} = V _{CCQMin} I _{OH} = -100 μA
V _{PPLK}	V _{PP} Lock-Out Voltage	1		1.0		1.0		1.0	V	Complete Write Protection
V _{PP1}	V _{PP} During Program / Erase Operations	1	1.65	3.6	1.65	3.6	1.65	3.6	V	
V _{PP2}		1,2	11.4	12.6	11.4	12.6	11.4	12.6	V	
V _{LKO}	V _{CC} Prog/ Erase Lock Voltage		1.5		1.5		1.5		V	
V _{LKO2}	V _{CCQ} Prog/ Erase Lock Voltage		1.2		1.2		1.2		V	

Notes:

- Erase and Program are inhibited when V_{PP} < V_{PPLK} and not guaranteed outside the valid V_{PP} ranges of V_{PP1} and V_{PP2}.
- V_{PP} = 11.4 V–12.6 V can be applied during program/erase only for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} can be connected to 12 V for a total of 80 hours maximum.

8.0 AC Characteristics

8.1 AC Read Characteristics

Table 15. Read Operations—8-Mbit Density

#	Sym	Parameter	Density	8 Mbit								Unit
			Product	90 ns				110 ns				
			V _{CC}	3.0 V – 3.6 V		2.7 V – 3.6 V		3.0 V – 3.6 V		2.7 V – 3.6 V		
			Note	Min	Max	Min	Max	Min	Max	Min	Max	
R1	t _{AVAV}	Read Cycle Time	3,4	80		90		100		110		ns
R2	t _{AVQV}	Address to Output Delay	3,4		80		90		100		110	ns
R3	t _{ELQV}	CE# to Output Delay	1,3,4		80		90		100		110	ns
R4	t _{GLQV}	OE# to Output Delay	1,3,4		30		30		30		30	ns
R5	t _{PHQV}	RP# to Output Delay	3,4		150		150		150		150	ns
R6	t _{ELQX}	CE# to Output in Low Z	2,3,4	0		0		0		0		ns
R7	t _{GLQX}	OE# to Output in Low Z	2,3,4	0		0		0		0		ns
R8	t _{EHQZ}	CE# to Output in High Z	2,3,4		20		20		20		20	ns
R9	t _{GHQZ}	OE# to Output in High Z	2,3,4		20		20		20		20	ns
R10	t _{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	2,3,4	0		0		0		0		ns

Notes:

1. OE# can be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.
3. See Figure 10 "Read Operation Waveform" on page 40.
4. See Figure 12 "AC Input/Output Reference Waveform" on page 46 for timing measurements and maximum allowable input slew rate.

Table 16. Read Operations—16-Mbit Density

#	Sym	Parameter	Density	16 Mbit										Unit	Notes		
			Product	70 ns		80 ns		90 ns		110 ns							
			V _{CC}	2.7 V–3.6 V		2.7 V–3.6 V		3.0 V–3.6 V		2.7 V–3.6 V		3.0 V–3.6 V				2.7 V–3.6 V	
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			Min	Max
R1	t _{AVAV}	Read Cycle Time	70		80		80		90		100		110		ns	3,4	
R2	t _{AVQV}	Address to Output Delay		70		80		80		90		100		110	ns	3,4	
R3	t _{ELQV}	CE# to Output Delay		70		80		80		90		100		110	ns	1,3,4	
R4	t _{GLQV}	OE# to Output Delay		20		20		30		30		30		30	ns	1,3,4	
R5	t _{PHQV}	RP# to Output Delay		150		150		150		150		150		150	ns	3,4	
R6	t _{ELQX}	CE# to Output in Low Z	0		0		0		0		0		0		ns	2,3,4	
R7	t _{GLQX}	OE# to Output in Low Z	0		0		0		0		0		0		ns	2,3,4	
R8	t _{EHQZ}	CE# to Output in High Z		20		20		20		20		20		20	ns	2,3,4	
R9	t _{GHQZ}	OE# to Output in High Z		20		20		20		20		20		20	ns	2,3,4	
R10	t _{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	0		0		0		0		0		0		ns	2,3,4	

Notes:

1. OE# can be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.
3. See [Figure 10 “Read Operation Waveform”](#) on page 40.
4. See [Figure 12 “AC Input/Output Reference Waveform”](#) on page 46 for timing measurements and maximum allowable input slew rate.

Table 17. Read Operations—32-Mbit Density

#	Sym	Parameter	Density	32 Mbit												Unit	Notes
			Product	70 ns		90 ns		100 ns		110 ns							
			V _{CC}	2.7 V–3.6 V		2.7 V–3.6 V		3.0 V–3.3 V		2.7 V–3.3 V		3.0 V–3.3 V		2.7 V–3.3 V			
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
R1	t _{AVAV}	Read Cycle Time	70		90		90		100		100		110		ns	3,4	
R2	t _{AVQV}	Address to Output Delay		70		90		90		100		100		110	ns	3,4	
R3	t _{ELQV}	CE# to Output Delay		70		90		90		100		100		110	ns	1,3,4	
R4	t _{GLQV}	OE# to Output Delay		20		20		30		30		30		30	ns	1,3,4	
R5	t _{PHQV}	RP# to Output Delay		150		150		150		150		150		150	ns	3,4	
R6	t _{ELQX}	CE# to Output in Low Z	0		0		0		0		0		0		ns	2,3,4	
R7	t _{GLQX}	OE# to Output in Low Z	0		0		0		0		0		0		ns	2,3,4	
R8	t _{EHQZ}	CE# to Output in High Z		20		20		20		20		20		20	ns	2,3,4	
R9	t _{GHQZ}	OE# to Output in High Z		20		20		20		20		20		20	ns	2,3,4	
R10	t _{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	0		0		0		0		0		0		ns	2,3,4	

Notes:

1. OE# can be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.
3. See [Figure 10 "Read Operation Waveform"](#) on page 40.
4. See [Figure 12 "AC Input/Output Reference Waveform"](#) on page 46 for timing measurements and maximum allowable input slew rate.

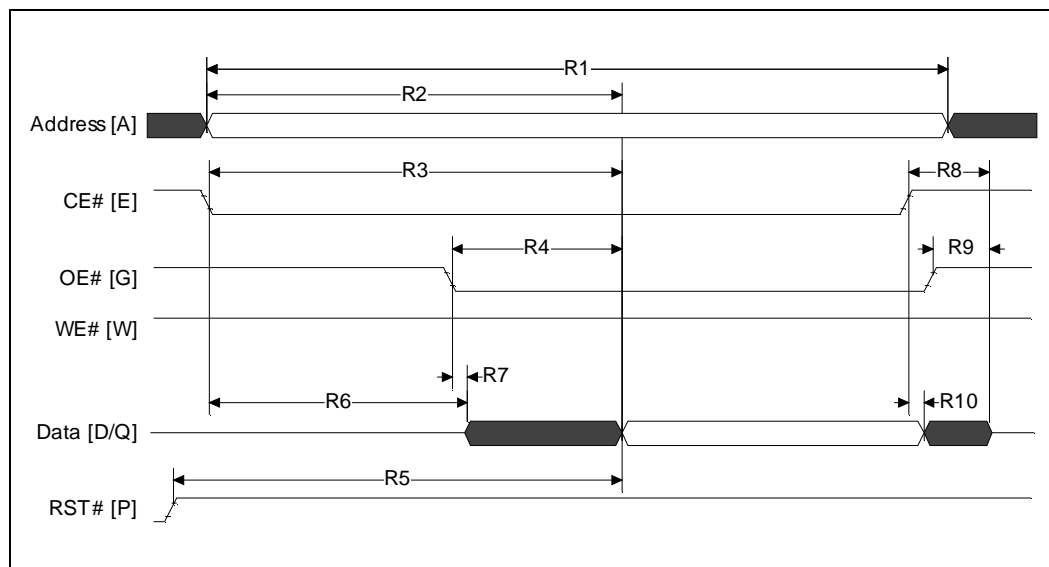
Table 18. Read Operations — 64-Mbit Density

#	Sym	Parameter	Density		64 Mbit				Unit
			Product		70 ns		80 ns		
			V _{CC}		2.7 V–3.6 V		2.7 V–3.6 V		
			Note	Min	Max	Min	Max		
R1	t _{AVAV}	Read Cycle Time	3,4		70		80		ns
R2	t _{AVQV}	Address to Output Delay	3,4			70		80	ns
R3	t _{ELQV}	CE# to Output Delay	1,3,4			70		80	ns
R4	t _{GLQV}	OE# to Output Delay	1,3,4			20		20	ns
R5	t _{PHQV}	RP# to Output Delay	3,4			150		150	ns
R6	t _{ELQX}	CE# to Output in Low Z	2,3,4		0		0		ns
R7	t _{GLQX}	OE# to Output in Low Z	2,3,4		0		0		ns
R8	t _{EHQZ}	CE# to Output in High Z	2,3,4			20		20	ns
R9	t _{GHQZ}	OE# to Output in High Z	2,3,4			20		20	ns
R10	t _{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	2,3,4		0		0		ns

Notes:

1. OE# can be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.
3. See Figure 10 “Read Operation Waveform” on page 40.
4. See Figure 12 “AC Input/Output Reference Waveform” on page 46 for timing measurements and maximum allowable input slew rate.

Figure 10. Read Operation Waveform



8.2 AC Write Characteristics

Table 19. Write Operations—8-Mbit Density

#	Sym	Parameter	Density		8 Mbit				Unit
			Product		90 ns		110 ns		
			V _{CC}	3.0 V – 3.6 V	80		100		
				2.7 V – 3.6 V		90		110	
		Note	Min	Min	Min	Min			
W1	t _{PHWL} / t _{PHEL}	RP# High Recovery to WE# (CE#) Going Low	4,5	150	150	150	150	ns	
W2	t _{ELWL} / t _{WLEL}	CE# (WE#) Setup to WE# (CE#) Going Low	4,5	0	0	0	0	ns	
W3	t _{WLWH} / t _{ELEH}	WE# (CE#) Pulse Width	4,5	50	60	70	70	ns	
W4	t _{DVWH} / t _{DVEH}	Data Setup to WE# (CE#) Going High	2,4,5	50	50	60	60	ns	
W5	t _{AVWH} / t _{AVEH}	Address Setup to WE# (CE#) Going High	2,4,5	50	60	70	70	ns	
W6	t _{WHEH} / t _{EHWH}	CE# (WE#) Hold Time from WE# (CE#) High	4,5	0	0	0	0	ns	
W7	t _{WHDX} / t _{EHDX}	Data Hold Time from WE# (CE#) High	2,4,5	0	0	0	0	ns	
W8	t _{WHAX} / t _{EHAX}	Address Hold Time from WE# (CE#) High	2,4,5	0	0	0	0	ns	
W9	t _{WHWL} / t _{EHEL}	WE# (CE#) Pulse Width High	2,4,5	30	30	30	30	ns	
W10	t _{VPWH} / t _{VPEH}	V _{PP} Setup to WE# (CE#) Going High	3,4,5	200	200	200	200	ns	
W11	t _{QVVL}	V _{PP} Hold from Valid SRD	3,4	0	0	0	0	ns	
W12	t _{BHWH} / t _{BHEH}	WP# Setup to WE# (CE#) Going High	3,4	0	0	0	0	ns	
W13	t _{QVBL}	WP# Hold from Valid SRD	3,4	0	0	0	0	ns	
W14	t _{WHGL}	WE# High to OE# Going Low	3,4	30	30	30	30	ns	

Notes:

- Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). So t_{VP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}.

Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). So t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}.

- Refer to [Table 27 “Bus Operations^{\(1\)}” on page 51](#) for valid A_{IN} or D_{IN}.
- Sampled, but not 100% tested.
- See [Figure 12 “AC Input/Output Reference Waveform” on page 46](#) for timing measurements and maximum allowable input slew rate.
- See [Figure 11 “Write Operations Waveform” on page 45](#).

Table 20. Write Operations—16-Mbit Density

#	Sym	Parameter	Density		16 Mbit						Unit
			Product		70 ns	80 ns	90 ns		110 ns		
			V _{CC}	3.0 V – 3.6 V			80		100		
				2.7 V – 3.6 V	70	80		90		110	
Note		Min	Min	Min	Min	Min	Min				
W1	t _{PHWL} / t _{PHEL}	RP# High Recovery to WE# (CE#) Going Low	4,5	150	150	150	150	150	150	ns	
W2	t _{ELWL} / t _{WLEL}	CE# (WE#) Setup to WE# (CE#) Going Low	4,5	0	0	0	0	0	0	ns	
W3	t _{WLWH} / t _{ELEH}	WE# (CE#) Pulse Width	1,4,5	45	50	50	60	70	70	ns	
W4	t _{DVWH} / t _{DVEH}	Data Setup to WE# (CE#) Going High	2,4,5	40	40	50	50	60	60	ns	
W5	t _{AVWH} / t _{AVEH}	Address Setup to WE# (CE#) Going High	2,4,5	50	50	50	60	70	70	ns	
W6	t _{WHEH} / t _{EHWH}	CE# (WE#) Hold Time from WE# (CE#) High	4,5	0	0	0	0	0	0	ns	
W7	t _{WHDX} / t _{EHDX}	Data Hold Time from WE# (CE#) High	2,4,5	0	0	0	0	0	0	ns	
W8	t _{WHAX} / t _{EHAX}	Address Hold Time from WE# (CE#) High	2,4,5	0	0	0	0	0	0	ns	
W9	t _{WHWL} / t _{EHEL}	WE# (CE#) Pulse Width High	1,4,5	25	30	30	30	30	30	ns	
W10	t _{VPWH} / t _{VPEH}	V _{PP} Setup to WE# (CE#) Going High	3,4,5	200	200	200	200	200	200	ns	
W11	t _{QVVL}	V _{PP} Hold from Valid SRD	3,4	0	0	0	0	0	0	ns	
W12	t _{BHWH} / t _{BHEH}	WP# Setup to WE# (CE#) Going High	3,4	0	0	0	0	0	0	ns	
W13	t _{QVBL}	WP# Hold from Valid SRD	3,4	0	0	0	0	0	0	ns	
W14	t _{WHGL}	WE# High to OE# Going Low	3,4	30	30	30	30	30	30	ns	

Notes:

- Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). So t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}.
Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). So t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}.
- Refer to [Table 27 "Bus Operations^{\(1\)}"](#) on page 51 for valid A_{IN} or D_{IN}.
- Sampled, but not 100% tested.
- See [Figure 12 "AC Input/Output Reference Waveform"](#) on page 46 for timing measurements and maximum allowable input slew rate.
- See [Figure 11 "Write Operations Waveform"](#) on page 45.

Table 21. Write Operations—32-Mbit Density

#	Sym	Parameter	Density		32 Mbit						Unit
			Product		70 ns	90 ns	100 ns		110 ns		
			V _{CC}	3.0 V – 3.6 V ⁶			90		100		
				2.7 V – 3.6 V	70	90		100		110	
Note		Min	Min	Min	Min	Min	Min				
W1	t _{PHWL} / t _{PHEL}	RP# High Recovery to WE# (CE#) Going Low	4,5	150	150	150	150	150	150	ns	
W2	t _{ELWL} / t _{WLEL}	CE# (WE#) Setup to WE# (CE#) Going Low	4,5	0	0	0	0	0	0	ns	
W3	t _{WLWH} / t _{ELEH}	WE# (CE#) Pulse Width	1,4,5	45	60	60	70	70	70	ns	
W4	t _{DVWH} / t _{DVEH}	Data Setup to WE# (CE#) Going High	2,4,5	40	40	50	60	60	60	ns	
W5	t _{AVWH} / t _{AVEH}	Address Setup to WE# (CE#) Going High	2,4,5	50	60	60	70	70	70	ns	
W6	t _{WHEH} / t _{EHWH}	CE# (WE#) Hold Time from WE# (CE#) High	4,5	0	0	0	0	0	0	ns	
W7	t _{WHDX} / t _{EHDX}	Data Hold Time from WE# (CE#) High	2,4,5	0	0	0	0	0	0	ns	
W8	t _{WHAX} / t _{EHAX}	Address Hold Time from WE# (CE#) High	2,4,5	0	0	0	0	0	0	ns	
W9	t _{WHWL} / t _{EHEL}	WE# (CE#) Pulse Width High	1,4,5	25	30	30	30	30	30	ns	
W10	t _{VPWH} / t _{VPEH}	V _{PP} Setup to WE# (CE#) Going High	3,4,5	200	200	200	200	200	200	ns	
W11	t _{QVVL}	V _{PP} Hold from Valid SRD	3,4	0	0	0	0	0	0	ns	
W12	t _{BHWH} / t _{BHEH}	WP# Setup to WE# (CE#) Going High	3,4	0	0	0	0	0	0	ns	
W13	t _{QVBL}	WP# Hold from Valid SRD	3,4	0	0	0	0	0	0	ns	
W14	t _{WHGL}	WE# High to OE# Going Low	3,4	30	30	30	30	30	30	ns	

Notes:

- Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). So t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}.
Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). So t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}.
- Refer to [Table 27 “Bus Operations^{\(1\)}” on page 51](#) for valid A_{IN} or D_{IN}.
- Sampled, but not 100% tested.
- See [Figure 12 “AC Input/Output Reference Waveform” on page 46](#) for timing measurements and maximum allowable input slew rate.
- See [Figure 11 “Write Operations Waveform” on page 45](#).
- V_{CC}Max = 3.3 V for 32-Mbit 0.25 Micron product.

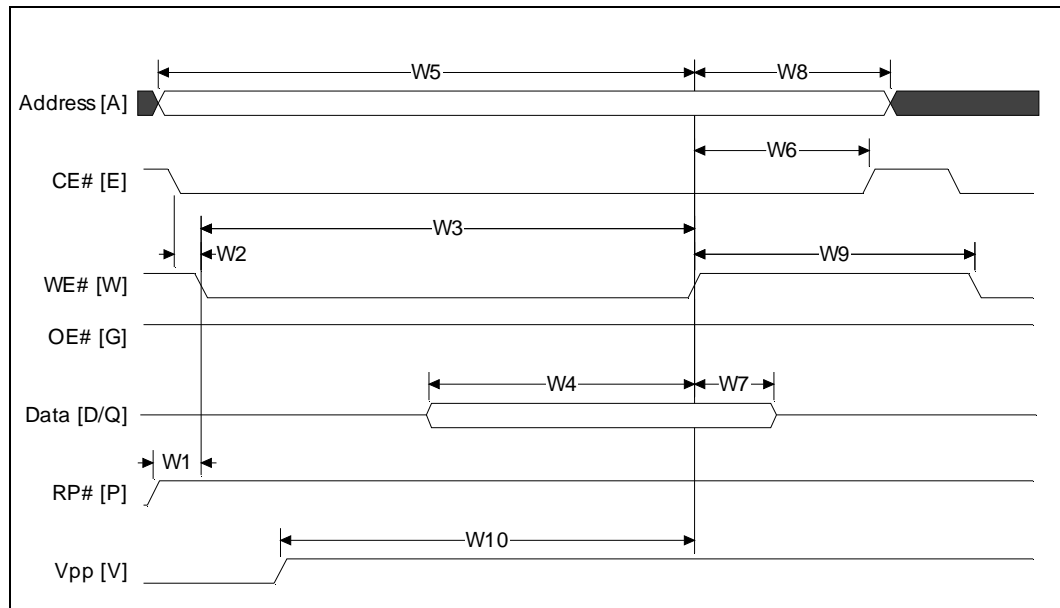
Table 22. Write Operations—64-Mbit Density

#	Symbol	Parameter	Density			64 Mbit	Unit
			Product			80 ns	
			V _{CC}	2.7 V – 3.6 V	Note	Min	
W1	t _{PHWL} / t _{PHEL}	RP# High Recovery to WE# (CE#) Going Low			4,5	150	ns
W2	t _{ELWL} / t _{WLEL}	CE# (WE#) Setup to WE# (CE#) Going Low			4,5	0	ns
W3	t _{WLWH} / t _{ELEH}	WE# (CE#) Pulse Width			1,4,5	60	ns
W4	t _{DVWH} / t _{DVEH}	Data Setup to WE# (CE#) Going High			2,4,5	40	ns
W5	t _{AVWH} / t _{AVEH}	Address Setup to WE# (CE#) Going High			2,4,5	60	ns
W6	t _{WHEH} / t _{EHWH}	CE# (WE#) Hold Time from WE# (CE#) High			4,5	0	ns
W7	t _{WHDX} / t _{EHDX}	Data Hold Time from WE# (CE#) High			2,4,5	0	ns
W8	t _{WHAX} / t _{EHAX}	Address Hold Time from WE# (CE#) High			2,4,5	0	ns
W9	t _{WHWL} / t _{EHEL}	WE# (CE#) Pulse Width High			1,4,5	30	ns
W10	t _{VPWH} / t _{VPEH}	V _{PP} Setup to WE# (CE#) Going High			3,4,5	200	ns
W11	t _{QVVL}	V _{PP} Hold from Valid SRD			3,4	0	ns
W12	t _{BHWH} / t _{BHEH}	WP# Setup to WE# (CE#) Going High			3,4	0	ns
W13	t _{QVBL}	WP# Hold from Valid SRD			3,4	0	ns
W14	t _{WHGL}	WE# High to OE# Going Low			3,4	30	ns

Notes:

- Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). So t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}.
Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). So t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}.
- Refer to [Table 27 “Bus Operations^{\(1\)}”](#) on page 51 for valid A_{IN} or D_{IN}.
- Sampled, but not 100% tested.
- See [Figure 12 “AC Input/Output Reference Waveform”](#) on page 46 for timing measurements and maximum allowable input slew rate.
- See [Figure 11 “Write Operations Waveform”](#) on page 45.

Figure 11. Write Operations Waveform



8.3 Erase and Program Timing

Table 23. Erase and Program Timing

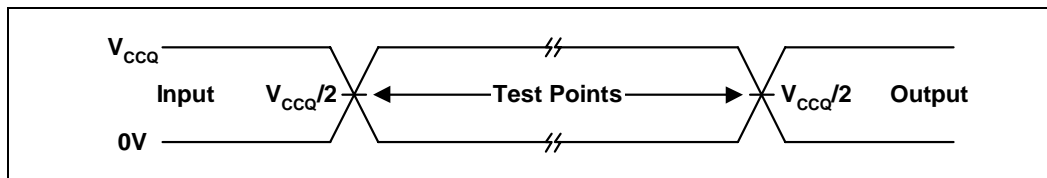
Symbol	Parameter	V _{PP}	1.65 V–3.6 V		11.4 V–12.6 V		Unit
		Note	Typ	Max	Typ	Max	
t _{BWPB}	4-KW Parameter Block Word Program Time	1, 2, 3	0.10	0.30	0.03	0.12	s
t _{BWMB}	32-KW Main Block Word Program Time	1, 2, 3	0.8	2.4	0.24	1	s
t _{WHQV1} / t _{EHQV1}	Word Program Time for 0.13 and 0.18 Micron Product	1, 2, 3	12	200	8	185	μs
	Word Program Time for 0.25 Micron Product	1, 2, 3	22	200	8	185	μs
t _{WHQV2} / t _{EHQV2}	4-KW Parameter Block Erase Time	1, 2, 3	0.5	4	0.4	4	s
t _{WHQV3} / t _{EHQV3}	32-KW Main Block Erase Time	1, 2, 3	1	5	0.6	5	s
t _{WHRH1} / t _{EHRH1}	Program Suspend Latency	1,3	5	10	5	10	μs
t _{WHRH2} / t _{EHRH2}	Erase Suspend Latency	1,3	5	20	5	20	μs

Notes:

1. Typical values measured at T_A = +25 °C and nominal voltages.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.

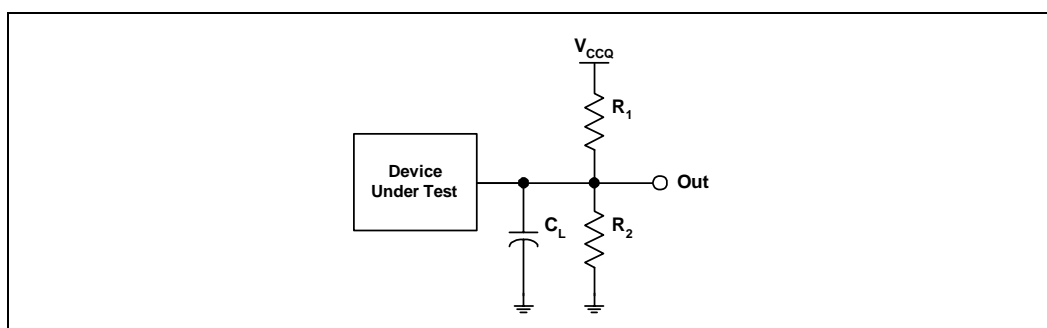
8.4 AC I/O Test Conditions

Figure 12. AC Input/Output Reference Waveform



Note: Input timing begins, and output timing ends, at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5 ns. Worst-case speed conditions are when $V_{CC} = V_{CCMin}$.

Figure 13. Transient Equivalent Testing Load Circuit



Note: See Table 24 for component values.

Table 24. Test Configuration Component Values for Worst Case Speed Conditions

Test Configuration	C_L (pF)	R_1 (k Ω)	R_2 (k Ω)
V_{CCQMin} Standard Test	50	25	25

Note: C_L includes jig capacitance.

8.5 Device Capacitance

$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$

Table 25. Device Capacitance

Symbol	Parameter [§]	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	$V_{IN} = 0.0\text{ V}$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0.0\text{ V}$

[§]Sampled, not 100% tested.

9.0 Power and Reset Specifications

9.1 Power-Up/Down Characteristics

To prevent any condition that might result in a spurious write or erase operation, power-up V_{CC} and V_{CCQ} together. Conversely, V_{CC} and V_{CCQ} must power-down together.

Also power-up V_{PP} with or slightly after V_{CC} . Conversely, V_{PP} must power-down with or slightly before V_{CC} .

If V_{CCQ} and/or V_{PP} are not connected to the V_{CC} supply, then V_{CC} must attain V_{CCMin} before applying V_{CCQ} and V_{PP} . Device inputs must not be driven before supply voltage = V_{CCMin} . Power supply transitions must occur only when $RP\#$ is low.

9.1.1 $RP\#$ Connected to System Reset

Use $RP\#$ during system reset with automated program/erase devices, because the system expects to read from the flash memory when the system exits reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization does not occur, because the flash memory might be providing status information instead of array data. Connecting $RP\#$ to the system CPU $RESET\#$ signal to allow proper CPU/flash initialization after a system reset.

System designers must guard against spurious writes when V_{CC} voltages are above V_{LKO} . Because both $WE\#$ and $CE\#$ must be low for a command write, driving either signal to V_{IH} inhibits writes to the flash memory device. The CUI architecture provides additional protection, because memory contents can be altered only after successful completion of the two-step command sequences. The flash memory device is also disabled until $RP\#$ is brought to V_{IH} , regardless of the state of its control inputs. By holding the device in reset ($RP\#$ connected to system $POWERGOOD$) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

9.1.2 V_{CC} , V_{PP} , and $RP\#$ Transitions

The CUI latches commands as issued by system software, and is not altered by V_{PP} or $CE\#$ transitions or WSM actions. The CUI default state upon power-up, after exit from reset mode or after V_{CC} transitions above V_{LKO} (Lockout voltage), is read-array mode.

After any program or Block-Erase operation is complete (even after V_{PP} transitions down to V_{PPLK}), the CUI must be reset to read-array mode, using the Read Array command if access to the flash-memory array is required.

9.2 Reset Specifications

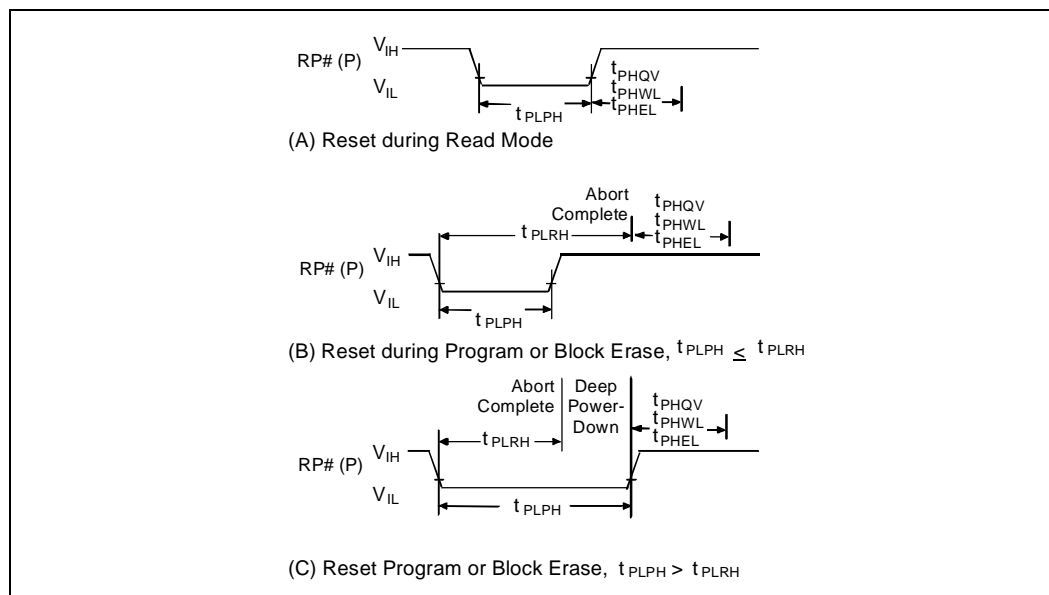
Table 26. Reset Specifications

Symbol	Parameter	V _{CC} 2.7 V – 3.6 V		Unit	Notes
		Min	Max		
t _{PLPH}	RP# Low to Reset during Read (If RP# is tied to V _{CC} , this specification is not applicable)	100		ns	1, 2
t _{PLRH1}	RP# Low to Reset during Block Erase		22	μs	3
t _{PLRH2}	RP# Low to Reset during Program		12	μs	3

Notes:

1. If t_{PLPH} is < 100 ns, the device can still reset, but reset is not guaranteed.
2. If RP# is asserted while a Block Erase or Word Program operation is not executing, the reset completes within 100 ns.
3. Sampled, but not 100% tested.

Figure 14. Deep Power-Down/Reset Operations Waveforms



9.3 Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers must consider the following three supply current issues:

1. Standby current levels (I_{CCS}).
2. Read current levels (I_{CCR}).
3. Transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device output capacitive and inductive loading. Two-line control and proper decoupling capacitor selection suppresses these transient voltage peaks. Each flash device must have a 0.1 μF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high-frequency, inherently low-inductance capacitors must be placed as close as possible to the package leads.

9.4 Power Consumption

Intel® flash memory devices use a tiered approach to power savings that can significantly reduce overall system power consumption. The Automatic Power Savings (APS) feature reduces power consumption when the flash memory device is selected but idle. If CE# is deasserted, the flash memory device enters its standby mode, where current consumption is even lower. The combination of these features can minimize memory power consumption, and therefore minimize overall system power consumption.

9.4.1 Active Power

When CE# is at a logic-low level and RP# is at a logic-high level, the flash memory device is in the active mode. Refer to the DC Characteristic tables for I_{CC} current values. Active power is the largest contributor to overall system power consumption. Minimizing the active current can profoundly affect system power consumption, especially for battery-operated devices.

9.4.2 Automatic Power Savings (APS)

Automatic Power Savings provides low-power operation during read mode. After data is read from the flash memory array and the address lines are quiescent, APS circuitry places the flash memory device in a mode where typical current is comparable to I_{CCS} . The flash memory stays in this static state with outputs valid until a new location is read.

9.4.3 Standby Power

When CE# is at a logic-high level (V_{IH}) and the flash memory device is in read mode, the flash memory is in standby mode. This mode disables much of the device circuitry, and substantially reduces power consumption. Outputs are placed in a high-impedance state independent of the status of the OE# signal. If CE# transitions to a logic-high level during Erase or Program operations, the flash memory device continues to perform the operation and consume corresponding active power until the operation is completed.

System engineers must analyze the breakdown of standby time versus active time and quantify the respective power consumption in each mode for their specific application. This approach provides a more accurate measure of application-specific power and energy requirements.

9.4.4 Deep Power-Down Mode

The deep power-down mode is activated when $RP\# = V_{IL}$ ($GND \pm 0.2 V$). During read modes, $RP\#$ going low deselects the flash memory and places the outputs in a high-impedance state. Recovery from deep power-down mode requires a minimum time of t_{PHQV} (see “AC Read Characteristics” on page 37).

During program or erase modes, $RP\#$ transitioning low aborts the in-progress operation. The memory contents of the address being programmed or the block being erased are no longer valid, because the abort compromises data integrity. During deep power-down, all internal circuits switch to a low-power savings mode ($RP\#$ transitioning to V_{IL} or turning off power to the flash memory device clears the Status Register).

10.0 Operations Overview

Flash memory combines EEPROM functionality with in-circuit electrical program-and-erase capability. The B3 flash memory device family uses a Command User Interface (CUI) and automated algorithms to simplify Program and Erase operations. The CUI allows for 100% CMOS-level control inputs and fixed power supplies during erasure and programming.

When $V_{PP} < V_{PPLK}$, the flash memory device executes only the following commands successfully:

- Read Array
- Read Status Register
- Clear Status Register
- Read Identifier

The flash memory device provides standard EEPROM read, standby, and Output-Disable operations.

Manufacturer identification and device identification data can be accessed through the CUI.

All functions that alter memory contents (program and erase) are accessible through the CUI. The internal Write State Machine (WSM) completely automates Program and Erase operations, while the CUI signals the start of an operation and the Status Register reports status.

The CUI handles the $WE\#$ interface to the data and address latches, and system status requests during WSM operation.

10.1 Bus Operations

The B3 flash memory device performs read, program, and erase in-system operations through the local CPU or microcontroller. All bus cycles to or from the flash memory conform to standard microcontroller bus cycles. Four control pins dictate the data flow in and out of the flash memory device:

- CE#
- OE#
- WE#
- RP#

Table 27 summarizes these bus operations.

Table 27. Bus Operations⁽¹⁾

Mode	Note	RP#	CE#	OE#	WE#	DQ ₀₋₇	DQ ₈₋₁₅
Read (Array, Status, or Identifier)	2-4	V _{IH}	V _{IL}	V _{IL}	V _{IH}	D _{OUT}	D _{OUT}
Output Disable	2	V _{IH}	V _{IL}	V _{IH}	V _{IH}	High Z	High Z
Standby	2	V _{IH}	V _{IH}	X	X	High Z	High Z
Reset	2, 7	V _{IL}	X	X	X	High Z	High Z
Write	2, 5-7	V _{IH}	V _{IL}	V _{IH}	V _{IL}	D _{IN}	D _{IN}

Notes:

1. 8-bit devices use only DQ[0:7].
16-bit devices use DQ[0:15].
2. X must be V_{IL}, V_{IH} for control pins and addresses.
3. See *DC Characteristics* for V_{PPLK}, V_{PP1}, V_{PP2}, V_{PP3}, V_{PP4} voltages.
4. Manufacturer and device codes can also be accessed in read identifier mode (A₁-A₂₁ = 0). See Table 29.
5. Refer to Table 30 for valid D_{IN} during a Write operation.
6. To program or erase the lockable blocks, hold WP# at V_{IH}.
7. RP# must be at GND ± 0.2 V to meet the maximum deep power-down current specified.

10.1.1 Read

The B3 flash memory device provides four read modes:

- read array
- read identifier
- read status
- read query

These modes are accessible independently of the V_{pp} voltage. Issue the appropriate Read Mode command to the CUI to enter the corresponding mode. Upon initial device power-up or after exit from reset, the flash memory device automatically defaults to read-array mode.

CE# and OE# must be driven active to obtain data at the outputs.

- CE# is the device selection control. When active, CE# enables the flash memory device.
- OE# is the data output control, and drives the selected memory data onto the I/O bus.

For all read modes, WE# and RP# must be at V_{IH}. Figure 10 on page 40 illustrates a read cycle.

10.1.2 Output Disable

When OE# is at a logic-high level (V_{IH}), the flash memory device outputs are disabled. Output pins are placed in a high-impedance state.

10.1.3 Standby

Deselecting the flash memory device by bringing CE# to a logic-high level (V_{IH}) places the device in standby mode. Standby mode substantially reduces device power consumption, without any latency for subsequent read accesses. In standby mode, outputs are placed in a high-impedance state independent of OE#. If deselected during Program or Erase operation, the flash memory device continues to consume active power until the Program or Erase operation is complete.

10.1.4 Deep Power-Down / Reset

From read mode, RP# at V_{IL} for time t_{PLPH} does the following:

- Deselects the flash memory.
- Places output drivers in a high-impedance state.
- Turns off all internal circuits.
- After a return from reset, a time t_{PHQV} is required until the initial read-access outputs are valid.
- After a return from reset, a delay (t_{PHWL} or t_{PHEL}) is required before a write can be initiated.

After this wake-up interval, normal operation is restored. The CUI resets to read-array mode, and the Status Register is set to 80H. [Figure 14 “Deep Power-Down/Reset Operations Waveforms” on page 48 \(A\)](#) illustrates this case.

If RP# is taken low for time t_{PLPH} during a Program or Erase operation, the operation aborts. The memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, because the data might be partially erased or written.

The abort process uses the following sequence:

1. When RP# goes low, the flash memory device shuts down the operation in progress, a process that takes time t_{PLRH} to complete.
2. After this time t_{PLRH} , the flash memory device either resets to read-array mode (if RP# has gone high during t_{PLRH} , see [Figure 14 “Deep Power-Down/Reset Operations Waveforms” on page 48 \(B\)](#)), or enters reset mode (if RP# is still logic low after t_{PLRH} , see [Figure 14 “Deep Power-Down/Reset Operations Waveforms” on page 48 \(C\)](#)).
3. In both cases, after returning from an aborted operation, the relevant time t_{PHQV} or t_{PHWL}/t_{PHEL} must elapse before initiating a Read or Write operation, as discussed in the previous paragraph. However, in this case, these delays are referenced to the end of t_{PLRH} rather than when RP# goes high.

As with any automated device, RP# must be asserted during system reset. When the system finishes reset, the processor expects to read from the flash memory. Automated flash memories provide status information when read during program or Block-Erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization cannot occur, because the flash memory might be providing status information instead of array data.

Intel® Flash memories allow proper CPU initialization after a system reset, using the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

10.1.5 Write

A write occurs when both CE# and WE# are low and OE# is high. Commands are written to the Command User Interface (CUI) using standard microprocessor write timings to control flash memory operations. The CUI does not occupy an addressable memory location. The address and data buses are latched on the rising edge of the second WE# or CE# pulse, whichever occurs first.

[Table 30](#) shows the available commands, and [Appendix A](#) provides detailed information about moving between the different modes of operation using CUI commands.

Two commands modify array data:

- Program (40H).
- Erase (20H).

Writing either of these commands to the internal Command User Interface (CUI) initiates a sequence of internally timed functions that culminate in the completion of the requested task (unless that operation is aborted by either RP# being driven to V_{IL} for t_{PLRH} or an appropriate Suspend command).

11.0 Operating Modes

The flash memory device has four read modes:

- read array
- read identifier
- read status
- read query

See [Figure 1 “B3 Architecture Block Diagram” on page 10](#)).

The flash memory device also has two write modes:

- program
- block erase

Three additional modes are available only during suspended operations:

- erase suspend to program
- erase suspend to read
- program suspend to read

[Table 28 “Command Codes and Descriptions” on page 54](#) summarizes the commands used to reach these modes.

[Appendix A, “Write State Machine Current/Next States,”](#) is a comprehensive chart showing the state transitions.

11.1 Read Array

When RP# transitions from V_{IL} (reset) to V_{IH} , the flash memory device defaults to read-array mode and responds to the read-control inputs (CE#, address inputs, and OE#) without any additional CUI commands.

When the flash memory device is in read-array mode, four control signals control data output:

- WE# must be logic high (V_{IH})
- CE# must be logic low (V_{IL})
- OE# must be logic low (V_{IL})
- RP# must be logic high (V_{IH})

In addition, the address of the preferred location must be applied to the address pins. If the flash memory device is not in read-array mode, such as after a Program or Erase operation, the Read Array command (FFH) must be written to the CUI before array reads can occur.

Table 28. Command Codes and Descriptions (Sheet 1 of 2)

Code	Device Mode	Description
00, 01, 60, 2F, C0, 98	Invalid/Reserved	Unassigned commands that must not be used. Intel reserves the right to redefine these codes for future functions.
FF	Read Array	Places the flash memory device in read-array mode, so that array data is output on the data pins.
40	Program Set-Up	A two-cycle command. <ul style="list-style-type: none"> • The first cycle prepares the CUI for a program operation. • The second cycle latches addresses and data information, and initiates the WSM to execute the program algorithm. The flash memory device outputs Status Register data when CE# or OE# is toggled. To read array data, a Read Array command is required after programming. See Section 11.4 .
10	Alternate Program Set-Up	(See 40H/Program Set-Up)
20	Erase Set-Up	Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI does the following: <ol style="list-style-type: none"> 1. Sets both SR.4 and SR.5 of the Status Register to 1. 2. Places the flash memory device into the read-Status Register mode. 3. Waits for another command. See Section 11.5, "Erase Mode" on page 58 .
D0	Erase Confirm Program / Erase Resume	If the previous command was an Erase Set-Up command, then the CUI closes the address and data latches, and begins erasing the block indicated on the address pins. During erase, the flash memory device responds only to the Read Status Register and Erase Suspend commands. The device outputs Status Register data when CE# or OE# is toggled. If a Program or Erase operation was previously suspended, this command resumes that operation.

Table 28. Command Codes and Descriptions (Sheet 2 of 2)

Code	Device Mode	Description
B0	Program / Erase Suspend	<p>Issuing this command suspends the currently executing Program/Erase operation.</p> <p>To indicate when the operation has been successfully suspended, the Status Register sets either the program suspend (SR.2) or erase suspend (SR.6), and sets the WSM status bit (SR.7) to 1 (ready).</p> <p>The WSM continues to idle in the SUSPEND state, regardless of the state of all input-control pins except RP#, which immediately shuts down the WSM and the remainder of the device, if it is driven to V_{IL}.</p> <p>See Section 11.4.1, "Suspending and Resuming Programming" on page 58 and Section 11.4.1, "Suspending and Resuming Programming" on page 58.</p>
70	Read Status Register	<p>This command places the flash memory device into Read-Status Register mode. Reading the device outputs the contents of the Status Register, regardless of the address presented to the device.</p> <p>The flash memory device automatically enters this mode after a Program or Erase operation is initiated. See Section 11.3, "Read Status Register" on page 56.</p>
50	Clear Status Register	<p>The WSM can set the block-lock status (SR.1), V_{PP} status (SR.3), program status (SR.4), and erase status (SR.5) bits in the Status Register to 1. However, the WSM cannot clear these bits to 0. Issuing this command clears these bits to 0.</p>
90	Read Identifier	<p>Places the flash memory device into the intelligent-identifier-read mode, so that reading the device outputs the manufacturer and device codes ($A_0 = 0$ for manufacturer, $A_0 = 1$ for the device; all other address inputs must be 0). See Section 11.2, "Read Identifier" on page 56.</p>

Note: See [Chapter 14.0, "Write State Machine Current/Next States,"](#) for mode transition information.

11.2 Read Identifier

To read the manufacturer and device codes, the flash memory device must be in read-identifier mode, which can be reached by writing the Read Identifier command (90H).

As shown in [Table 29](#), once in read-identifier mode:

- $A_0 = 0$ outputs the manufacturer identification code.
- $A_0 = 1$ outputs the device identifier.

Note: $A_1-A_{21} = 0$.

To return to read-array mode, write the Read-Array command (FFH).

Table 29. Read Identifier Table

Size	Mfr. ID	Device Identifier	
		-T (Top Boot)	-B (Bottom Boot)
28F004B3	0089H	D4H	D5H
28F400B3		8894H	8895H
28F008B3	0089H	D2H	D3H
28F800B3		8892H	8893H
28F016B3		D0H	D1H
28F160B3	0089H	8890H	8891H
28F320B3		8896H	8897H
28F640B3		8898H	8899H

11.3 Read Status Register

The flash memory device Status Register indicates when a Program or Erase operation is complete, and the success or failure of that operation.

- To read the Status Register, issue the Read Status Register (70H) command to the CUI.
This command causes all subsequent Read operations to output data from the Status Register until another command is written to the CUI.
- To return to reading from the array, issue the Read Array (FFH) command.

The Status Register bits are output on DQ_0-DQ_7 . The upper byte, DQ_8-DQ_{15} , outputs 00H during a Read Status Register command.

The contents of the Status Register are latched on the falling edge of $OE\#$ or $CE\#$, which prevents possible Bus errors that might occur if Status Register contents change while being read. $CE\#$ or $OE\#$ must be toggled with each subsequent status read, or the Status Register does not indicate completion of a Program or Erase operation.

When the WSM is active, SR.7 indicates the status of the WSM. The remaining bits in the Status Register indicate whether the WSM was successful in performing the preferred operation (see [Table 31 on page 60](#)).

11.3.1 Clearing the Status Register

The WSM sets status bits 1 through 7 to 1, and clears bits 2, 6, and 7 to 0. However, the WSM cannot clear status bits 1 or 3 through 5 to 0.

Because bits 1, 3, 4, and 5 indicate various error conditions, these bits can be cleared only through the Clear Status Register (50H) command. By allowing the system software to control the resetting of these bits, several operations can be performed (such as cumulatively programming several addresses or erasing multiple blocks in sequence) before reading the Status Register to determine if an error occurred during that series.

Clear the Status Register before beginning another command or sequence.

Note: The Read Array command must be issued before data can be read from the flash memory array.

11.4 Program Mode

Programming is executed using a two-write sequence.

1. The Program Setup command (40H) is written to the CUI.
2. A second write specifies the address and data to program.

The WSM executes a sequence of internally timed events to program preferred bits of the addressed location.

The WSM then verifies that the bits are sufficiently programmed.

Programming the memory changes specific bits within an address location to 0. If users attempt to program 1 instead of 0, the memory cell contents do not change and no error occurs.

The Status Register indicates the programming status: while the program sequence executes, status bit 7 is 0.

To poll the Status Register, toggle either CE# or OE#.

While programming, the only valid commands are:

- Read Status Register
- Program Suspend
- Program Resume

When programming is complete, the program-status bits must be checked.

- If the programming operation was unsuccessful, SR.4 is set, indicating a program failure.
- If SR.3 is set, then V_{PP} was not within acceptable limits, and the WSM did not execute the program command.
- If SR.1 is set, a program operation was attempted on a locked block and the operation aborted.

Clear the Status Register before attempting the next operation. Any CUI instruction can follow after programming is completed; however, to prevent inadvertent Status Register reads, be sure to reset the CUI to read-array mode.

11.4.1 Suspending and Resuming Programming

The Program Suspend command halts the in-progress program operation to read data from another flash memory location.

1. After the programming process starts, writing the Program Suspend command to the CUI requests that the WSM suspend the program sequence (at predetermined points in the program algorithm).
2. The flash memory device continues to output Status Register data after the Program Suspend command is written.
3. Polling SR.7 and SR.2 determines when the program operation has been suspended (both are set to 1).
 t_{WHRHI}/t_{EHRHI} specifies the program- suspend latency.
4. A Read Array command can now be written to the CUI to read data from blocks other than the suspended block.

The only other valid commands while program is suspended are:

- Read Status Register
 - Read Identifier
 - Program Resume
5. After the Program Resume command is written to the flash memory, the WSM continues with the program process, and Status Register bits SR.2 and SR.7 are automatically cleared.
 6. After the Program Resume command is written, the flash memory device automatically outputs Status Register data when read.
See [Appendix B, “Program and Erase Flowcharts.”](#)

Note: V_{pp} must remain at the same V_{pp} level used for program while in program-suspend mode. RP# must also remain at V_{IH} .

11.5 Erase Mode

To erase a block:

1. Write the Erase Set-up and Erase Confirm commands to the CUI, along with an address identifying the block to be erased.
This address is latched internally when the Erase Confirm command is issued.
Block erasure sets all bits within the block to 1. Only one block can be erased at a time.
2. The WSM executes a sequence of internally timed events :
 - a. programs all bits within the block to 0.
 - b. Erases all bits within the block to 1.
 - c. Verifies that all bits within the block are sufficiently erased.

While the erase executes, status bit 7 is 0.

3. When the Status Register indicates that erasure is complete, check the erase-status bit to verify that the Erase operation was successful.
 - If the Erase operation was unsuccessful, SR.5 of the Status Register is set to 1, indicating an erase failure.
 - If V_{PP} was not within acceptable limits after the Erase Confirm command was issued, the WSM does not execute the erase sequence. Instead, SR.5 is set to indicate an Erase error, and SR.3 is set to 1, indicating that the V_{PP} supply voltage was not within acceptable limits.
4. After an Erase operation, clear the Status Register (50H) before attempting the next operation. Any CUI instruction can follow after erasure is completed.
5. To prevent inadvertent status- register reads, place the flash memory device in read-array mode after the erase is complete.

11.5.1 Suspending and Resuming Erase

Because an Erase operation requires on the order of seconds to complete, an Erase Suspend command is provided. Erase Suspend interrupts an erase sequence to read data from—or program data to— another block in memory.

After the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pauses the erase sequence at a predetermined point in the erase algorithm.

Note:

The Status Register will indicate if/when the Erase operation has been suspended.

- A Read Array/Program command can now be written to the CUI, to read data from/ program data to blocks other than the one currently suspended.
- The Program command can subsequently be suspended to read yet another array location.

The only valid commands while Erase is suspended are:

- Erase Resume
- Program
- Read Array
- Read Status Register
- Read Identifier

During erase-suspend mode, to place the flash memory device in a pseudo-standby mode, set CE# to V_{IH} , which reduces active current consumption.

Erase Resume continues the erase sequence when CE# = V_{IL} . As with the end of a standard Erase operation, the Status Register must be read and cleared before the next instruction is issued.

Table 30. Command Bus Definitions (1,4)

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH			
Read Identifier	2	Write	X	90H	Read	IA	ID
Read Status Register		Write	X	70H	Read	X	SRD
Clear Status Register		Write	X	50H			
Program	3	Write	X	40H / 10H	Write	PA	PD
Block Erase/Confirm		Write	X	20H	Write	BA	D0H
Program/Erase Suspend		Write	X	B0H			
Program/Erase Resume		Write	X	D0H			

Notes:

PA: Program Address **PD:** Program Data **BA:** Block Address
IA: Identifier Address **ID:** Identifier Data **SRD:** Status Register Data

- Bus operations are defined in [Table 27](#).
- Following the Intelligent Identifier command, two Read operations access manufacturer and device codes.
 - $A_0 = 0$ for manufacturer code.
 - $A_0 = 1$ for device code.
 - $A_1-A_{21} = 0$.
- Either the 40H or 10H command is valid. The standard is 40H.
- When writing commands to the flash memory device, the upper data bus [DQ₈-DQ₁₅] must be either V_{IL} or V_{IH} , to minimize current draw.

Table 31. Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0

Bits	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check Write State Machine bit first to determine word program or block-erase completion, before checking program or erase-status bits.
SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed	When erase suspend is issued, WSM halts execution and sets both WSMS and ESS bits to 1. ESS bit remains set at 1 until an Erase Resume command is issued.
SR.5 = ERASE STATUS (ES) 1 = Error In Block Erasure 0 = Successful Block Erase	When this bit is set to 1, WSM has applied the maximum number of erase pulses to the block and is still unable to verify successful block erasure.
SR.4 = PROGRAM STATUS (PS) 1 = Error in Word Program 0 = Successful Word Program	When this bit is set to 1, WSM has attempted but failed to program a word.

Bits	NOTES:
SR.3 = V _{PP} STATUS (VPPS) 1 = V _{PP} Low Detect, Operation Abort 0 = V _{PP} OK	The V _{PP} status bit does not continuously indicate the V _{PP} level. The WSM interrogates the V _{PP} level only after the Program or Erase command sequences are entered, and informs the system if V _{PP} has not been switched on. The V _{PP} is also checked before the WSM verifies the operation. The V _{PP} status bit is not guaranteed to report accurate feedback between V _{PP1K} max and V _{PP1} min or between V _{PP1} max and V _{PP4} min.
SR.2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed	When program suspend is issued, WSM halts execution and sets both WSMS and PSS bits to 1. The PSS bit remains set to 1 until a Program Resume command is issued.
SR.1 = BLOCK LOCK STATUS 1 = Program/Erase attempted on locked block; Operation aborted 0 = No operation to locked blocks	If a Program or Erase operation is attempted to one of the locked blocks, the WSM sets this bit. The operation specified is aborted and the flash memory device returns to read status mode.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	This bit is reserved for future use and must be masked out when polling the Status Register.

Note: A Command Sequence Error is indicated when SR.4, SR.5, and SR.7 are set.

12.0 Block Locking

The B3 flash memory device architecture features two hardware-lockable parameter blocks.

12.1 WP# = V_{IL} for Block Locking

The lockable blocks are locked when WP# = V_{IL}; any program or Erase operation to a locked block results in an error, which is reflected in the Status Register:

- For top configuration, the top two parameter blocks are lockable:
 - blocks #133 and #134 for 64 Mbit
 - blocks #69 and #70 for 32 Mbit
 - blocks #37 and #38 for 16 Mbit
 - blocks #21 and #22 for 8 Mbit
 - blocks #13 and #14 for 4 Mbit
- For the bottom configuration, the bottom two parameter blocks are lockable. These are blocks #0 and #1 for 4, 8, 16, 32, and 64 Mbit.

Unlocked blocks can be programmed or erased normally (unless V_{PP} is below V_{PPLK}).

12.2 WP# = V_{IH} for Block Unlocking

WP# = V_{IH} unlocks all lockable blocks. These blocks can now be programmed or erased.

Note: RP# does not override WP# locking for the B3 flash memory device, as in previous Boot Block devices.

- WP# controls all block locking.
- V_{PP} provides protection against spurious writes.

Table 32 defines the write- protection methods.

Table 32. Write-Protection Truth Table for the B3 Device Family

V _{PP}	WP#	RP#	Write Protection Provided
X	X	V _{IL}	All Blocks Locked
V _{IL}	X	V _{IH}	All Blocks Locked
≥ V _{PPLK}	V _{IL}	V _{IH}	Lockable Blocks Locked
≥ V _{PPLK}	V _{IH}	V _{IH}	All Blocks Unlocked

13.0 V_{PP} Program and Erase Voltages

The B3 flash memory device products provide in-system programming and erase at 2.7 V. For customers requiring fast programming in their manufacturing environment, the B3 flash memory device includes an additional low-cost 12-V programming feature.

The 12-V V_{PP} mode enhances programming performance during the short period of time typically found in manufacturing processes. However, this mode is not intended for extended use. 12 V can be applied to V_{PP} during program and Erase operations for a maximum of 1000 cycles on the main blocks, and 2500 cycles on the parameter blocks. V_{PP} can be connected to 12 V for a total of 80 hours maximum.

Warning: Stressing the flash memory device beyond these limits might cause permanent damage.

During Read operations or idle times, V_{PP} can be tied to a 5-V supply. For Program and Erase operations, a 5-V supply is not permitted. The V_{PP} must be supplied with either 2.7 V to 3.6 V or 11.4 V to 12.6 V during Program and Erase operations.

13.1 $V_{PP} = V_{IL}$ for Complete Protection

The V_{PP} programming voltage can be held low for complete write protection of all blocks in the flash memory device. When V_{PP} is below V_{PPLK} , any Program or Erase operation results in an error, prompting the corresponding SR.3 to be set.

14.0 Additional Information

Order Number	Document/Tool
297948	Intel® Advanced Boot Block Flash Memory Family Specification Update
292199	AP-641 Achieving Low Power with the 3 Volt Advanced Boot Block Flash Memory
292200	AP-642 Designing for Upgrade to the 3 Volt Advanced Boot Block Flash Memory
Note 2	3 Volt Advanced Boot Block Algorithms ('C' and assembly) http://developer.intel.com/design/flash/swtools
Contact your Intel Representative	Intel® Flash Data Integrator (IFDI) Software Developer's Kit
297874	IFDI Interactive: Play with Intel® Flash Data Integrator on Your PC

Notes:

1. Call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers must contact their local Intel or distribution sales office.
2. Visit the Intel home page at <http://www.intel.com> or <http://developer.intel.com> for technical documentation and tools.
3. For the most current information about Intel® Advanced Boot Block Flash memory and Intel® Advanced+ Boot Block Flash memory, visit <http://developer.intel.com/design/flash/>

Appendix A Write State Machine Current/Next States

Table 33. Write State Machine (Sheet 1 of 2)

Current State	SR.7	Data When Read	Command Input (and Next State)								
			Read Array (FFH)	Program Setup (10/40H)	Erase Setup (20H)	Erase Confirm (D0H)	Prog/Ers Suspend (B0H)	Prog/Ers Resume (D0H)	Read Status (70H)	Clear Status (50H)	Read Identifier. (90H)
Read Array	"1"	Array	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Read Status	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Read Identifier	"1"	Identifier	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Prog. Setup	"1"	Status	Program (Command Input = Data to be Programmed)								
Program (continue)	"0"	Status	Program (continue)			Prog. Sysop. to Rd. Status	Program (continue)				
Program Suspend to Read Status	"1"	Status	Prog. Susp. to Read Array	Program Suspend to Read Array		Program (continue)	Program Susp. to Read Array	Program (continue)	Prog. Susp. to Read Status	Prog. Susp. to Read Array	Prog. Susp. to Read Identifier
Program Suspend to Read Array	"1"	Array	Prog. Susp. to Read Array	Program Suspend to Read Array		Program (continue)	Program Susp. to Read Array	Program (continue)	Prog. Susp. to Read Status	Prog. Sus. to Read Array	Prog. Susp. to Read Identifier
Prog. Susp. to Read Identifier	"1"	Identifier	Prog. Susp. to Read Array	Program Suspend to Read Array		Program (continue)	Program Susp. to Read Array	Program (continue)	Prog. Susp. to Read Status	Prog. Sus. to Read Array	Prog. Susp. to Read Identifier
Program (complete)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Erase Setup	"1"	Status	Erase Command Error			Erase (continue)	Erase Cant. Error	Erase (continue)	Erase Command Error		
Erase Cant. Error	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Erase (continue)	"0"	Status	Erase (continue)			Erase Sus. to Read Status	Erase (continue)				

Table 33. Write State Machine (Sheet 2 of 2)

Current State	SR.7	Data When Read	Command Input (and Next State)								
			Read Array (FFH)	Program Setup (10/40H)	Erase Setup (20H)	Erase Confirm (D0H)	Prog/Ers Suspend (B0H)	Prog/Ers Resume (D0H)	Read Status (70H)	Clear Status (50H)	Read Identifier. (90H)
Erase Suspend to Status	"1"	Status	Erase Susp. to Read Array	Program Setup	Erase Susp. to Read Array	Erase	Erase Susp. to Read Array	Erase	Erase Susp. to Read Status	Erase Susp. to Read Array	Ers. Susp. to Read Identifier
Erase Susp. to Read Array	"1"	Array	Erase Susp. to Read Array	Program Setup	Erase Susp. to Read Array	Erase	Erase Susp. to Read Array	Erase	Erase Susp. to Read Status	Erase Susp. to Read Array	Ers. Susp. to Read Identifier
Erase Susp. to Read Identifier	"1"	Identifier	Erase Susp. to Read Array	Program Setup	Erase Susp. to Read Array	Erase	Erase Susp. to Read Array	Erase	Erase Susp. to Read Status	Erase Susp. to Read Array	Ers. Susp. to Read Identifier
Erase (complete)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier

Appendix B Program and Erase Flowcharts

Figure 15. Program Flowchart

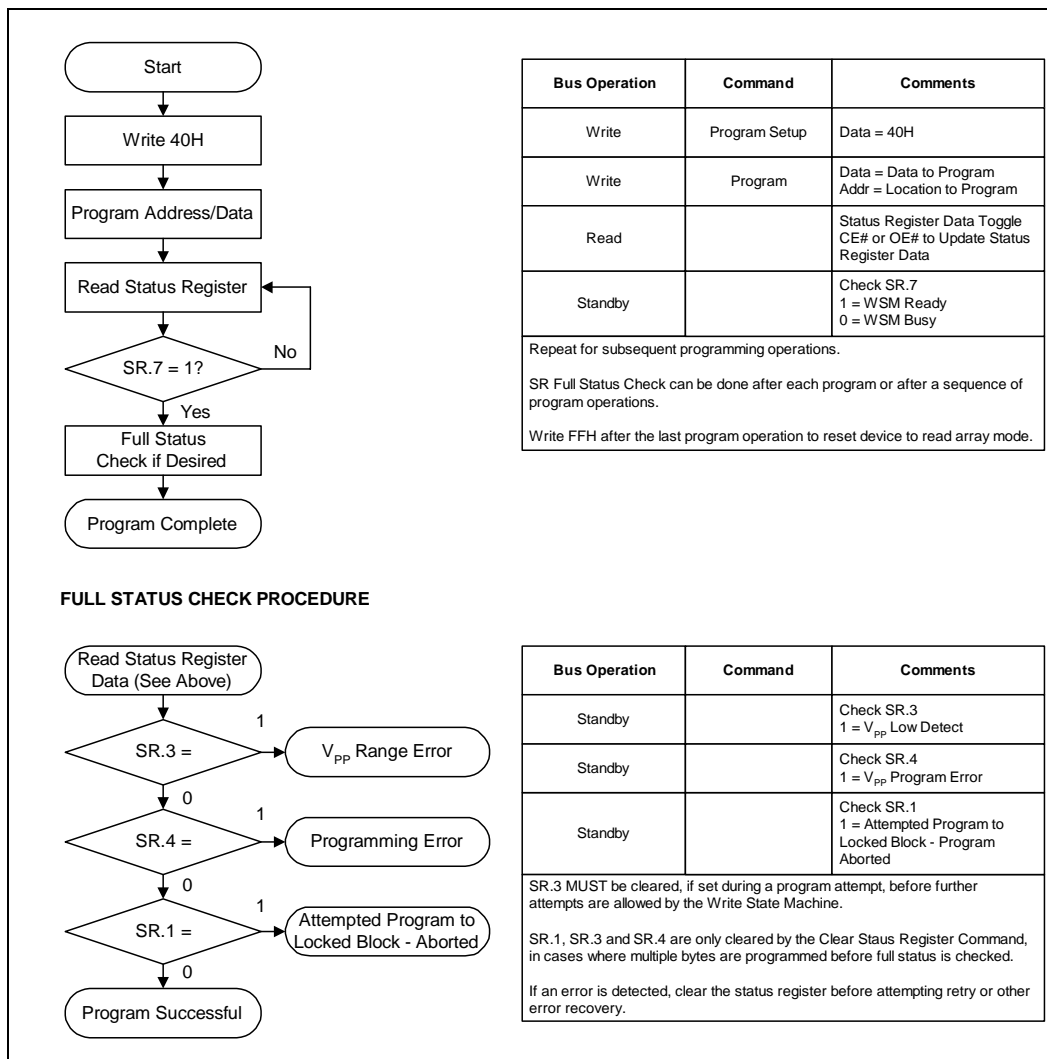


Figure 16. Program Suspend/Resume Flowchart

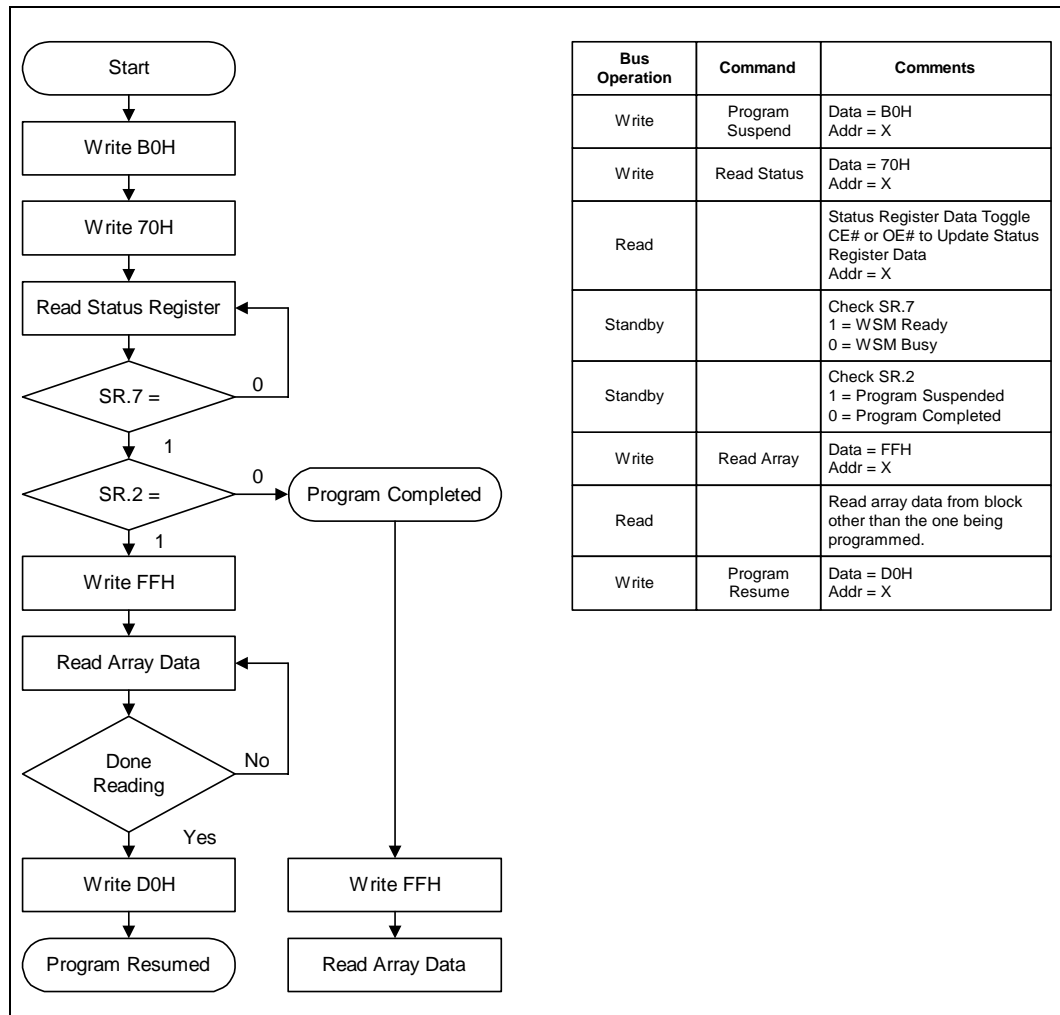


Figure 17. Block Erase Flowchart

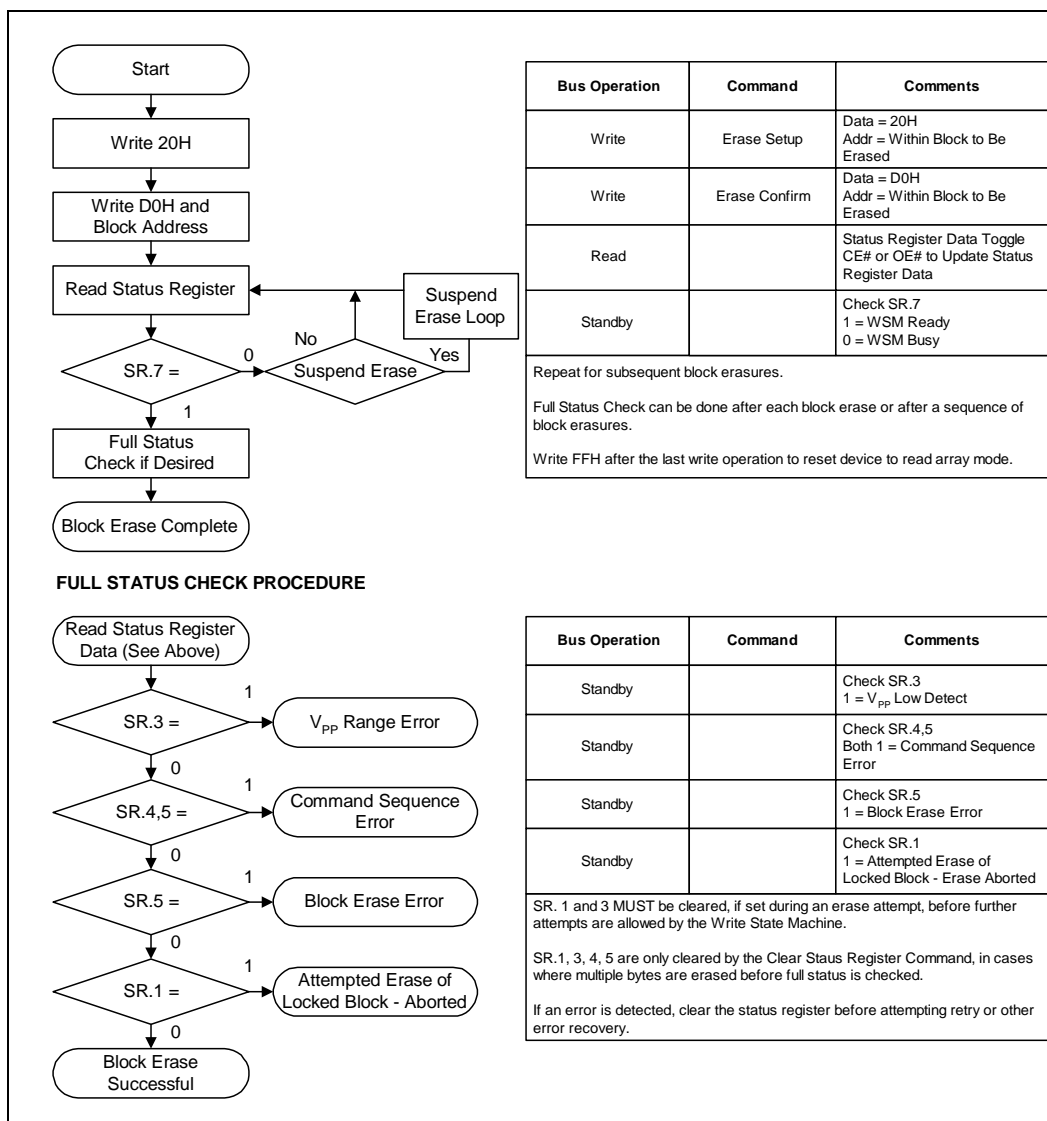
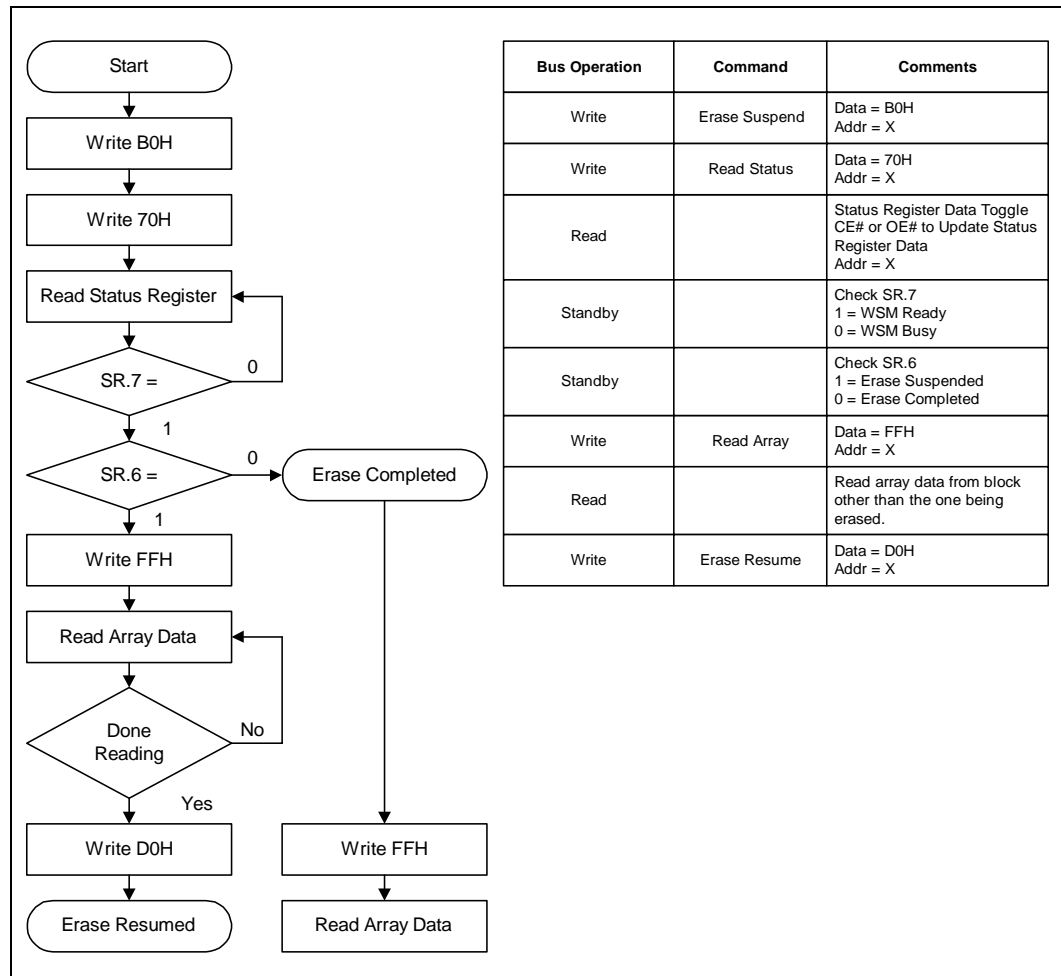


Figure 18. Erase Suspend/Resume Flowchart



Appendix C Ordering Information

Figure 19. Ordering Information

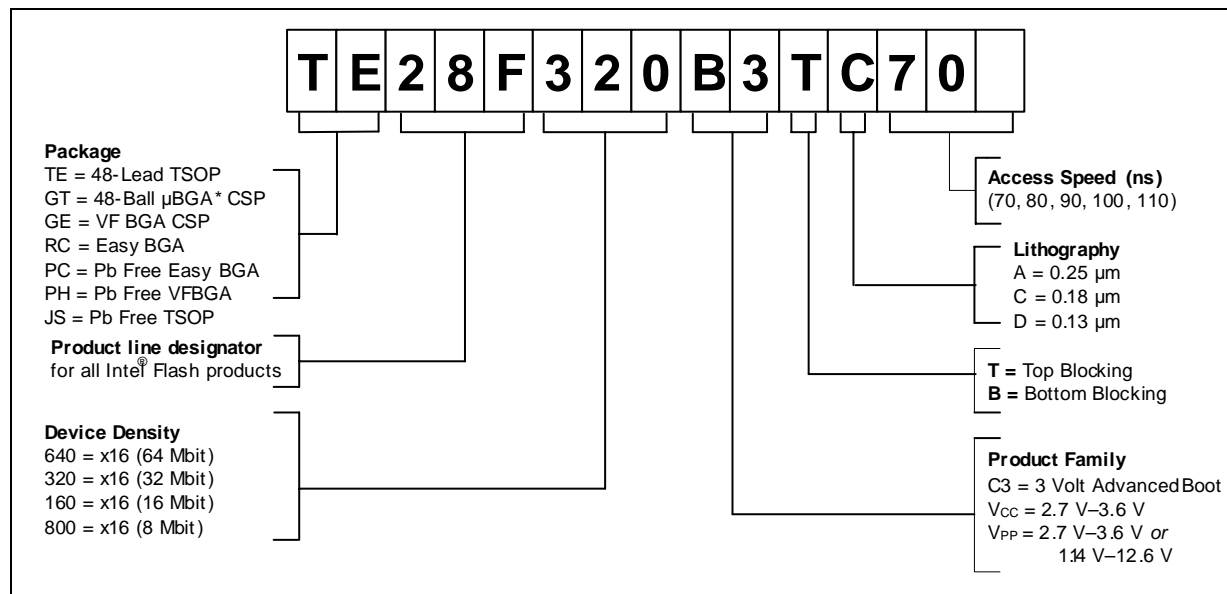


Table 34. Ordering Information: Valid Combinations (Sheet 1 of 2)

	40-Lead TSOP	48-Lead TSOP	48-Ball μ BGA CSP ^(1,2)	48-Ball VF BGA
Ext. Temp. 64 Mbit		TE28F640B3TC80 TE28F640B3BC80		GE28F640B3TC80 GE28F640B3BC80
Ext. Temp. 32 Mbit		TE28F320B3TD70 TE28F320B3BD70 TE28F320B3TC70 TE28F320B3BC70 TE28F320B3TC90 TE28F320B3BC90 TE28F320B3TA100 TE28F320B3BA100 TE28F320B3TA110 TE28F320B3BA110 JS28F320B3TD70 JS28F320B3BD70		GE28F320B3TD70 GE28F320B3BD70 GE28F320B3TC70 GE28F320B3BC70 GE28F320B3TC90 GE28F320B3BC90 PH28F320B3BD70

Table 34. Ordering Information: Valid Combinations (Sheet 2 of 2)

	40-Lead TSOP	48-Lead TSOP	48-Ball μ BGA CSP ^(1,2)	48-Ball VF BGA
Ext. Temp. 16 Mbit	TE28F016B3TA90 TE28F016B3BA90 TE28F016B3TA110 TE28F016B3BA110	TE28F160B3TD70 TE28F160B3BD70 TE28F160B3TC70 TE28F160B3BC70 TE28F160B3TC80 TE28F160B3BC80 TE28F160B3TC90 TE28F160B3BC90 TE28F160B3TA90 TE28F160B3BA90 TE28F160B3TA110 TE28F160B3BA110 JS28F160B3TA70 JS28F160B3BD70	GT28F160B3TA90 ⁽³⁾ GT28F160B3BA90 ⁽³⁾ GT28F160B3TA110 ⁽³⁾ GT28F160B3BA110 ⁽³⁾	GE28F160B3TD70 GE28F160B3BD70 GE28F160B3TC70 GE28F160B3BC70 GE28F160B3TC80 GE28F160B3BC80 GE28F160B3TC90 GE28F160B3BC90 PH28F160B3TD70 PH28F160B3BD70
Ext. Temp. 8 Mbit		TE28F800B3TA90 TE28F800B3BA90 TE28F800B3TA110 TE28F800B3BA110		GE28F800B3TA70 GE28F800B3BA70 GE28F800B3TA90 GE28F800B3BA90

Notes:

- The 48-ball μ BGA package top side mark reads F160B3. This mark is identical for both x8 and x16 products. All product shipping boxes or trays provide the correct information regarding bus architecture. However, once the flash memory devices are removed from the shipping media, differentiating based on the top side mark might be difficult. The device identifier (accessible through the Device ID command: see [Section 11.2, "Read Identifier" on page 56](#) for further details) enables x8 and x16 μ BGA package product differentiation.
- The second line of the 48-ball μ BGA package top side mark specifies assembly codes. For samples only, the first character signifies either:
 - E for engineering samples, or
 - S for silicon daisy-chain samples.
 All other assembly codes without an E or an S as the first character are production units.
- Intel recommends using 18 μ m Intel[®] Advanced Boot Block Products.