VCC1A

CMOS Crystal Oscillator

Features

- Ultra-Low Jitter, Fundamental or 3rd Overtone Crystal Design
- CMOS Output Crystal Oscillator
- Output Frequencies from 32 kHz to 160.000 MHz
- 1.8V, 2.5V, 3.3V, or 5.0V Operation
- Output Disable Feature
- Excellent ±25 ppm Temperature Stability
- –10°C to +70°C, –40°C to +85°C, –40°C to +105°C, –40°C to +125°C, or –55°C to +125°C Operating Temperature
- Small, Industry-Standard 7 mm x 5 mm LDFN Package
- Product is Compliant to RoHS Directive and Fully Compatible with Lead-Free Assembly (Excluding Solder-Dipped _SNPB Option)

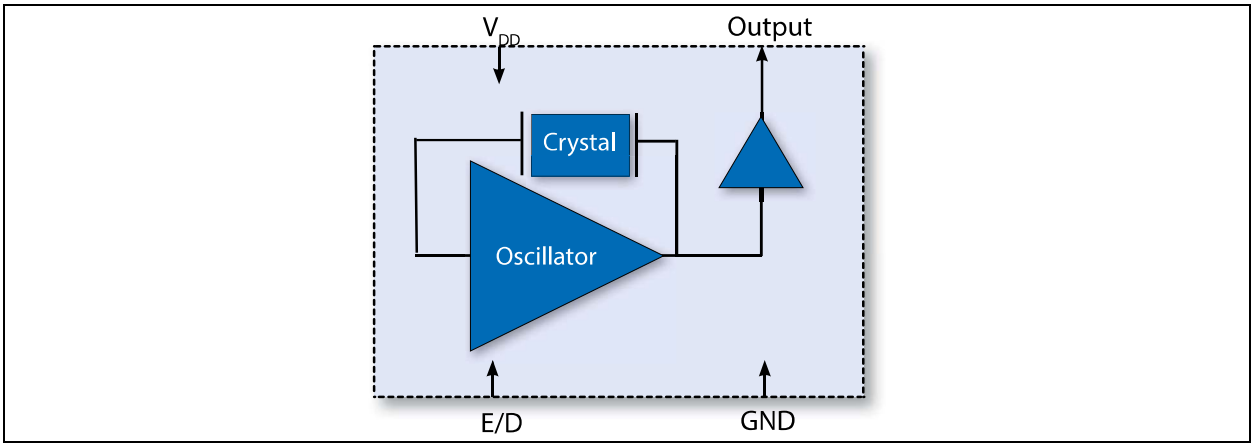
Applications

- SONET/SDH/DWDM
- Ethernet, GE, SyncE
- Storage Area Networking
- Fibre Channel
- Digital Video
- Broadband Access
- Base Stations, Picocells
- Driving A/Ds, D/As, FPGAs
- Test and Measurement
- COTS

General Description

Microchip's VCC1A crystal oscillator (XO) is a quartz stabilized, square wave generator with a CMOS output. The VCC1A uses a fundamental or 3rd overtone crystal that results in very low jitter performance and uses a monolithic IC that improves reliability and reduces cost.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Storage Temperature (T_S) .....–55°C to +125°C
Soldering Temp/Time (T_{LS}) ..... +260°C/30 seconds
ESD Rating, Human Body Model (Note 1) 400V
ESD Rating, Charged Device Model (Note 1) .....2 kV

† Notice: Stresses in excess of the Absolute Maximum Ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods may adversely affect device reliability.

Note 1: Although ESD protection circuitry has been designed into the VCC1A, proper precautions should be taken when handling and mounting. Microchip employs a Human Body Model (HBM) and a Charged Device Model (CDM) for ESD susceptibility testing and design protection evaluation. Human Body Model tested to JES22-A115 conditions. Charged Device Model tested to JESD22-C101 conditions.

ELECTRICAL CHARACTERISTICS, 5V OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply						
Voltage	V_{DD}	4.5	5.0	5.5	V	Note 1
Max. Supply Voltage	—	–0.5	—	7.0	V	—
Max. Voltage E/D	—	–0.5	—	V_{DD} + 0.5	V	—
Current (Note 2)	I_{DD}	—	—	5	mA	≤12 MHz
		—	—	13		12.001 MHz to 20.000 MHz
		—	—	21		20.001 MHz to 65 MHz
		—	—	30		65.001 MHz to 100 MHz
Current, Output Disabled	—	—	—	10	µA	—
Frequency						
Nominal Frequency	f_{NOM}	0.032	—	100.000	MHz	—
Stability (Note 3)	—	—	—	±25	ppm	Ordering Option
		—	—	±32		
		—	—	±50		
		—	—	±100		

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 µF and 0.01 µF.

2: Parameters are tested with the test circuit shown in Figure 1-1. Add ((50 pF – 15 pF) x V_{DD} x f_{OUT} (in MHz) x 0.001) mA for the ±50 pF option

3: Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

4: Duty Cycle is measured as ON Time/Period. See Figure 1-2.

5: Broadband Period Jitter measured using LeCroy Wavemaster 610Zi, 100K samples.

6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.

7: The output is enabled if the Enable/Disable is left open. A 10 kΩ pull-up to V_{DD} is recommended. In disable mode, oscillation stops and the output is high impedance for both Tri-state and Disable mode ordering options.

ELECTRICAL CHARACTERISTICS, 5V OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Outputs						
Output Logic Level High	V_{OH}	0.9 x V_{DD}	—	—	V	Note 2
Output Logic Level Low	V_{OL}	—	—	0.1 x V_{DD}	V	Note 2
Load	I_{OUT}	—	15	—	pF	—
Output Rise/Fall Time (Note 2)	t_R/t_F	—	—	30	ns	<1.024 MHz
		—	—	8	ns	1.024 MHz to 20 MHz
		—	—	5	ns	20.001 MHz to 50.000 MHz
		—	—	3	ns	50.001 MHz to 100 MHz
Output Leakage	I_Z	—	—	±10	µA	Output Disabled
Duty Cycle	—	45	50	55	%	Note 2, Note 4
Period Jitter (Note 5) 100 MHz	Φ_J	—	2.4	—	ps	RMS
		—	23	—	ps	Peak-to-peak
RMS Jitter (Note 6)	Φ_J	—	65	100	fs	12 kHz to 20 MHz
Enable/Disable						
Output Enable/Disable (Note 7)	V_{IH}	0.7 x V_{DD}	—	—	V	Output Enable
	V_{IL}	—	—	0.4	V	Output Disable
Disable Time	t_D	—	—	100	ns	—
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	70	°C	Ordering Option
		–40	—	85	°C	
		–40	—	105	°C	
		–40	—	125	°C	
		–55	—	125	°C	

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 µF and 0.01 µF.

2: Parameters are tested with the test circuit shown in Figure 1-1. Add ((50 pF – 15 pF) x V_{DD} x f_{OUT} (in MHz) x 0.001) mA for the ±50 pF option

3: Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

4: Duty Cycle is measured as ON Time/Period. See Figure 1-2.

5: Broadband Period Jitter measured using LeCroy Wavemaster 610Zi, 100K samples.

6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.

7: The output is enabled if the Enable/Disable is left open. A 10 kΩ pull-up to V_{DD} is recommended. In disable mode, oscillation stops and the output is high impedance for both Tri-state and Disable mode ordering options.

ELECTRICAL CHARACTERISTICS, 3.3V OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply						
Voltage	V_{DD}	2.97	3.3	3.63	V	Note 1
Max. Supply Voltage	—	–0.5	—	7.0	V	—
Max. Voltage E/D	—	–0.5	—	V_{DD} + 0.5	V	—
Current (Note 2)	I_{DD}	—	—	3	mA	≤12 MHz
		—	—	4		12.001 MHz to 20.000 MHz
		—	—	12		20.001 MHz to 65 MHz
		—	—	21		65.001 MHz to 133 MHz
		—	—	27		133.001 MHz to 160 MHz
Current, Output Disabled	—	—	—	10	µA	—
Frequency						
Nominal Frequency	f_{NOM}	0.032	—	160.000	MHz	—
Stability (Note 3)	—	—	—	±25	ppm	Ordering Option
		—	—	±32		
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level High	V_{OH}	0.9 x V_{DD}	—	—	V	Note 2
Output Logic Level Low	V_{OL}	—	—	0.1 x V_{DD}		Note 2
Load	I_{OUT}	—	15	—	pF	—
Output Rise/Fall Time (Note 2)	t_R/t_F	—	—	30	ns	<1.024 MHz
		—	—	8		1.024 MHz to 20 MHz
		—	—	5		20.001 MHz to 50.000 MHz
		—	—	3		50.001 MHz to 160 MHz
Output Leakage	I_Z	—	—	±10	µA	Output Disabled
Duty Cycle	—	45	50	55	%	Note 2, Note 4
Period Jitter (Note 5) 100 MHz	Φ_J	—	2.8	—	ps	RMS
		—	25	—		Peak-to-peak
RMS Jitter (Note 6)	Φ_J	—	76	115	fs	12 kHz to 20 MHz

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 µF and 0.01 µF.

2: Parameters are tested with the test circuit shown in Figure 1-1. Add ((50 pF – 15 pF) x V_{DD} x f_{OUT} (in MHz) x 0.001) mA for the ±50 pF option

3: Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

4: Duty Cycle is measured as ON Time/Period. See Figure 1-2.

5: Broadband Period Jitter measured using LeCroy Wavemaster 610Zi, 100K samples.

6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.

7: The output is enabled if the Enable/Disable is left open. A 10 kΩ pull-up to V_{DD} is recommended. In disable mode, oscillation stops and the output is high impedance for both Tri-state and Disable mode ordering options.

ELECTRICAL CHARACTERISTICS, 3.3V OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Enable/Disable						
Output Enable/Disable (Note 7)	V_{IH}	0.7 x V_{DD}	—	—	V	Output Enable
	V_{IL}	—	—	0.4	V	Output Disable
Disable Time	t_D	—	—	100	ns	—
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	70	°C	Ordering Option
		–40	—	85	°C	
		–40	—	105	°C	
		–40	—	125	°C	
		–55	—	125	°C	

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 µF and 0.01 µF.

2: Parameters are tested with the test circuit shown in Figure 1-1. Add ((50 pF – 15 pF) x V_{DD} x f_{OUT} (in MHz) x 0.001) mA for the ±50 pF option

3: Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

4: Duty Cycle is measured as ON Time/Period. See Figure 1-2.

5: Broadband Period Jitter measured using LeCroy Wavemaster 610Zi, 100K samples.

6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.

7: The output is enabled if the Enable/Disable is left open. A 10 kΩ pull-up to V_{DD} is recommended. In disable mode, oscillation stops and the output is high impedance for both Tri-state and Disable mode ordering options.

ELECTRICAL CHARACTERISTICS, 2.5V OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply						
Voltage	V_{DD}	2.25	2.5	2.75	V	Note 1
Max. Supply Voltage	—	–0.5	—	7.0	V	—
Max. Voltage E/D	—	–0.5	—	V_{DD} + 0.5	V	—
Current (Note 2)	I_{DD}	—	—	2	mA	≤12 MHz
		—	—	3		12.001 MHz to 20 MHz
		—	—	9		20.001 MHz to 65 MHz
		—	—	16		65.001 MHz to 133 MHz
		—	—	23		133.001 MHz to 160 MHz
Current, Output Disabled	—	—	—	10	µA	—
Frequency						
Nominal Frequency	f_{NOM}	0.032	—	160.000	MHz	—
Stability (Note 3)	—	—	—	±25	ppm	Ordering Option
		—	—	±32		
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level High	V_{OH}	0.9 x V_{DD}	—	—	V	Note 2
Output Logic Level Low	V_{OL}	—	—	0.1 x V_{DD}		Note 2
Load	I_{OUT}	—	15	—	pF	—
Output Rise/Fall Time (Note 2)	t_R/t_F	—	—	30	ns	<1.024 MHz
		—	—	8		1.024 MHz to 20 MHz
		—	—	5		20.001 MHz to 50.000 MHz
		—	—	3		50.001 MHz to 160 MHz
Output Leakage	I_Z	—	—	±10	µA	Output Disabled
Duty Cycle	—	45	50	55	%	Note 2, Note 4
Period Jitter (Note 5) 100 MHz	Φ_J	—	2.8	—	ps	RMS
		—	26	—		Peak-to-peak
RMS Jitter (Note 6)	Φ_J	—	97	145	fs	12 kHz to 20 MHz

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 µF and 0.01 µF.

2: Parameters are tested with the test circuit shown in Figure 1-1. Add ((50 pF – 15 pF) x V_{DD} x f_{OUT} (in MHz) x 0.001) mA for the ±50 pF option

3: Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

4: Duty Cycle is measured as ON Time/Period. See Figure 1-2.

5: Broadband Period Jitter measured using LeCroy Wavemaster 610Zi, 100K samples.

6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.

7: The output is enabled if the Enable/Disable is left open. A 10 kΩ pull-up to V_{DD} is recommended. In disable mode, oscillation stops and the output is high impedance for both Tri-state and Disable mode ordering options.

ELECTRICAL CHARACTERISTICS, 2.5V OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Enable/Disable						
Output Enable/Disable (Note 7)	V_{IH}	0.7 x V_{DD}	—	—	V	Output Enable
	V_{IL}	—	—	0.4	V	Output Disable
Disable Time	t_D	—	—	100	ns	—
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	70	°C	Ordering Option
		–40	—	85	°C	
		–40	—	105	°C	
		–40	—	125	°C	
		–55	—	125	°C	

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 µF and 0.01 µF.

2: Parameters are tested with the test circuit shown in Figure 1-1. Add ((50 pF – 15 pF) x V_{DD} x f_{OUT} (in MHz) x 0.001) mA for the ±50 pF option

3: Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

4: Duty Cycle is measured as ON Time/Period. See Figure 1-2.

5: Broadband Period Jitter measured using LeCroy Wavemaster 610Zi, 100K samples.

6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.

7: The output is enabled if the Enable/Disable is left open. A 10 kΩ pull-up to V_{DD} is recommended. In disable mode, oscillation stops and the output is high impedance for both Tri-state and Disable mode ordering options.

ELECTRICAL CHARACTERISTICS, 1.8V OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply						
Voltage	V_{DD}	1.71	1.8	1.89	V	Note 1
Max. Supply Voltage	—	–0.5	—	7.0	V	—
Max. Voltage E/D	—	–0.5	—	V_{DD} + 0.5	V	—
Current (Note 2)	I_{DD}	—	—	2	mA	≤12 MHz
		—	—	3		12.001 MHz to 20 MHz
		—	—	7		20.001 MHz to 65 MHz
		—	—	13		65.001 MHz to 133 MHz
		—	—	19		133.001 MHz to 160 MHz
Current, Output Disabled	—	—	—	10	µA	—
Frequency						
Nominal Frequency	f_{NOM}	0.032	—	160.000	MHz	—
Stability (Note 3)	—	—	—	±25	ppm	Ordering Option
		—	—	±32		
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level High	V_{OH}	0.9 x V_{DD}	—	—	V	Note 2
Output Logic Level Low	V_{OL}	—	—	0.1 x V_{DD}		Note 2
Load	I_{OUT}	—	15	—	pF	—
Output Rise/Fall Time (Note 2)	t_R/t_F	—	—	30	ns	<1.024 MHz
		—	—	8		1.024 MHz to 20 MHz
		—	—	5		20.001 MHz to 50.000 MHz
		—	—	3		50.001 MHz to 100 MHz
Output Leakage	I_Z	—	—	±10	µA	Output Disabled
Duty Cycle	—	45	50	55	%	Note 2, Note 4
Period Jitter (Note 5) 100 MHz	Φ_J	—	3.4	—	ps	RMS
		—	33	—		Peak-to-peak
RMS Jitter (Note 6)	Φ_J	—	212	320	fs	12 kHz to 20 MHz

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 µF and 0.01 µF.

2: Parameters are tested with the test circuit shown in Figure 1-1. Add ((50 pF – 15 pF) x V_{DD} x f_{OUT} (in MHz) x 0.001) mA for the ±50 pF option

3: Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

4: Duty Cycle is measured as ON Time/Period. See Figure 1-2.

5: Broadband Period Jitter measured using LeCroy Wavemaster 610Zi, 100K samples.

6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.

7: The output is enabled if the Enable/Disable is left open. A 10 kΩ pull-up to V_{DD} is recommended. In disable mode, oscillation stops and the output is high impedance for both Tri-state and Disable mode ordering options.

ELECTRICAL CHARACTERISTICS, 1.8V OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Enable/Disable						
Output Enable/Disable (Note 7)	V_{IH}	0.7 x V_{DD}	—	—	V	Output Enable
	V_{IL}	—	—	0.4	V	Output Disable
Disable Time	t_D	—	—	100	ns	—
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	70	°C	Ordering Option
		–40	—	85	°C	
		–40	—	105	°C	
		–40	—	125	°C	
		–55	—	125	°C	

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 µF and 0.01 µF.

2: Parameters are tested with the test circuit shown in Figure 1-1. Add ((50 pF – 15 pF) x V_{DD} x f_{OUT} (in MHz) x 0.001) mA for the ±50 pF option

3: Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

4: Duty Cycle is measured as ON Time/Period. See Figure 1-2.

5: Broadband Period Jitter measured using LeCroy Wavemaster 610Zi, 100K samples.

6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.

7: The output is enabled if the Enable/Disable is left open. A 10 kΩ pull-up to V_{DD} is recommended. In disable mode, oscillation stops and the output is high impedance for both Tri-state and Disable mode ordering options.

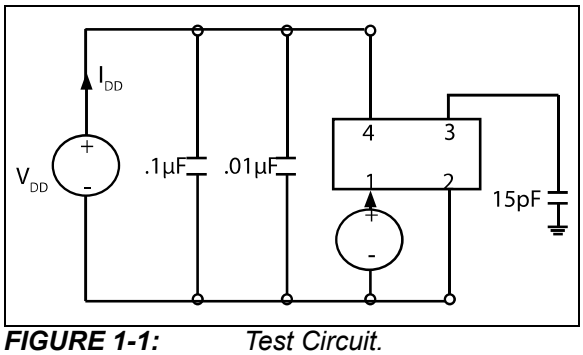


FIGURE 1-1: *Test Circuit.*

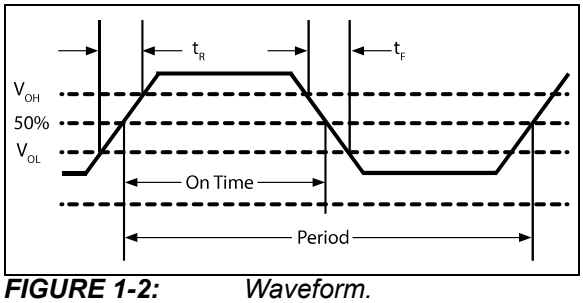


FIGURE 1-2: *Waveform.*

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	E/D	Enable/Disable
2	GND	Case and Electrical Ground
3	Output	Output
4	V_{DD}	Power Supply Voltage

TABLE 2-2: ENABLE/DISABLE FUNCTION

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

3.0 RELIABILITY

Microchip qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VCC1A family is capable of meeting the following qualification tests.

TABLE 3-1: ENVIRONMENTAL COMPLIANCE

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Temperature Cycle	MIL-STD-883, Method 1010
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold (0.3 µm min. to 1.0 µm max.) over Nickel
Contact Pads, _SNPB Option	Tinned using solder alloy SN63Pb37 in accordance with J-STD-006
Weight	178 mg

4.0 IR REFLOW

The VCC1A is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VCC1A device is hermetically sealed, so an aqueous wash is not an issue. Note, devices that have been solder dipped (_SNPB option) will not be Pb-Free.

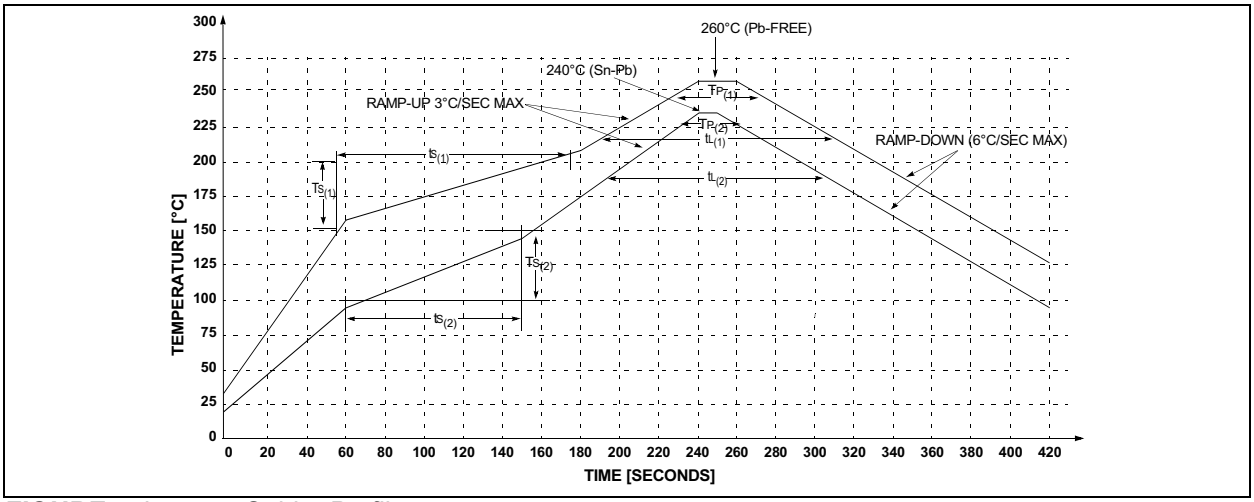


FIGURE 4-1: *Solder Profile.*

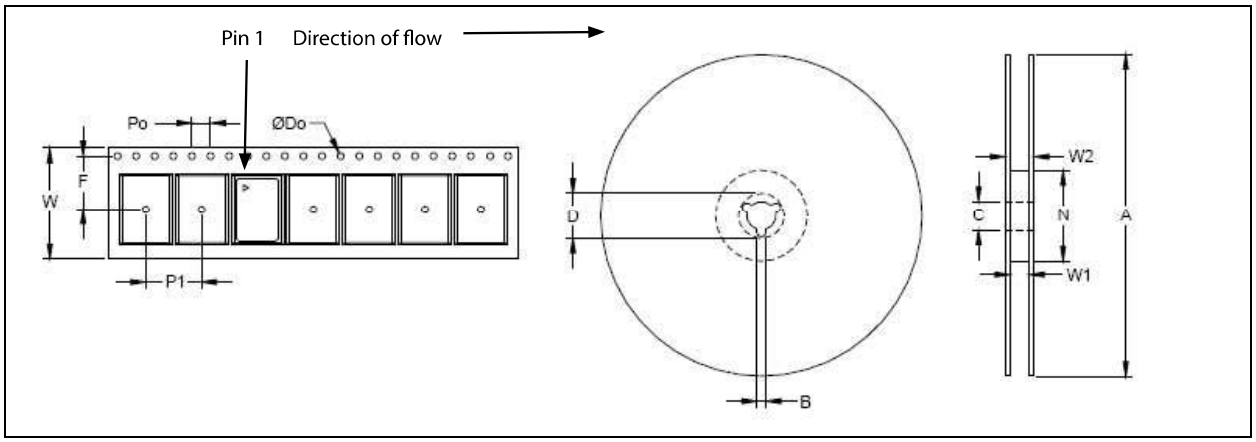
TABLE 4-1: REFLOW PROFILE

Symbol	Minimum	Maximum	Conditions
$T_{S(1)}$	150°C	200°C	Pb-Free
$T_{S(2)}$	100°C	150°C	_SNPB Option
$t_{S(1)}$	60 sec.	180 sec.	Pb-Free
$t_{S(2)}$	60 sec.	120 sec.	_SNPB Option
$t_{l(1)}$	60 sec.	150 sec.	Pb-Free
$t_{l(2)}$	60 sec.	150 sec.	_SNPB Option
$T_{p(1)}$	245°C	260°C	Pb-Free
$T_{p(2)}$	225°C	240°C	_SNPB Option

5.0 TAPE AND REEL

TABLE 5-1: TAPE AND REEL DIMENSIONS

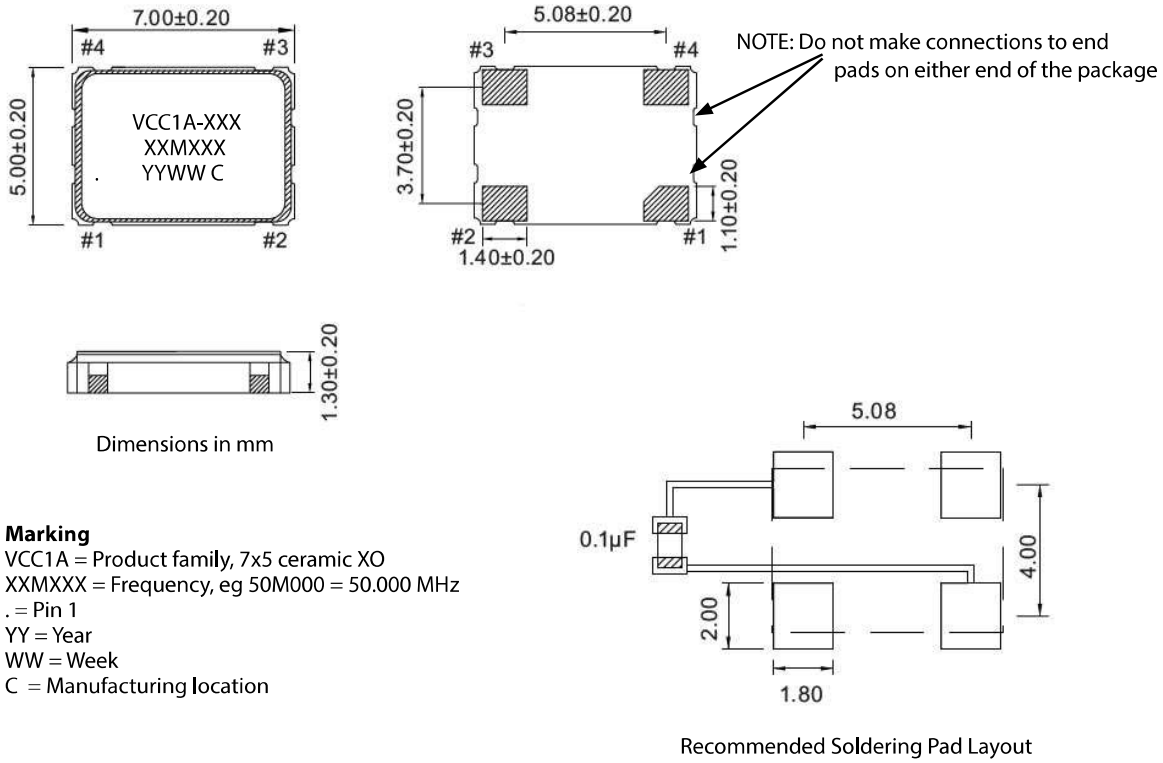
Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	**W**	**F**	**Do**	**Po**	**P1**	**A**	**B**	**C**	**D**	**N**	**W1**	**W2**	**# per Reel**
Tolerance	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Max**	
VCC1A	16	7.5	1.5	4	8	180	2	13	21	60	17	21	1000



6.0 PACKAGING INFORMATION

4-Lead 7.0 mm x 5.0 mm LDFN Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Marking
VCC1A = Product family, 7x5 ceramic XO
XXMXXX = Frequency, eg 50M000 = 50.000 MHz
. = Pin 1
YY = Year
WW = Week
C = Manufacturing location

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2022)

- Converted Vectron document VCC1A to Microchip data sheet template DS20006675A.
- Minor grammatical text changes throughout.

Revision B (March 2023)

- Added two new stability options (P and R) to the Product Identification System section.
- Corrected various values in Table 4-1.
- Added –55°C to +125°C temperature option throughout document.
- Updated frequency capability throughout document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	-X	X	X	-XXMXXXXXXX	XX
Part No.	Power Supply	Electrical Options	Stability	Frequency	Packaging

Device:	VCC1A:	CMOS Crystal Oscillator in a 7.0 mm x 5.0 mm LDFN
Power Supply:	A = 5.0VDC, 15 pF B = 3.3VDC, 15 pF C = 3.0VDC, 15 pF E = 5.0VDC, 50 pF F = 3.3VDC, 50 pF G = 2.5VDC, 15 pF H = 1.8VDC, 15 pF	
Electrical Options:	3 =	Tri-State 45%/55% Duty Cycle (Note 1)
Stability:	A = ±100 ppm over –10°C to +70°C B = ±50 ppm over –10°C to +70°C C = ±100 ppm over –40°C to +85°C D = ±50 ppm over –40°C to +85°C E = ±25 ppm over –10°C to +70°C F = ±25 ppm over –40°C to +85°C K = ±32 ppm over –10°C to +70°C O = ±32 ppm over –40°C to +85°C P = ±100 ppm over –55°C to +125°C R = ±50 ppm over –55°C to +125°C S = ±100 ppm over –40°C to +105°C V = ±100 ppm over –40°C to +125°C	
Frequency:	xxMxxxxxxx=Frequency in MHz xxKxxxxxxx=Frequency in kHz	
Packaging:	TR = 1,000/Reel <blank>= Cut Tape/ non-TR quantities _SNPB= Tin Lead Solder dipped	

Examples:

a) VCC1A-A3F-24M5760000TR:
VCC1A, 5.0VDC, 15 pF, Tri-State 45%/55% Duty Cycle, ±25 ppm over –40°C to +85°C, 24.576 MHz, 1000/Reel

b) VCC1A-G3A-38M4000000:
VCC1A, 2.5VDC, 15 pF, Tri-State 45%/55% Duty Cycle, ±100 ppm over –10°C to +70°C, 38.400 MHz, Cut Tape

c) VCC1A-C3V-65M2500000_SNPB:
VCC1A, 3.0VDC, 15 pF, Tri-State 45%/55% Duty Cycle, ±100 ppm over –40°C to +125°C, 65.250 MHz, Tin Lead Solder Dipped

d) VCC1A-E3R-22M2500000TR:
VCC1A, 5.0VDC, 50 pF, Tri-State 45%/55% Duty Cycle, ±50 ppm over –55°C to +125°C, 22.250 MHz, 1000/Reel

e) VCC1A-F3P-66M6000000:
VCC1A, 3.3VDC, 50 pF, Tri-State 45%/55% Duty Cycle, ±100 ppm over –55°C to +125°C, 66.600 MHz, Cut Tape

f) VCC1A-B3D-42M0000000_SNPB:
VCC1A, 3.3VDC, 15 pF, Tri-State 45%/55% Duty Cycle, ±50 ppm over –40°C to +85°C, 42.000 MHz, Tin Lead Solder Dipped

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note 1: The following codes are not recommended for new designs:
0: No tri-state, 40%/60% duty cycle
1: Tri-state, 40%/60% duty cycle
2: No tri-state, 45%/55% duty cycle
5: Enable, 40%/60% duty cycle
6: Enable, 45%/55% duty cycle.

Please note that not all combination of options are available. Other specifications may be available upon request. 50 pF load option is available at 3.3V and 5.0V, <60 MHz.

TABLE 1: 20 PPM STABILITY ORDERING INFORMATION

VCC1A-105-xxMxxxxxxx = ±20 ppm over –10°C to +70°C, 5.0VDC, 45%/55% duty cycle, 15 pF load.
VCC1A-103-xxMxxxxxxx = ±20 ppm over –10°C to +70°C, 3.3VDC, 45%/55% duty cycle, 15 pF load.
VCC1A-118-xxMxxxxxxx = ±20 ppm over –10°C to +70°C, 2.5VDC, 45%/55% duty cycle, 15 pF load.
VCC1A-119-xxMxxxxxxx = ±20 ppm over –10°C to +70°C, 1.8VDC, 45%/55% duty cycle, 15 pF load.

Note: The Packaging options from the section above also apply to the 20 ppm version listed here.

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
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