



F100125 Hex ECL-to-TTL Translator

General Description

The F100125 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides V_{BB} for single-ended operation or for use in Schmitt trigger applications. All inputs have 50 k Ω pull-down resistors; therefore, the outputs will go LOW when the inputs are left unconnected.

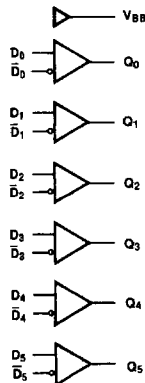
When used in the differential mode, the inputs have a common mode rejection of +1V, making this device tolerant of ground offsets and transients between the signal source and the translator. The V_{EE} and V_{TTL} power may be applied in either order.

Refer to the F100325 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

Logic Symbol

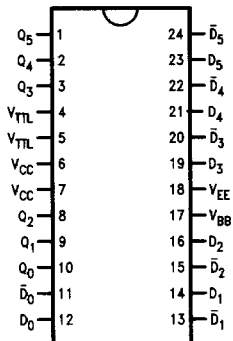


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Pin Names	Description
D_0 - D_5	Data Inputs
\bar{D}_0 - \bar{D}_5	Inverting Data Inputs
Q_0 - Q_5	Data Outputs

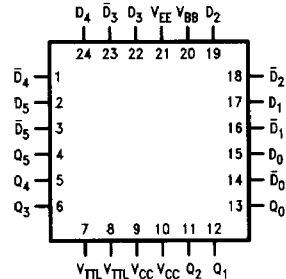
Connection Diagrams

24-Pin DIP



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24-Pin Quad Cerpak



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Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Maximum Junction Temperature (T _J)	+150°C
Case Temperature under Bias (T _C)	0°C to +85°C

V _{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
V _{TTL} Pin Potential to Ground Pin	+6.0V to -0.5V
Input Voltage (DC)	V _{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA
Operating Range (Note 2)	-5.7V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)
V _{BB}	Output Reference Voltage	-1380	-1320	-1260	mV	I _{VBB} = -2.1 mA
V _{IH}	Single-Ended Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V _{BB})
V _{IL}	Single-Ended Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to V _{BB})
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)
V _{BB}	Output Reference Voltage	-1396	-1320	-1244	mV	I _{VBB} = -2.1 mA
V _{IH}	Single-Ended Input HIGH Voltage	-1150		-880	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V _{BB})
V _{IL}	Single-Ended Input LOW Voltage	-1810		-1490	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to V _{BB})
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)
V _{BB}	Output Reference Voltage	-1396	-1320	-1244	mV	I _{VBB} = -2.1 mA
V _{IH}	Single-Ended Input HIGH Voltage	-1150		-880	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V _{BB})
V _{IL}	Single-Ended Input LOW Voltage	-1810		-1490	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to V _{BB})
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.5			V	$I_{OH} = -2.0$ mA
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20$ mA
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage			1.0	V	Permissible $\pm V_{CM}$ with Respect to V_{BB}
I_{IH}	Input HIGH Current			350	μA	$V_{IN} = V_{IH} (Max)$, $D_0-D_5 = V_{BB}$, $\bar{D}_0-\bar{D}_5 = V_{IL} (Min)$
I_{IL}	Input LOW Current	0.5			μA	$V_{IN} = V_{IL} (Min)$, $D_0-D_5 = V_{BB}$
I_{OS}	Output Short-Circuit Current	-100		-40	mA	$V_{OUT} = GND^*$
I_{EE}	V_{EE} Power Supply Current	-85	-60	-40	mA	$D_0-D_5 = V_{BB}$
I_{TTL}	V_{TTL} Power Supply Current		75	115	mA	$D_0-D_5 = V_{BB}$

*Test one output at a time.

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.50	0.90	3.70	1.00	4.00	ns	Figures 1 and 2

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.30	0.90	3.50	1.00	3.80	ns	Figures 1 and 2

Truth Table

Inputs		Outputs
D_n	\bar{D}_n	Q_n
L	H	L
H	L	H
L	L	U
H	H	U
Open	Open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
U = Undefined

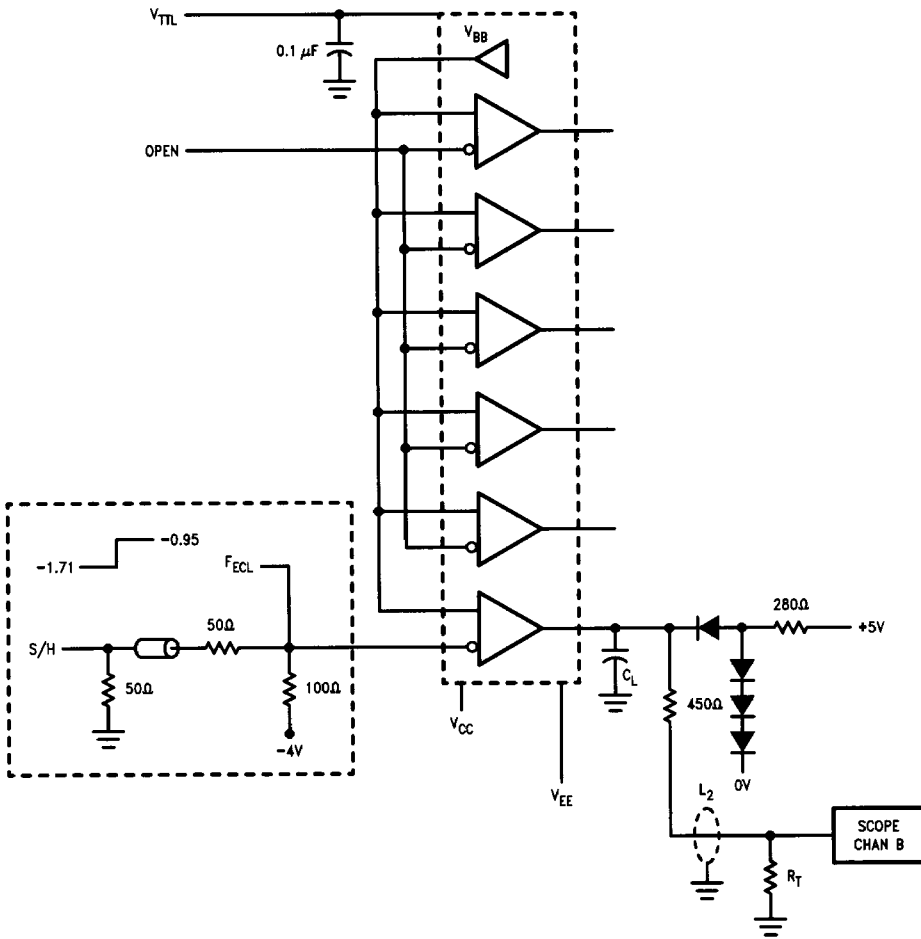


FIGURE 1. AC Test Circuit

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Notes:

- $V_{CC} = 0V, V_{EE} = -4.5V, V_{TTL} = +5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
- All unused outputs are loaded with 500Ω to GND
- C_L = Fixture and stray capacitance = 15 pF

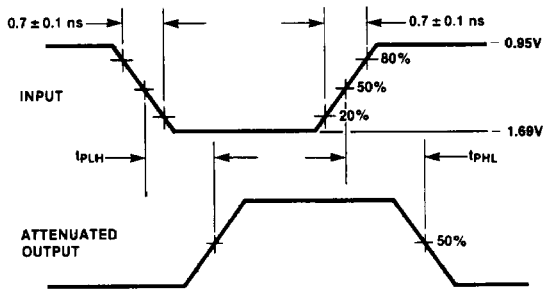


FIGURE 2. Propagation Delay Times

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