Freescale Semiconductor
Data Sheet: Advance Information

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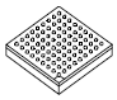
P1010

P1010 QorIQ Integrated Processor Hardware Specifications



TePBGA1-425
19 mm x 19 mm

The following list provides an overview of the P1010 feature set:

- High-performance 32-bit Book E-enhanced core based on the Power Architecture technology:
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache
  - 400- to 1000-MHz clock frequency
- 256-Kbyte L2 cache with ECC. Also configurable as SRAM and stashing memory
- Secure boot capability
- Three enhanced three-speed Ethernet controllers (eTSECs)
  - 10/100/1000 Mbps support
  - TCP/IP acceleration, quality of service, and classification capabilities
  - IEEE Std 1588™ support
  - RGMII, SGMII
  - eTSEC1 supports both RGMII/SGMII interfaces and eTSEC2, eTSEC3 support SGMII interface
- High-speed interfaces supporting the following multiplexing options:
  - Two PCI Express 1.1 interfaces
  - Two SATA Revision 2.0 interfaces
  - Six lanes of high-speed serial interfaces to be shared between PCI Express, SATA, and SGMII
- High-speed USB controller (USB 2.0)
  - Host and device support
  - On-chip USB 2.0 high-speed PHY
  - Enhanced host controller interface (EHCI)
  - ULPI interface
- Enhanced secure digital host controller (SD/MMC)
- Enhanced serial peripheral interface (eSPI)
- Integrated security engine (ULE CAAM)
  - Protocol support includes DES, AES, RNG, CRC, MDE, PKE, SHA, and MD5.
- DDR3/DDR3L SDRAM memory controller supports 32-bit without ECC and 16-bit with ECC
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- One 4-channel DMA controller
- Two I^2C interfaces
- Four UART interfaces
- Two FlexCAN (version 2.0b) interfaces
- Integrated Flash controller (IFC)
- TDM
- 16 general-purpose I/O signals
- Operating temperature (Ta - T_j) range: 0–105° C (standard) and –40° C to 105° C (extended)
- 19 × 19 mm 425-ball wirebond TePBGA-1 package with 0.8 mm pitch

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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This figure shows the major functional units within the P1010.

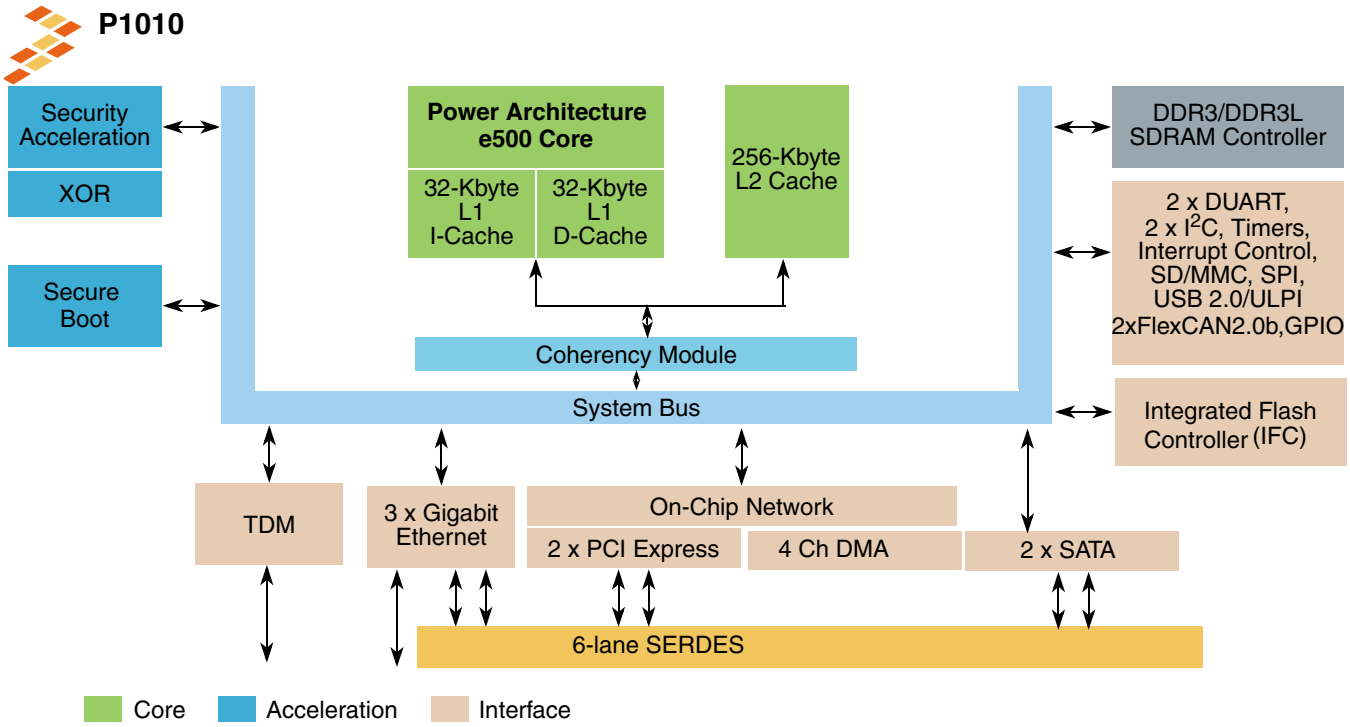
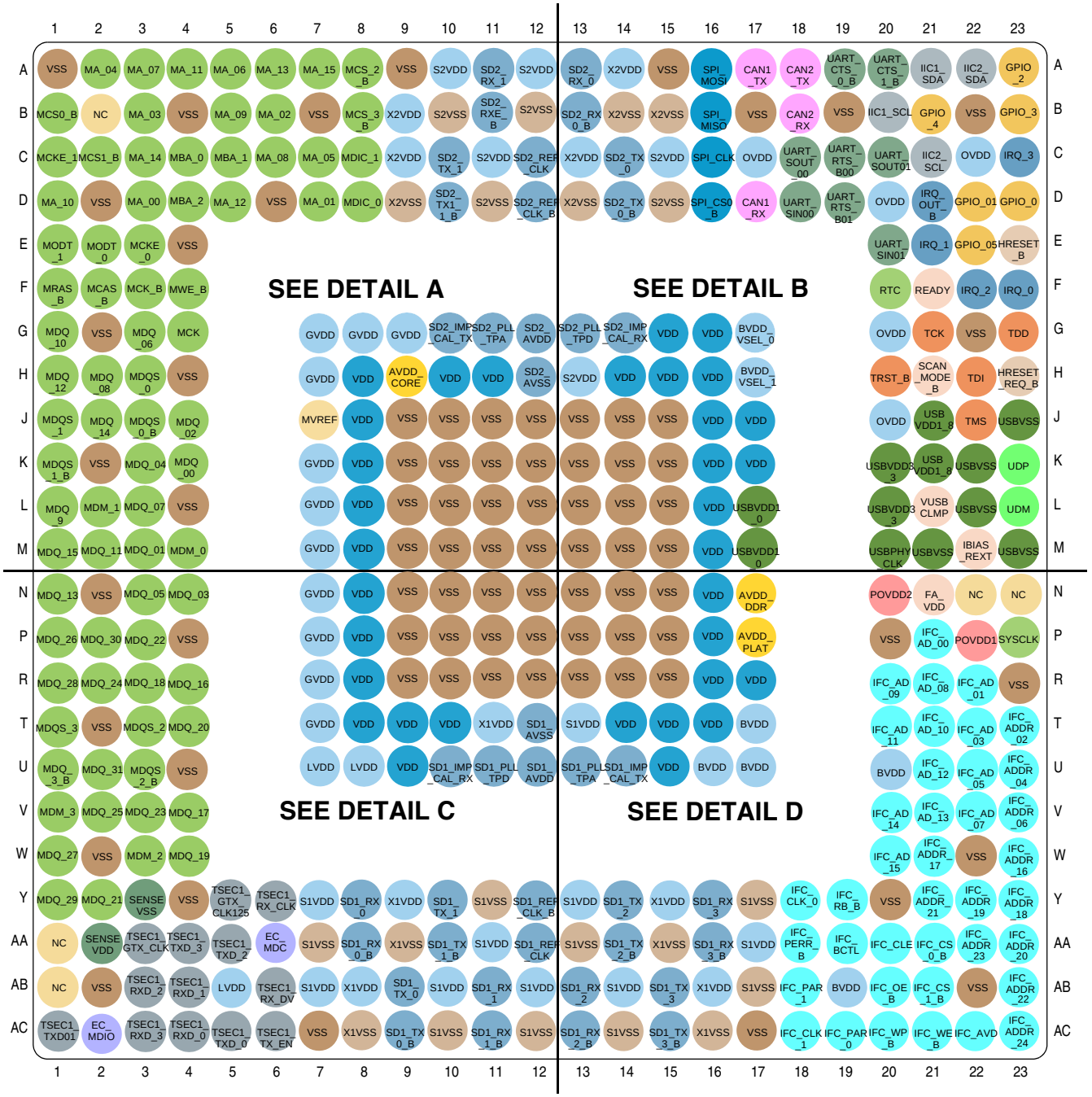


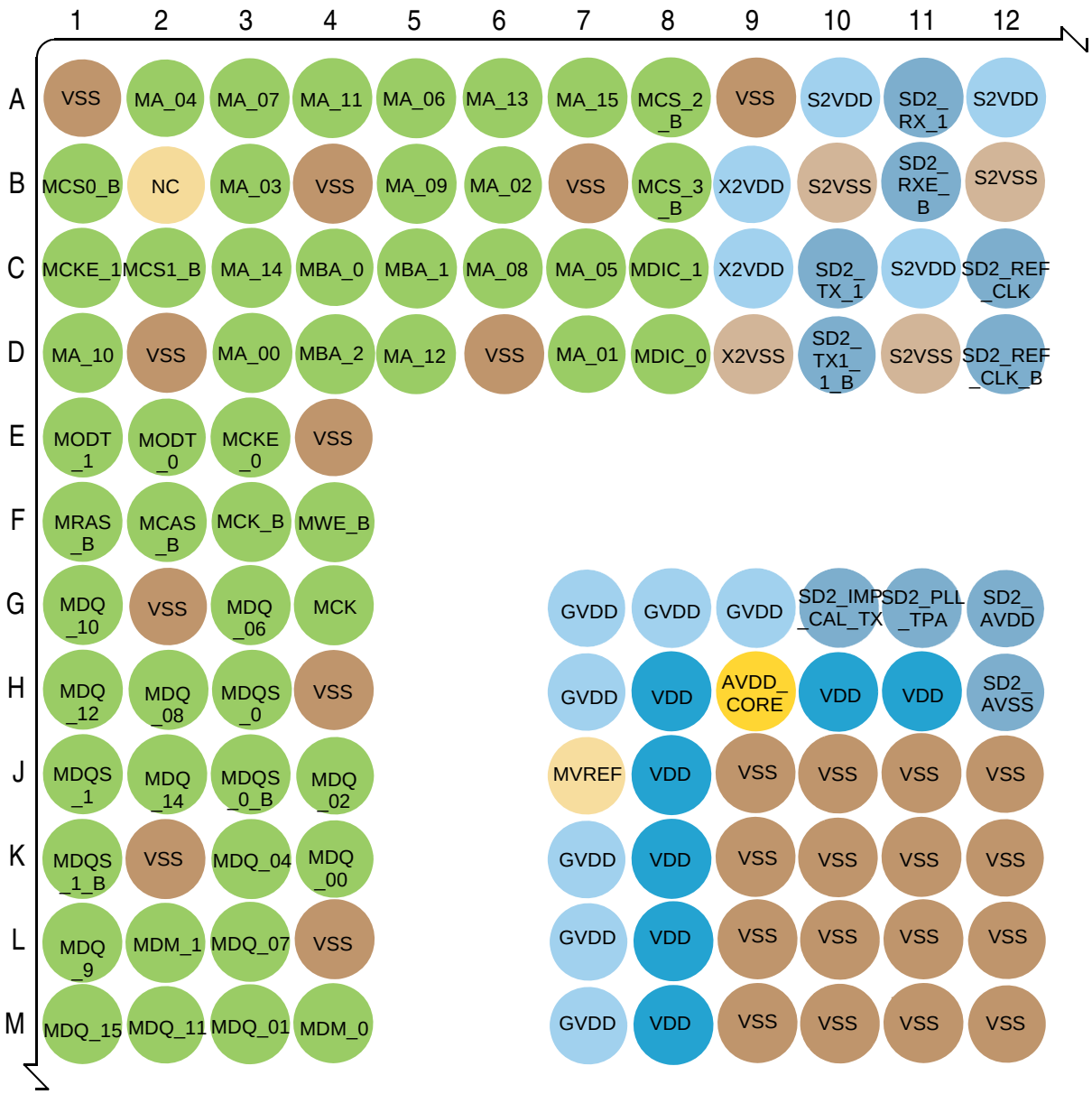
Figure 1. P1010 block diagram

1 Pin assignments and reset states

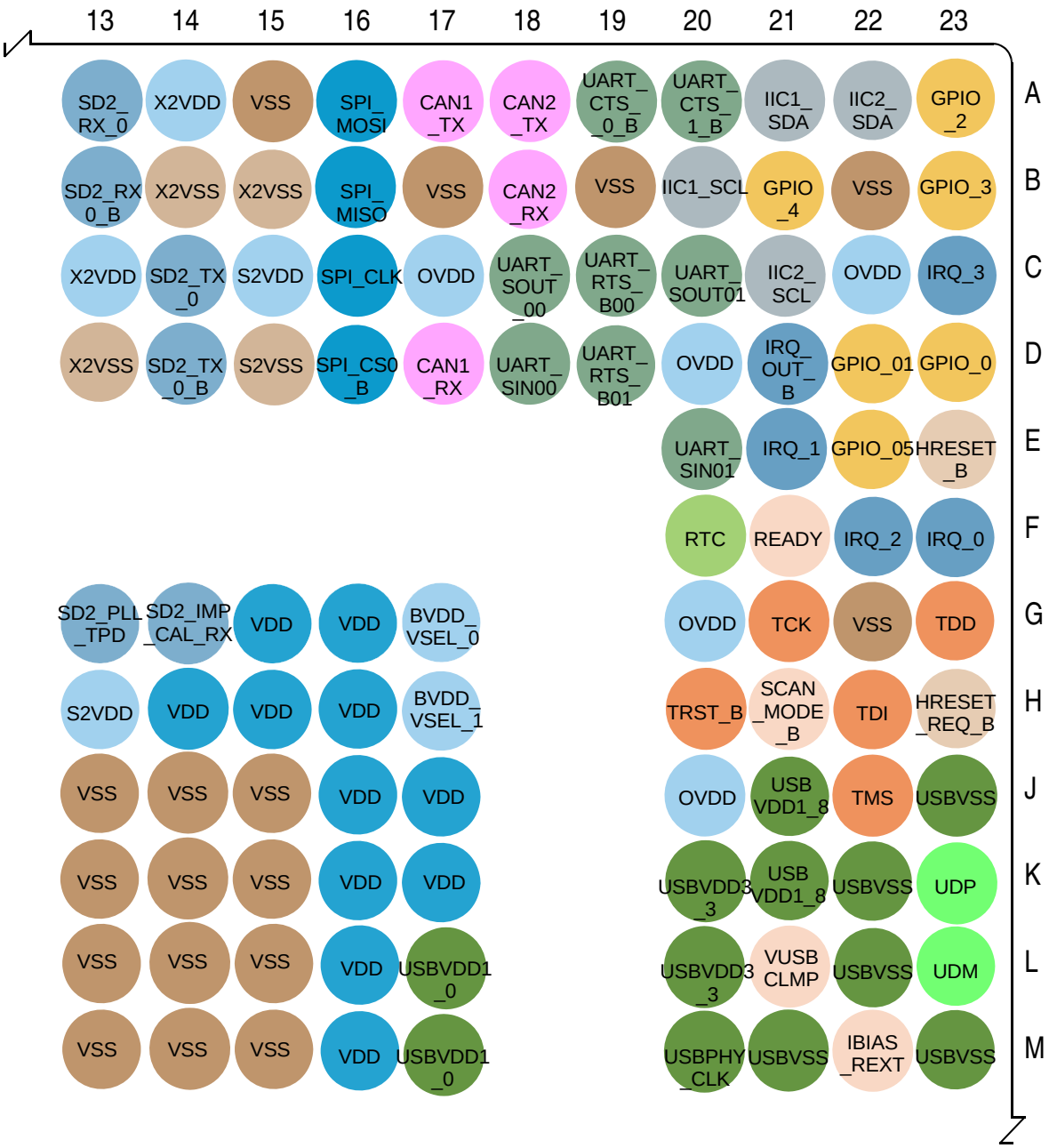
1.1 Ball layout diagrams



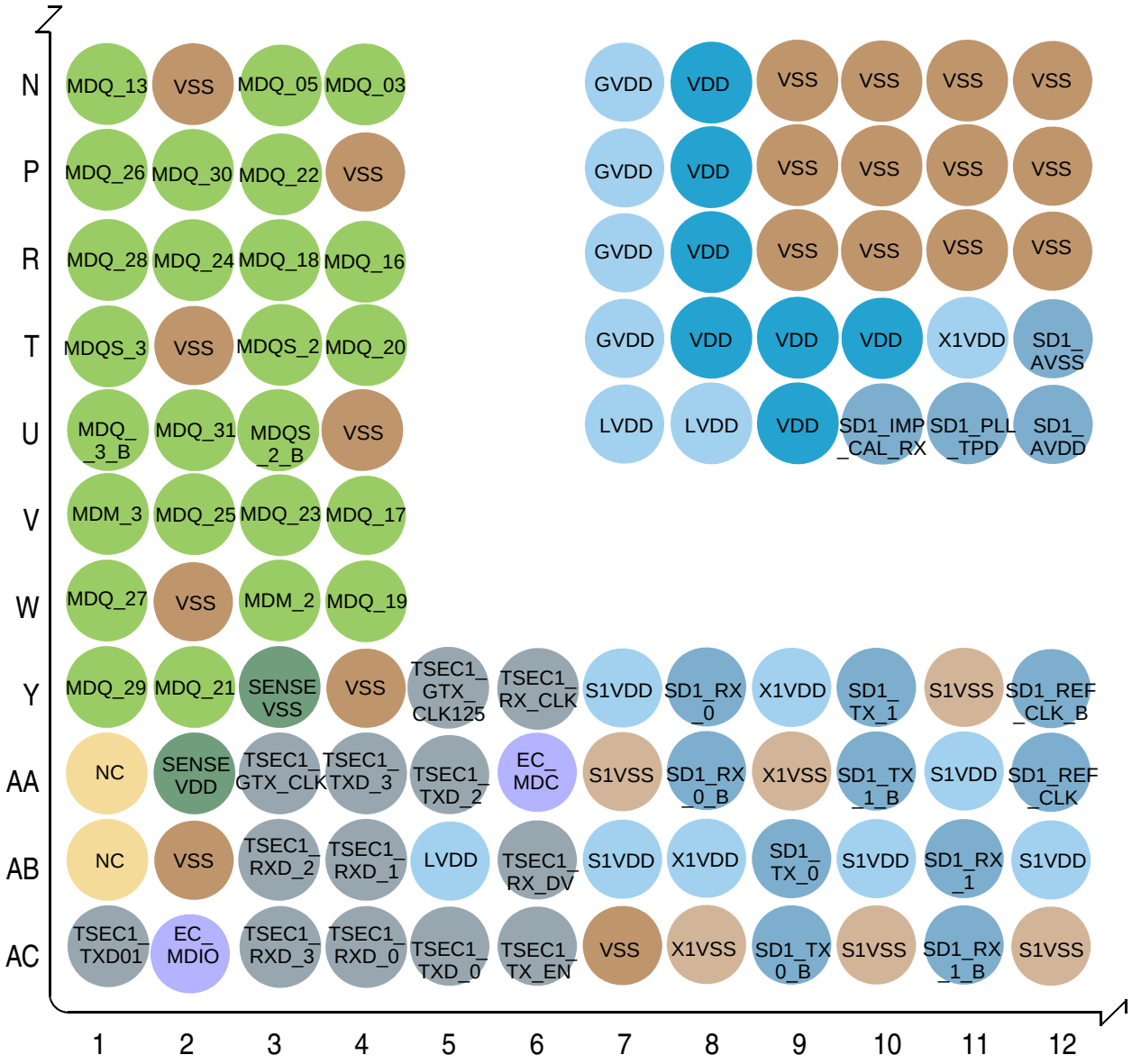
DETAIL A


1 2 3 4 5 6 7 8 9 10 11 12
A VSS MA_04 MA_07 MA_11 MA_06 MA_13 MA_15 MCS_2_B VSS S2VDD SD2_RX_1 S2VDD
B MCS0_B NC MA_03 VSS MA_09 MA_02 VSS MCS_3_B X2VDD S2VSS SD2_RXE_B S2VSS
C MCKE_1 MCS1_B MA_14 MBA_0 MBA_1 MA_08 MA_05 MDIC_1 X2VDD SD2_TX_1 S2VDD SD2_REF_CLK
D MA_10 VSS MA_00 MBA_2 MA_12 VSS MA_01 MDIC_0 X2VSS SD2_TX1_1_B S2VSS SD2_REF_CLK_B
E MODT_1 MODT_0 MCKE_0 VSS
F MRAS_B MCAS_B MCK_B MWE_B
G MDQ_10 VSS MDQ_06 MCK GVDD GVDD GVDD SD2_IMP_CAL_TX SD2_PLL_TPA SD2_AVDD
H MDQ_12 MDQ_08 MDQS_0 VSS GVDD VDD AVDD_CORE VDD VDD SD2_AVSS
J MDQS_1 MDQ_14 MDQS_0_B MDQ_02 MVREF VDD VSS VSS VSS VSS
K MDQS_1_B VSS MDQ_04 MDQ_00 GVDD VDD VSS VSS VSS VSS
L MDQ_9 MDM_1 MDQ_07 VSS GVDD VDD VSS VSS VSS VSS
M MDQ_15 MDQ_11 MDQ_01 MDM_0 GVDD VDD VSS VSS VSS VSS

DETAIL B


13 14 15 16 17 18 19 20 21 22 23
A
SD2_RX_0
X2VDD
VSS
SPI_MOSI
CAN1_TX
CAN2_TX
UART_CTS_0_B
UART_CTS_1_B
IIC1_SDA
IIC2_SDA
GPIO_2
B
SD2_RX0_B
X2VSS
X2VSS
SPI_MISO
VSS
CAN2_RX
VSS
IIC1_SCL
GPIO_4
VSS
GPIO_3
C
X2VDD
SD2_TX_0
S2VDD
SPI_CLK
OVDD
UART_SOUT_00
UART_RTS_B00
UART_SOUT01
IIC2_SCL
OVDD
IRQ_3
D
X2VSS
SD2_TX_0_B
S2VSS
SPI_CS0_B
CAN1_RX
UART_SIN00
UART_RTS_B01
OVDD
IRQ_OUT_B
GPIO_01
GPIO_0
E
UART_SIN01
IRQ_1
GPIO_05
HRESET_B
F
RTC
READY
IRQ_2
IRQ_0
G
SD2_PLL_TPD
SD2_IMP_CAL_RX
VDD
VDD
BVDD_VSEL_0
OVDD
TCK
VSS
TDD
H
S2VDD
VDD
VDD
VDD
BVDD_VSEL_1
TRST_B
SCAN_MODE_B
TDI
HRESET_REQ_B
J
VSS
VSS
VSS
VDD
VDD
OVDD
USB VDD1_8
TMS
USBVSS
K
VSS
VSS
VSS
VDD
VDD
USBVDD3_3
USB VDD1_8
USBVSS
UDP
L
VSS
VSS
VSS
VDD
USBVDD1_0
USBVDD3_3
VUSB CLMP
USBVSS
UDM
M
VSS
VSS
VSS
VDD
USBVDD1_0
USBPHY_CLK
USBVSS
IBIAS_REXT
USBVSS

DETAIL C


N
P
R
T
U
V
W
Y
AA
AB
AC
1
2
3
4
5
6
7
8
9
10
11
12
MDQ_13 VSS MDQ_05 MDQ_03
MDQ_26 MDQ_30 MDQ_22 VSS
MDQ_28 MDQ_24 MDQ_18 MDQ_16
MDQS_3 VSS MDQS_2 MDQ_20
MDQ_ _3_B MDQ_31 MDQS _2_B VSS
MDM_3 MDQ_25 MDQ_23 MDQ_17
MDQ_27 VSS MDM_2 MDQ_19
MDQ_29 MDQ_21 SENSE VSS VSS TSEC1_ GTX_ CLK125 TSEC1_ RX_CLK S1VDD SD1_RX _0 X1VDD SD1_ TX_1 S1VSS SD1_REF _CLK_B
NC SENSE VDD TSEC1_ GTX_CLK TSEC1_ TXD_3 TSEC1_ TXD_2 EC_ MDC S1VSS SD1_RX _0_B X1VSS SD1_TX _1_B S1VDD SD1_REF _CLK
NC VSS TSEC1_ RXD_2 TSEC1_ RXD_1 LVDD TSEC1_ RX_DV S1VDD X1VDD SD1_ TX_0 S1VDD SD1_RX _1 S1VDD
TSEC1_ TXD01 EC_ MDIO TSEC1_ RXD_3 TSEC1_ RXD_0 TSEC1_ TXD_0 TSEC1_ TX_EN VSS X1VSS SD1_TX 0_B S1VSS SD1_RX _1_B S1VSS
GVDD VDD VSS VSS VSS VSS
GVDD VDD VSS VSS VSS VSS
GVDD VDD VSS VSS VSS VSS
GVDD VDD VDD VDD X1VDD SD1_ AVSS
LVDD LVDD VDD SD1_IMP _CAL_RX SD1_PLL _TPD SD1_ AVDD

DETAIL D

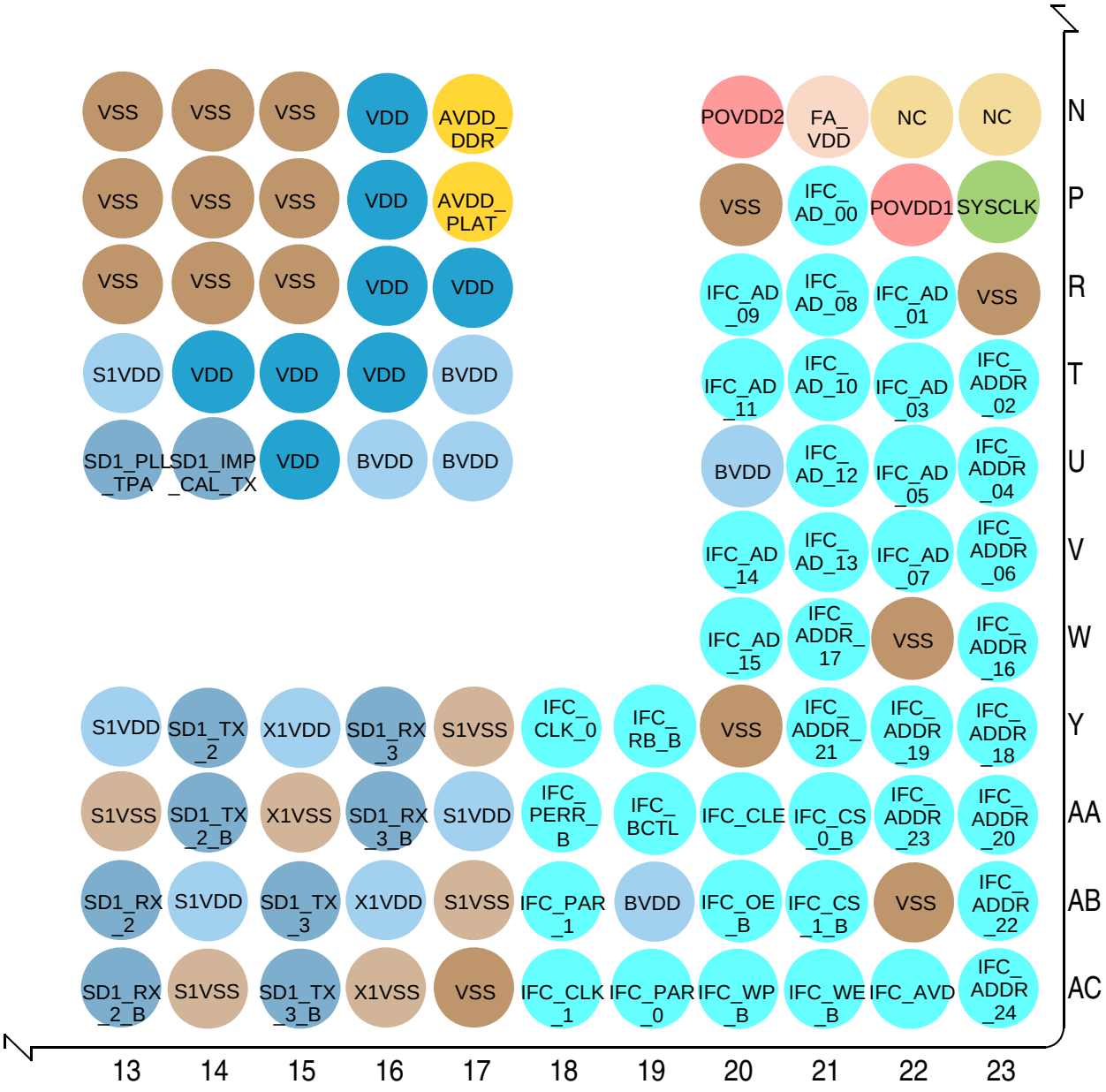

VSS VSS VSS VDD AVDD_DDR
VSS VSS VSS VDD AVDD_PLAT
VSS VSS VSS VDD VDD
S1VDD VDD VDD VDD BVDD
SD1_PLL_TPA SD1_IMP_CAL_TX VDD BVDD BVDD
POVDD2 FA_VDD NC NC
VSS IFC_AD_00 POVDD1 SYSCLK
IFC_AD_09 IFC_AD_08 IFC_AD_01 VSS
IFC_AD_11 IFC_AD_10 IFC_AD_03 IFC_ADDR_02
BVDD IFC_AD_12 IFC_AD_05 IFC_ADDR_04
IFC_AD_14 IFC_AD_13 IFC_AD_07 IFC_ADDR_06
IFC_AD_15 IFC_ADDR_17 VSS IFC_ADDR_16
S1VDD SD1_TX_2 X1VDD SD1_RX_3 S1VSS IFC_CLK_0 IFC_RB_B VSS IFC_ADDR_21 IFC_ADDR_19 IFC_ADDR_18
S1VSS SD1_TX_2_B X1VSS SD1_RX_3_B S1VDD IFC_PERR_B IFC_BCTL IFC_CLE IFC_CS_0_B IFC_ADDR_23 IFC_ADDR_20
SD1_RX_2 S1VDD SD1_TX_3 X1VDD S1VSS IFC_PAR_1 BVDD IFC_OE_B IFC_CS_1_B VSS IFC_ADDR_22
SD1_RX_2_B S1VSS SD1_TX_3_B X1VSS VSS IFC_CLK_1 IFC_PAR_0 IFC_WP_B IFC_WE_B IFC_AVD IFC_ADDR_24
N P R T U V W Y AA AB AC
13 14 15 16 17 18 19 20 21 22 23

Table 1: Signals color coding

	Name	Color
	DDR Signals	Dew
	LVDD, SVDD, BVDD, S1VDD, X1VD, OVDD, GVDD, X2VDD, S2VDD	Cloud LT
	VDD	Mist
	AVDD	Yellow
	VSS	Cork DK
	IFC	Cyan
	UDP, UDM	Green
	POVDD	Red

Table 1: Signals color coding (continued)

	Name	Color
	SYSCLK, RTC	Dew
	S1VSS, X1VSS	Cork DK
	Serdes	Mist DK
	TSEC1	Slate
	NC	Yellow LT
	SENSE	Moss DK
	Ethernet Management	Blue
	USB	Dew DK

Table 1: Signals color coding (continued)

	Name	Color
	IRQ	Mist DK
	FlexCAN/DUART	Magenta
	READY, SCAN, VUSB, IBIAS, FA	Orange
	HRESET_B	Cork
	TCK, TDD, TDI, TMS, TRST_B	Orange
	MVREF	Yellow

1.2 Pinout assignments

This table provides the pinout listing for the P1010.

Table 1. P1010 pinout listing[1]

Signal	Pin Number	Pin Type	Supply	Note
DDR Memory Controller Interface				
MDQ_00	K4	IO	GVDD	—
MDQ_01	M3	IO	GVDD	—
MDQ_02	J4	IO	GVDD	—

Table 1. P1010 pinout listing[1] (continued)

Signal	Pin Number	Pin Type	Supply	Note
MDQ_03	N4	IO	GVDD	—
MDQ_04	K3	IO	GVDD	—
MDQ_05	N3	IO	GVDD	—
MDQ_06	G3	IO	GVDD	—
MDQ_07	L3	IO	GVDD	—
MDQ_08	H2	IO	GVDD	—
MDQ_09	L1	IO	GVDD	—
MDQ_10	G1	IO	GVDD	—
MDQ_11	M2	IO	GVDD	—
MDQ_12	H1	IO	GVDD	—
MDQ_13	N1	IO	GVDD	—
MDQ_14	J2	IO	GVDD	—
MDQ_15	M1	IO	GVDD	—
MDQ_16/MECC_0	R4	IO	GVDD	—
MDQ_17/MECC_1	V4	IO	GVDD	—
MDQ_18/MECC_2	R3	IO	GVDD	—
MDQ_19/MECC_3	W4	IO	GVDD	—
MDQ_20/MECC_4	T4	IO	GVDD	—
MDQ_21/MECC_5	Y2	IO	GVDD	—
MDQ_22/MECC_6	P3	IO	GVDD	—
MDQ_23/MECC_7	V3	IO	GVDD	—
MDQ_24	R2	IO	GVDD	—
MDQ_25	V2	IO	GVDD	—
MDQ_26	P1	IO	GVDD	—
MDQ_27	W1	IO	GVDD	—
MDQ_28	R1	IO	GVDD	—
MDQ_29	Y1	IO	GVDD	—
MDQ_30	P2	IO	GVDD	—
MDQ_31	U2	IO	GVDD	—
MDQS_0	H3	IO	GVDD	—
MDQS_1	J1	IO	GVDD	—
MDQS_2	T3	IO	GVDD	—
MDQS_3	T1	IO	GVDD	—
MDQS_0_B	J3	IO	GVDD	—

Table 1. P1010 pinout listing[1] (continued)

Signal	Pin Number	Pin Type	Supply	Note
MDQS_1_B	K1	IO	GVDD	—
MDQS_2_B	U3	IO	GVDD	—
MDQS_3_B	U1	IO	GVDD	—
MDM_0	M4	O	GVDD	—
MDM_1	L2	O	GVDD	—
MDM_2	W3	O	GVDD	—
MDM_3	V1	O	GVDD	—
MA_00	D3	O	GVDD	—
MA_01	D7	O	GVDD	—
MA_02	B6	O	GVDD	—
MA_03	B3	O	GVDD	—
MA_04	A2	O	GVDD	—
MA_05	C7	O	GVDD	—
MA_06	A5	O	GVDD	—
MA_07	A3	O	GVDD	—
MA_08	C6	O	GVDD	—
MA_09	B5	O	GVDD	—
MA_10	D1	O	GVDD	—
MA_11	A4	O	GVDD	—
MA_12	D5	O	GVDD	—
MA_13	A6	O	GVDD	—
MA_14	C3	O	GVDD	—
MA_15	A7	O	GVDD	—
MBA_0	C4	O	GVDD	—
MBA_1	C5	O	GVDD	—
MBA_2	D4	O	GVDD	—
MCS_0_B	B1	O	GVDD	—
MCS_1_B	C2	O	GVDD	—
MCS_2_B	A8	O	GVDD	—
MCS_3_B	B8	O	GVDD	—
MRAS_B	F1	O	GVDD	—
MCAS_B	F2	O	GVDD	—
MWE_B	F4	O	GVDD	—
MCKE_0	E3	O	GVDD	6

Table 1. P1010 pinout listing[1] (continued)

Signal	Pin Number	Pin Type	Supply	Note
MCKE_1	C1	O	GVDD	6
MCK	G4	O	GVDD	—
MCK_B	F3	O	GVDD	—
MODT_0	E2	O	GVDD	—
MODT_1	E1	O	GVDD	—
MDIC_0	D8	IO	GVDD	17
MDIC_1	C8	IO	GVDD	18
Ethernet MI				
EC_MDC/cfg_cpu_boot	AA6	O	LVDD	3
EC_MDIO	AC2	IO	LVDD	—
eTSEC1/1588/DMA/GPIO				
TSEC1_TXD_0/1588_ALARM_OUT1/cfg_rom_loc[0]	AC5	O	LVDD	20
TSEC1_TXD_1/1588_ALARM_OUT2/cfg_rom_loc[1]	AC1	O	LVDD	20
TSEC1_TXD_2/1588_PULSE_OUT1/cfg_rom_loc[2]	AA5	O	LVDD	20
TSEC1_TXD_3/1588_PULSE_OUT2/cfg_rom_loc[3]	AA4	O	LVDD	20
TSEC1_TX_EN/cfg_svr	AC6	O	LVDD	3, 7
TSEC1_RXD_0/1588_TRIG_IN1	AC4	I	LVDD	—
TSEC1_RXD_1/1588_TRIG_IN2/GPIO_12	AB4	IO	LVDD	—
TSEC1_RXD_2/1588_CLK_IN	AB3	I	LVDD	—
TSEC1_RXD_3/1588_CLK_OUT	AC3	IO	LVDD	—
TSEC1_RX_DV/DMA_DREQ_0_B/GPIO_13	AB6	IO	LVDD	—
TSEC1_RX_CLK/DMA_DACK_0_B/GPIO_14	Y6	IO	LVDD	—
TSEC1_GTX_CLK/DMA_DDONE_0_B	AA3	O	LVDD	7
TSEC1_GTX_CLK125/GPIO_15	Y5	IO	LVDD	—
IFC/eSDHC/USB ULPI/DMA				
IFC_AD_00/cfg_sys_pll_0	P21	IO	BVDD	20
IFC_AD_01/cfg_sys_pll_1	R22	IO	BVDD	20
IFC_AD_02/cfg_sys_pll_2	T23	IO	BVDD	20
IFC_AD_03/cfg_core_pll_0	T22	IO	BVDD	20
IFC_AD_04/cfg_core_pll_1	U23	IO	BVDD	20
IFC_AD_05/cfg_core_pll_2	U22	IO	BVDD	20
IFC_AD_06/cfg_core_speed	V23	IO	BVDD	3
IFC_AD_07/cfg_ddr_pll_0	V22	IO	BVDD	20

Table 1. P1010 pinout listing[1] (continued)

Signal	Pin Number	Pin Type	Supply	Note
IFC_AD_08/cfg_ddr_pll_1	R21	IO	BVDD	20
IFC_AD_09/cfg_ifc_pb_0	R20	IO	BVDD	3
IFC_AD_10/cfg_ifc_pb_1	T21	IO	BVDD	3
IFC_AD_11/cfg_ifc_pb_2	T20	IO	BVDD	3
IFC_AD_12/cfg_srds_refclk	U21	IO	BVDD	3
IFC_AD_13/cfg_io_ports_0	V21	IO	BVDD	3
IFC_AD_14/cfg_io_ports_1	V20	IO	BVDD	3
IFC_AD_15/cfg_ifc_adm	W20	IO	BVDD	3
IFC_ADDR_16/SDHC_CLK/USB_CLK/IFC_CS_2_B	W23	IO	BVDD	8
IFC_ADDR_17/SDHC_CMD/USB_D_0/DMA_DREQ_1_B	W21	IO	BVDD	—
IFC_ADDR_18/SDHC_DATA_0/USB_D_1/DMA_DACK_1_B	Y23	IO	BVDD	—
IFC_ADDR_19/SDHC_DATA_1/USB_D_2/DMA_DDONE_1_B	Y22	IO	BVDD	—
IFC_ADDR_20/SDHC_DATA_2/USB_D_3	AA23	IO	BVDD	—
IFC_ADDR_21/SDHC_DATA_3/USB_D_4	Y21	IO	BVDD	—
IFC_ADDR_22/SDHC_WP/USB_D_5	AB23	IO	BVDD	—
IFC_ADDR_23/SDHC_CD/USB_D_6	AA22	IO	BVDD	—
IFC_ADDR_24/USB_D_7	AC23	IO	BVDD	—
IFC_AVD/cfg_dram_type	AC22	O	BVDD	3
IFC_CS_0_B	AA21	O	BVDD	—
IFC_CS_1_B	AB21	O	BVDD	—
IFC_WE_B/cfg_ifc_flash_mode	AC21	O	BVDD	3
IFC_CLE/cfg_host_agt_0	AA20	O	BVDD	3
IFC_OE_B/cfg_host_agt_1	AB20	O	BVDD	3
IFC_WP_B	AC20	O	BVDD	7
IFC_RB_B	Y19	I	BVDD	—
IFC_BCTL/cfg_boot_seq_0	AA19	O	BVDD	3
IFC_PAR_0/USB_STP	AC19	IO	BVDD	7
IFC_PAR_1/cfg_plat_speed	AB18	IO	BVDD	3
IFC_PERR_B/USB_DIR	AA18	I	BVDD	—
IFC_CLK_0	Y18	O	BVDD	—
IFC_CLK_1/USB_NXT/IFC_CS_3_B	AC18	IO	BVDD	8
SPI/GPIO				
SPI_MOSI/GPIO_6	A16	IO	OVDD	—
SPI_MISO/GPIO_7	B16	IO	OVDD	—

Table 1. P1010 pinout listing[1] (continued)

Signal	Pin Number	Pin Type	Supply	Note
SPI_CLK/GPIO_8	C16	IO	OVDD	—
SPI_CS0_B/GPIO_9	D16	IO	OVDD	—
FlexCAN/DUART/TDM				
CAN1_TX/UART_SOUT_2/TDM_TX_DATA/cfg_boot_seq_1	A17	O	OVDD	3
CAN1_RX/UART_SIN_2/TDM_RX_DATA	D17	IO	OVDD	—
CAN2_TX/UART_SOUT_3/TDM_TFS	A18	IO	OVDD	—
CAN2_RX/UART_SIN_3/TDM_RFS	B18	IO	OVDD	—
DUART/TDM/GPIO				
UART_SOUT_0	C18	O	OVDD	7
UART_SIN_0	D18	I	OVDD	—
UART_CTS_0_B	A19	I	OVDD	—
UART_RTS_0_B/cfg_ifc_ecc_0	C19	O	OVDD	3
UART_SOUT_1/cfg_ifc_ecc_1	C20	O	OVDD	3
UART_SIN_1	E20	I	OVDD	—
UART_CTS_1_B/GPIO_10/TDM_TX_CLK/IRQ_10	A20	IO	OVDD	—
UART_RTS_1_B/GPIO_11/IRQ_11/TDM_RX_CLK	D19	IO	OVDD	—
I2C				
IIC1_SDA	A21	IO	OVDD	10
IIC1_SCL	B20	IO	OVDD	10
IIC2_SDA	A22	IO	OVDD	10
IIC2_SCL	C21	IO	OVDD	10
Interrupts				
IRQ_0	F23	I	OVDD	—
IRQ_1	E21	I	OVDD	—
IRQ_2/TRIG_IN	F22	I	OVDD	—
IRQ_3/SRESET_B/TMP_DETECT	C23	I	OVDD	—
IRQ_OUT_B	D21	O	OVDD	10
GPIO				
GPIO_0/IRQ_4/DRVVBUS/MDVAL	D23	IO	OVDD	—
GPIO_1/IRQ_5/VBUSPWRFAULT/MSRCID_0	D22	IO	OVDD	—
GPIO_2/IRQ_6/CKSTP_IN_B/MSRCID_1	A23	IO	OVDD	—
GPIO_3/IRQ_7/CKSTP_OUT_B/MSRCID_2	B23	IO	OVDD	9
GPIO_4/IRQ_8/MCP_B/MSRCID_3/CLK_OUT	B21	IO	OVDD	—

Table 1. P1010 pinout listing[1] (continued)

Signal	Pin Number	Pin Type	Supply	Note
GPIO_5/IRQ_9/UDE_B/MSRCID_4	E22	IO	OVDD	—
System Control/Power Management				
HRESET_B	E23	I	OVDD	—
HRESET_REQ_B/cfg_sb_dis	H23	O	OVDD	3
READY/TRIG_OUT/ASLEEP	F21	O	OVDD	7
Clocking				
SYSCLK	P23	I	OVDD	—
RTC	F20	I	OVDD	—
USBPHY_CLK	M20	I	OVDD	—
IO_VSEL				
BVDD_VSEL_0	G17	I	OVDD	—
BVDD_VSEL_1	H17	I	OVDD	—
DFT				
SCAN_MODE_B	H21	I	OVDD	2
JTAG				
TCK	G21	I	OVDD	—
TDI	H22	I	OVDD	4
TDO	G23	O	OVDD	6
TMS	J22	I	OVDD	4
TRST_B	H20	I	OVDD	4
Serdes1 (x4)				
SD1_TX_3	AB15	O	XVDD	—
SD1_TX_2	Y14	O	XVDD	—
SD1_TX_1	Y10	O	XVDD	—
SD1_TX_0	AB9	O	XVDD	—
SD1_TX_3_B	AC15	O	XVDD	—
SD1_TX_2_B	AA14	O	XVDD	—
SD1_TX_1_B	AA10	O	XVDD	—
SD1_TX_0_B	AC9	O	XVDD	—
SD1_RX_3	Y16	I	XVDD	—
SD1_RX_2	AB13	I	XVDD	—
SD1_RX_1	AB11	I	XVDD	—
SD1_RX_0	Y8	I	XVDD	—

Table 1. P1010 pinout listing[1] (continued)

Signal	Pin Number	Pin Type	Supply	Note
SD1_RX_3_B	AA16	I	XVDD	—
SD1_RX_2_B	AC13	I	XVDD	—
SD1_RX_1_B	AC11	I	XVDD	—
SD1_RX_0_B	AA8	I	XVDD	—
SD1_REF_CLK	AA12	I	XVDD	—
SD1_REF_CLK_B	Y12	I	XVDD	—
SD1_IMP_CAL_TX	U14	I	XVDD	11
SD1_IMP_CAL_RX	U10	I	XVDD	12
SD1_PLL_TPA	U13	O	XVDD	—
SD1_PLL_TPD	U11	O	XVDD	—
Serdes2 (x2)				
SD2_TX_1	C10	O	XVDD	—
SD2_TX_0	C14	O	XVDD	—
SD2_TX_1_B	D10	O	XVDD	—
SD2_TX_0_B	D14	O	XVDD	—
SD2_RX_1	A11	I	XVDD	—
SD2_RX_0	A13	I	XVDD	—
SD2_RX_1_B	B11	I	XVDD	—
SD2_RX_0_B	B13	I	XVDD	—
SD2_REF_CLK	C12	I	XVDD	—
SD2_REF_CLK_B	D12	I	XVDD	—
SD2_IMP_CAL_TX	G10	I	XVDD	11
SD2_IMP_CAL_RX	G14	I	XVDD	12
SD2_PLL_TPA	G11	O	XVDD	—
SD2_PLL_TPD	G13	O	XVDD	—
USB PHY				
VBUSCLMP	L21	IO	$USBV_{DD3\_3}$	—
IBIAS_REXT	M22	I	$USBV_{DD3\_3}$	13
UDP	K23	IO	$USBV_{DD3\_3}$	—
UDM	L23	IO	$USBV_{DD3\_3}$	—
Analog				
MVREF	J7	—	GVDD/2	—
SENSEVDD	AA2	—	—	5

Table 1. P1010 pinout listing[1] (continued)

Signal	Pin Number	Pin Type	Supply	Note
SENSEVSS	Y3	—	—	5
Power and Ground Pins				
AVDD_CORE	H9	—	—	—
AVDD_PLAT	P17	—	—	—
AVDD_DDR	N17	—	—	—
FA_VDD	N21	—	—	5
POVDD1	P22	—	—	16
POVDD2	N20	—	—	14
SD1_AVDD	U12	—	—	—
SD2_AVDD	G12	—	—	—
SD1_AVSS	T12	—	—	—
SD2_AVSS	H12	—	—	—
BVDD	T17,U16, U17,U20, AB19	—	—	—
GVDD	G7,G8,G9, H7,K7,L7,M7,N7,P7, R7,T7	—	—	—
LVDD	U7,U8,AB5	—	—	—
OVDD	C17,C22, D20,G20, J20	—	—	—
S1VDD	T13,Y7,Y13,AA11,AA17, AB7, AB10,AB12,AB14	—	—	—
S1VSS	Y11,Y17, AA7,AA13, AB17,AC10,AC12,AC14	—	—	—
S2VDD	A10,A12, C11,C15, H13	—	—	—
S2VSS	B10,B12, D11,D15	—	—	—
USBVDD1_0	L17,M17	—	—	19
USBVDD1_8	J21,K21	—	—	15
USBVDD3_3	K20,L20	—	—	—
USBVSS	J23,K22,L22,M21,M23	—	—	—
VDD	G15,G16,H8,H10,H11, H14,H15, H16, J8,J16,J17, K8,K16,K17,L8,L16,M8, M16,N8,N16,P8,P16,R8, R16,R17,T8,T9,T10,T14, T15,T16,U9,U15	—	—	—

Table 1. P1010 pinout listing[1] (continued)

Signal	Pin Number	Pin Type	Supply	Note
VSS	A1,A9,B4, A15,B7,B17,B19,B22,D2, D6,E4,G2, G22,H4,J9, J10,J11,J12,J13,J14,J15, K2,K9,K10, K11,K12,K13,K14,K15,L4 ,L9,L10,L11, L12,L13,L14,L15,M9,M10 ,M11,M12, M13,M14, M15,N2,N9,N10,N11, N12,N13, N14,N15,P4,P9,P10,P11, P12,P13, P14,P15, P20,R9,R10,R11,R12, R13,R14, R15,R23,T2,U4,W2,W22, Y4,Y20,AB2,AB22,AC7, AC17	—	—	—
X1VDD	T11,Y9,Y15,AB8,AB16	—	—	—
X1VSS	AA9,AA15, AC8,AC16	—	—	—
X2VDD	A14,B9,C9, C13	—	—	—
X2VSS	B14,B15,D9,D13	—	—	—
Not Connected				
NC	B2,N22, AA1, N23, AB1	—	—	—

Table 1. P1010 pinout listing[1] (continued)

Signal	Pin Number	Pin Type	Supply	Note

Note:

1. All multiplexed signals are listed only once and do not re-occur. For example, IFC_ADDR[17]/SDHC_CMD/USB_D[1]/DMA_DREQ_B[1] is listed only once in the IFC section, and is not mentioned in the DMA section even though the pin also functions as DMA_DREQ_B[1].
2. These are test signals for factory use only and must be pulled up (with 100 Ω–1 kΩ) to OVDD for normal operation.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
4. These pins have weak internal pull-up P-FETs that are always enabled.
5. Treat these pins as no connects (NC).
6. This output is actively driven during reset rather than being three-stated during reset.
7. This pin must NOT be pulled down, by a resistor or the component it is connected to, during power-on reset.
8. If this pin is configured for chip select usage than it is recommend to have a weak pull-up resistor (2-10 KΩ) be placed on this pin to BVDD, to ensure no random chip select assertion due to possible noise and etc.
9. If this pin is configured for check stop usage than it will behave as an open drain signal.
10. This pin is an open drain signal.
11. This pin should be pulled down with 100Ω±1% resistor if used in autocalibration mode and should be tied to 1V if fixed calibration mode is used.
12. This pin should be pulled down with 200Ω±1% resistor if used in autocalibration mode and should be tied to 1V if fixed calibration mode is used.
13. For this pin the recommendations mentioned in Section 2.12.4, “IBIAS_REXT filter and Section 2.12.5, “Threshold detect increase must be followed.
14. This pin is used for fuse programming. Should be tied to Vss for normal operation (fuse read). See section Section 2.2, “Power sequencing” for more details.
15. This pin should be connected to Vss through 1μF.No need to supply power to this pin. 1.8V output may be observed on this pin during normal working conditions.
16. Connect these pins to Vss.
17. This is a DDR drive strength calibration pin. This should be connected to V_{SS} through a 20Ω (Full-strength mode) or 40Ω (Half-strength mode) precision 1% resistor.
18. This is a DDR drive strength calibration pin. This should be connected to GV_{DD} through a 20Ω (Full-strength mode) or 40Ω (Half-strength mode) precision 1% resistor.
19. This pin and V_{DD} should be fed from the same source, with a filter circuit as described in Section 3.3.1, “PLL power supply filtering.
20. This pin is a reset configuration pin. During reset sequence this should be pulled-up or down as needed, to the corresponding power bank, with a weak pull-up/down resistor.

2 Electrical characteristics

This section provides the AC and DC electrical specifications for the P1010. The P1010 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference.These are not purely I/O buffer design specifications.

2.1 Overall DC electrical characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum ratings[1]

Characteristic	Symbol	Max Value	Unit	Note
Platform supply voltage	V_{DD}	–0.3 to 1.05	V	—
PLL supply voltage	AV_{DD_CORE} AV_{DD_DDR} AV_{DD_PLAT} $SD1\_AV_{DD}$ $SD2\_AV_{DD}$	–0.3 to 1.05	V	7
Fuse programming supply	POV_{DD2}	–0.3 to 1.65	V	—
Core power supply for SerDes transceivers	$S1V_{DD}$ $S2V_{DD}$	–0.3 to 1.05	V	—
Pad power supply for SerDes transceivers	$X1V_{DD}$ $X2V_{DD}$	–0.3 to 1.05	V	—
USB PHY supply	$USBV_{DD1\_0}$ $USBV_{DD3\_3}$	–0.3 to 1.05 –0.3 to 3.63	V	—
DDR3/DDR3L DRAM I/O voltage	GV_{DD}	–0.3 to 1.65 –0.3 to 1.45	V	—
Three-speed Ethernet I/O (eTSEC), MII management, GPIO_(12-15), DMA, 1588 voltage	LV_{DD}	–0.3 to 2.75	V	—
SPI, DUART, TDM, I^2C, FlexCAN, GPIO_(0-11) and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—
IFC, eSDHC, USB-ULPI voltage	BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—

Table 2. Absolute maximum ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR3/DDR3L DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 6
	DDR3/DDR3L DRAM reference	MV_{REF}	–0.3 to (GV_{DD}/2 + 0.3)	V	—
	Three-speed Ethernet,1588, DMA, GPIO_(12-15), signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	3, 6
	IFC, USB, eSDHC signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	4
	DUART, SYSCLK, system control and power management, I^2C, eSPI, clocking, I/O voltage select, GPIO_(0-11)and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	5, 6
	Serdes signals	XV_{IN}	–0.3 to (XV_{DD} + 0.3)	V	—
Storage temperature range		T_{STG}	–55 to 150	°C	—

Note:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: MVIN must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. Caution: LVIN must not exceed LVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. Caution: BVIN must not exceed BVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. Caution: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. (X,B,G,L,O)VIN and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
7. AV_{DD} is measured at the input to the filter and not at the pin of the device. The filter circuit is provided in Section 3.3.1, "PLL power supply filtering.

2.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this device. Note that the values in Table 3 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions[4]

Characteristic	Symbol	Recommended Value	Unit	Note
Platform supply voltage	V_{DD}	1 ± 50 mV	V	—
PLL supply voltage	AV_{DD_CORE} AV_{DD_DDR} AV_{DD_PLAT} $SD1\_AV_{DD}$ $SD2\_AV_{DD}$	1 ± 50 mV	V	—
Fuse supply voltage	POV_{DD2}	1.5 V ± 75 mV	V	—
Core power supply for SerDes transceivers	$S1V_{DD}$ $S2V_{DD}$	1 ± 50 mV	V	—

Table 3. Recommended operating conditions[4]

Characteristic		Symbol	Recommended Value	Unit	Note
Pad power supply for SerDes transceivers and PCI Express		$X1V_{DD}$ $X2V_{DD}$	1 ± 50 mV	V	—
USB PHY supply		$USBV_{DD1\_0}$ $USBV_{DD3\_3}$	1 ± 50 mV 3.3 V ± 165 mV	V	—
DDR3 DRAM I/O voltage		GV_{DD}	1.5 V ± 75 mV	—	—
DDR3L DRAM I/O voltage		GV_{DD}	1.35 V +100mV / -67mV	—	—
Three-speed Ethernet I/O (eTSEC), MII management, GPIO_(12-15), DMA, 1588 voltage		LV_{DD}	2.5 V ± 125 mV	V	—
DUART, system control and power management, I^2C, GPIO_(0-11), and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Integrated Flash Controller I/O		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Input voltage	DDR3/DDR3L DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR3/DDR3L DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	—
	Three-speed Ethernet,1588, DMA, GPIO_(12-15), signals	LV_{IN}	GND to LV_{DD}	V	3
	IFC, USB, eSDHC signals	BV_{IN}	GND to BV_{DD}	V	3
	DUART, SYSCLK, system control and power management, I^2C, eSPI, GPIO_(0-11) and JTAG signals	OV_{IN}	GND to OV_{DD}	V	3
	Serdes signals	XV_{IN}	GND to $X1V_{DD}$	V	3
Operating Temperature range	Standard Temperature Range	T_A/T_J	T_A=0 (min) to T_J=105 (max)	°C	—
	Extended Temperature Range	T_A/T_J	T_A=–40 (min) to T_J=105 (max)	°C	—
	Secure Boot Fuse Programming	T_A/T_J	T_A=0 (min) to T_J=70 (max)	°C	2

Note:

1. BV_{DD} = 3.3 V or 1.8 V is selected for USB, all other signals associated with BV_{DD} must meet all V_{IH} requirements associated with external device inputs.
2. POV_{DD} must be supplied 1.5 V and the P1010 must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power sequencing."
3. (L,X,B,O,G)V_{IN} may overshoot (for V_{IH}) or undershoot (for V_{IL}) to the voltages and maximum duration shown in Figure 2.
4. Power should be applied to all power pins even if the corresponding interface is not used.

This figure shows the undershoot and overshoot voltages at the interfaces of the P1010.

NOTE

1. t_{CLOCK} refers to the clock period associated with the respective interface:

- For I^2C and JTAG, t_{CLOCK} references SYSCLK.
- For DDR, t_{CLOCK} references MCLK.
- For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
- For IFC, t_{CLOCK} references IFC_CLK.
- For SERDES, t_{CLOCK} references SDx_REF_CLK.

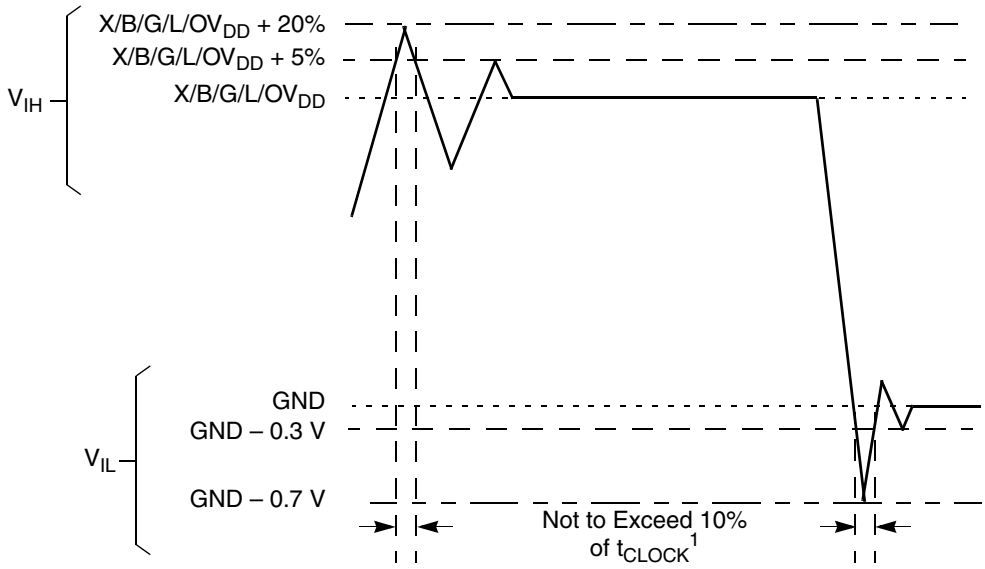


Figure 2. Overshoot/Undershoot voltage for $BV_{IN}/MV_{IN}/LV_{IN}/OV_{IN}/XV_{IN}$

The core voltage must always be provided at nominal 1V (see Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. BV_{DD}, OV_{DD} and LV_{DD}-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR3 SDRAM interface uses a differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$). The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output driver characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output drive capability

Driver Type	Output Impedance (Ω)	Supply Voltage	Note
IFC, GPIO, USB, eSDHC	45 45 45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR3 signal (Programmable)	20 (full strength) 40 (half strength)	GV_{DD} = 1.5 V DDR3 GV_{DD} = 1.35 V DDR3L	1
TSEC signals	45	LV_{DD} = 2.5V	—
DUART, system control, JTAG, SPI	45	OV_{DD} = 3.3 V	—
I^2C	45	OV_{DD} = 3.3 V	—

Table 4. Output drive capability (continued)

Driver Type	Output Impedance (Ω)	Supply Voltage	Note

Note:

1. The drive strength of the DDR3 interface in half-strength mode is at T_j = 105°C and at GV_{DD} (min).

2.2 Power sequencing

The P1010 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD_CORE}, AV_{DD_DDR}, AV_{DD_PLAT}, $SD1\_AV_{DD}$, $SD2\_AV_{DD}$, $S1V_{DD}$, $S2V_{DD}$, $X1V_{DD}$, $X2V_{DD}$, BV_{DD}, LV_{DD}, OV_{DD}.
2. $USBV_{DD3\_3}$, GV_{DD}.
3. For secure boot fuse programming: After deassertion of $\overline{\text{HRESET}}$, drive POV_{DD} = 1.5 V after a required minimum delay per Table 5. After fuse programming is completed, it is required to return POV_{DD} = GND before the system is power cycled ($\overline{\text{HRESET}}$ assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 5. See Section 5, "Security fuse processor," for additional details.

WARNING

Only one secure boot fuse programming event is permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND.

This figure provides the POV_{DD} timing diagram.

NOTE

POVDD must be stable at 1.5 V prior to initiating fuse programming.

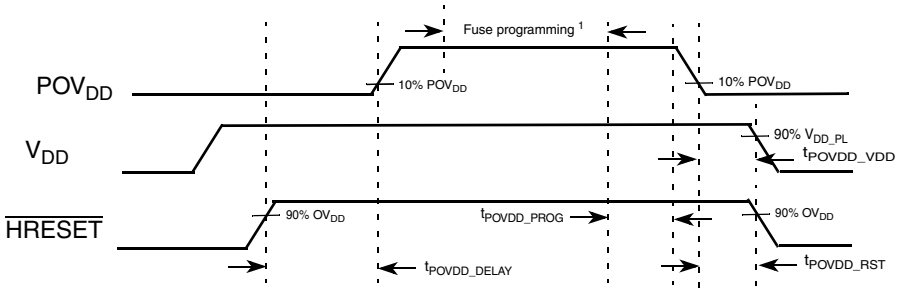


Figure 3. POV_{DD} timing diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD}.

Table 5. POV_{DD} timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	1500	—	t_{SYSCLK}	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3

Table 5. POV_{DD} timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_RST}	0	—	μs	4

Note:

1. Delay required from the deassertion of $\overline{\text{HRESET}}$ to driving POV_{DD} ramp up. Delay measured from $\overline{\text{HRESET}}$ deassertion at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND. After fuse programming is completed, it is required to return POV_{DD} = GND.
3. Delay required from POV_{DD} ramp down complete to V_{DD} ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before V_{DD} is at 90% V_{DD}.
4. Delay required from POV_{DD} ramp down complete to $\overline{\text{HRESET}}$ assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before $\overline{\text{HRESET}}$ assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

All supplies must be at their stable values within 50 ms from the start of first supply.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power-down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

2.4 Reset Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table provides the RESET initialization AC timing specifications.

Table 6. RESET initialization timing specifications

Parameter	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$	600	—	μs	1, 2, 5
Minimum assertion time of $\overline{\text{TRESET}}$ simultaneous to $\overline{\text{HRESET}}$ assertion	25	—	ns	3
Maximum rise/fall time of $\overline{\text{HRESET}}$	—	1	t_{SYSCLK}	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	t_{SYSCLK}	4
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	25	—	μs	—

Table 6. RESET initialization timing specifications

Parameter	Min	Max	Unit	Note
Input setup time for POR configurations (other than PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	4	—	t_{SYSCLK}	4
Input hold time for all POR configurations (including PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	2	—	t_{SYSCLK}	4
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{HRESET}}$	—	5	t_{SYSCLK}	4

Note:

1. There may be some extra current leakage when driving signals high during this time.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.
3. TRST is an asynchronous level sensitive signal. For guidance on how this requirement can be met, refer to the JTAG signal termination guidelines in Section 3.10.1, "Termination of unused signals."
4. SYSCLK is the primary clock input for the P1010.
5. Reset initialization should start only after all power supplies are stable.

This table provides the PLL lock times.

Table 7. PLL lock times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

2.5 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 8. Power supply ramp rate

Parameter	Min	Max	Unit	Note
Required ramp rate for all voltage supplies (including $OV_{DD}/GV_{DD}/BV_{DD}/SV_{DD}/LV_{DD}$, All V_{DD} supplies, MV_{REF} and all AV_{DD} supplies except $USBV_{DD3\_3}$.)	—	36000	Volts/Sec	1,3
Required ramp rate for $USBV_{DD3\_3}$	—	3300	Volts/Sec	2

Note:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Ramp rate is specified as a linear ramp from 10 to 90%.
3. Over full recommended operating temperature range. See Table 3.

2.6 Power characteristics

This table shows the power dissipations of the V_{DD} supply for various operating core complex bus clock (CCB_clk) frequencies versus the core and DDR clock frequencies. Note that these numbers are based on design estimates only and are preliminary. More accurate power numbers will be available after the measurement on the silicon is complete.

Table 9. P1010 power dissipation

Power Mode	Core Frequency (MHz)	CCB Frequency (MHz)	DDR Data Rate (MHz)	V_{DD} Core (V)	Junction Temperature (°C)	Core[1] Power (W)	SVDD Power (W)	Note
Typical	533	266	667	1.0	65	1.04	0.20	2, 3
Thermal					105	1.97	0.20	5, 7
Maximum					105	2.17	0.20	4, 6, 7
Typical	667	333	667	1.0	65	1.08	0.20	2, 3
Thermal					105	2.06	0.20	5, 7
Maximum					105	2.27	0.20	4, 6, 7
Typical	800	400	800	1.0	65	1.13	0.20	2, 3
Thermal					105	2.15	0.20	5, 7
Maximum					105	2.37	0.20	4, 6, 7
Typical	1000	400	800	1.0	65	1.63	0.20	2, 3
Thermal					105	3.09	0.20	5, 7
Maximum					105	3.18	0.20	4, 6, 7

Note:

1. Combined power of all 1 volt supplies except SVDD with DDR controller/s and all SerDes banks active. Does not include I/O power.
2. Typical power assumes that Dhrystone is running with an activity factor of 90% and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes that Dhrystone is running with an activity factor of 100% and executing DMA on the platform at 100% activity factor.
5. Thermal power assumes a Dhrystone activity factor of 90% and executing DMA on the platform at 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

2.6.1 I/O DC power supply recommendation

This table provides estimated I/O power numbers for each block: DDR, PCI Express, eLBC, eTSEC, SGMII, eSDHC, USB, eSPI, DUART, I2C and GPIO.

Table 10. I/O power supply estimated values

Interface	Parameter	Symbol	Typical	Max	Unit	Note
DDR3 (32 bit)	667 MHz data rate	GV_{DD} (1.5 V)	0.63	0.82	W	1, 2, 6
	800 MHz data rate	GV_{DD} (1.5 V)	0.76	0.98	W	1, 2, 6

Table 10. I/O power supply estimated values (continued)

Interface	Parameter	Symbol	Typical	Max	Unit	Note
DDR3 (16 bit, w/ ECC)	667 MHz data rate	GV_{DD} (1.5 V)	0.40	0.45	W	1, 2, 6
	800 MHz data rate	GV_{DD} (1.5 V)	0.40	0.45	W	1, 2, 6
DDR3L (32 bit)	667 MHz data rate	GV_{DD} (1.35 V)	0.55	0.70	W	1,2
	800 MHz data rate	GV_{DD} (1.35 V)	0.65	0.80	W	1,2
DDR3L (16 bit, w/ ECC)	667 MHz data rate	GV_{DD} (1.35 V)	0.35	0.40	W	1,2
	800 MHz data rate	GV_{DD} (1.35 V)	0.35	0.40	W	1,2
PCI Express	×1, 2.5 G-baud	XVDD (1.0 V)	0.02	0.02	W	1
SGMII	×1, 1.25G-baud	XVDD (1.0 V)	0.014	0.014	W	1
SATA	3.0G-baud	XVDD (1.0 V)	0.022	0.022	W	1
IFC	16-bit, 100MHz	BV_{DD} (1.8 V)	0.017	0.025	W	1,3,7
		BV_{DD} (2.5 V)	0.03	0.038	W	1,3,7
		BV_{DD} (3.3 V)	0.047	0.063	W	1,3,7
RGMII	—	LV_{DD} (2.5 V)	0.075	0.1	W	1,3,4,7
eSDHC	—	BV_{DD} (1.8 V)	0.0042	0.0053	W	1,3,7
	—	BV_{DD} (3.3 V)	0.014	0.0175	W	1,3
USB (ULPI)	—	BV_{DD} (1.8 V)	0.004	0.004	W	1,3
	—	BV_{DD} (2.5 V)	0.008	0.008	W	1,3
	—	BV_{DD} (3.3 V)	0.012	0.012	W	1,3
USB (PHY)	—	USBVDD3_3 (3.3V)	0.15	0.15	W	1,3,7
eSPI	—	OV_{DD} (1.8 V)	0.01	0.0125	W	1,3,7
I^2C	—	OV_{DD} (3.3 V)	0.002	0.002	W	1,3
DUART	—	OV_{DD} (3.3 V)	0.006	0.008	W	1,3,7
TDM	—	OVDD (3.3 V)	0.004	0.005	W	1,3,7
IEEE1588	—	LV_{DD} (2.5 V)	0.004	0.005	W	1,3,7
GPIO	x8	OV_{DD} (3.3 V)	0.009	0.011	W	1,3,5,7
	x8	LV_{DD} (2.5 V)	0.007	0.009	W	1,3,5,7
CAN	—	OV_{DD} (3.3 V)	0.01	0.0125	W	1,3
POV_{DD}	For fuse burning	POV_{DD}(1.5V)	0.045	0.045	W	1

Table 10. I/O power supply estimated values (continued)

Interface	Parameter	Symbol	Typical	Max	Unit	Note

Note:
1. The typical values are estimates based on simulations at 65°C junction temperature.
2. Typical DDR power numbers are based on one rank DIMM with 40% utilization.
3. Assuming 15pF total capacitance load per pin.
4. The current values are per each eTSEC used.
5. GPIO are supported on OVDD and LVDD power rails.
6. Maximum DDR power numbers are based on two ranks DIMM with 75% utilization.
7. The maximum values are estimated and they are based on simulations at 105°C junction temperature.

2.7 Input clocks

2.7.1 System clock specifications

This table provides the system clock (SYSCLK) 3.3 V DC specifications.

Table 11. SYSCLK DC electrical characteristics

At recommended operating conditions with OVDD = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = $V_{DD)}$	I_{IN}	—	—	±50	μA	2

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the system clock (SYSCLK) AC timing specifications.

Table 12. SYSCLK AC timing specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK frequency	f_{SYSCLK}	64	—	100	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	10	—	15.6	ns	1, 2
SYSCLK duty cycle	t_{KHK}/ t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at –56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Table 12. SYSCLK AC timing specifications (continued)

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note

Note:
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency does not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.7.2 Spread spectrum sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 13 considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the P1010 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns. The P1010 is compatible with spread spectrum sources if the recommendations listed in Table 13 are observed.

Table 13. Spread spectrum clock source recommendations

At recommended operating conditions. See Table 3.

Parameter	Min	Max	Unit	Note
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Note:
1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 81.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device

CAUTION

The processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded, regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

2.7.3 Real time clock specifications

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock; that is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded, if not needed.

2.7.4 eTSEC gigabit reference clock specifications

This table lists the eTSEC gigabit reference clock (TSEC1_GTX_CLK125) DC electrical characteristics for the P1010.

Table 14. eTSEC gigabit reference clock DC electrical characteristics

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	1.7	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±40	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values can be found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the P1010.

Table 15. EC_GTX_CLK125 AC timing specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD} = 2.5 V	t_{G125R}/t_{G125F}	—	—	0.75	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	47	—	53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Note:
1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 2.11.1.2, "RGMII AC timing specifications," for the duty cycle for 10Base-T and 100Base-T reference clock.

2.7.5 Other input clocks

A description of the overall clocking of this device is available in the *P1010 QorIQ Integrated Processor Reference Manual*, in the form of a clock subsystem block diagram. For information about the input clock requirements of other functional blocks such as SerDes, Ethernet Management, eSDHC, and IFC, see the specific interface section.

2.8 DDR3, and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3, and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V, and 1.35 V when interfacing to DDR3, or DDR3L SDRAMrespectively.

2.8.1 DDR3, and DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 16. DDR3 SDRAM interface DC electrical characteristics

At recommended operating condition with GV_{DD} = 1.5 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed ±1% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must meet the specification states in Table 19.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 17. DDR3L SDRAM interface DC electrical characteristics

At recommended operating condition with GV_{DD} = 1.35 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.09	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.09	V	5
Output high current (V_{OUT} = 0.641V)	I_{OH}	—	–23.3	mA	6, 7
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.3	—	mA	6, 7
I/O leakage current	I_{OZ}	–50	50	μA	8

Table 17. DDR3L SDRAM interface DC electrical characteristics (continued)

At recommended operating condition with GV_{DD} = 1.35 V[1]

Parameter	Symbol	Min	Max	Unit	Note

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver.Peak-to-peak noise on MVREFn may not exceed the MVREFn DC level by more than ±1% of GV_{DD} (i.e. ±13.5 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must meet the specification states in Table 19.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. IOH and IOL are measured at GVDD = 1.282 V
7. See the IBIS model for the complete output IV curve characteristics.
8. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR controller interface capacitance for DDR3.

Table 18. DDR3 SDRAM capacitance

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	—
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	—

This table provides the current draw characteristics for MVREF*n*.

Table 19. Current draw characteristics for MVREF*n*

For recommended operating conditions, seeTable 3.

Parameter	Symbol	Min	Max	Unit	Note
Current draw for DDR3 SDRAM for MVREF*n*	I_{MVREFn}	—	1250	μA	—
Current draw for DDR3L SDRAM for MVREF*n*	I_{MVREFn}	—	1150	μA	—

2.8.2 DDR3 and DDR3L SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 memories. Note that the required GV_{DD}(typ) voltage is 1.5 V or 1.35 V when interfacing to DDR3 or DDR3L SDRAM respectively.

2.8.2.1 DDR3 and DDR3L SDRAM interface Input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 20. DDR3 SDRAM interface input AC timing specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{ILAC}	—	MVREF*n* – 0.175	V	—
AC input high voltage	V_{IHAC}	MVREF*n* + 0.175	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 21. DDR3L SDRAM interface Input AC timing specifications

At recommended operating conditions with GVDD of 1.35 V ± 5%

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{ILAC}	—	MVREF*n* – 0.160	V	—
AC input high voltage	V_{IHAC}	MVREF*n* + 0.160	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 22. DDR3, and DDR3L SDRAM interface input AC timing specifications

At recommended operating conditions with GVDD of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1
800 MHz data rate		–350	350		1
667 MHz data rate		–390	390		1
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}	—	—	ps	3
800 MHz data rate		–275	275		3
667 MHz data rate		–360	360		3

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. DDR3 only
3. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure shows the DDR3 SDRAM interface input timing diagram.

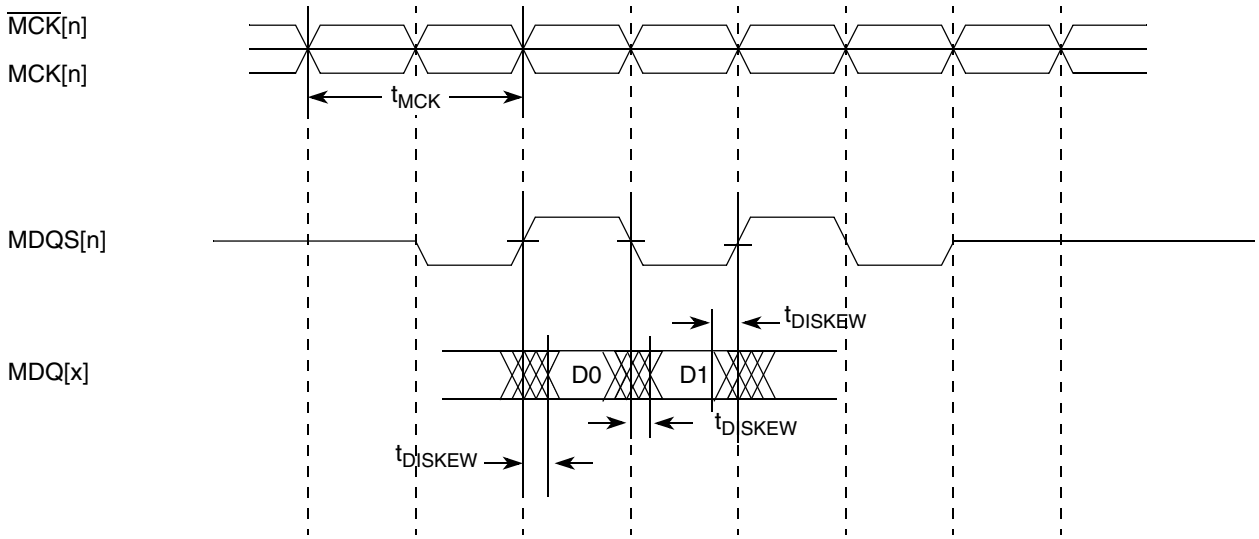


Figure 4. DDR3 SDRAM interface input timing diagram

2.8.2.2 DDR3 SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR3 and DDR3L SDRAM interface.

Table 23. DDR3 SDRAM interface output AC timing specifications

At recommended operating conditions with GVDD of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK[n] cycle time	t_{MCK}	2.5	3	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}	—	—	ns	3
800 MHz data rate		0.767	—		3
667 MHz data rate		0.95	—		3
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}	—	—	ns	3
800 MHz data rate		0.767	—		3
667 MHz data rate		0.95	—		3
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}	—	—	ns	3
800 MHz data rate		0.767	—		3
667 MHz data rate		0.95	—		3
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}	—	—	ns	3
800 MHz data rate		0.767	—		3
667 MHz data rate		0.95	—		3

Table 23. DDR3 SDRAM interface output AC timing specifications (continued)

At recommended operating conditions with GVDD of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK to MDQS Skew	t_{DDKHMH}	—	—	ns	4
800 MHz data rate		–0.525	0.525		4
667 MHz data rate		–0.6	0.6		4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}	—	—	ps	5
800 MHz data rate		225	—		5
667 MHz data rate		325	—		5
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}	—	—	ps	5
800 MHz data rate		225	—		5
667 MHz data rate		325	—		5
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ and MDQS/$\overline{\text{MDQS}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *P1010 QorIQ Integrated Processor Reference Manual* for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in Table 23, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows theDDR3 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

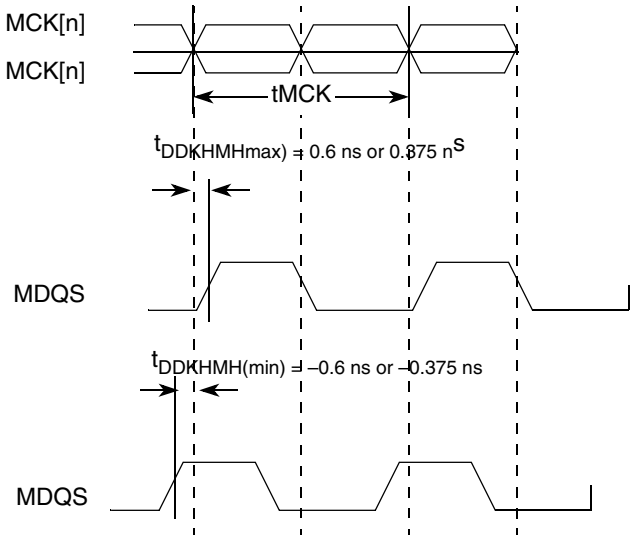


Figure 5. t_{DDKHMH} timing diagram

This figure shows the DDR3 SDRAM output timing diagram.

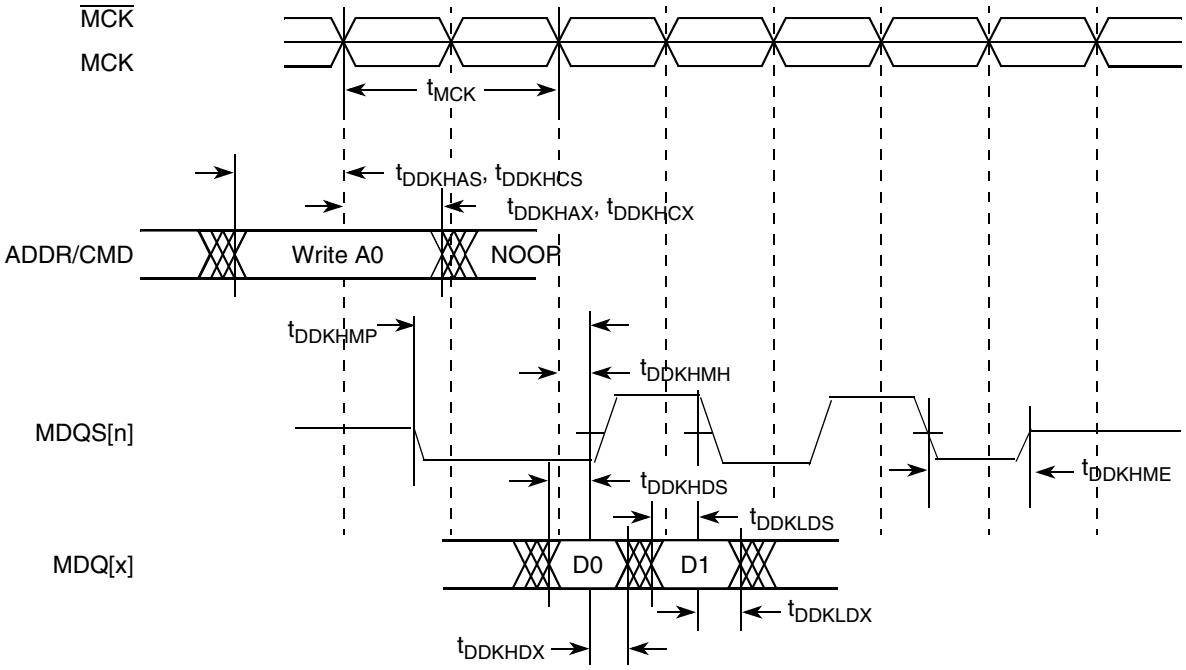


Figure 6. DDR3 output timing diagram

This figure provides the AC test load for the DDR3 controller bus.

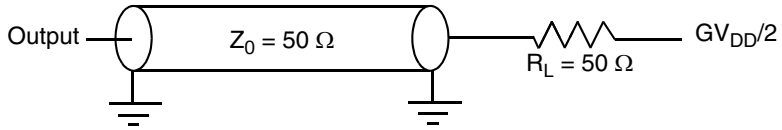


Figure 7. DDR3 controller bus AC test load

2.8.2.3 DDR3 and DDR3L SDRAM differential timing specifications

This section describes the DC and AC differential timing specifications for the DDR3 SDRAM controller interface. This figure shows the differential timing specification.

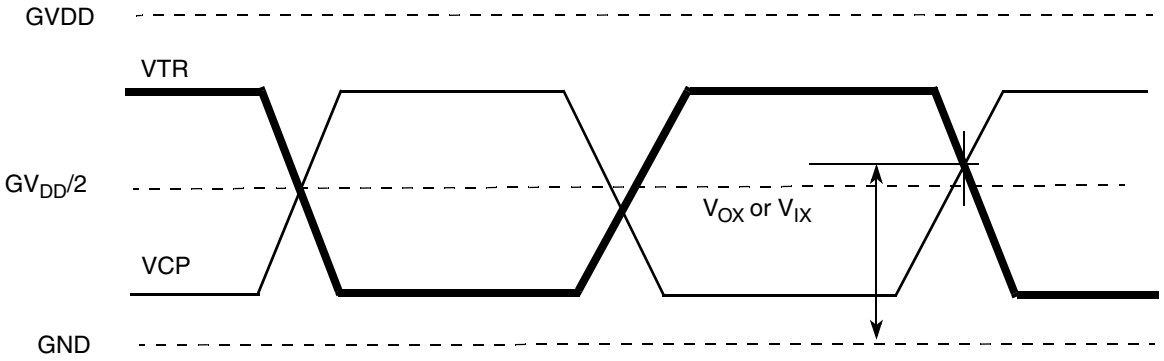


Figure 8. DDR3, and DDR3L SDRAM differential timing specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

This table provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 24. DDR3 SDRAM differential electrical characteristics

Parameter	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-Point Voltage	V_{IXAC}	0.5 × GVDD – 0.150	0.5 × GVDD + 0.150	V	1
Output AC Differential Cross-Point Voltage	V_{OXAC}	0.5 × GVDD – 0.115	0.5 × GVDD + 0.115	V	1

Note:
1. I/O drivers are calibrated before making measurements.

This table provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 25. DDR3L SDRAM differential electrical characteristics

Parameter	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-Point Voltage	V_{IXAC}	0.5 × GVDD – 0.135	0.5 × GVDD + 0.135	V	1
Output AC Differential Cross-Point Voltage	V_{OXAC}	0.5 × GVDD – 0.105	0.5 × GVDD + 0.105	V	1

Note:
1. I/O drivers are calibrated before making measurements.

2.9 eSPI

This section describes the DC and AC electrical specifications for the SPI of the P1010.

2.9.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the device SPI.

Table 26. SPI DC Electrical characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($0 V \le V_{IN} \le CV_{DD}$)	I_{IN}	—	±10	μA	2
Output high voltage (I_{OH} = –6.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (I_{OL} = 6.0mA)	V_{OL}	—	0.5	V	—
Output low voltage (IOL = 3.2mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

2.9.2 eSPI AC timing specifications

This table provides the SPI input and output AC timing specifications.

Table 27. SPI AC timing specifications [1]

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note
SPI clock (SPI_CLK) clock period	t_{SPK}	10	—	ns	—
SPI outputs—Master data (internal clock) hold time	t_{NIKHOX}	0.5+(t_{IPSPI} x SPMODE [HO_ADJ])	—	ns	2, 3
SPI outputs—Master data (internal clock) delay	t_{NIKHOV}	—	2.5+(t_{IPSPI} x SPMODE [HO_ADJ])	ns	2, 3
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
SPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	—
SPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Table 27. SPI AC timing specifications (continued)[1]

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. t_{IPSPI} represents the clock period of the clock on which eSPI block is running. In P1010/14 eSPI runs on CCB/2 freq.

This figure provides the AC test load for the SPI.

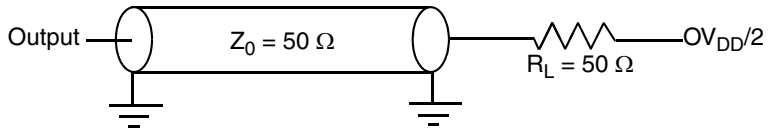
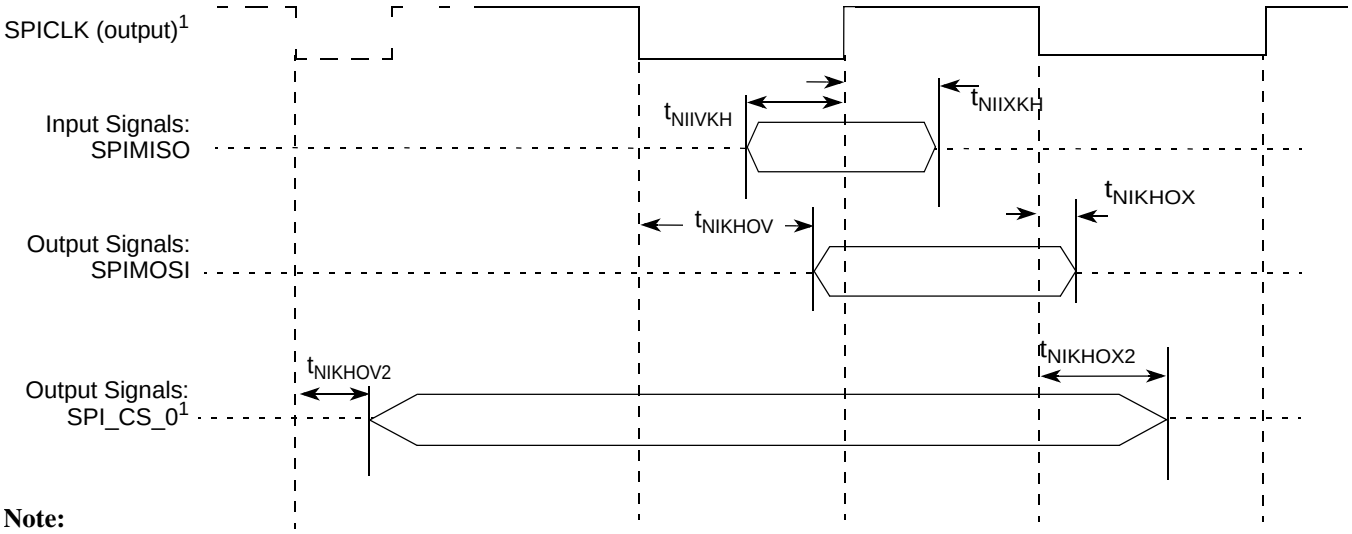


Figure 9. SPI AC Test Load

This figure represents the AC timing, from Table 27, in master mode (internal clock). Note that although the specifications generally refer to the rising edge of the clock, Figure 9 also applies when the falling edge is the active edge. Also, note that the clock edge is selectable on SPI.



Note:

1 A part of SPICLK has been shown as dotted because SPICLK appears on the interface only after CS assertion.

Figure 10. SPI AC timing in master mode (internal clock) diagram

2.10 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the P1010.

2.10.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 28. DUART DC electrical characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Figure 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Figure 3.

2.10.2 DUART AC electrical specifications

This table provides the AC timing parameters for the DUART interface.

Table 29. DUART AC timing specifications

Parameter	Value	Unit	Note
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Note:

1. CCB clock refers to the platform clock.
2. Actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.11 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for enhanced three-speed Ethernet10/100/1000 controller and MII management.

2.11.1 RGMII interface electrical specifications

This section provides AC and DC electrical characteristics of RGMII interface for eTSEC.

2.11.1.1 RGMII DC electrical characteristics

This table shows the RGMII DC electrical characteristics when operating from a 2.5-V supply.

Table 30. RGMII DC electrical characteristics (2.5 V)

At recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	10	μA	—
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	1
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 3.

2.11.1.2 RGMII AC timing specifications

This table presents the RGMII AC timing specifications.

Table 31. RGMII AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Note:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of GTX_CLK125 by more than 300 ppm.

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

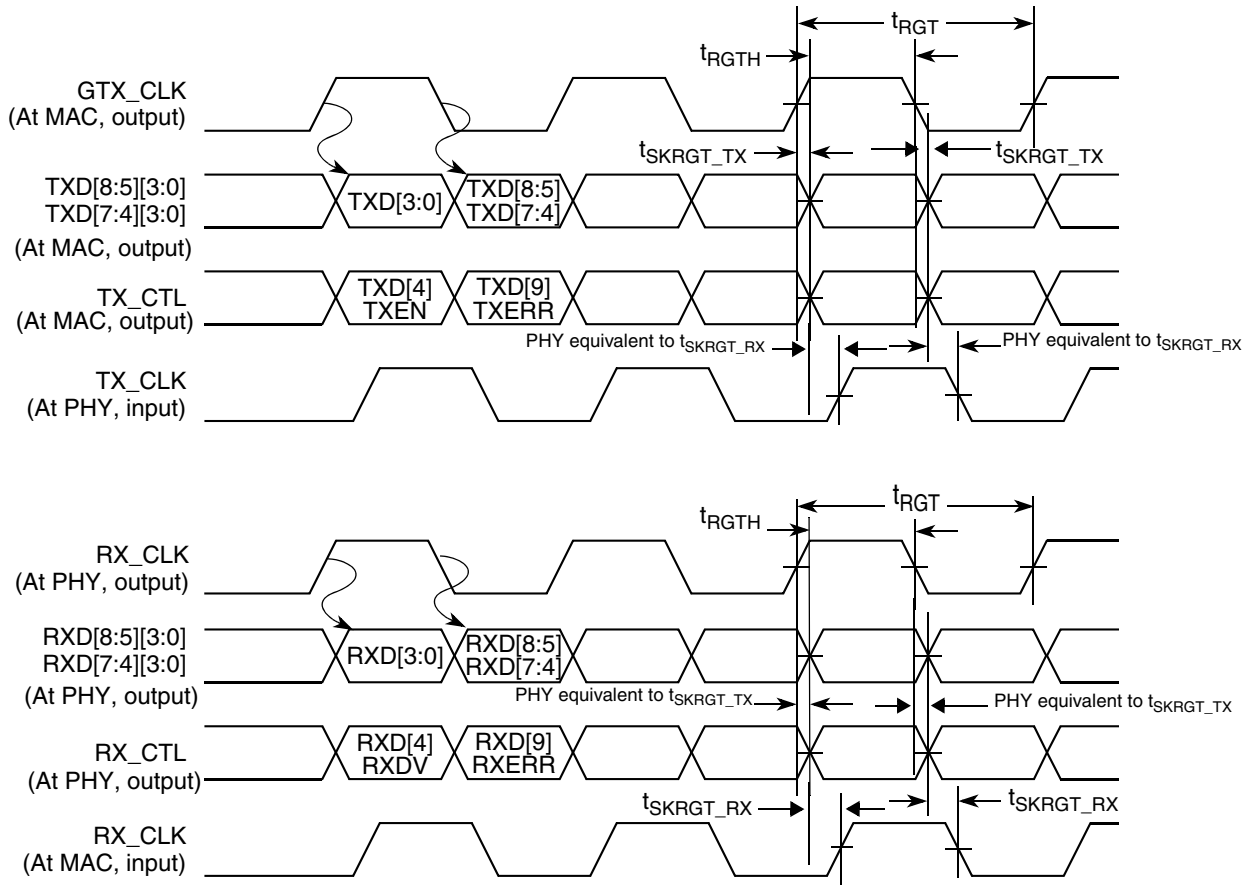


Figure 11. RGMII and RTBI AC timing and multiplexing diagrams

WARNING

Freescale guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

2.11.2 SGMII Interface electrical characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes interface of P1010, as shown in Figure 12, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to SGND_SRDS. The reference circuit of the SerDes transmitter and receiver is shown in Figure 43.

2.11.2.1 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.11.2.1.1 DC requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.21.2.2, "DC level requirement for SerDes reference clocks."

2.11.2.1.2 SGMII transmit DC Timing specifications

This table describes the SGMII SerDes transmitter AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX[n] and $\overline{\text{SD}n\text{\_TX}}$[n]), as shown in Figure 12.

Table 32. SGMII DC transmitter electrical characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output high voltage	V_{OH}	—	—	$XV_{DD\_SRDS2\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\_SRDS2\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output differential voltage[2, 3, 4]	$\lvert V_{OD}\rvert$	304	475	689	mV	Equalization setting: 1.0x
		279	436	632		Equalization setting: 1.09x
		254	396	574		Equalization setting: 1.2x
		229	357	518		Equalization setting: 1.33x
		202	316	459		Equalization setting: 1.5x
		178	277	402		Equalization setting: 1.71x
		152	237	344		Equalization setting: 2.0x
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Note:

1. This does not align to DC-coupled SGMII.
2. $\lvert V_{OD}\rvert = \lvert V_{SD2\_TXn} - V_{\overline{SD2\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes lanes A and B) or XMITEQ**EF** (for SerDes lanes E and E) bit field of P1010's SerDes 2 Control Register:
4. The MSB (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
5. The LSB (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
6. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500 mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TX[n] and SD_TX[n].

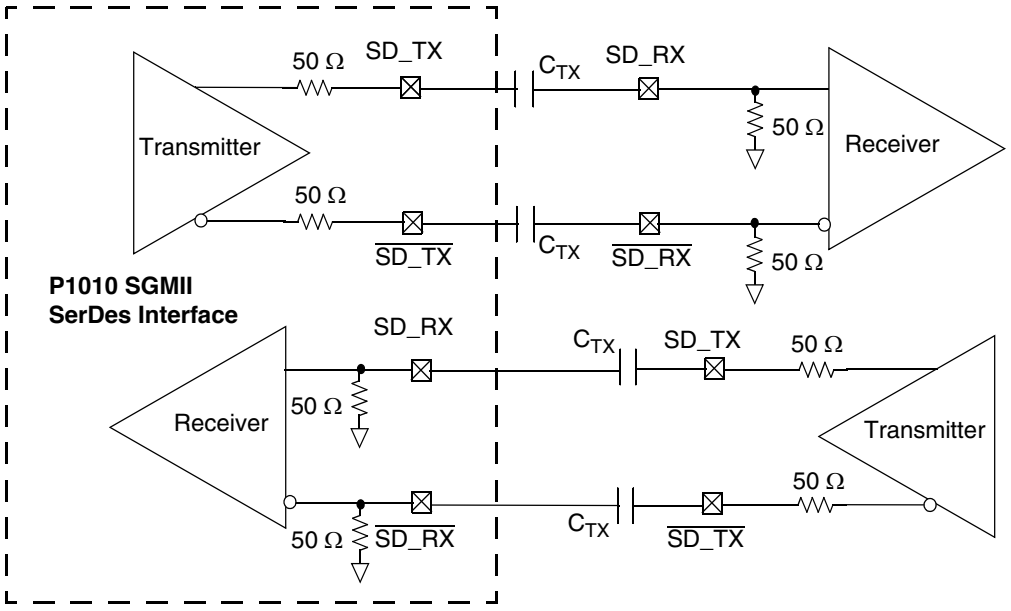


Figure 12. 4-Wire AC-coupled SGMII serial link connection example

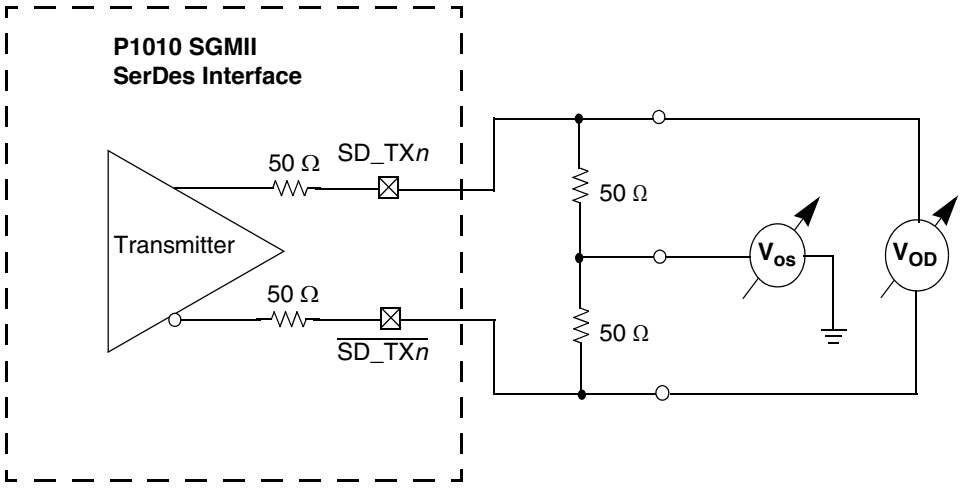


Figure 13. SGMII transmitter DC measurement circuit

2.11.2.1.3 SGMII DC receiver timing specification

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. The clock is recovered from the data.

Table 33. SGMII DC receiver electrical characteristics[5]

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
DC Input voltage range	—	N/A			—	1

Table 33. SGMII DC receiver electrical characteristics[5] (continued)

For recommended operating conditions, see Table 3.

Parameter		Symbol	Min	Typ	Max	Unit	Note
Input differential voltage	LSTS = 001	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	LSTS = 100		175	—			
Loss of signal threshold	LSTS = 001	VLOS	30	—	100	mV	3, 4
	LSTS = 100		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Note:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. See Section Table 67., "PCI Express (2.5 Gb/s) differential receiver (RX) input DC specifications section for further explanation.
4. The LSTS shown in the table refers to the EIC2[0:2] or EIC3[0:2] bit field of P1010's SerDes Control Register.
5. The supply voltage is 1 V.

2.11.2.2 SGMII AC timing specifications

This section describes the AC timing specifications for the SGMII interface.

2.11.2.2.1 AC requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Note that the SGMII clock requirements for SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.21.2.3, "AC requirements for SerDes reference clocks."

2.11.2.2.2 SGMII transmit AC timing specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter

Table 34. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS} = 1V ± 50mV

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	—
Unit Interval	UI	799.92	800	800.08	ps	—
AC coupling capacitor	C_{TX}	5	100	200	nF	3

Note:
1. Each UI is 800 ps ± 100 ppm.
2. See Figure 15 for single frequency sinusoidal jitter limits.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.11.2.2.3 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD\_TX}}$[n]) or at the receiver inputs (SD_RX[n] and $\overline{\text{SD\_RX}}$[n]) as depicted in Figure 14, respectively.

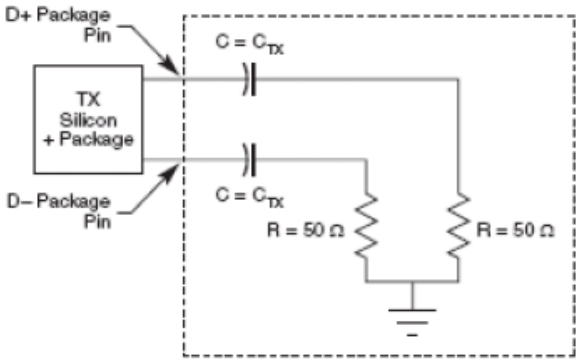


Figure 14. SGMII AC test/measurement load

2.11.2.2.4 SGMII receiver AC timing specifications

This table provides the SGMII receive AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 35. SGMII receive AC timing specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1 V ± 50 mV

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1, 2
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit interval	UI	799.92	800	800.08	ps	3

Note:

1. Measured at receiver
2. See RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Each UI is 800 ps ± 100 ppm.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

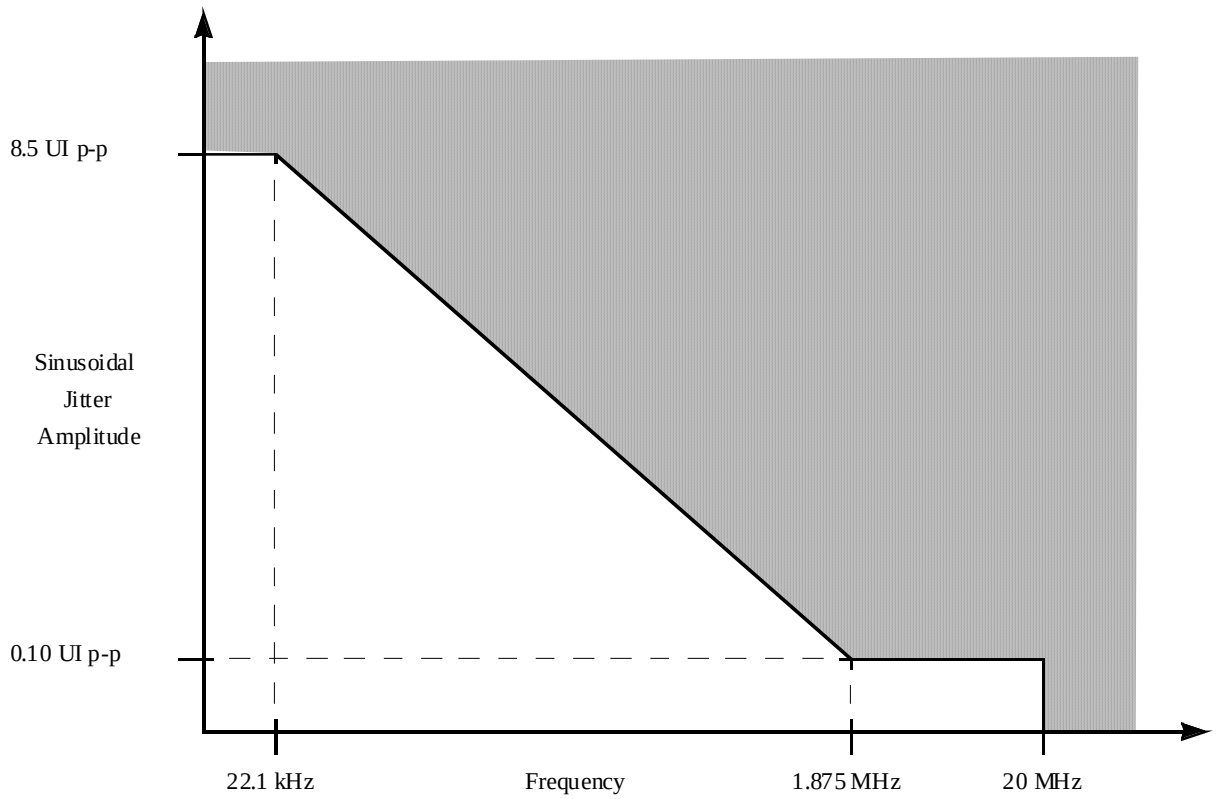


Figure 15. Single frequency sinusoidal jitter limits

2.11.3 MII management

This section provides electrical and thermal design recommendations for successful application of the P1010.

2.11.3.1 MII management DC electrical characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Table 36. MII management DC electrical characteristics

At recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	10	μA	1, 2

Table 36. MII management DC electrical characteristics

At recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	—

Note:

1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. In this case, the symbol V_{IN} represents the LV_{IN} and TV_{IN} symbols referenced in Table 3.

2.11.3.1.1 MII management AC electrical specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16*t_{plb\_clk}) - 3$	—	$(16*t_{plb\_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the platform (CCB) clock.

This figure shows the MII management interface timing diagram.

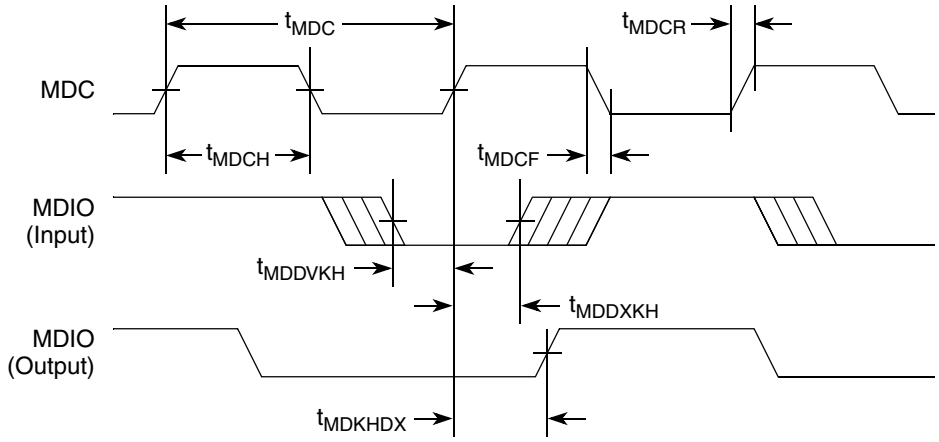


Figure 16. MII management interface timing diagram

2.11.4 eTSEC IEEE Std 1588™ timing specifications

2.11.4.1 eTSEC IEEE Std 1588 DC electrical characteristics

This table shows the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 38. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3..
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3..

2.11.5 eTSEC IEEE 1588 AC specifications

This table provides the IEEE 1588 AC timing specifications.

Table 39. eTSEC IEEE 1588 AC timing specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	t_{CCB}/2	—	T_{RX_CLK}*7	ns	1, 3, 4
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—

Table 39. eTSEC IEEE 1588 AC timing specifications (continued)

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2 x $t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	2*$t_{T1588CLK\_MAX}$	—	—	ns	2

Note:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *P1010 QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *P1010 QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns respectively.
4. t_{CCB} denotes the clock period of system clock (CCB).

This figure shows the data and command output AC timing diagram.

NOTE

In the following figure, the output delay is counted by starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

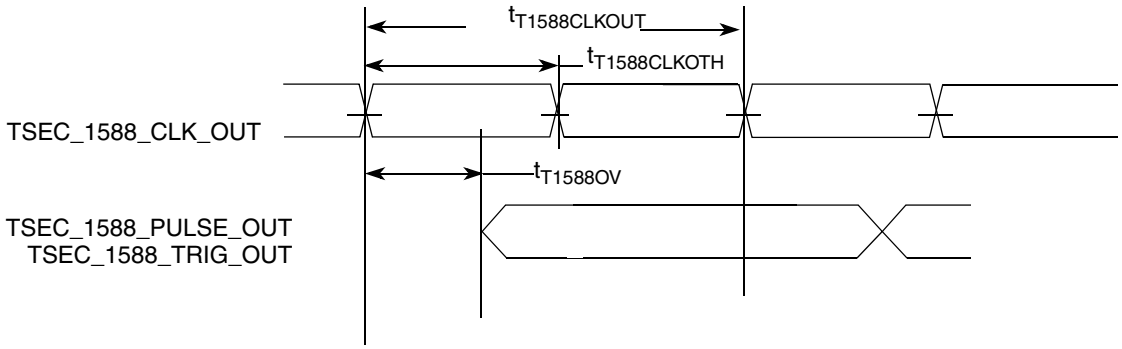


Figure 17. eTSEC IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

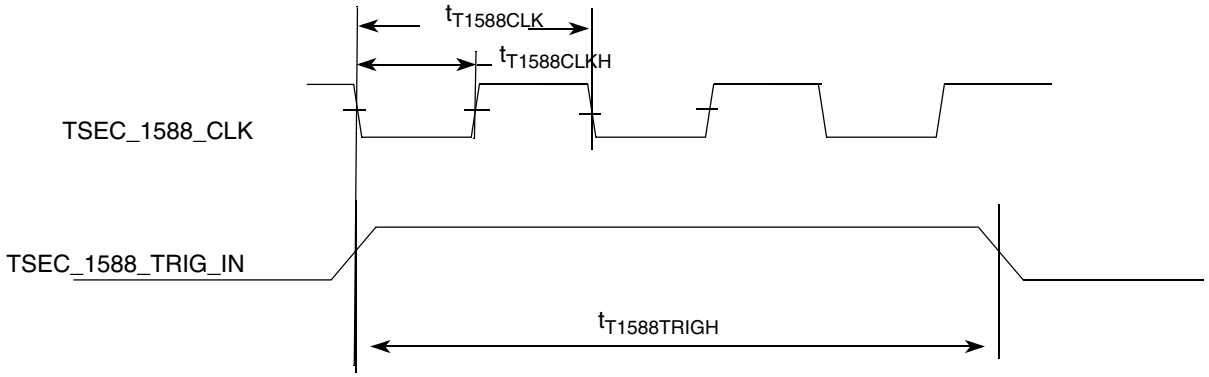


Figure 18. eTSEC IEEE 1588 input AC timing

2.12 USB

This section provides the AC and DC electrical specifications for the USB interface.

2.12.1 USB DC electrical characteristics

This table provides the DC electrical characteristics for the ULPI interface when operating at BV_{DD} = 3.3 V.

Table 40. USB DC electrical characteristics (3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the ULPI interface when operating at BV_{DD} = 2.5 V.

Table 41. USB DC electrical characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—

Table 41. USB DC electrical characteristics (2.5 V) (continued)

For recommended operating conditions, see Table 3.

Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the ULPI interface when operating at BV_{DD} = 1.8 V.

Table 42. USB DC Electrical characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.12.2 USB AC electrical specifications

This table describes the general timing parameters of the USB interface of the device.

Table 43. USB general timing parameters (ULPI Mode Only)[6]

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Table 43. USB general timing parameters (ULPI Mode Only)[6] (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.
6. When switching the data pins from outputs to inputs using the USBn_DIR pin, the output timings will be violated on that cycle because the output buffers are tristated asynchronously. This should not be a problem, because the PHY should not be functionally looking at these signals on that cycle as per ULPI specifications.

These two figures provide the USB AC test load and signals, respectively.

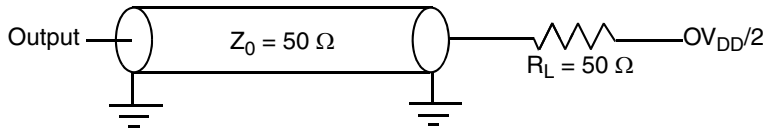


Figure 19. USB AC test load

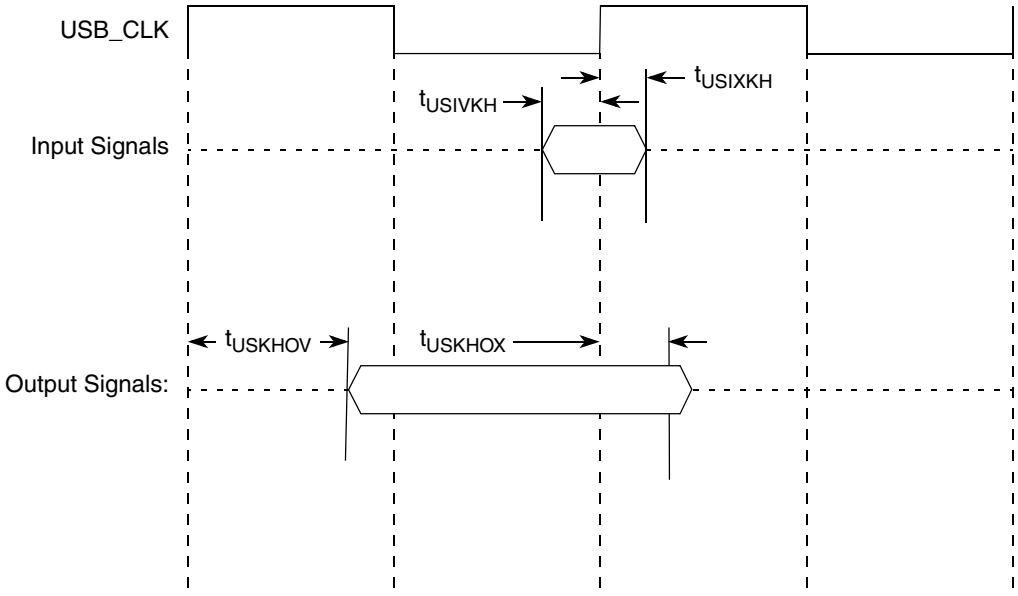


Figure 20. USB signals

This table provides the USB clock input (USB_CLK) AC timing specifications.

Table 44. USB_CLK AC timing specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	Steady state	$f_{USB\_CLK\_IN}$	59.97	60	60.03	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.05	0	0.05	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

2.12.3 On-chip USB PHY

This section describes the AC electrical specifications for the on-chip USB PHY. See Chapter 7 in the USB Specifications, Rev. 2, for more information.

This table provides the USB clock input (USBPHY_CLK) AC timing specifications.

Table 45. USBPHY_CLK AC Timing specifications

For recommended operating conditions, see Table 3.

Parameter	Conditions	Symbol[1]	Min	Max	Unit	Note
Frequency range	Steady state	$f_{USB\_CLK\_IN}$	24	24	MHz	—
Rise/Fall time	—	t_{USRF}	—	6	ns	—
Clock frequency tolerance	—	t_{CLK_TOL}	–0.005	+0.005	%	—
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	60	%	—
Total input jitter/time interval error	RMS value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	5	ps	—

2.12.4 IBIAS_REXT filter

Following filter circuit must be implemented on IBIAS_REXT pin.

Filter component should be placed as much close to SoC pin as possible.

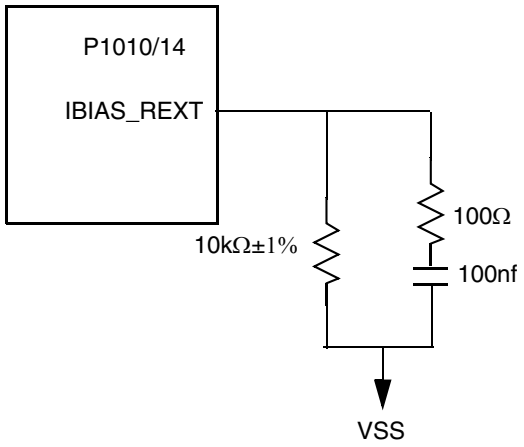


Figure 21. IBIAS_REXT filter circuit

2.12.5 Threshold detect increase

Following register programming should be performed during USB PHY initialization

1. Read S1[26:31]
2. Set C1[8] and C1[9] to '1'
3. Write C2[11] = 1 and C2[13:15] = S1[29:31] and C2[16:18] = S1[26:28]

where C1 is the register at (CCSRBAR + 0xe5000), C2 is the register at (CCSRBAR + 0xe5004) and S1 is the register at (CCSRBAR + 0xe5014).

2.13 Integrated flash controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

2.13.1 Integrated flash controller DC electrical characteristics

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 3.3 V.

Table 46. Integrated flash controller DC electrical characteristics (3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.8	—	V	—
Output low voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Table 46. Integrated flash controller DC electrical characteristics (3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 2.5 V.

Table 47. Integrated flash controller DC electrical characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 1.8 V.

Table 48. Integrated Flash controller DC electrical characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

2.13.2 Integrated flash controller AC Timing specifications

This section describes the AC timing specifications for the integrated flash controller.

2.13.2.1 Integrated flash controller AC timing specifications

All output signal timings are relative to the falling edge of any IFC_CLK. The external circuit must use the rising edge of the IFC_CLKs to latch the data. All input timings are relative to the rising edge of IFC_CLKs.

This table describes the timing specifications of the integrated flash controller interface.

Table 49. Integrated Flash controller timing specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
IFC_CLK cycle time	t_{IBK}	10	—	ns	—
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	—
IFC_CLK[n] skew to IFC_CLK[m]	$t_{IBKSKEW}$	—	150	ps	2
Input setup	t_{IBIVKH}	4	—	ns	—
Input hold	t_{IBIXKH}	1	—	ns	—
Output delay (Except AVD)	$t_{IBKLOV1}$	—	1.5	ns	—
Output delay (For AVD)	$t_{IBKLOV2}$	—	1	ns	—
Output hold	t_{IBKLOX}	–2	—	ns	5
IFC_CLK to output high impedance for AD	t_{IBKLOZ}	—	2	ns	3
AVD output negation to AD output transition (LATCH hold time)	t_{IBONOT}	0.5	—	ns	4

Note:
1. All signals are measured from $BV_{DD}/2$ of the rising/falling edge of IFC_CLK to $BV_{DD}/2$ of the signal in question.
2. Skew is measured between different IFC_CLK signals at $BV_{DD}/2$.
3. For the purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{IBONOT} is a measurement of the maximum time between the negation of AVD and any change in AD when FTIM0_CSn[TEAHC]=0.
5. Here the negative sign means output transit happens earlier than the falling edge of IFC_CLK.

2.13.2.2 Test condition

This figure provides the AC test load for the integrated flash controller.

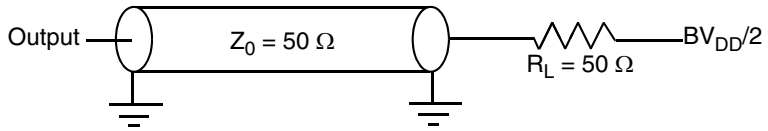


Figure 22. Integrated flash controller AC Test load

This figure shows the AC timing diagram.

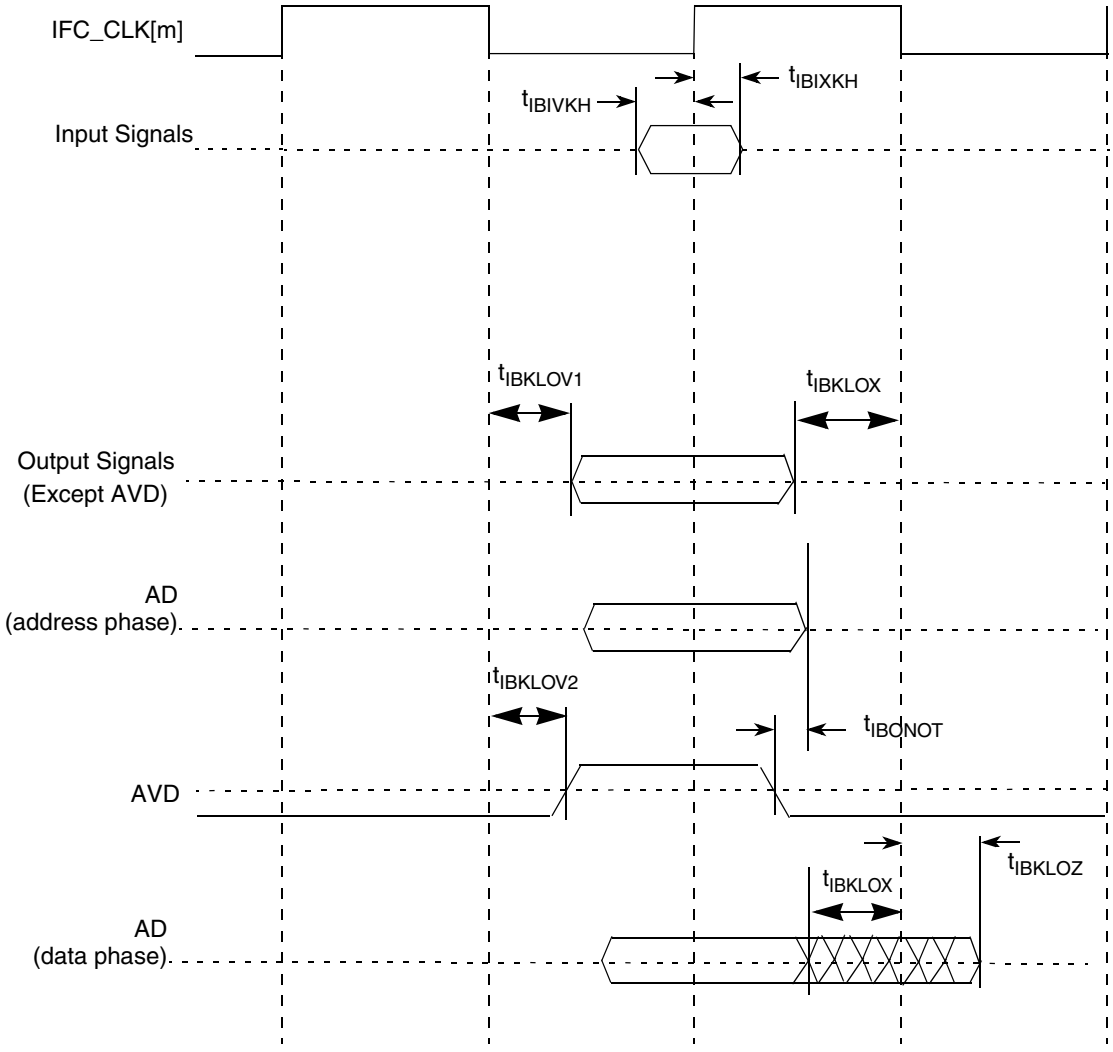


Figure 23. Integrated flash controller signals

This figure applies to all the controllers that IFC supports.

For input signals, the AC timing data is used directly for all controllers. For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

This figure shows how the AC timing diagram applies to GPCM. The same principle also applies to other controllers of IFC.

NOTE

In the following figure, t_{aco}, t_{rad}, t_{eahc}, t_{eadc}, t_{acse}, t_{cs}, t_{ch}, t_{wp} are programmable. See the P1010 reference manual.
For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

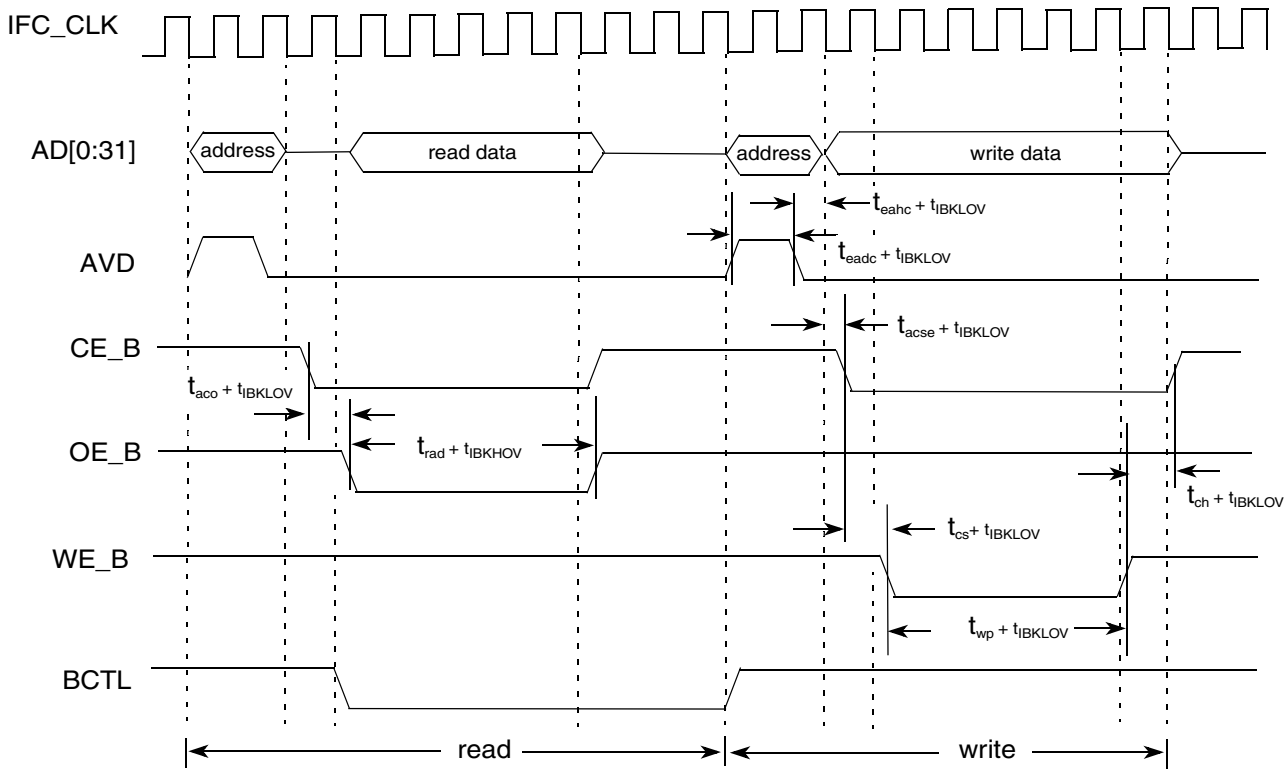


Figure 24. GPCM output timing diagram

2.14 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the P1010.

2.14.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the P1010.

Table 50. eSDHC interface DC electrical characteristics

At recommended operating conditions with BV_{DD} = 3.3 V or 1.8V

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	0.625 × BV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × BV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 uA at BV_{DD}min	0.75 × BV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100uA at BV_{DD}min	—	0.125 × BV_{DD}	V	—
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.

2.14.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in Figure 26.

Table 51. eSDHC AC Timing Specifications

At recommended operating conditions with BV_{DD} = 3.3 V or 1.8V

Parameter	Symbol	Min	Max	Unit	Note
SDHC_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SFSCK}	0	 25/50 20/52	MHz	2, 4
SDHC_CLK clock low time—Full-speed/High-speed mode	t_{SFSCKL}	10/7	—	ns	4
SDHC_CLK clock high time—Full-speed/High-speed mode	t_{SFSCKH}	10/7	—	ns	4
SDHC_CLK clock rise and fall times	t_{SFSCKR}/ t_{SFSCKF}	—	3	ns	4
Input setup times: SDHC_CMD, SDHC_DAT_x, SDHC_CD to SDHC_CLK	$t_{SFSIVKH}$	2.5	—	ns	4
Input hold times: SDHC_CMD, SDHC_DAT_x, SDHC_CD to SDHC_CLK	$t_{SFSIXKH}$	2.5	—	ns	3,4
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DAT_x valid	$t_{SHSKHOV}$	–3	3	ns	4

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52 MHz for a MMC card.
3. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF

This figure provides the eSDHC clock input timing diagram.

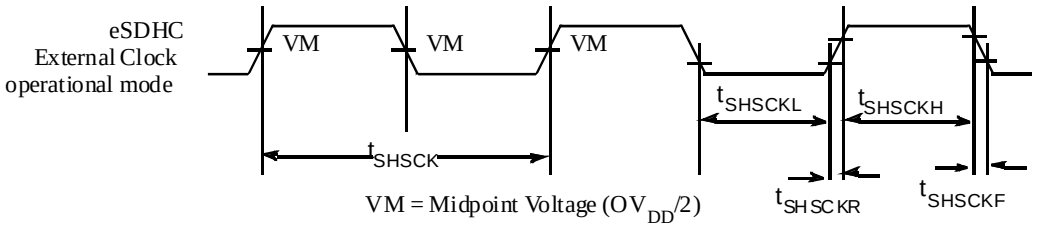


Figure 25. eSDHC Clock input timing diagram

This figure provides the data and command input/output timing diagram.

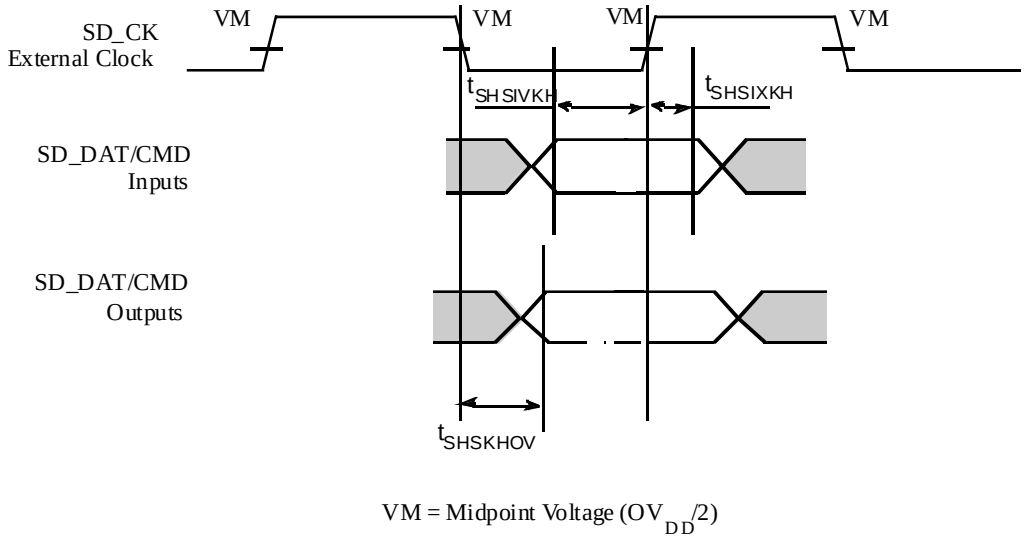


Figure 26. eSDHC data and command input/output timing diagram referenced to clock

2.15 Programmable Interrupt Controller (PIC) specifications

This section describes the DC and AC electrical specifications for PIC on the P1010.

2.15.1 PIC DC electrical characteristics

This table provides the DC electrical characteristics for the PIC interface.

Table 52. PIC DC electrical characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.15.2 PIC AC timing specifications

This table provides the PIC input and output AC timing specifications.

Table 53. PIC input AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs should be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.16 JTAG

This section describes the AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface of the P1010.

2.16.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 54. JTAG DC electrical characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.16.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 27 through Figure 30.

Table 55. JTAG AC timing specifications

For recommended operating conditions see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	2	ns	—

Table 55. JTAG AC timing specifications (continued)

For recommended operating conditions see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}		—	ns	—
Boundary-scan USB only		14			
TDI, and TMS		4			—
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times	t_{JTKLDV}	—		ns	3
Boundary Scan Data			15		
TDO			10		
Output hold times	t_{JTKLDX}	30	—	ns	3
JTAG external clock to output high impedance	t_{JTKLDZ}	4	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs.

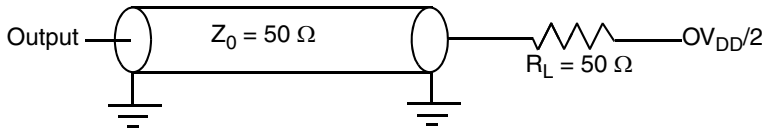


Figure 27. AC Test load for the JTAG interface

This figure provides the JTAG clock input timing diagram.

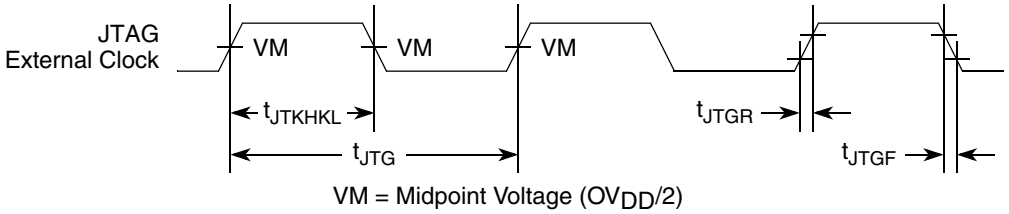


Figure 28. JTAG clock input timing diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

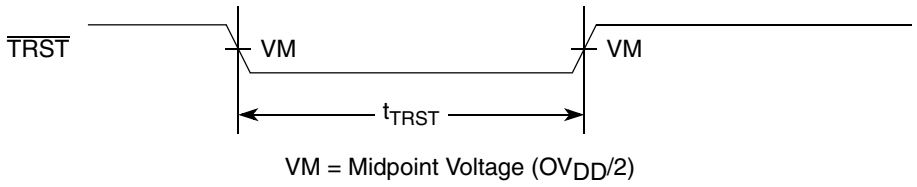


Figure 29. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

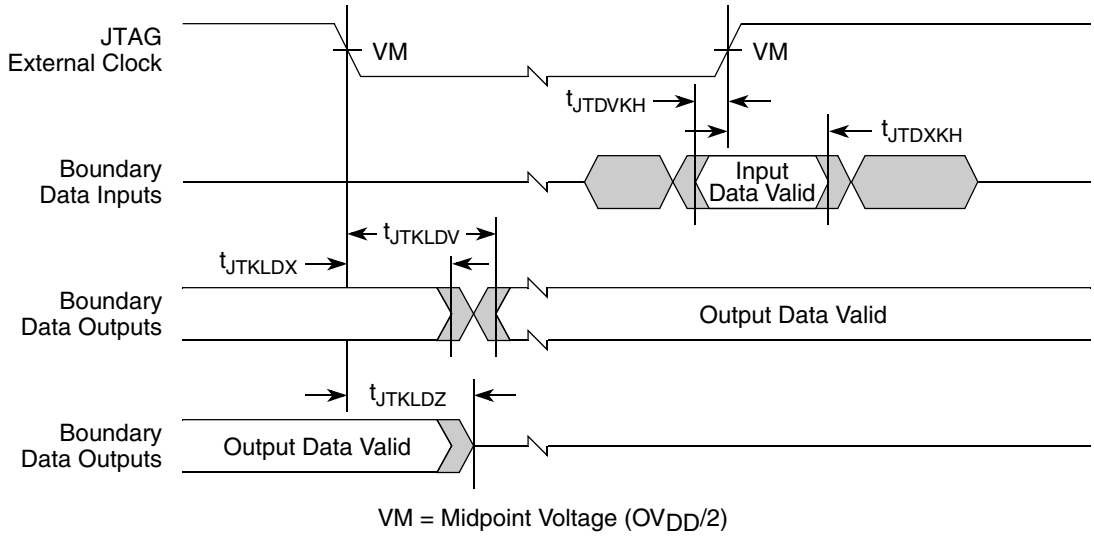


Figure 30. Boundary-scan timing diagram

2.17 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the P1010.

2.17.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interfaces.

Table 56. I²C DC electrical characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output high voltage	V_{OH}	2.4	—	V	—
Output low voltage	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD}(max)	I_I	–10	10	μA	4

Table 56. I^2C DC electrical characteristics (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Capacitance for each I/O pin	C_I	—	10	pF	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the *P1010 QorIQ Integrated Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.17.2 I^2C AC electrical specifications

This table provides the AC timing parameters for the I^2C interfaces.

Table 57. I^2C AC electrical specifications

For recommended operating conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 56)

Parameter	Symbol	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Table 57. I²C AC electrical specifications (continued)

For recommended operating conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 56)

Parameter	Symbol	Min	Max	Unit	Note

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the P1010 provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the P1010 acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the P1010 does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the P1010 as transmitter, application note AN2919 referred to in note 4 below is recommended.
4. The maximum t_{I2OVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

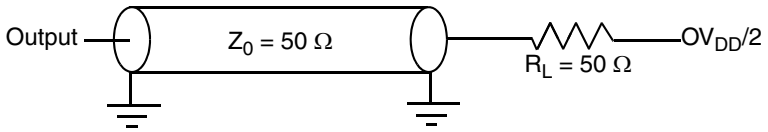


Figure 31. I²C AC test load

This figure shows the AC timing diagram for the I²C bus.

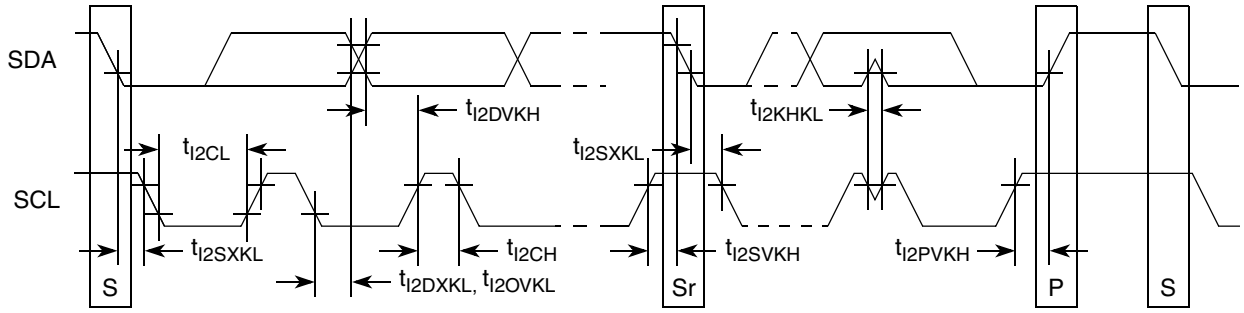


Figure 32. I²C Bus AC timing diagram

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the P1010.

2.18.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for the GPIO interface when operating from 3.3V supply.

Table 58. GPIO_[0:11] DC electrical characteristics (3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{IN}= min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{IN} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from 2.5V supply.

Table 59. GPIO_[12:15] DC electrical characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{IN} = min, I_{OH} = 2 mA)	V_{OH}	1.7	—	V	—
Low-level output voltage (LV_{IN} = min, I_{OL} = 2 mA)	V_{OL}	—	0.7	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the min and max LV_{IN} respective values found in Table 3.
2. The symbol LV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

NOTE

- GPIO_[0:11] are powered by OV_{DD}.
- GPIO_[12:15] are powered by LV_{DD}.

2.18.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 60. GPIO input AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Unit	Note
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

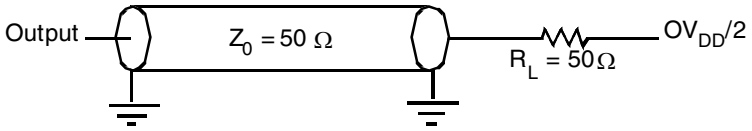


Figure 33. GPIO AC test load

2.19 FlexCAN

This section describes the DC and AC electrical specifications for the FlexCAN interface.

2.19.1 FlexCAN DC electrical characteristics

This table provides the DC electrical characteristics for the FlexCAN interface when operating from a 3.3 V supply.

Table 61. FlexCAN DC electrical characteristics (3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.19.2 FlexCAN AC timing specifications

This table provides the AC timing specifications for the FlexCAN interface.

Table 62. FlexCAN AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Min	Max	Unit	Note
Baud rate	10	1000	Kbps	—

2.20 TDM

This section describes the DC and AC electrical specifications for the TDM of the P1010

2.20.1 TDM DC electrical characteristics

This table provides the DC electrical characteristics TDM.

Table 63. TDM DC electrical characteristics

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	–0.3	0.8	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. The symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.20.2 TDM AC electrical characteristics

This table provides input and output AC timing specifications for TDM interface.

Table 64. TDM AC timing specifications

Parameter/Condition	Symbol	Min	Max	Unit	Note
TDM_TX_CLK/TDM_RX_CLK	t_{DM}	62.5	—	ns	—
TDM_TX_CLK/TDM_RX_CLK rise/fall time	t_{DMR}/t_{DMF}	—	5	ns	—
TDM_TX_CLK/TDM_RX_CLK high pulse width	t_{DM_HIGH}	8.0	—	ns	—
TDM_TX_CLK/TDM_RX_CLK low pulse width	t_{DM_LOW}	8.0	—	ns	—
TDM all input setup time	t_{DMIVKH}	3.0	—	ns	—
TDM_RX_DATA hold time	$t_{DMRDIXKH}$	3.5	—	ns	—
TDM_TFS/TDM_RFS input hold time	$t_{DMFSIXKH}$	2.0	—	ns	2

Table 64. TDM AC timing specifications (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note
TDM_TX_CLK High to TDM_TX_DATA output active	t_{DM_OUTAC}	4.0	—	ns	2
TDM_TX_CLK High to TDM_TX_DATA output valid	$t_{DMTKHOV}$	—	14.0	ns	—
TDM_TX_DATA hold time	$t_{DMTKHOX}$	2.0	—	ns	—
TDM_TX_CLK High to TDM_TX_DATA output high impedance	t_{DM_OUTHI}	—	10.0	ns	—
TDM_TFS/TDM_RFS output valid	$t_{DMFSKHOV}$	—	13.5	ns	—
TDM_TFS/TDM_RFS output hold time	$t_{DMFSKHOX}$	2.5	—	ns	—

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TDMIVKH}$ symbolizes TDM timing (DM) with respect to the time the input signals (I) reach the valid state (V) relative to the TDM Clock, t_{TC}, reference (K) going to the high (H) state or setup time. Also, output signals (O), hold (X).
2. Output values are based on 30 pF capacitive load.
3. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. TDMxTCK and TDMxRCK are shown using the rising edge.

This figure shows the TDM receive signal timing.

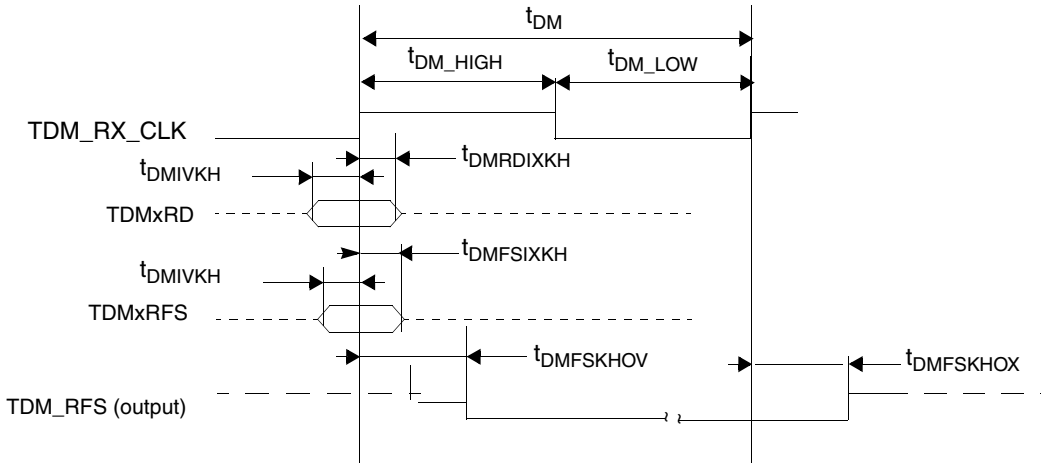


Figure 34. TDM receive signals

This figure shows the TDM transmit signal timing.

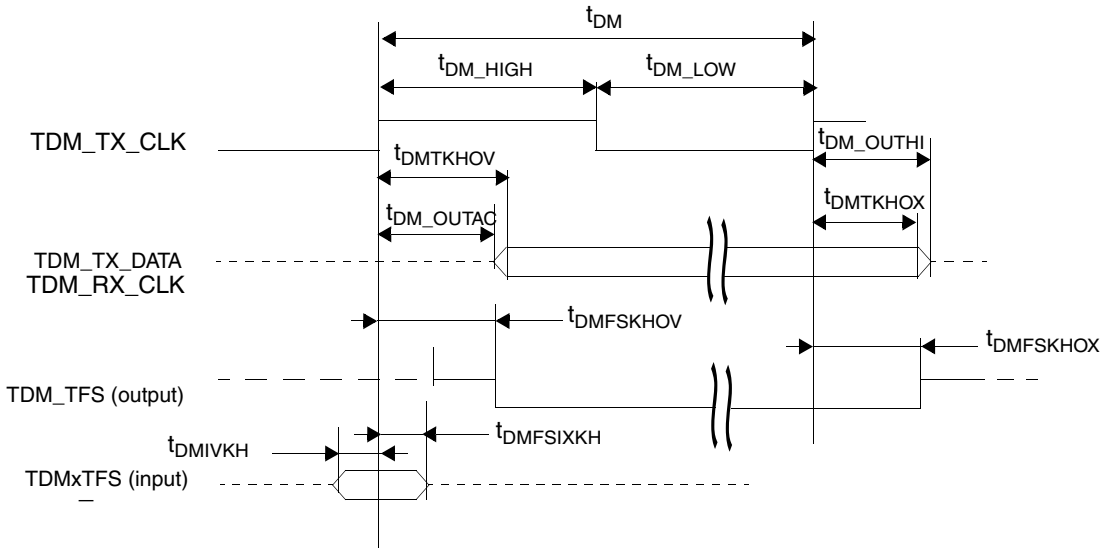


Figure 35. TDM Transmit Signals

2.21 High-Speed Serial Interfaces (HSSI)

The P1010 features one Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express data transfers and for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. This section also shows the SerDes data lane's transmitter and receiver reference circuits.

2.21.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 36 shows how the signals are defined. For the purpose of illustration, only one SerDes lane is used for description. The figure shows the waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{\_TX}}$, SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's Single-Ended Swing.
2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.
3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

   The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.
4. **Differential Peak Voltage, V_{DIFFp}**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

6. **Differential Waveform**

   The differential waveform is constructed by subtracting the inverting signal (SD*n*_TX, for example) from the non-inverting signal (SD*n*_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 36 as an example for differential waveform.

7. **Common Mode Voltage, V_{cm}**

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, V_{cm_out} = (VSD*n*_TX + VSD*n*_TX)/2 = (A + B) / 2, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may even be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset occasionally.

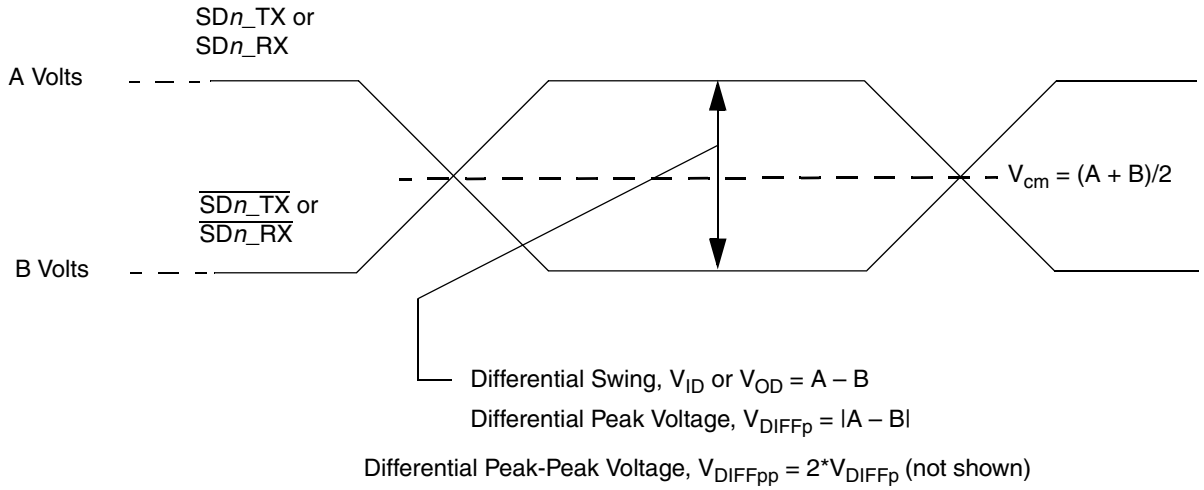


Figure 36. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.21.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SD_REF_CLK and $\overline{SD\_REF\_CLK}$ for PCI Express and SGMII interface.

The following sections describe the SerDes reference clock requirements and some application information.

2.21.2.1 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

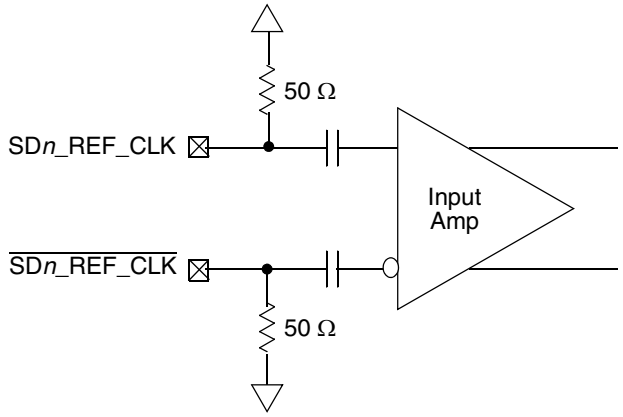


Figure 37. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 2 and Table 3.
- SerDes reference clock receiver reference circuit structure:
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 37. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to SGND_SRDS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range:
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

2.21.2.2 DC level requirement for SerDes reference clocks

The DC level requirement for the P1010 SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For **external DC-coupled** connection, as described in Section 2.21.2.1, "SerDes reference clock receiver characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 38 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS). Figure 39 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

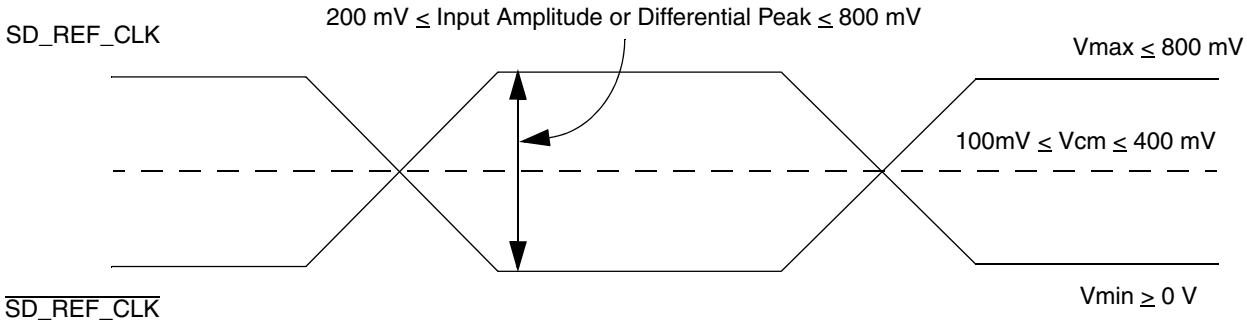


Figure 38. Differential reference clock input DC requirements (external DC-coupled)

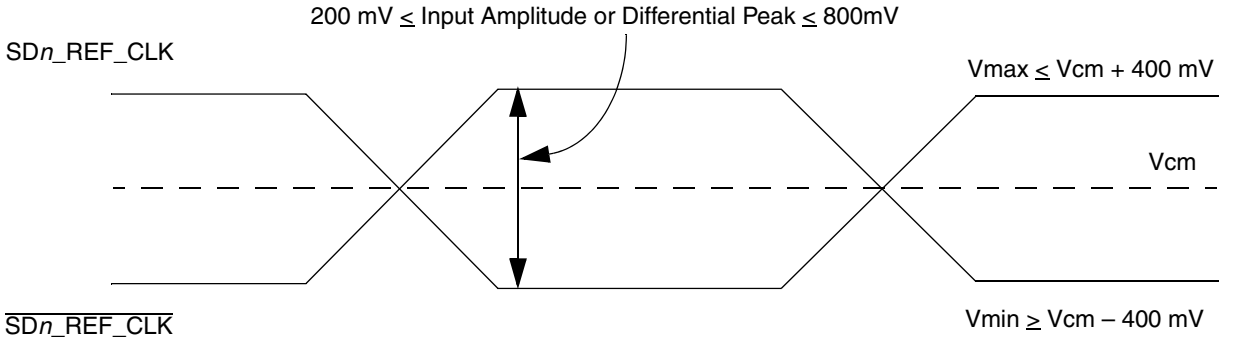


Figure 39. Differential Reference clock input DC requirements (external AC-coupled)

- **Single-ended Mode**
  — The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 40 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use

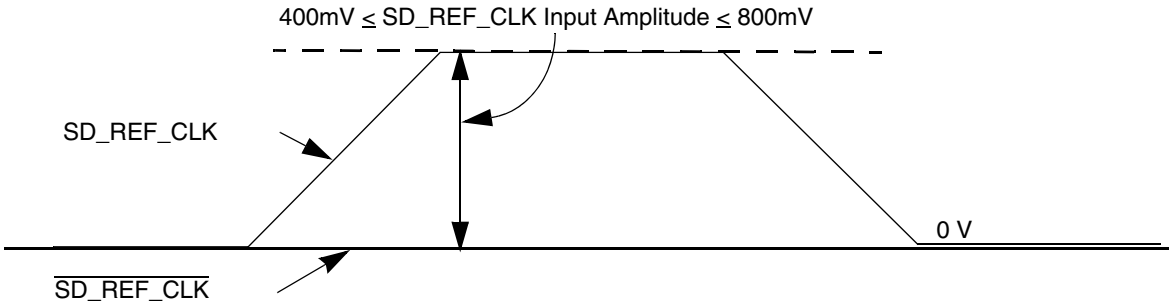


Figure 40. Single-Ended reference clock input DC requirements

2.21.2.3 AC requirements for SerDes reference clocks

This table lists the AC requirements, for the PCI Express and SGMII SerDes reference clocks, that should be guaranteed by the customer's application design.

Table 65. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ input clock requirements

Parameter	Symbol	Min	Typ	Max	Unit	Note
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	-350	—	+350	ppm	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	4
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak Jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (Peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD*n*_REF_CLK) to falling edge rate (SD*n*_REF_CLK) matching	Rise-Fall Matching	—	—	20	%	5, 6

Table 65. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ input clock requirements (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note

Note:

1. Only 100/125 have been tested. Other in-between values do not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus SDn_REF_CLK).The signal must be monotonic through the measurement region for rise and fall time. The 400-mV measurement window is centered on the differential zero crossing.
4. Measurement is taken from the differential waveform.
5. Measurement is taken from the single-ended waveform.
6. Matching applies to the rising edge for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 42.

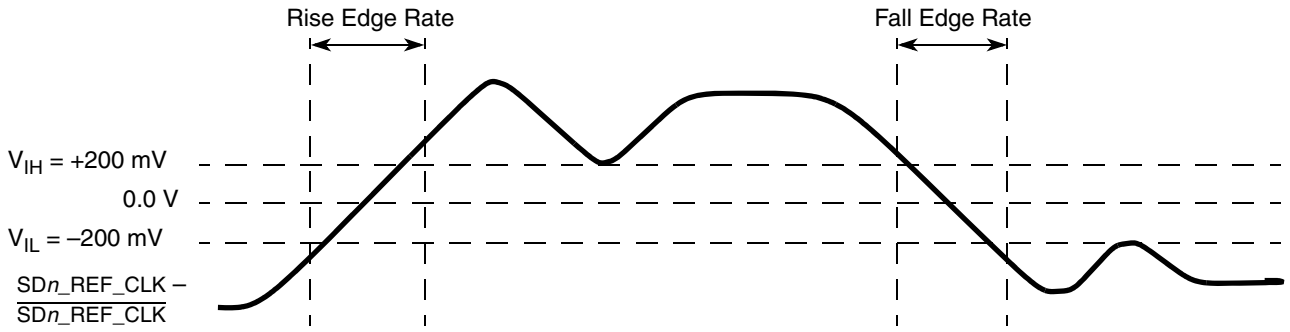


Figure 41. Differential measurement points for rise and fall time

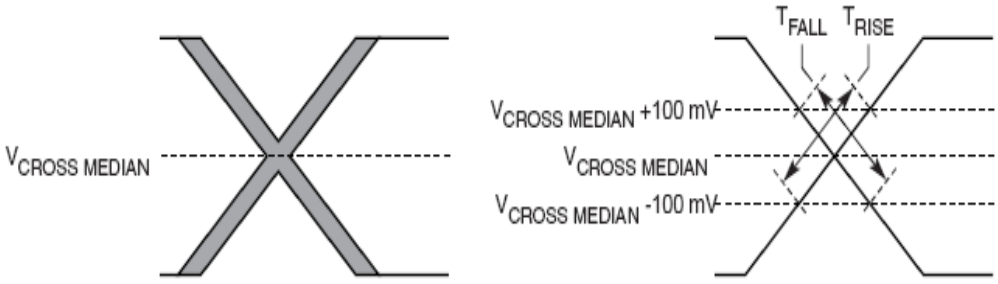


Figure 42. Single-ended measurement points for rise and fall time matching

2.21.2.4 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

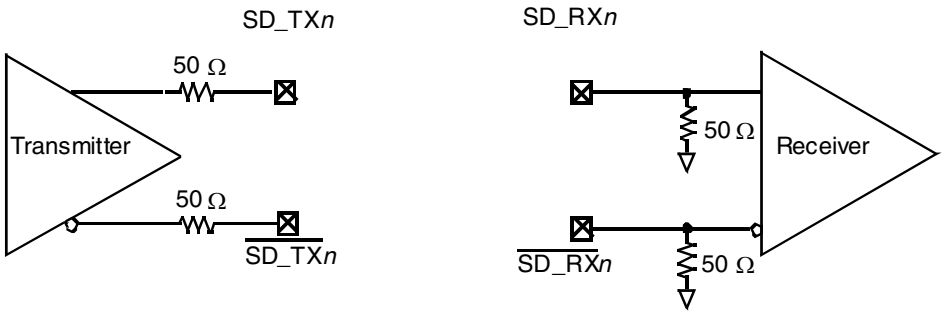


Figure 43. SerDes transmitter and receiver reference circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below, based on the application usage:

- Section 2.22, "PCI Express"
- Section 2.23, "Serial ATA (SATA)"
- Section 2.11.2, "SGMII Interface electrical characteristics"

Note that external AC Coupling capacitor is required for the above three serial transmission protocols per the protocol's standard requirements.

2.22 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the P1010.

2.22.1 DC requirements for PCI Express SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 2.21.2.2, "DC level requirement for SerDes reference clocks."

2.22.2 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.22.2.1 PCI Express DC physical layer transmitter specifications

This section discusses PCI Express DC physical layer transmitter specifications for 2.5 Gb/s.

This table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 66. PCI Express (2.5Gb/s) Differential transmitter (TX) output DC specifications

For recommended operating conditions, see Table 3.

Symbol	Parameter	Min	Typical	Max	Unit	Comments
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$. See Note 1.

Table 66. PCI Express (2.5Gb/s) Differential transmitter (TX) output DC specifications (continued)

For recommended operating conditions, see Table 3.

Symbol	Parameter	Min	Typical	Max	Unit	Comments
$V_{TX-DE-RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	50	60	Ω	Required TX D+ as well as D- DC Impedance during all states

Note:

1. Specified at the measurement point into a timing and voltage compliance test load, as shown in Figure 44, and measured over any 250 consecutive TX UIs.

2.22.2.2 PCI Express DC physical layer receiver specifications

This section discusses PCI Express DC physical layer receiver specifications for 2.5 Gb/s.

This table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 67. PCI Express (2.5 Gb/s) differential receiver (RX) input DC specifications

For recommended operating conditions, see Table 3.

Symbol	Parameter	Min	Typical	Max	Unit	Comments
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	175	—	1200	mV	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$. See Note 1.
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 2
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	50 k	—	—	Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 3.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	235	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the Receiver

Note:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 44 should be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
3. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

2.22.3 PCI Express AC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.22.3.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5Gb/s.

This table defines the PCI Express (2.5Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 68. PCI Express (2.5Gb/s) differential transmitter (TX) output AC specifications

Symbol	Parameter	Min	Typical	Max	Unit	Comments
UI	Unit Interval	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
T_{TX-EYE}	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load, as shown in Figure 44, and measured over any 250 consecutive TX UIs.
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. P1010 SerDes transmitter does not have CTX built-in. An external AC Coupling capacitor is required.

2.22.3.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 Gb/s.

This table defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 69. PCI Express (2.5 Gb/s) Differential Receiver (rx) input AC specifications

Symbol	Parameter	Min	Typical	Max	Unit	Comments
UI	Unit Interval	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.

Table 69. PCI Express (2.5 Gb/s) Differential Receiver (rx) input AC specifications (continued)

Symbol	Parameter	Min	Typical	Max	Unit	Comments
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}= 0.6 UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 4.

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 44 should be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.22.3.3 Compliance test and measurement load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in this figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

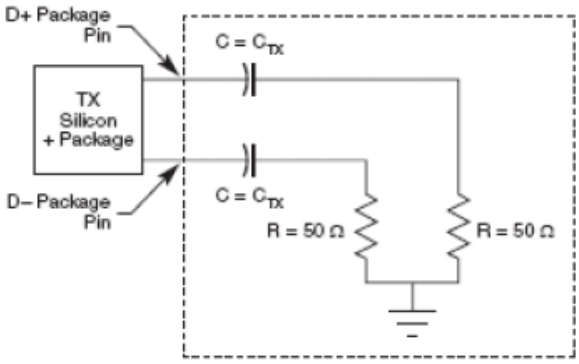


Figure 44. Compliance Test/Measurement Load

2.23 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) interface.

2.23.1 SATA DC Electrical characteristics

This section describes the DC electrical characteristics for SATA.

2.23.1.1 SATA DC transmitter output characteristics

This table provides the DC differential transmitter output DC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 70. Gen1i/1.5G transmitter (Tx) DC specifications

At recommended operating conditions with SDx_AV_{DD} = 1.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Tx differential output voltage	V_{SATA_TXDIFF}	400	475	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	2

Note:
1. Terminated by 50 Ω load.
2. DC impedance

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 71. Gen 2i/3G transmitter (Tx) DC specifications

At recommended operating conditions with SDx_AV_{DD} = 1.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Tx diff output voltage	V_{SATA_TXDIFF}	400	522.5	700	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Table 71. Gen 2i/3G transmitter (Tx) DC specifications (continued)

At recommended operating conditions with SDx_AV_{DD} = 1.

Parameter	Symbol	Min	Typ	Max	Unit	Note

Note:
1. Terminated by 50 Ω load.

2.23.1.2 SATA DC receiver (Rx) input characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 72. Gen1i/1.5 G receiver (Rx) input DC specifications

At recommended operating conditions with SDx_AV_{DD} = 1.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{SATA_RXDIFF}	240	475	600	mV p-p	1
Differential Rx input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	—
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	5

Note:
1. Voltage relative to common of either signal comprising a differential pair

This table provides the Gen2i or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 73. Gen2i/3 G receiver (Rx) input DC specifications

At recommended operating conditions with SDx_AV_{DD} = 1.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{SATA_RXDIFF}	275	475	750	mV p-p	1
Differential Rx input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	275	mV p-p	2

Note:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

2.23.2 SATA AC timing specifications

This section discusses the SATA AC timing specifications.

2.23.2.1 AC requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in this table to be guaranteed by the customer's application design.

Table 74. SATA Reference clock input requirements

At recommended operating conditions with SDx_AV_{DD} = 1

Parameter	Symbol	Min	Typ	Max	Unit	Note
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125/150	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	+350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	2
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter, phase jitter (peak-peak)	t_{CLK_PJ}	–50	—	+50	ps	2, 3, 4

Note:
1. **Caution:** Only 100, 125, and 150 MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}
4. Total peak-to-peak deterministic jitter should be less than or equal to 50 ps.

This figure shows the reference clock timing waveform.

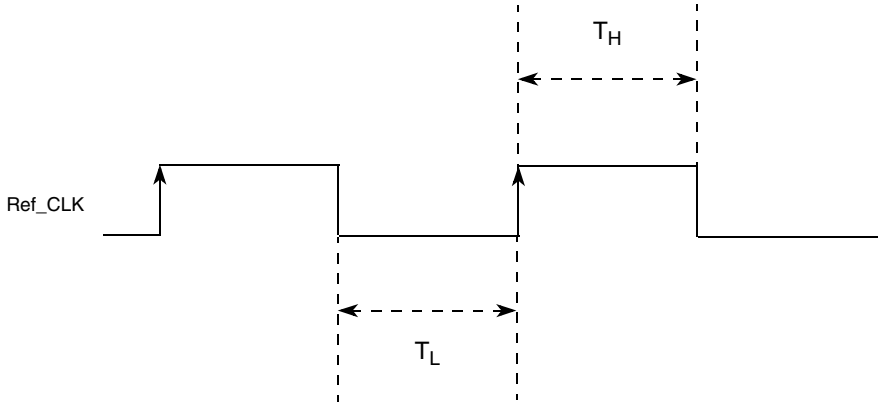


Figure 45. Reference clock timing waveform

2.23.3 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 75. Gen1i/1.5 G transmitter (Tx) AC specifications

At recommended operating conditions with SDx_AV_{DD} = 1

Parameter	Symbol	Min	Typ	Max	Unit	Note
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.22	UI p-p	1

Note:

1. Measured at Tx output pins peak to peak phase variation, random data pattern.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 76. Gen 2i/3 G transmitter (Tx) AC specifications

At recommended operating conditions with SDx_AV_{DD} = 1

Parameter	Symbol	Min	Typ	Max	Unit	Note
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.3	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.17	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at Tx output pins peak-to-peak phase variation, random data pattern

2.23.4 AC differential receiver input characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 77. Gen 1i/1.5G receiver (Rx) AC specifications

At recommended operating conditions with SDx_AV_{DD} = 1

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.35	UI p-p	1

Note:
1. Measured at receiver

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 78. Gen 2i/3G receiver (Rx) AC specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.46	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.35	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:
1. Measured at receiver

3 Hardware design considerations

3.1 System clocking

This section describes the PLL configuration of the P1010. Note that the platform clock is identical to the internal Core Complex Bus (CCB) clock.

This device includes 6 PLLs, as follows:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, “Platform to SYSCLK PLL ratio.”

- The e500 core PLL generates the core clock from the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 3.1.3, "e500 core to platform clock PLL ratio."
- The DDR PLL generates the clocking for the DDR SDRAM controller. The frequency ratio between DDR clock and platform clock is selected using the DDR PLL ratio configuration bits as described in section Section 3.1.4, "DDR/SYSCLK PLL ratio."
- Each of the two SerDes blocks has a PLL.
- USB PHY PLL generates the clocking for internal USB PHY.

3.1.1 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory.

Table 79. Processor clocking specifications

Characteristic	Maximum Frequency		Unit	Note
	Min	Max		
e500 core processor frequency	400	1000	MHz	1, 2, 3
Platform CCB bus clock frequency	267	400	MHz	1, 4, 5

Note:

1. **Caution:** The platform clock to SYSCLK ratio and e500 core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 3.1.2, "Platform to SYSCLK PLL ratio," and Section 3.1.3, "e500 core to platform clock PLL ratio," and Section 3.1.4, "DDR/SYSCLK PLL ratio," for ratio settings.
2. The minimum e500 core frequency is based on the minimum platform clock frequency of 267 MHz.
3. The reset config signal cfg_core_speed must be pulled low if the core frequency is 500MHz or below.
4. These values are preliminary and subject to change.
5. The reset config signal cfg_plat_speed must be pulled low if the CCB bus frequency is lower than 300 MHz.

3.1.1.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode.

This table provides the clocking specifications for the memory bus.

Table 80. Memory Bus Clocking specifications

Characteristic	Min	Max	Unit	Note
Memory bus clock frequency	333	400	MHz	1, 2, 3

Note:

1. **Caution:** The platform clock to SYSCLK ratio and e500 core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Section 3.1.2, "Platform to SYSCLK PLL ratio," and Section 3.1.3, "e500 core to platform clock PLL ratio," and Section 3.1.4, "DDR/SYSCLK PLL ratio," for ratio settings.
2. The memory bus clock refers to the P1010 memory controllers' Dn_MCK[0:5] and $\overline{\text{Dn\_MCK}}$[0:5] output clocks, running at half of the DDR data rate.
3. In asynchronous mode, if the DDR data rate to the CCB clock rate is greater than 3:1 (i.e. DDR=3:CCB=1), than the DDR performance monitor statistic accuracy cannot be guaranteed.

As a general guideline, the following procedures can be used for selecting the DDR data rate or platform frequency:

1. Start with the processor core frequency selection.

2. Once the processor core frequency is determined, select the platform frequency from the options listed in Table 82.
3. Check the platform to SYSCLK ratio to verify a valid ratio can be choose from Table 84.
4. DDR data rate must be greater than the platform frequency. In other words, running DDR data rate lower than the platform frequency in asynchronous mode is not supported by the P1010.
5. Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

3.1.2 Platform to SYSCLK PLL ratio

The clock that drives the internal CCB bus is called the platform clock. The frequency of the platform clock is set using the following reset signals, as shown in Table 81:

- SYSCLK input signal
- Binary value on IFC_AD[0:2] at power up

These signals must be pulled to the desired values.

Table 81. Platform/SYSCLK clock ratios

Binary Value of IFC_AD[0:2]Signals	Platform: SYSCLK Ratio
000	4:1
001	5:1
010	6:1
All Others	Reserved

3.1.3 e500 core to platform clock PLL ratio

The clock ratio between the e500 core and the platform clock is determined by the binary value of IFC_AD[3:5] signals at power up. Table 82 describes the supported ratios. Note that IFC_AD[6] must be pulled low if the core frequency is 450 MHz or below.

Table 82. e500 core to platform clock ratios

Binary Value of IFC_AD[3:5]Signals	e500 Core: Platform Ratio
010	1:1
011	1.5:1
100	2:1
101	2.5:1
110	3:1
All Others	Reserved

3.1.4 DDR/SYSCLK PLL ratio

This table describes the clock ratio between the DDR memory controller complex and the DDR PLL reference clock, SYSCLK, which is not the memory bus clock. The DDR memory controller complex clock frequency is equal to the DDR data rate.

Table 83. DDR Clock ratio

Binary Value of IFC_AD[7:8]Signals	DDR:SYSCLK Ratio
00	8:1
01	10:1
10	12:1
11	Reserved

3.1.5 Frequency options

This section discusses interface frequency options.

3.1.5.1 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 84. SYSCLK and platform frequency options

Platform: SYSCLK Ratio	SYSCLK (MHz)		
	66.66	83.33	100.00
	Platform Frequency (MHz)[1]		
4:1	267	333	400
5:1	333	—	—
6:1	400	—	—

Note:

1 Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.2 Supply power default setting

P1010 is capable of supporting multiple power supply levels on its I/O supply. Table 85 shows the encoding used to select the voltage level for each I/O supply.

Table 85. Default voltage level for BV_{DD}

BV_{DD}_VSEL [0:1]	I/O Voltage Level
00	3.3 V
01	2.5 V
10	1.8 v
11	3.3 v

3.3 Power supply design and sequencing

3.3.1 PLL power supply filtering

Each of the PLLs is provided with power through independent power supply pins. The AV_{DD} level should always be equivalent to V_{DD}, and these voltages must be derived directly from V_{DD} through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 46, one for each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of device footprint, without the inductance of vias.

This figure shows the PLL power supply filter circuit for AV_{DD_CORE}, AV_{DD_DDR}, AV_{DD_PLAT}.

NOTE

- R = 5Ω ± 5%
- C1 = 10µF ± 10%, 603, X5R with ESL ≤ 0.5nH
- C2 = 1µF ± 10%, 402 X5R with ESL ≤ 0.5 nH

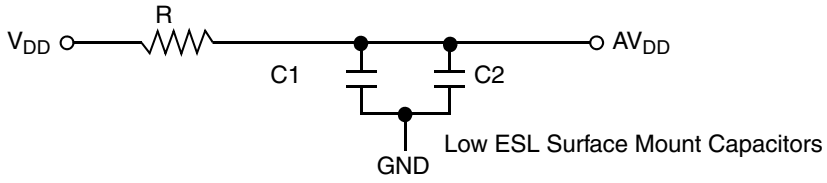
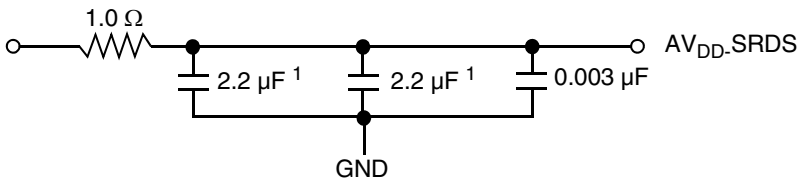


Figure 46. P1010 PLL power supply filter circuit

The $SD1\_AV_{DD}$, $SD2\_AV_{DD}$ and USBVDD1_0 signals provides power for the analog portions of the SerDes PLL and USB PHY PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 47. For maximum effectiveness, the filter circuit should be placed as closely as possible to the device balls to ensure it filters out as much noise as possible. The ground connection should be near the $SD1\_AV_{DD}$, $SD2\_AV_{DD}$ and USBVDD1_0 balls. The 0.003-µF capacitor is closest to the balls, followed by two 2.2-µF capacitor, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from $SD1\_AV_{DD}$, $SD2\_AV_{DD}$ and USBVDD1_0 to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.

This figure shows the PLL power supply filter circuit for $SD1\_AV_{DD}$, $SD2\_AV_{DD}$ and USBVDD1_0.



1. An 0805 sized capacitor is recommended for system initial bring-up

Figure 47. SerDes PLL power supply filter circuit

3.4 Decoupling recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the P1010 system. The device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate $V_{DD,}$ BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

3.5 SerDes block power supply decoupling recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

1. The board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
2. There should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
3. Between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

3.6 Connection recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to V_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}$ BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} and GND pins of the device.

3.7 Pull-up and pull-down resistor requirements

The P1010 requires weak pull-up resistors on open drain type pins including I^2C pins (1 kΩ is recommended) and MPIC interrupt pins (2–10 kΩ is recommended).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 50.

NOTE

Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior, and spurious assertion gives unpredictable results.

3.8 Output buffer DC impedance

The P1010 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 (output impedance) for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 61). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$. Here OV_{DD} refers to the power supply associated with that particular pin, to know about the supply associated with any pin see Table 48.

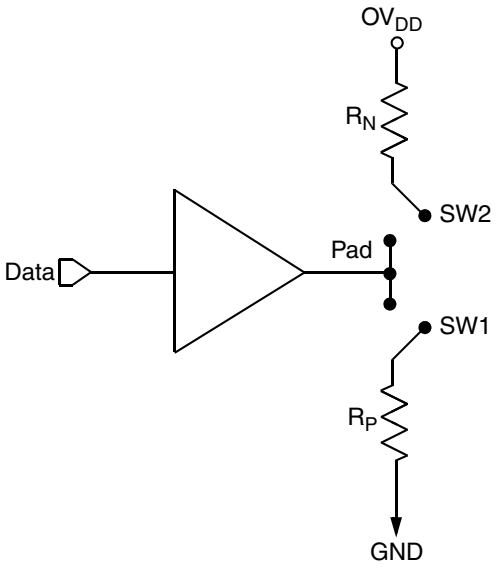


Figure 48. Driver Impedance measurement

This table summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 90°C.

Table 86. Impedance characteristics

Impedance	IFC, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R_N	43	20	Z_0	Ω
R_P	43	20	Z_0	Ω

Note: Nominal supply voltages. See Table 3.

3.9 Configuration pin muxing

The P1010 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled

only during HRESET (and for platform /system clocks after HRESET deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout, including stubless connections to these pull-down resistors, coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

3.10 JTAG configuration signals

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

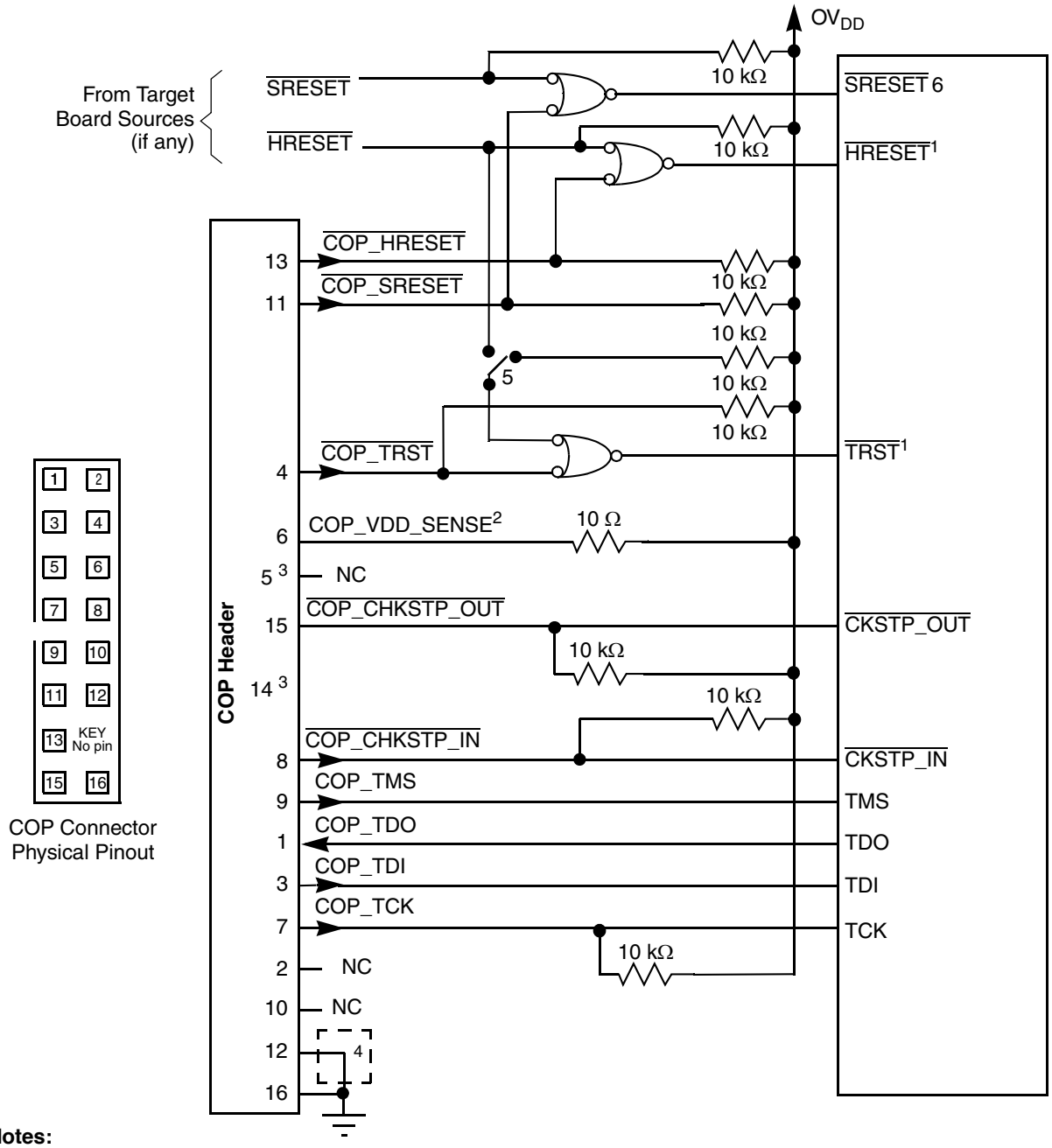
The arrangement shown in Figure 50 allows the COP port to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well.

The COP interface has a standard header, shown in Figure 50 for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC).

Regardless of the numbering, the signal placement recommended in Figure 50 is common to all known emulators.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 49. JTAG interface connection

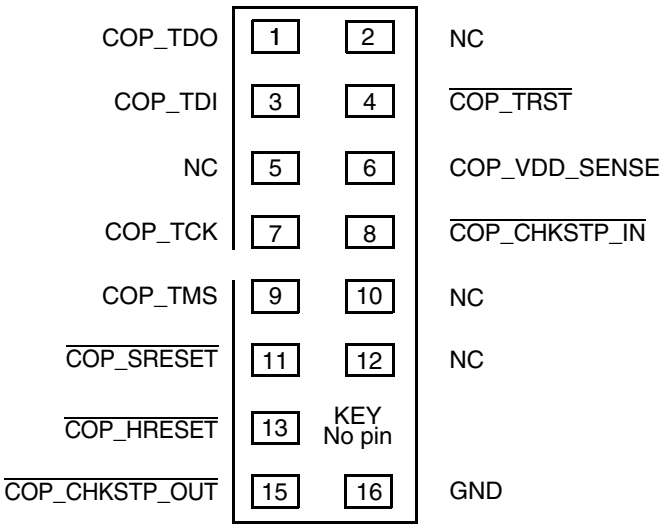


Figure 50. COP connector physical pinout

3.10.1 Termination of unused signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 50. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 kΩ resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

3.11 Guidelines for high-speed interface termination

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins.

The following pins must be left unconnected (float):

- SD_TX[3:0]
- $\overline{\text{SD\_TX}}$[3:0]

The following pins must be connected to GND:

- SD_RX[3:0]
- $\overline{\text{SD\_RX}}$[3:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

3.12 Thermal

This section describes the thermal specifications of the P1010.

3.12.1 Thermal characteristics

This table provides the package thermal characteristics.

Table 87. Package thermal characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Note
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	34	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	22	°C/W	1, 2, 3
Junction-to-ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	27	°C/W	1, 3
Junction-to-ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction-to-board thermal	—	$R_{\theta JB}$	11	°C/W	4
Junction-to-case thermal	—	$R_{\theta JC}$	7	°C/W	5
Junction-to-package top thermal	Natural Convection	Ψ_{JT}	2	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Per JEDEC JESD51-6 with board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

This table provides the thermal resistance with heat sink in open flow.

Table 88. Thermal resistance with heat sink in open flow

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
23x23x10 mm Pin Fin	Natural Convection	16.9
	0.5 m/s	13.4
	1 m/s	11.6
	2 m/s	10.0
35x35x18 mm Pin Fin	Natural Convection	13.8
	0.5 m/s	10.7
	1 m/s	9.3
	2 m/s	8.6

Table 88. Thermal resistance with heat sink in open flow (continued)

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
53x54x25 mm Pin Fin	Natural Convection	11.5
	0.5 m/s	9.1
	1 m/s	8.3
	2 m/s	7.9

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. A power value of TBD was used for the heat sink simulations.The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.

3.12.2 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.12.3 Thermal management information

This section provides thermal management information for the plastic ball grid array (WB-TePBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is shown in Figure 51. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

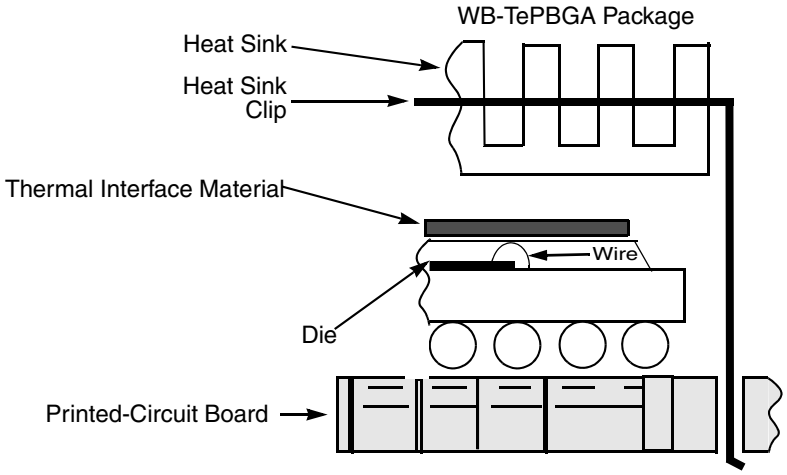


Figure 51. Package exploded cross-sectional view with several heat sink options

The system board designer can choose between several types of heat sinks to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

4 Package information

The following section describes the detailed content and mechanical description of the package.

4.1 Package parameters for P1010

The package type is 19mm × 19mm, 425 plastic ball grid array (WB-TePBGA-1). The package parameters are as follows:

Package outline	19 mm × 19mm
Interconnects	425
Pitch	0.8 mm
Module height (typical)	1.50 mm to 1.90 mm (Maximum)
Solder Balls	3.5% Ag, 96.5% Sn
Ball diameter (typical)	0.45 mm

4.2 Mechanical dimensions of P1010 WB-TePBGA

This figure shows mechanical dimensions and bottom surface nomenclature of the P1010 WB-TePBGA.

NOTE

- All dimensions are in millimeters.
- Dimensioning and tolerancing per ASME Y14. 5M-1994.
- Maximum solder ball diameter measured parallel to Datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

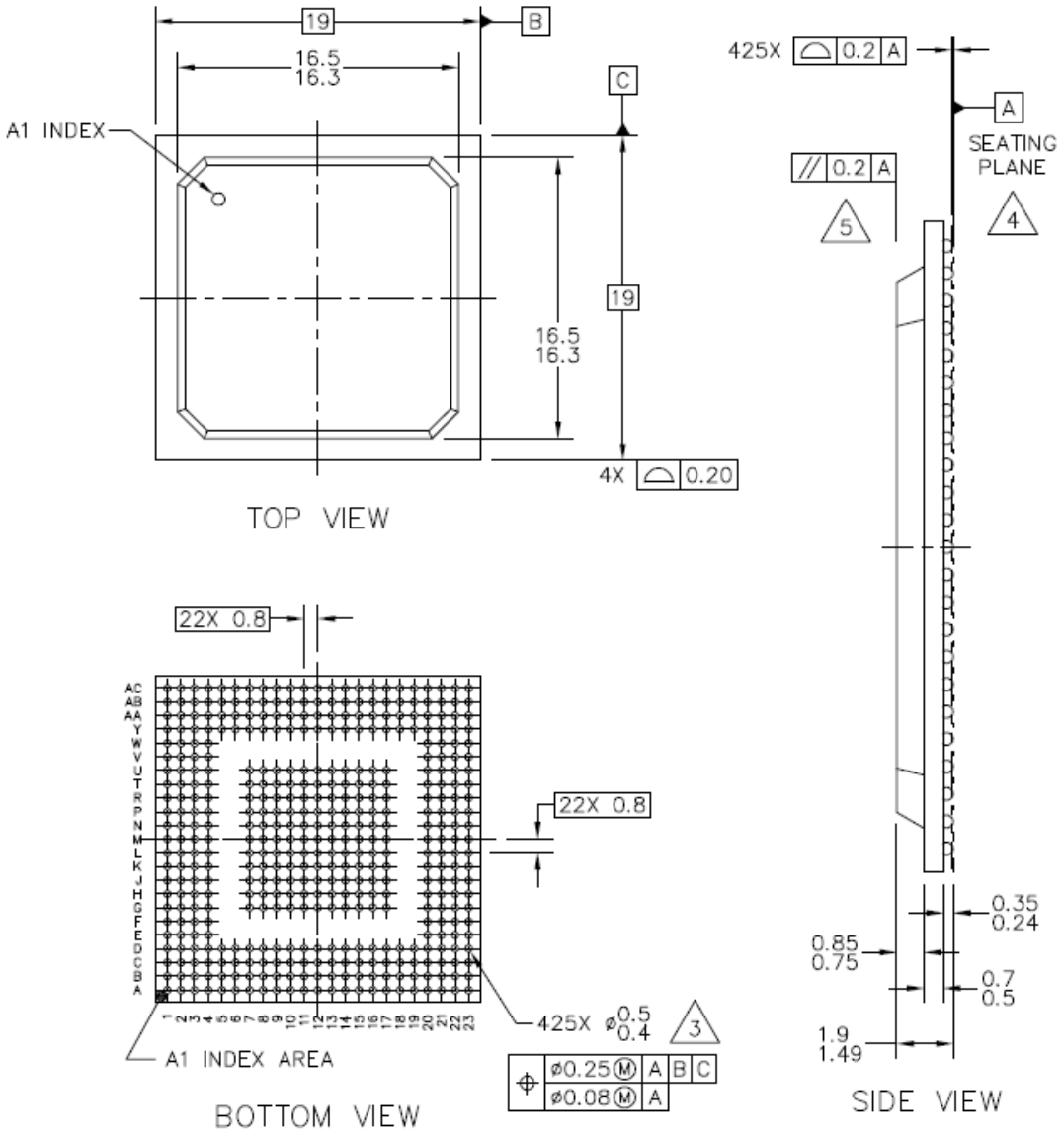


Figure 52. Mechanical Dimensions of P1010 WB-TePBGA package

5 Security fuse processor

The P1010 implements the QorIQ platform's trust architecture, supporting capabilities such as secure boot. Use of the trust architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the *P1010 QorIQ Integrated Processor Reference Manual*.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD} pin per Section 2.2, "Power sequencing." POV_{DD} should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times POV_{DD} should be connected to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in Figure 3. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's trust architecture features are not required to program fuses and should connect POV_{DD} to GND.

6 Ordering information

This table provides the Freescale part numbering nomenclature for the P1010. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Each part number also contains a revision code which refers to the die mask revision number.

Table 89. Part numbering nomenclature

p	1	01	a	x	t	e	n	c	d	r
Generation	Platform	Number of Cores	Derivative	Qual Status	Temp. Range	Encryption	Package Type	CPU Frequency	DDR Speed	Die Revision
P = 45 nm	1	01 = Single core	0	P = Prototype C = Qual'd to Commercial Tier N = Qual'd to Industrial Tier	S = Std Temp X = Ext. Temp	E = SEC Present N = SEC Not Present	5 = TEPBGA-1 Pb free	H = 800 MHz F = 667 MHz D = 533 MHz K = 1000MHz	H = 800 MHZ F= 667 MHz	A = Rev 1.0 B = Rev 2.01

6.1 Part marking

Parts are marked as the example shown in Figure 53.

NOTE

- ATWLYYWW is the traceability code.
- CCCCC is the country code.
- MMMMM is the mask number.
- YWWLAZ is the assembly traceability code.
- P101axtencdr is the orderable part number. See Table 89 for details.

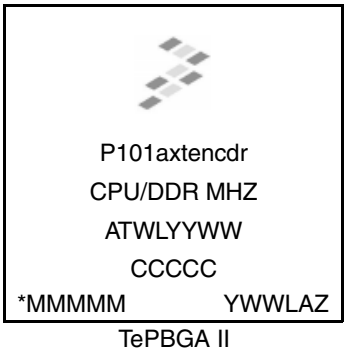


Figure 53. Part marking for WB-TePBGA device

7 Product documentation

The following documents are required for a complete description of the device and are needed to design properly with the part:

- *P1010 QorIQ Integrated Processor Reference Manual* (P1010RM)
- *e500 PowerPC Core Reference Manual* (E500CORERM)

8 Revision history

This table summarizes a revision history for this document.

Table 90. Revision history

Rev. Number	Date	Substantive Change(s)
4	05/2014	• In Table 89 added part numbering information for die revision 2.01.
3	04/2014	• In Table 1, modified IO type of SD2_RX_1 from output to input. • In note above Figure 2, added serdes reference clock. • In Table 2, modified characteristics column for symbol 'LVDD', 'LVIN', 'OVDD', and 'OVIN'. • In Table 3, modified characteristics column for symbol 'LVDD', 'LVIN', 'OVDD', and 'OVIN'. • In Table 45, added min frequency for USB_CLK_IN. • In Table 58, replaced BV_{IN} with OV_{IN}. • In Table 59, replaced BV_{IN} with LV_{IN}. • Removed the table, "GPIO DC electrical characteristics (1.8 V)". • Added a note in Section 2.18.1, "GPIO DC electrical characteristics.
2	03/2013	• In Table 3, modified names of temperature ranges. • In Table 9, added power numbers for 1000 MHz CPU frequency. • In Table 9, added power numbers for SVDD power for typical and maximum. • In Table 79, modified max core clock frequency to 1000 MHz. • In Table 89, added option for parts with CPU frequency of 1000 MHz.
1	06/2012	• Everywhere replaced signal name ALE with AVD. • In Table 1, replaced note references from 5 to 25 for following signals, cfg_sys_pll_0, cfg_sys_pll_1, cfg_sys_pll_2, cfg_ddr_pll_0, cfg_ddr_pll_1, cfg_core_pll_0, cfg_core_pll_1, cfg_core_pll_2, cfg_rom_loc[0], cfg_rom_loc[1], cfg_rom_loc[2], cfg_rom_loc[3] because these signals doesn't have internal pull-ups during POR sequence. • In Table 1, modified note associated with IBIAS_REXT signal. Modified IBIAS_REXT termination circuit and added an programming sequence. • In Table 3, removed note 4. Not applicable. • In Table 10, modified typical and max I/O power numbers for USB PHY. • In Table 6, modified "Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of HRESET (max)" from 8 to 5. • In Table 23, modified tDDKHDX, tDDKLDX (min) for 800MHz from 275 to 225 ns. • In Table 33, modified note 4 to represent correct register fields. • In note 4 of Table 49, replaced tLBOTOT with tIBOTOT. • In Table 55, modified specifications for tJTDVKH and tJTKLDV. • From Figure 32, removed tI2CR and tI2CF because those are not needed. These parameters are not mentioned in table either. • In Table 45, under conditions colum for total input jitter spec for USBPHY_CLK, changed "peak to peak" to "RMS".
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