74HC237

3-to-8 line decoder, demultiplexer with address latches

Rev. 7 — 29 January 2016 Product data sheet

1. General description

The 74HC237 is a high-speed Si-gate CMOS device and is pin compatible with low-power Schottky TTL (LSTTL). The 74HC237 is specified in compliance with JEDEC standard no. 7A.

The 74HC237 is a 3-to-8 line decoder, demultiplexer with latches at the three address inputs (An). The 74HC237 essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the 74HC237 acts as a 3-to-8 active LOW decoder. When the latch enable ($\overline{LE}$) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH. The output enable input ($\overline{E}1$ and E2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless $\overline{E}1$ is LOW and E2 is HIGH. The 74HC237 is ideally suited for implementing non-overlapping decoders in 3-state systems and strobes (stored address) applications in bus-oriented systems.

2. Features and benefits

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active HIGH mutually exclusive outputs
- Low-power dissipation
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC237D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC237DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1

4. Functional diagram

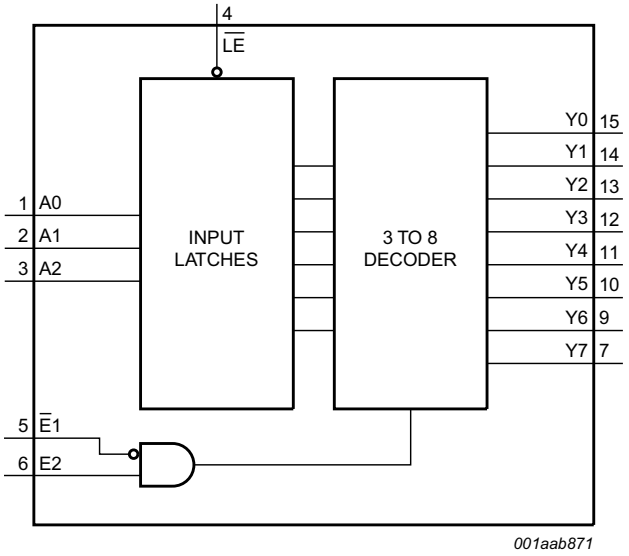


Fig 1. Functional diagram

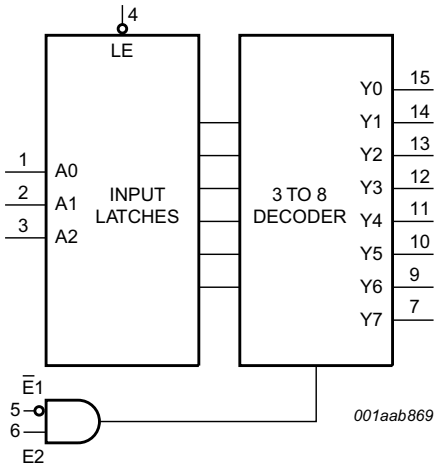


Fig 2. Logic symbol

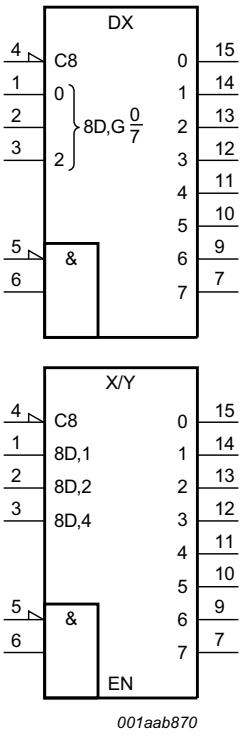


Fig 3. IEC logic symbol

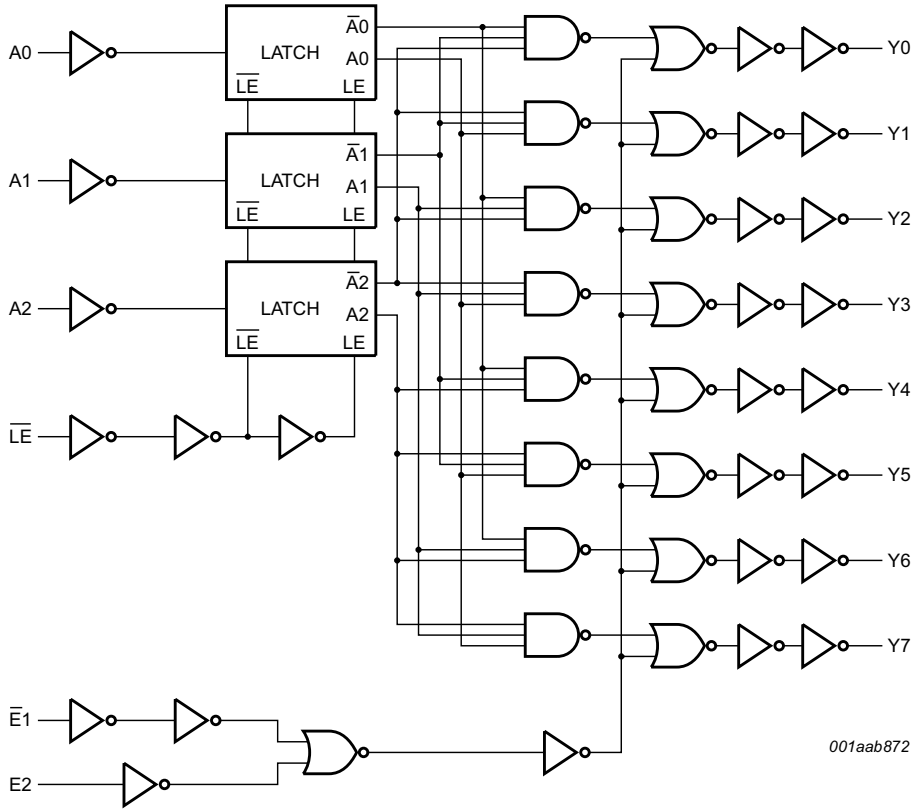


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

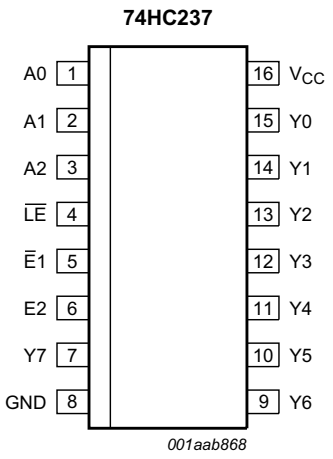


Fig 5. Pin configuration SO16

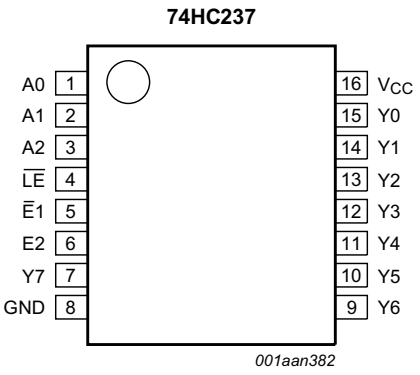


Fig 6. Pin configuration SSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0 to A2	1, 2, 3	data input
$\overline{LE}$	4	latch enable input (active LOW)
$\overline{E}1$	5	data enable input 1 (active LOW)
E2	6	data enable input 2 (active HIGH)
Y0 to Y7	15, 14, 13, 12, 11, 10, 9, 7	output
GND	8	ground (0 V)
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

Enable			Input			Output							
$\overline{LE}$	$\overline{E}1$	E2	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	L	H	X	X	X	stable							
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
			H	L	L	L	H	L	L	L	L	L	L
			L	H	L	L	L	H	L	L	L	L	L
			H	H	L	L	L	L	H	L	L	L	L
			L	L	H	L	L	L	L	H	L	L	L
			H	L	H	L	L	L	L	L	H	L	L
			L	H	H	L	L	L	L	L	L	H	L
			H	H	H	L	L	L	L	L	L	L	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-	−50	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	SO16 and SSOP16 packages [1]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For SSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	An to Yn; see Figure 7 [1]								
		V_{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V_{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V_{CC} = 5 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	27	-	34	-	41	ns
		$\overline{LE}$ to Yn; see Figure 7 [1]								
		V_{CC} = 2.0 V	-	61	190	-	240	-	285	ns
		V_{CC} = 4.5 V	-	22	38	-	48	-	57	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	18	32	-	41	-	48	ns
		$\overline{E}$1to Yn; see Figure 8 [1]								
		V_{CC} = 2.0 V	-	47	145	-	180	-	220	ns
		V_{CC} = 4.5 V	-	17	29	-	36	-	44	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	25	-	31	-	38	ns
		E2 to Yn; see Figure 7 [1]								
		V_{CC} = 2.0 V	-	47	145	-	180	-	220	ns
		V_{CC} = 4.5 V	-	17	29	-	36	-	44	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	25	-	31	-	38	ns
t_t	transition time	Yn; see Figure 7 and Figure 8 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	$\overline{LE}$ HIGH; see Figure 9								
		V_{CC} = 2.0 V	50	11	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	4	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	3	-	11	-	13	-	ns
t_{su}	set-up time	An to $\overline{LE}$; see Figure 9								
		V_{CC} = 2.0 V	50	6	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	2	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	2	-	11	-	13	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 10.

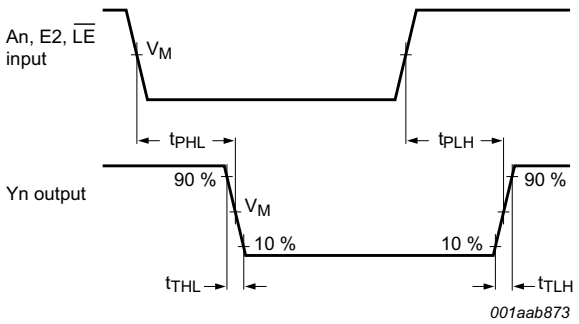
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_h	hold time	An to $\overline{LE}$; see Figure 9					-			
		V_{CC} = 2.0 V	30	3	-	40	-	45	-	ns
		V_{CC} = 4.5 V	6	1	-	8	-	9	-	ns
		V_{CC} = 6.0 V	5	1	-	7	-	8	-	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [3]	-	60	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

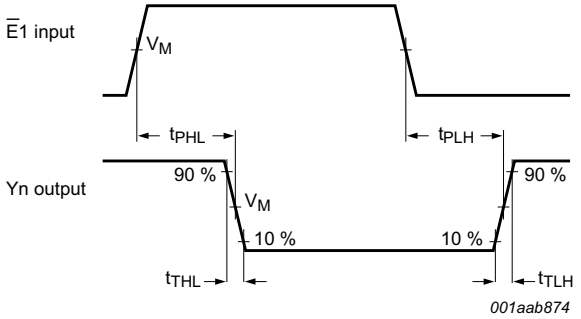
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

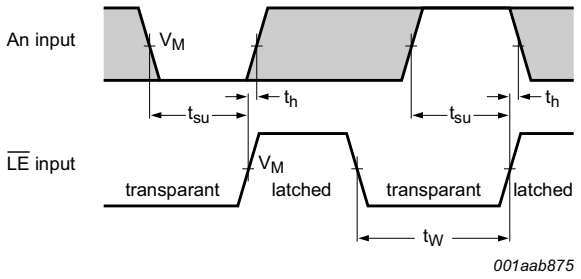
Fig 7. Propagation delay input (An) and enable inputs (E2, $\overline{LE}$) to output (Yn) and output transition time



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Propagation enable inputs ($\overline{E}$1) to output (Yn) and output transition time



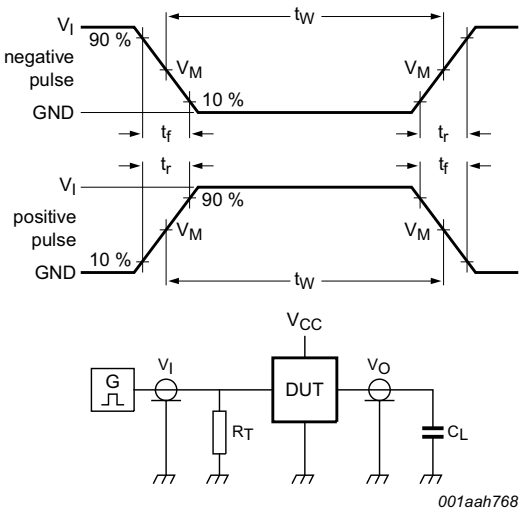
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. The data input (An) to latch enable input ($\overline{LE}$) set-up times, latch enable input ($\overline{LE}$) to data input (An) hold times and latch enable input (LE) pulse width

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC237	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 10. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC237	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Application information

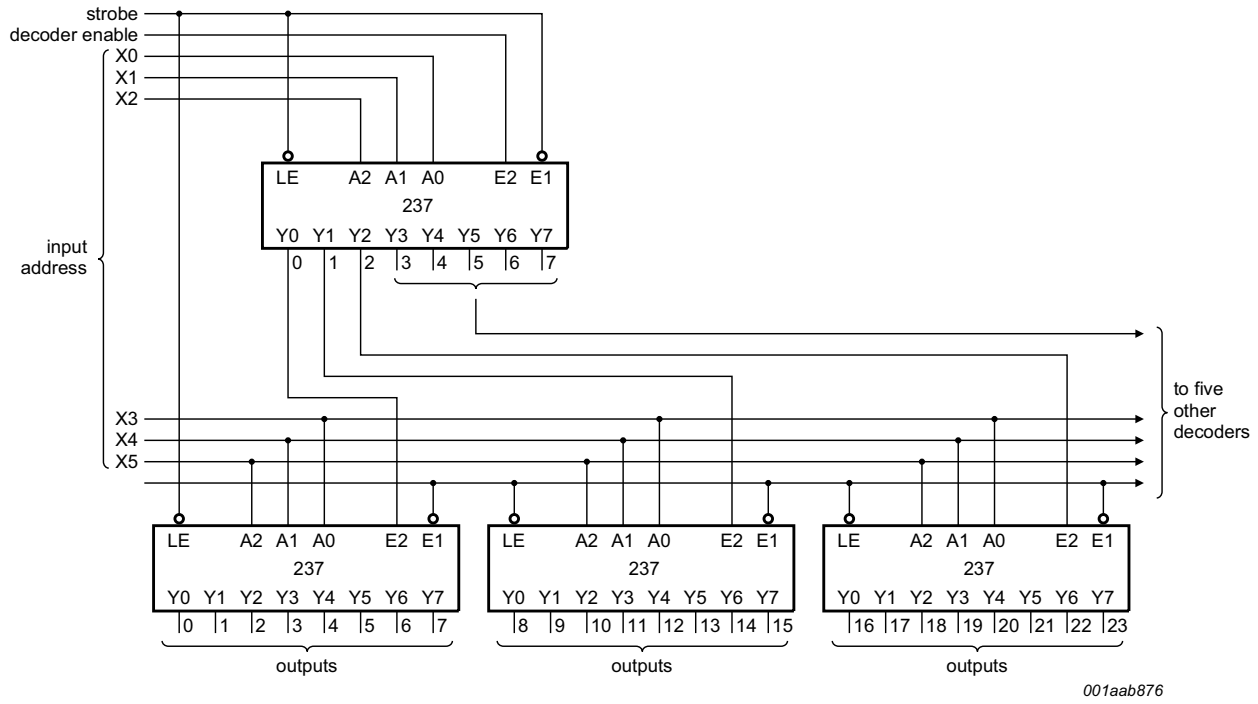
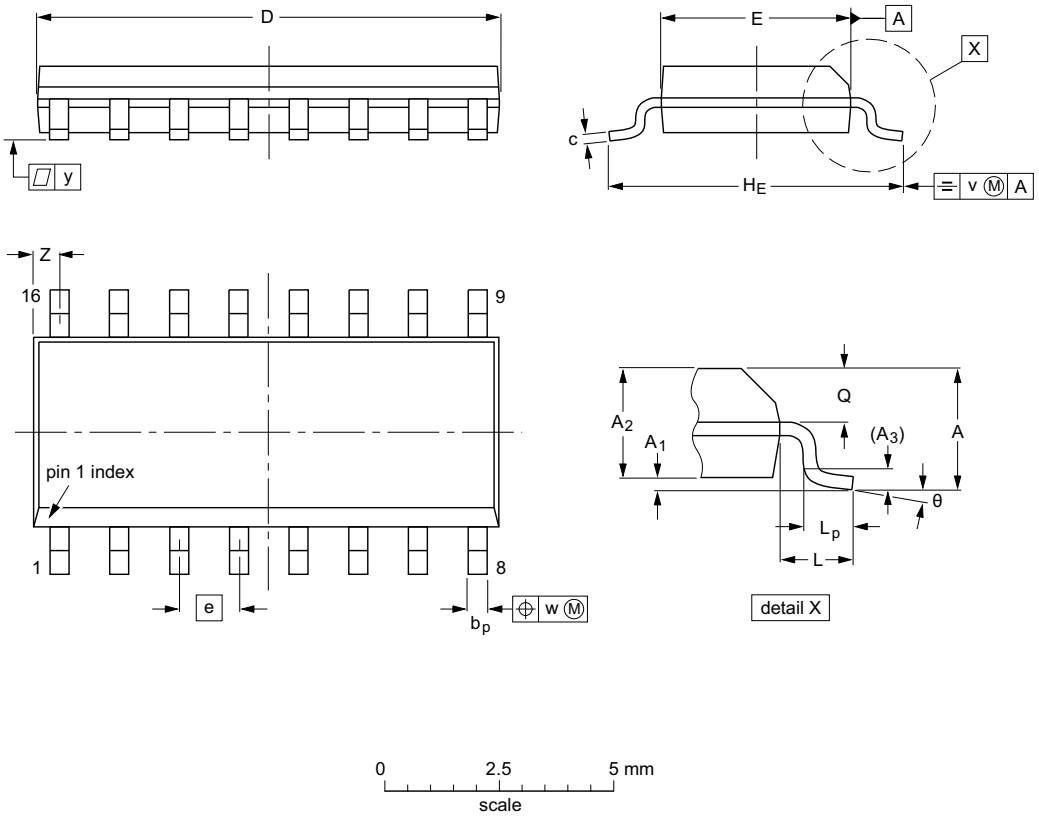


Fig 11. 6-to-64 line decoder with input address storage

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

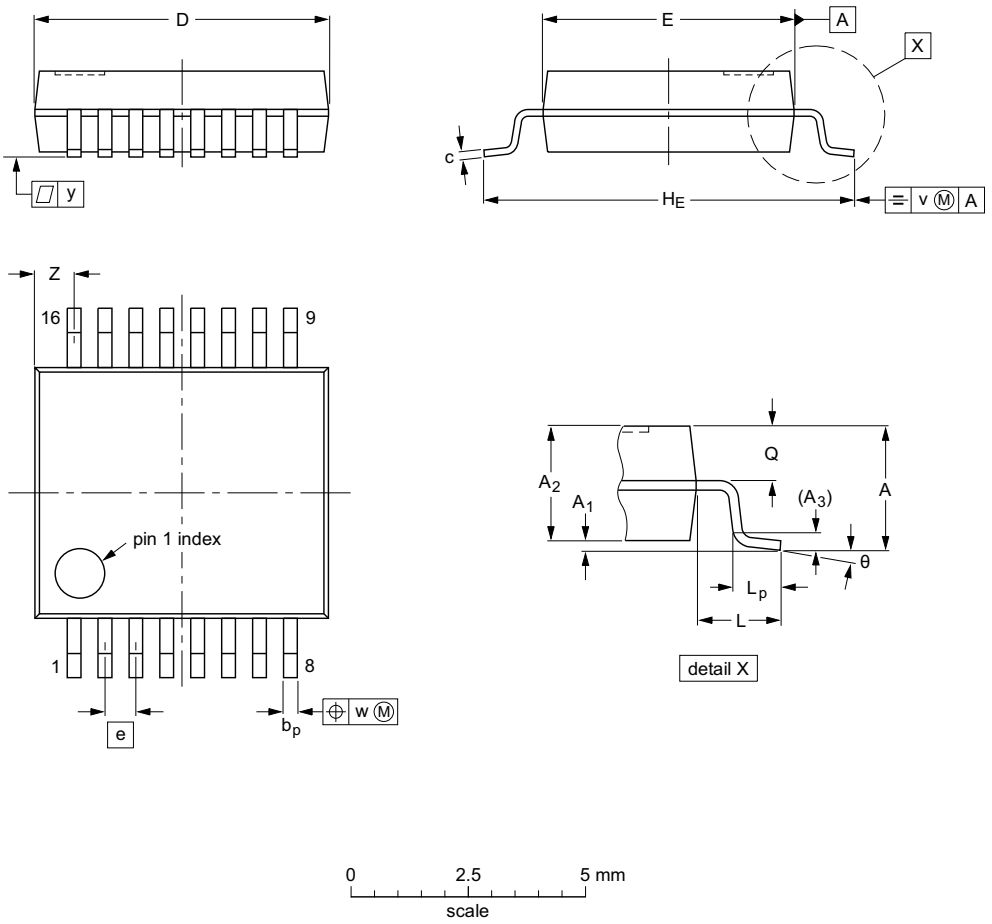
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT338-1 (SSOP16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC237 v.7	20160129	Product data sheet	-	74HC237 v.6
Modifications:	• Type number 74HC237N removed.			
74HC237 v.6	20120823	Product data sheet	-	74HC237 v.5
Modifications:	• Measurement points added to Figure 7 and Figure 8 (errata).			
74HC237 v.5	20111209	Product data sheet	-	74HC237 v.4
Modifications:	• Legal pages updated.			
74HC237 v.4	20110110	Product data sheet	-	74HC237 v.3
74HC237 v.3	20041112	Product data sheet	-	74HC_HCT237_CNV v.2
74HC_HCT237_CNV v.2	19970828	Product specification	-	74HC_HCT237 v.1
74HC_HCT237 v.1	19901201	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contact information

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

18. Contents

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