FAIRCHILD

SEMICONDUCTOR ™

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NM25C020
2K-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI) Synchronous Bus)

General Description

The NM25C020 is a 2048-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C020 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C020 is implemented in Fairchild Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate WRITE enable and WRITE disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against inadvertent programming. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 2.1 MHz clock rate @ 2.7V to 5.5V
- 2048 bits organized as 256 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor READY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
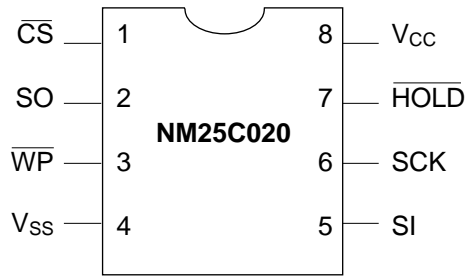- Packages available: 8-pin DIP, 8-pin SO, or 8-pin TSSOP

Block Diagram

DS012400-1

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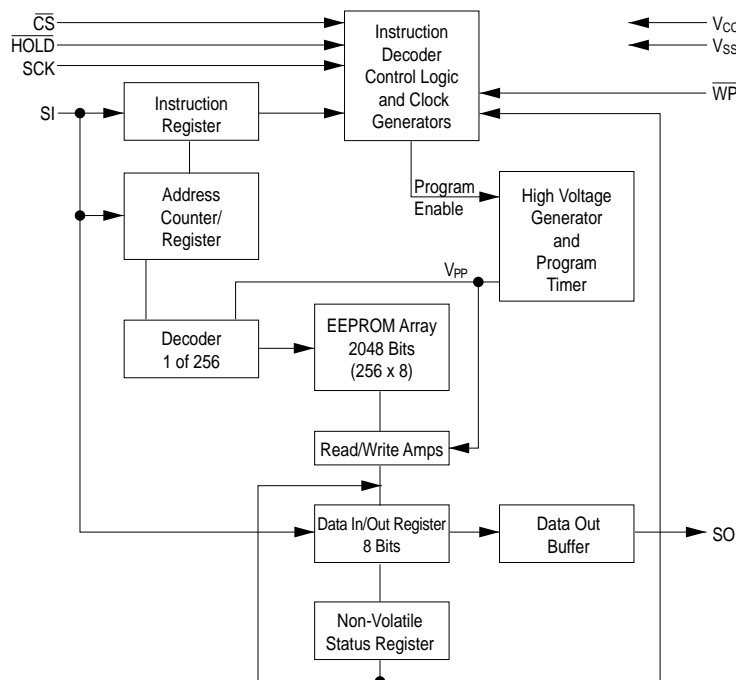
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Connection Diagram

**Dual-In-Line Package (N), SO Package (M8),
and TSSOP Package (MT8)**

$\overline{CS}$ — 1   8 — V_{CC}

SO — 2   7 — $\overline{HOLD}$

$\overline{WP}$ — 3   NM25C020   6 — SCK

V_{SS} — 4   5 — SI

DS012400-2

**Top View
See Package Number N08E (N), M08A (M8), and MTC08 (MT8)**

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

NM   **25**   **C**   **XX**   **LZ**   **E**   **XX**

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
Density/Mode	020	2K, mode 0
	C	CMOS technology
Interface	25	SPI
NM		**Fairchild Nonvolatile Memory Prefix**

Standard Voltage $4.5 \leq V_{CC} \leq 5.5V$ Specifications

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C020	0°C to +70°C
NM25C020E	-40°C to +85°C
NM25C020V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \leq V_{CC} \leq 5.5V$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS} = V_{IL}$		3	mA
I_{CCSB}	Standby Current	$\overline{CS} = V_{CC}$		50	μA
I_{IL}	Input Leakage	$V_{IN} = 0$ to V_{CC}	-1	+1	μA
I_{OL}	Output Leakage	$V_{OUT} = GND$ to V_{CC}	-1	+1	μA
V_{IL}	CMOS Input Low Voltage		-0.3	$V_{CC} * 0.3$	V
V_{IH}	CMOS Input High Voltage		$0.7 * V_{CC}$	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6$ mA		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -0.8$ mA	$V_{CC} - 0.8$		V
f_{OP}	SCK Frequency			2.1	MHz
t_{RI}	Input Rise Time			2.0	μs
t_{FI}	Input Fall Time			2.0	μs
t_{CLH}	Clock High Time	(Note 2)	190		ns
t_{CLL}	Clock Low Time	(Note 2)	190		ns
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time		240		ns
t_{DIS}	Data Setup Time		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		240		ns
t_{DIN}	Data Hold Time		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay	$C_L = 200$ pF		240	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			100	ns
t_{DF}	Output Disable Time	$C_L = 200$ pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			100	ns
t_{WP}	Write Cycle Time	1–4 Bytes		10	ms

Capacitance $T_A = 25$°C, f = 2.1/1 MHz (Note 4)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	$C_L = 200$ pF
Input Pulse Levels	$0.1 * V_{CC} – 0.9 * V_{CC}$
Timing Measurement Reference Level	$0.3 * V_{CC} - .07 * V_{CC}$

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, $t_{CLH} + t_{CLL}$ must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 3: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

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Low Voltage 2.7V ≤ V$_{CC}$ ≤ 4.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C020L/LZ	0°C to +70°C
NM25C020LE/LZE	-40°C to +85°C
NM25C020LV	-40°C to +125°C
Power Supply (V$_{CC}$)	2.7V–4.5V

DC and AC Electrical Characteristics 2.7V ≤ V$_{CC}$ ≤ 4.5V (unless otherwise specified)

Symbol	Parameter	Part	Conditions	25C020L/LE 25C020LZ/LZE Min.	Max.	25C020LV Min	Max	Units
I$_{CC}$	Operating Current		$\overline{CS}$ = V$_{IL}$		3		3	mA
I$_{CCSB}$	Standby Current	L LZ	$\overline{CS}$ = V$_{CC}$		10 1		10 N/A	μA μA
I$_{IL}$	Input Leakage		V$_{IN}$ = 0 to V$_{CC}$	-1	1	-1	1	μA
I$_{OL}$	Output Leakage		V$_{OUT}$ = GND to V$_{CC}$	-1	1	-1	1	μA
V$_{IL}$	Input Low Voltage			-0.3	V$_{CC}$ * 0.3	-0.3	V$_{CC}$ * 0.3	V
V$_{IH}$	Input High Voltage			0.7 * V$_{CC}$	V$_{CC}$ + 0.3	0.7 * V$_{CC}$	V$_{CC}$ + 0.3	V
V$_{OL}$	Output Low Voltage		I$_{OL}$ = 0.8 mA		0.4		0.4	V
V$_{OH}$	Output High Voltage		I$_{OH}$ = −0.8 mA	V$_{CC}$ - 0.8		V$_{CC}$ - 0.8		V
f$_{OP}$	SCK Frequency				1.0		1.0	MHz
t$_{RI}$	Input Rise Time				2.0		2.0	μs
t$_{FI}$	Input Fall Time				2.0		2.0	μs
t$_{CLH}$	Clock High Time		(Note 6)	410		410		ns
t$_{CLL}$	Clock Low Time		(Note 6)	410		410		ns
t$_{CSH}$	Min. $\overline{CS}$ High Time		(Note 7)	500		500		ns
t$_{CSS}$	$\overline{CS}$ Setup Time			500		500		ns
t$_{DIS}$	Data Setup Time			100		100		ns
t$_{HDS}$	$\overline{HOLD}$ Setup Time			240		240		ns
t$_{CSN}$	$\overline{CS}$ Hold Time			500		500		ns
t$_{DIN}$	Data Hold Time			100		100		ns
t$_{HDN}$	$\overline{HOLD}$ Hold Time			240		240		ns
t$_{PD}$	Output Delay		C$_L$ = 200 pF		500		500	ns
t$_{DH}$	Output Hold Time			0		0		ns
t$_{LZ}$	$\overline{HOLD}$ Output Low Z				240		240	ns
t$_{DF}$	Output Disable Time		C$_L$ = 200 pF		500		500	ns
t$_{HZ}$	$\overline{HOLD}$ to Output Hi Z				240		240	ns
t$_{WP}$	Write Cycle Time		1-4 Bytes		15		15	ms

Capacitance T$_A$ = 25°C, f = 2.1/1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C$_{OUT}$	Output Capacitance	3	8	pF
C$_{IN}$	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	I$_{OL}$ = 10 μA, I$_{OH}$ = 10 μA
Input Pulse Levels	0.3V to 3.5V
Timing Measurement Reference Level	
Input	0.4V and 1.6V
Output	0.8V and 1.6V

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 6: The f$_{OP}$ frequency specification specifies a minimum clock period of 1/f$_{OP}$. Therefore, for every f$_{OP}$ clock cycle, t$_{CLH}$ + t$_{CLL}$ must be equal to or greater than 1/f$_{OP}$. For example, if the 2.1MHz period = 476ns and t$_{CLH}$ = 190ns, t$_{CLL}$ must be 286ns.

Note 7: $\overline{CS}$ must be brought high for a minimum of t$_{CSH}$ between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

AC Test Conditions (Continued)

FIGURE 1. Synchronous Data Timing Diagram
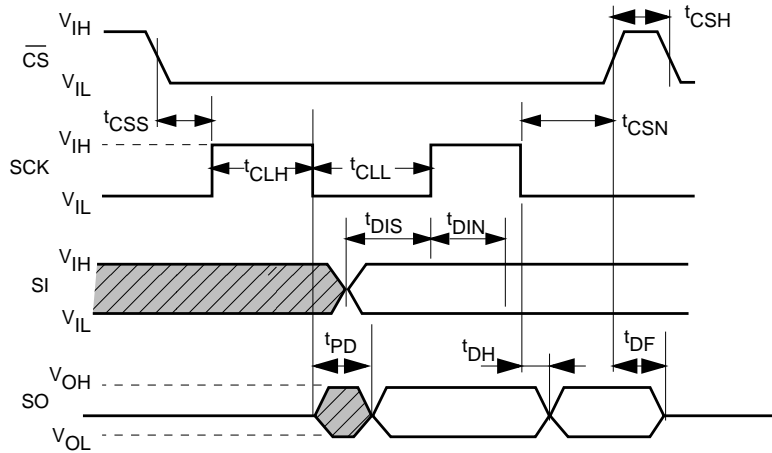
DS012400-3

FIGURE 2. HOLD Timing
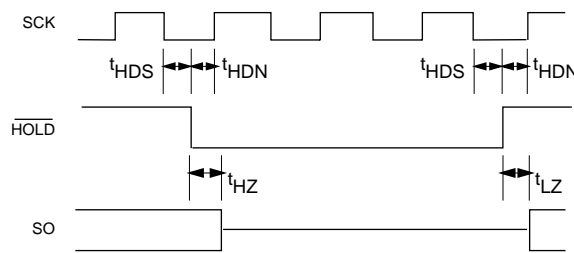
DS012400-6

FIGURE 3. SPI Serial Interface

DS012400-4

NM25C020 Rev. D.1
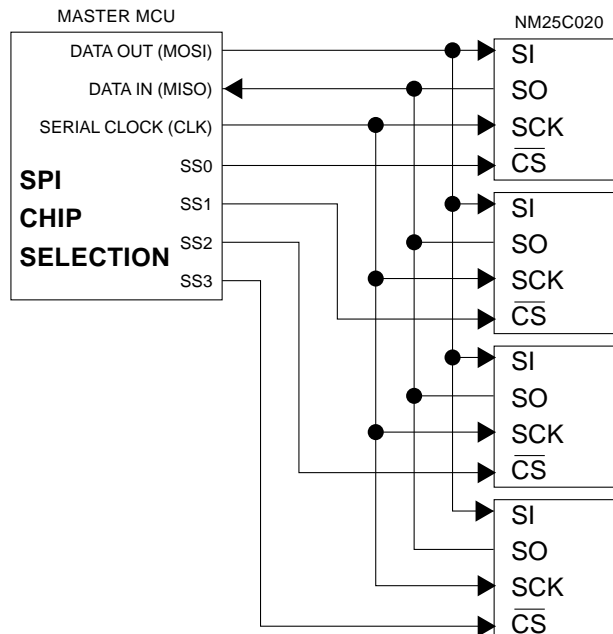
Functional Description

TABLE 1. Instruction Set

Instruction Name	Instruction Opcode	Operation
WREN	00000110	Set Write Enable Latch
WRDI	00000100	Reset Write Enable Latch
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	00000011	Read Data from Memory Array
WRITE	00000010	Write Data to Memory Array

MASTER: The device that generates the serial clock is designated as the master. The NM25C020 can never function as a master.

SLAVE: The NM25C020 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C020 has separate pins for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with CS going low contains the op-code that defines the operation to be performed.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C020 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See Figure 4.

FIGURE 4. SPI Protocol

DS012400-5
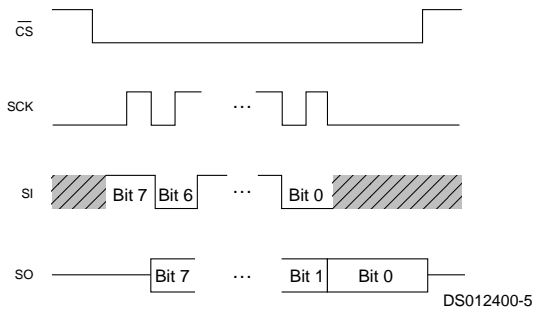
Data is clocked in on the positive SCK edge and out on the negative SCK edge.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, HOLD may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. The SO pin is at a high impedance state during $\overline{HOLD}$.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C020, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge reinitializes the serial communication. See Figure 5.

FIGURE 5. Invalid Op-Code

DS012400-7
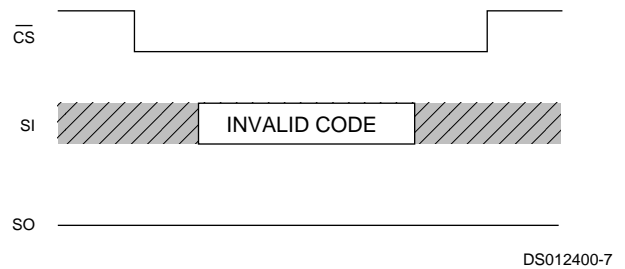
Functional Description (Continued)

READ SEQUENCE: Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code is transmitted on the SI line followed by the byte address (A7–A0) to be read. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte adress is automatically incremented and data will continue to be shifted out as clock pulses are continuously applied. When the highest address is reached (FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 6.

FIGURE 6. Read Sequence

DS012400-8

READ STATUS REGISTER (RDSR) : The Read Status Register (RDSR) instruction provides access to the status register and is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. (Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION.) The status register format is shown in Table 2.

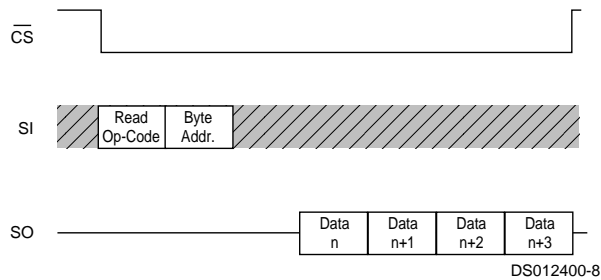### TABLE 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

X = Don't Care

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. **Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid.** All other bits are 1s. See Figure 7.

FIGURE 7. Read Status

DS012400-9
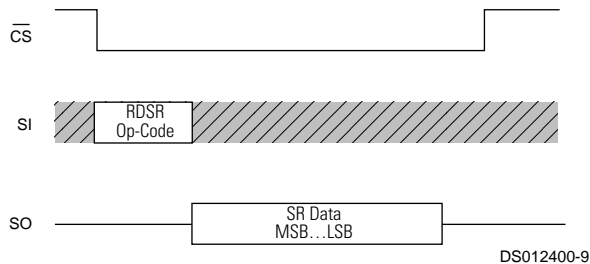
TABLE 3. Block Write Protection Levels

Level	Status Register Bits		Array Address Protected
	BP1	**BP0**	
0	0	0	None
1	0	1	C0-FF
2	1	0	80-FF
3	1	1	00-FF

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. **At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state.** Note that a WRITE DISABLE (WRDI) instruction will also return the device to the write disable state. See Figure 8.

FIGURE 8. Write Enable

DS012400-10
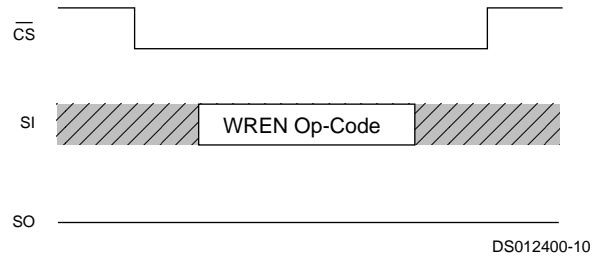
WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. See Figure 9.

FIGURE 9. Write Disable

DS012400-11
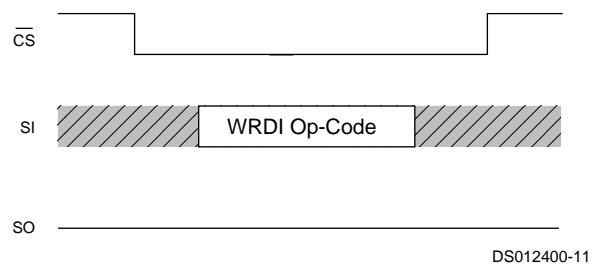
WRITE SEQUENCE: **To program the device, the WRITE PRO-TECT ($\overline{WP}$) pin must be held high** and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code is transmitted on the SI line followed by the byte address(A7–A0) and the corresponding data (D7-D0) to be written. **Programming will start after the $\overline{CS}$ pin is forced back to a high level.** Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See Figure 10.

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Functional Description (Continued)

FIGURE 10. Write Sequence
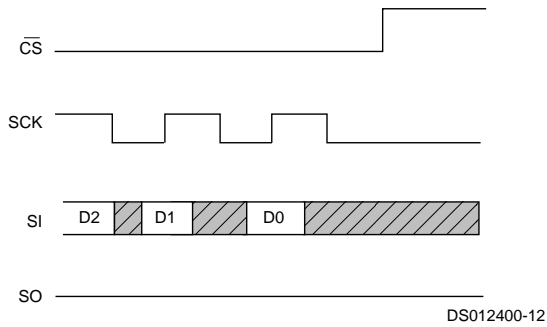
DS012400-12

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

The NM25C020 is capable of a 4 byte PAGE WRITE operation. After receipt of each byte of data the two low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than 4 bytes of data, the address counter will "roll over," and the previously loaded data will be reloaded. See Figure 11.

FIGURE 11. 4 Byte Page Write

DS012400-13

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when $\overline{CS}$ is forced high. A new $\overline{CS}$ falling edge is required to re-initialize the serial communication.

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 a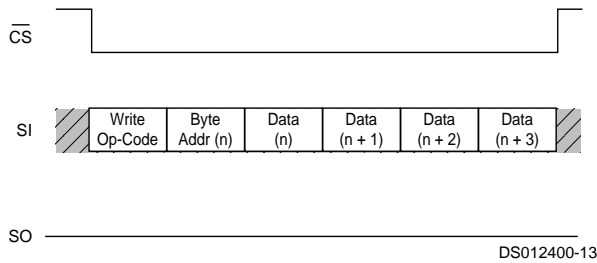nd BP1). The WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

The WRSR command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See Figure 12.

FIGURE 12. Write Status Register

DS012400-14
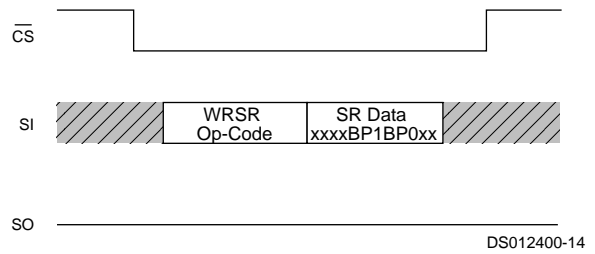
Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the $\overline{CS}$ pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 13.

FIGURE 13. Start WRSR Condition
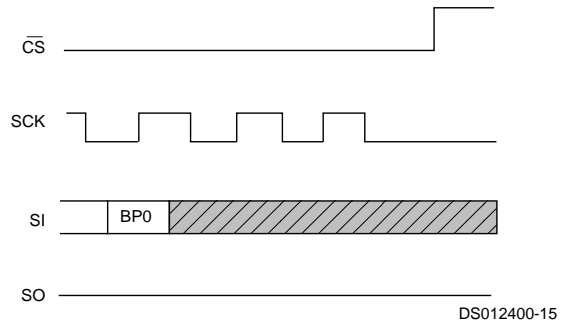
DS012400-15

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

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Physical Dimensions inches (millimeters) unless otherwise noted

0.189 - 0.197
(4.800 - 5.004)

8 7 6 5

0.228 - 0.244
(5.791 - 6.198)

1 2 3 4

Lead #1
IDENT

0.150 - 0.157
(3.810 - 3.988)

0.010 - 0.020
(0.254 - 0.508) x 45°

8° Max, Typ.
All leads

0.04
(0.102)
All lead tips

0.0075 - 0.0098
(0.190 - 0.249)
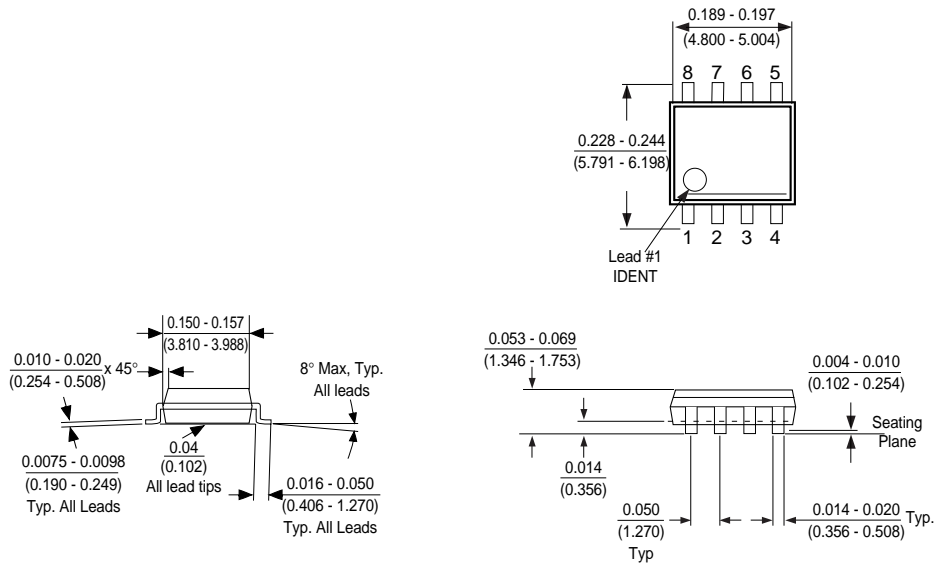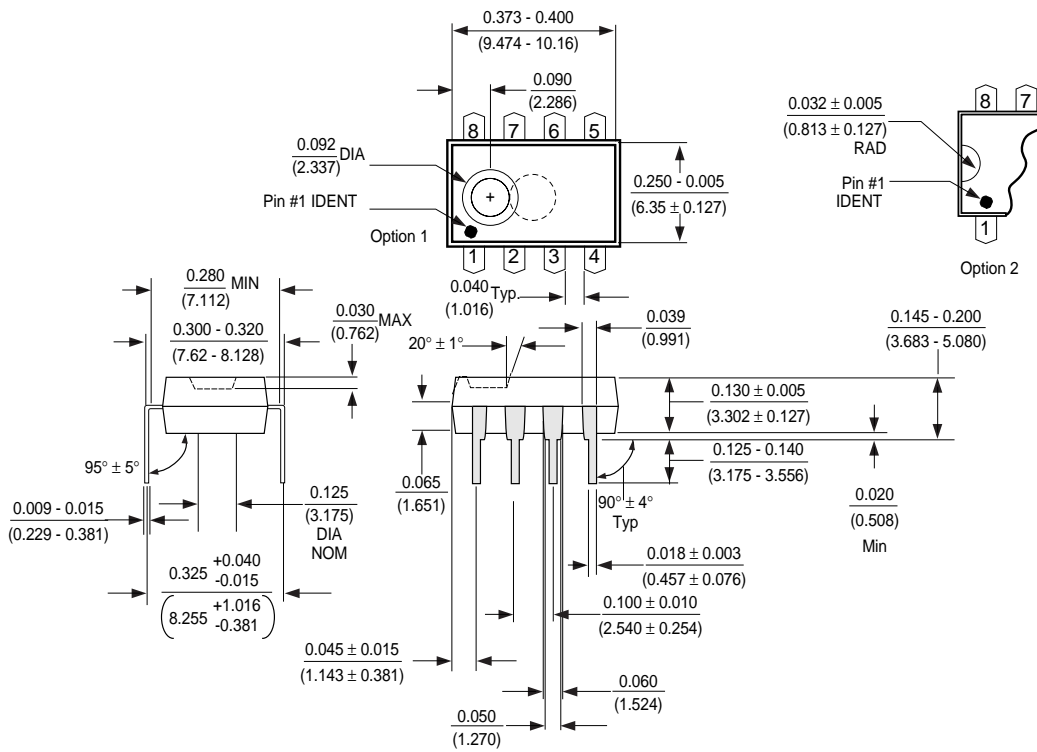Typ. All Leads

0.016 - 0.050
(0.406 - 1.270)
Typ. All Leads

0.053 - 0.069
(1.346 - 1.753)

0.004 - 0.010
(0.102 - 0.254)

Seating
Plane

0.014
(0.356)

0.050
(1.270)
Typ

0.014 - 0.020
(0.356 - 0.508) Typ.

Molded Small Out-Line Package (M8)
Package Number M08A

0.373 - 0.400
(9.474 - 10.16)

0.090
(2.286)

0.092
(2.337) DIA

Pin #1 IDENT

Option 1

8 7 6 5

1 2 3 4

0.250 - 0.005
(6.35 ± 0.127)

0.040
(1.016) Typ.

0.032 ± 0.005
(0.813 ± 0.127)
RAD

8 7

Pin #1
IDENT

1

Option 2

0.280 MIN
(7.112)

0.300 - 0.320
(7.62 - 8.128)

0.030 MAX
(0.762)

20° ± 1°

0.039
(0.991)

0.145 - 0.200
(3.683 - 5.080)

0.130 ± 0.005
(3.302 ± 0.127)

95° ± 5°

0.009 - 0.015
(0.229 - 0.381)

0.125
(3.175)
DIA
NOM

0.325 +0.040 -0.015
(8.255 +1.016 -0.381)

0.065
(1.651)

90° ± 4°
Typ

0.125 - 0.140
(3.175 - 3.556)

0.020
(0.508)
Min

0.018 ± 0.003
(0.457 ± 0.076)

0.100 ± 0.010
(2.540 ± 0.254)

0.045 ± 0.015
(1.143 ± 0.381)

0.060
(1.524)

0.050
(1.270)

Molded Dual-In-Line Package (N)
Package Number N08E

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Physical Dimensions inches (millimeters) unless otherwise noted

0.114 - 0.122
(2.90 - 3.10)

8   5

0.246 - 0.256
(6.25 - 6.5)

0.169 - 0.177
(4.30 - 4.50)

0.123 - 0.128
(3.13 - 3.30)

1   4

Pin #1 IDENT

(4.16) Typ   (7.72) Typ

(1.78) Typ

(0.42) Typ

(0.65) Typ

Land pattern recommendation

$\frac{0.0433}{(1.1)}$ Max
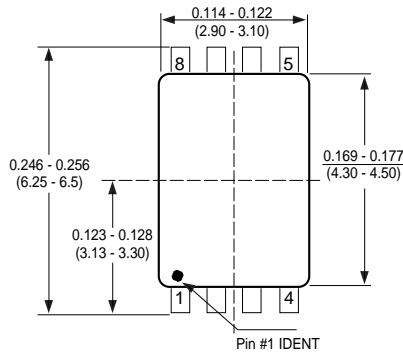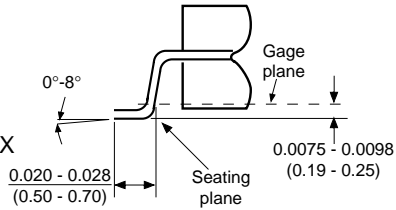
0.002 - 0.006
(0.05 - 0.15)

0.0256 (0.65)
Typ.

0.0075 - 0.0098
(0.19 - 0.30)

See detail A

0.0035 - 0.0079

DETAIL A
Typ. Scale: 40X

0°-8°

Gage
plane

0.0075 - 0.0098
(0.19 - 0.25)

0.020 - 0.028
(0.50 - 0.70)

Seating
plane
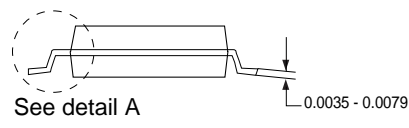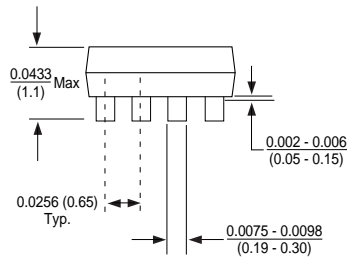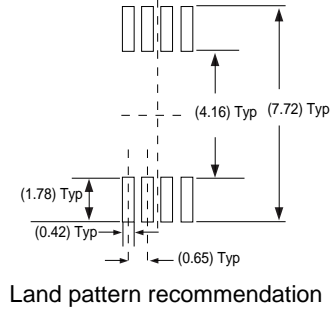
Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

NM25C020 Rev. D.1

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NM25C020
Product information

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General description | Features | Product status/pricing/packaging | Application notes

General description

The NM25C020 is a 2048-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C020 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C020 is implemented in Fairchild Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select (CS#), Clock (SCK), Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate WRITE enable and WRITE program disable instructions are provided for data protection.

Hardware data protection is provided by the WP# pin to protect against accidental data changes. The HOLD# pin allows the serial communication to be suspended without resetting the serial sequence.

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Features

- 2.1 MHz clock rate @ 2.7V to 5.5V
- 2048-bits organized as 256 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor READY/BUSY
- Write Protect (WP#) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO or 8-pin TSSOP

Product status/pricing/packaging

Product	Product status	Pricing*	Package type	Leads	Package marking	Packing method
NM25C020DWF	Not recommended for new designs	N/A	Wafer	N/A	N/A	RAIL
NM25C020LEMT8X	Not recommended for new designs	$1.06	TSSOP	8	&2&T $Y502 &Z25C020 LEMT8	TAPE REEL
NM25C020LZEM8	Not recommended for new designs	$1.03	SOIC	8	$Y&Z&2&T 25020 LZE	RAIL
NM25C020VM8	Not recommended for new designs	$1.04	SOIC	8	$Y&Z&2&T 25C02 0VM8	RAIL
NM25C020LEM8	Not recommended for new designs	$1.03	SOIC	8	$Y&Z&2&T 25C02 0LE	RAIL
NM25C020LEMT8	Not recommended for new designs	$1.06	TSSOP	8	&2&T $Y502 &Z25C020 LEMT8	RAIL

NM25C020LZEMT8	Not recommended for new designs	$1.07	TSSOP	8	&2&T $Y502 &Z25C020 LZE	RAIL
NM25C020LN	Not recommended for new designs	$1.00	DIP	8	$Y&Z&2&T 25C020 LN	RAIL
NM25C020VM8X	Not recommended for new designs	$1.04	SOIC	8	$Y&Z&2&T 25C02 0VM8	TAPE REEL
NM25C020M8X	Not recommended for new designs	$0.97	SOIC	8	$Y&Z&2&T 25C02 0M8	TAPE REEL
NM25C020LEN	Not recommended for new designs	$1.03	DIP	8	$Y&Z&2&T 25C020 LEN	RAIL
NM25C020LZM8X	Not recommended for new designs	$1.01	SOIC	8	$Y&Z&2&T 25C20 LZM8	TAPE REEL
NM25C020DICE	Not recommended for new designs	N/A	Wafer	N/A	N/A	RAIL
NM25C020LZEMT8X	Not recommended for new designs	$1.07	TSSOP	8	&2&T $Y502 &Z25C020 LZE	TAPE REEL
NM25C020N	Not recommended for new designs	$0.97	DIP	8	$Y&Z&2&T 25C020 N	RAIL
NM25C020LZM8	Not recommended for new designs	$1.01	SOIC	8	$Y&Z&2&T 25020 LZM8	RAIL
NM25C020LZEM8X	Not recommended for new designs	$1.03	SOIC	8	$Y&Z&2&T 25020 LZE	TAPE REEL
NM25C020EM8X	Not recommended for new designs	$1.00	SOIC	8	$Y&Z&2&T 25C02 0EM8	TAPE REEL
NM25C020EM8	Not recommended for new designs	$1.00	SOIC	8	$Y&Z&2&T 25C02 0EM8	RAIL
NM25C020M8	Not recommended for new designs	$0.97	SOIC	8	$Y&Z&2&T 25C02 0M8	RAIL
NM25C020LVM8	Not recommended for new designs	$1.06	SOIC	8	$Y&Z&2&T 25020 LVM8	RAIL
NM25C020LM8X	Not recommended for new designs	$1.00	SOIC	8	$Y&Z&2&T 25C02 0LM8	TAPE REEL

NM25C020LM8	Not recommended for new designs	$1.00	SOIC	8	$Y&Z&2&T 25C02 0LM8	RAIL
NM25C020LEM8X	Not recommended for new designs	$1.03	SOIC	8	$Y&Z&2&T 25C02 0LE	TAPE REEL
NM25C020EN	Not recommended for new designs	$1.00	DIP	8	$Y&Z&2&T 25C020 EN	RAIL

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