March 2015

FAN6100HM
Secondary-Side Constant Voltage and Constant Current Controller Compatible with MediaTek Pump Express™ Plus

Features

- Supports MediaTek Pump Express™ Plus and Fairchild's FCP-Single Communication Protocol Specifications
- Secondary-Side Constant Voltage (CV) and Constant Current (CC) Regulation
- Built-in Charge-Pump Circuit for Low Output Voltage Operation
- Internal, Accurate, Adaptive CV/CC Reference Voltage
- Low-Value Current Sensing Resistor for High Efficiency
- Programmable Cable Voltage Drop Compensation
- Two Operational Transconductance Amplifiers with Open-Drain Type for Dual-Loop CV/CC Control
- Compatible with Fairchild's FAN501A
- Adaptive Secondary-Side Output Over-Voltage Protection through Photo-Coupler
- Output Under-Voltage Protection
- Low Quiescent Current Consumption in Green Mode < 850 µA
- Maximum Current Rating: 3 A
- Available in 20-Pin 3 x 4 mm MLP Package

Applications

- Battery Chargers for Quick Charge Application

AC/DC Adapters for Portable Devices that Require CV/CC Control

Description

The FAN6100HM is a highly integrated secondary side constant voltage and constant current controller that is compatible with MediaTek Pump Express™ Plus and Fairchild's FCP-Single communication protocol specifications. It is designed for use in applications that requires Constant Voltage (CV) and Constant Current (CC) regulations.

The controller consists of two operational amplifiers for voltage and current loop regulation with adjustable reference voltage. The CC control loop also incorporates a current sense amplifier with gain of 10. Outputs of the CV and CC amplifiers are tied together in open drain configuration.

The FAN6100HM enables power adaptor's output voltage adjustment if it detects a protocol capable powered device. It can be capable of outputting 5 V at the beginning, and then 7 V, 9 V or 12 V to meet requirements of a High Voltage Dedicated Charging Port (HVDCP) power supply or 4.8 V, 4.6 V, 4.4 V, 4.2 V or 4 V to maximize the charging current which is controlled by the power adaptor. If a non compliant powered device is detected, the controller disables output voltage adjustment to ensure safe operation with smart phones and tablets that support only 5 V.

FAN6100HM also incorporates an internal charge pump circuit to maintain CC regulation down to the power supply's output voltage, Vbus of 2 V without an external voltage supply to the IC. Programmable cable voltage drop compensation allows precise CV regulation at end of USB cable via adjusting one external resistor.

Compared to the FAN6100M, the FAN6100HM's maximum current rating is 3 A which can support higher power system design.

The device is available in the 20-pin MLP 3 x 4 package.

MediaTek® PumpExpress+

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6100HMMPX	-40°C to +125°C	20-Lead, MLP, QUAD, JEDEC MO-220, 3 mm x 4 mm, 0.5 mm Pitch, Single DAP	Tape & Reel

Application Diagram

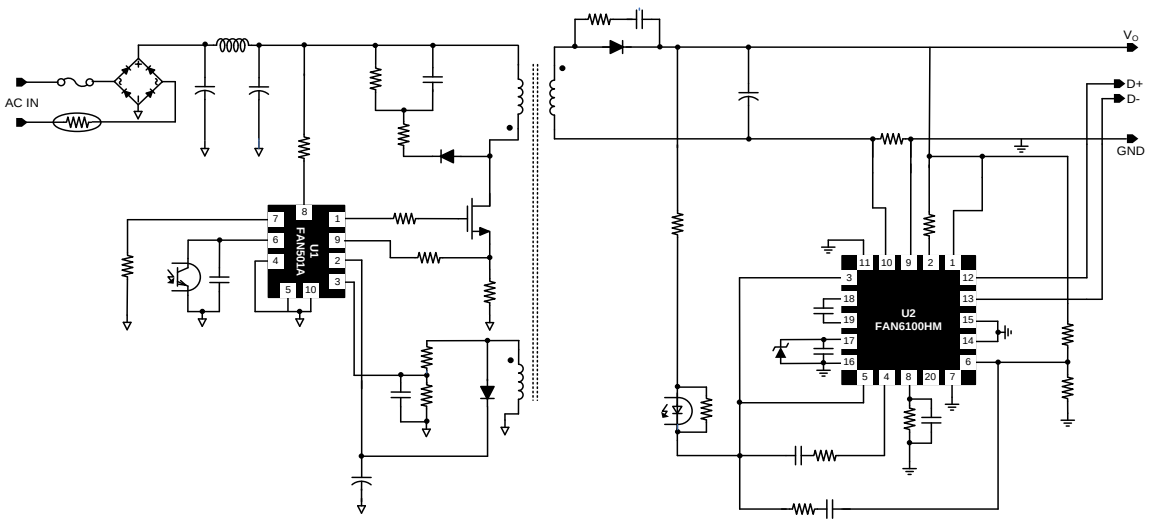


Figure 1. Typical Application

Internal Block Diagram

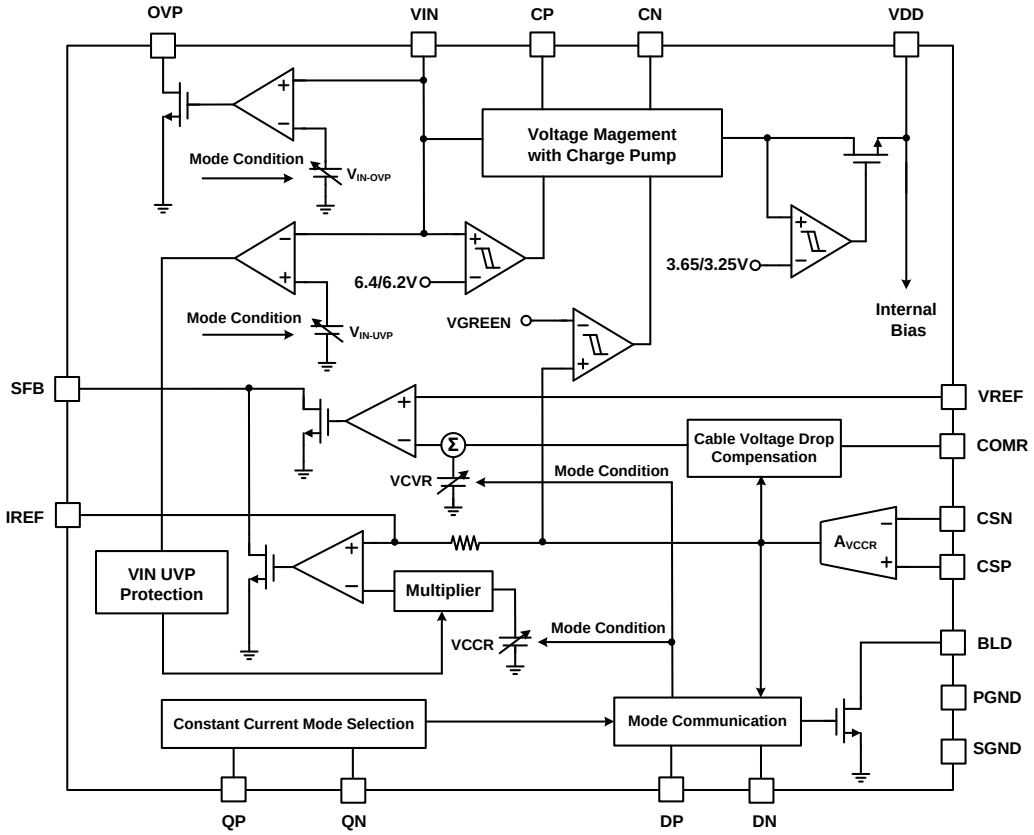
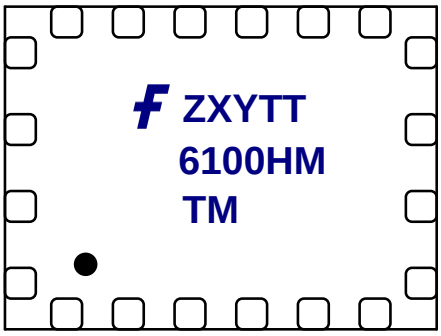


Figure 2. Function Block Diagram

Marking Information



***F*- Fairchild Logo**
Z: Assembly Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
T: Package Type (MP=MLP)
M: Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

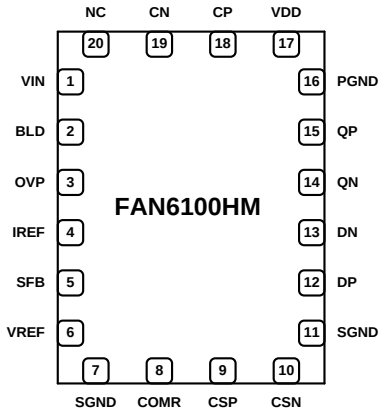


Figure 4. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	VIN	Input Voltage Detection. This pin is tied to output terminal of the power adaptor to monitor output voltage and supply internal charge pump circuit.
2	BLD	Output Bleeder Current Setting. This pin connects to output terminal of the power adaptor via an external resistor to form an output discharging path when mode changes from high-output voltage to low-output voltage.
3	OVP	Output Over-Voltage-Protection. This pin is used for adaptive output over-voltage protection. Typically an opto-coupler is connected to this pin to generate pull-low protection signal.
4	IREF	Reference Output Current Sensing Voltage. The voltage is the amplifying output current sensing voltage. This pin is tied to the internal CC loop amplifier positive terminal.
5	SFB	Secondary-Side Feedback Signal. Common output terminal of the dual operational transconductance amplifiers with open drain operation. Typically an opto-coupler is connected to this pin to provide feedback signal to the primary-side PWM controller.
6	VREF	Reference Output Voltage Sensing Voltage. This pin is used to sense the output voltage for CV regulation via resistor divider. It is tied to the internal CV loop amplifier positive terminal.
7	SGND	Signal Ground.
8	COMR	Programmable Cable-Drop Voltage Compensation. An external resistor is connected to this pin to adjust output voltage compensation weighting.
9	CSP	Positive Terminal of Output Current Sensing Amplifier. This pin connects directly to the positive voltage terminal of the current sense resistor. CSP need to be tied to ground of power adaptor via short PCB trace.
10	CSN	Negative Terminal of Output Current Sensing Amplifier. This pin connects directly to the negative voltage terminal of the current sense resistor. CSN need to be tied to negative terminal of output capacitor via short PCB trace.
11	SGND	Signal Ground.
12	DP	Positive Terminal of Communication Interface. This pin is tied to the USB D+ data line input.
13	DN	Negative Terminal of Communication Interface. This pin is tied to the USB D- data line input.
14	QN	LSB Switch for Mode Selection of Output Current.
15	QP	MSB Switch for Mode Selection of Output Current.
16	PGND	Power Ground.
17	VDD	Power Supply. IC operating current is supplied through this pin. This pin is typically connected to an external VDD capacitor.
18	CP	Positive Voltage Terminal of Charge Pump.
19	CN	Negative Voltage Terminal of Charge Pump. An external capacitor is necessary to be connected between CP pin and CN pin.
20	NC	No Connect

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{VIN}	VIN Pin Input Voltage			20	V
V_{BLD}	BLD Pin Input Voltage			20	V
V_{OVP}	OVP Pin Input Voltage			20	V
V_{SFB}	SFB Pin Input Voltage		-0.3	20	V
V_{IREF}	IREF Pin Input Voltage		-0.3	6.0	V
V_{VREF}	VREF Pin Input Voltage		-0.3	6.0	V
V_{COMR}	COMR Pin Input Voltage		-0.3	6.0	V
V_{CSP}	CSP Pin Input Voltage		-0.3	6.0	V
V_{CSN}	CSN Pin Input Voltage		-0.3	6.0	V
V_{DP}	DP Pin Input Voltage		-0.3	6.0	V
V_{DN}	DN Pin Input Voltage		-0.3	6.0	V
V_{QN}	QN Pin Input Voltage		-0.3	6.0	V
V_{QP}	QP Pin Input Voltage		-0.3	6.0	V
V_{DD}	VDD Pin Input Voltage		-0.3	6.0	V
V_{CP}	CP Pin Input Voltage		-0.3	6.0	V
V_{CN}	CN Pin Input Voltage		-0.3	6.0	V
P_D	Power Dissipation (T_A=25°C)			0.88	W
θ_{JA}	Thermal Resistance (Junction-to-Air)			110	°C/W
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-40	+150	°C
T_L	Lead Temperature, (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22_A114		2.5	kV
		Charged Device Model, JEDEC:JESD22_C101		2.0	

Note:

1. All voltage values, except differential voltages, are given with respect to GND pin.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_J	Junction Temperature	-40	+125	°C
V_{DD-OP}	VDD operating voltage	3.12	6.00	V
V_{IN-OP}	VIN operating voltage		16	V

Electrical Characteristics

Recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIN Section						
$I_{IN-OP-LV}$	Operating Supply Current at 5 V (5 V, 4.8 V, 4.6 V, 4.4 V, 4.2 V, 4 V)	V_{IN}=5 V, V_{CSP}=100 mV, V_{CSN}=0 V		2.4	3.2	mA
$I_{IN-OP-HV}$	Operating Supply Current Over 5 V (7 V, 9 V, 12V)	V_{IN}=12 V, V_{CSP}=100 mV, V_{CSN}=0 V		1.2	2.0	mA
$I_{IN-Green}$	Green Mode Operating Supply Current	V_{IN}=5 V, V_{CSP}=V_{CSN}=0 V		850	1050	µA
I_{IN-ST}	Startup Current	V_{IN}=1 V, V_{CSP}=100 mV, V_{CSN}=0 V			15	µA
$V_{IN-UVP-L-LV}$	VIN Under-Voltage-Protection Enable Voltage under 5 V		2.35	2.50	2.65	V
$V_{IN-UVP-H-LV}$	VIN Under-Voltage-Protection Disable Voltage under 5 V		2.85	3.00	3.15	V
$V_{IN-UVP-L-7V}$	VIN Under-Voltage-Protection Enable Voltage at 7 V		5.05	5.25	5.45	V
$V_{IN-UVP-H-7V}$	VIN Under-Voltage-Protection Disable Voltage at 7 V		5.75	5.95	6.15	V
$V_{IN-UVP-L-9V}$	VIN Under-Voltage-Protection Enable Voltage at 9 V		6.50	6.75	7.00	V
$V_{IN-UVP-H-9V}$	VIN Under-Voltage-Protection Disable Voltage at 9 V		7.40	7.65	7.90	V
$V_{IN-UVP-L-12V}$	VIN Under-Voltage-Protection Enable Voltage at 12 V		8.70	9.00	9.30	V
$V_{IN-UVP-H-12V}$	VIN Under-Voltage-Protection Disable Voltage at 12 V		9.85	10.20	10.55	V
$t_{D-VIN-UVP}$	VIN Under-Voltage-Protection Debounce Time		10	15	20	ms
$V_{IN-EN-L}$	Charge-Pump Enable Threshold Voltage		1.5	2.0	2.5	V
V_{IN-CP}	Charge Pump Disable Threshold Voltage		6.20	6.40	6.60	V
$V_{IN-CP-Hys}$	Hysteresis Voltage for Charge Pump Disable Threshold Voltage			0.20		V
$V_{IN-OVP-LV}$	VIN Over-Voltage-Protection Voltage under 5 V		5.80	6.00	6.20	V
$V_{IN-OVP-7V}$	VIN Over-Voltage-Protection Voltage at 7 V		8.10	8.40	8.70	V
$V_{IN-OVP-9V}$	VIN Over-Voltage-Protection Voltage at 9 V		10.50	10.80	11.10	V
$V_{IN-OVP-12V}$	VIN Over-Voltage-Protection Voltage at 12 V		14.00	14.40	14.80	V
$t_{D-VIN-OVP}$	VIN Over-Voltage-Protection Debounce Time		16	28	40	µs
VDD Section						
V_{DD-ON}	Turn-on Threshold Voltage		3.50	3.65	3.80	V
V_{DD-OFF}	Turn-off Threshold Voltage		3.12	3.25	3.38	V
f_{S-CP}	Charge Pump Switching Frequency[2]		120	125	130	kHz
CC Mode Selection Section						
QP/QN-M1	QP/QN State for Mode 1		QP=0 and QN=0			
QP/QN-M2	QP/QN State for Mode 2		QP=0 and QN=1			
QP/QN-M3	QP/QN State for Mode 3		QP=1 and QN=0			
QP/QN-M4	QP/QN State for Mode 4		QP=1 and QN=1			
t_{D_Mode}	CC Mode Selection De-bounce Time		3.5	4.0	4.5	ms

Continued on the following page…

Electrical Characteristics

Recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Constant Current Sensing Section						
A_{V-CCR}	Output Current Sensing Amplifier Gain[3]		9.7	10.0	10.3	V/V
$V_{CSP-CSN-M1}$	Voltage difference between CSP and CSN at Mode 1		108.8	113.4	118.0	mV
$V_{CSP-CSN-M2}$	Voltage difference between CSP and CSN at Mode 2		133.0	138.6	144.2	mV
$V_{CSP-CSN-M2-12V}$	Voltage difference between CSP and CSN at Mode 2 and 12 V		100.8	105.0	109.2	mV
$V_{CSP-CSN-M3}$	Voltage difference between CSP and CSN at Mode 3		157.2	163.8	170.4	mV
$V_{CSP-CSN-M4}$	Voltage difference between CSP and CSN at Mode 4		157.2	163.8	170.4	mV
$V_{CSP-CSN-M4-12V}$	Voltage difference between CSP and CSN at Mode 4 and 12 V		120.9	126.0	131.1	mV
$A_{V-CCR-UVP}$	Constant Current Attenuator for V_{IN} Under-Voltage Protection				0.125	V/V
$V_{CSP-CSN\_Green-L}$	Voltage difference between CSP and CSN to Enable Green Mode		42	47	52	mV
$V_{CSP-CSN\_Green-H}$	Voltage difference between CSP and CSN to Disable Green Mode		55.4	63.0	70.6	mV
$t_{Green-BLANK}$	Green Mode Blanking Time at Startup[3]			40		ms
Constant Voltage Sensing Section						
V_{CVR-4V}	Reference Voltage for Constant Voltage Regulation at 4 V		0.770	0.800	0.830	V
$V_{CVR-4.2V}$	Reference Voltage for Constant Voltage Regulation at 4.2 V		0.810	0.840	0.870	V
$V_{CVR-4.4V}$	Reference Voltage for Constant Voltage Regulation at 4.4 V		0.850	0.880	0.910	V
$V_{CVR-4.6V}$	Reference Voltage for Constant Voltage Regulation at 4.6 V		0.890	0.920	0.950	V
$V_{CVR-4.8V}$	Reference Voltage for Constant Voltage Regulation at 4.8 V		0.930	0.960	0.990	V
V_{CVR-5V}	Reference Voltage for Constant Voltage Regulation at 5 V		0.980	1.000	1.020	V
V_{CVR-7V}	Reference Voltage for Constant Voltage Regulation at 7 V		1.375	1.400	1.425	V
V_{CVR-9V}	Reference Voltage for Constant Voltage Regulation at 9 V		1.765	1.800	1.835	V
$V_{CVR-12V}$	Reference Voltage for Constant Voltage Regulation at 12 V		2.355	2.400	2.445	V
Cable Drop Compensation Section						
$K_{COMR-CDC}$	Design Parameter for Cable-Drop Voltage Compensation		0.90	1.00	1.10	µA/V
Constant Current Amplifier Section						
G_{m-CC}	CC Amplifier Transconductance[3]			3.5		S
f_{P-CC}	CC Amplifier Dominate Pole[3]			10		kHz
$R_{CC-IN-CC}$	CC Amplifier Input Resistor[3]		8.50	13.75	19.00	kΩ

Continued on the following page…

Electrical Characteristics

Recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Constant Voltage Amplifier Section						
$G_{m\text{-}CV}$	CV Amplifier Transconductance[3]			3.5		S
$f_{P\text{-}CV}$	CV Amplifier Dominate Pole[3]			10		kHz
$I_{Bias\text{-}IN\text{-}CV}$	CV Amplifier Input Bias Current[3]				30	nA
Output Bleeder Section						
I_{BLD}	Output Bleeder Current[3]		100		700	mA
t_{BLD}	Output Bleeder Current Discharging Time		290	320	350	ms
Secondary-Side Feedback Section						
$I_{SFB\text{-}Sink\text{-}MAX}$	Maximum SFB Pin Sink Current [3]		2			mA
OVP Section						
$I_{OVP\text{-}Sink\text{-}MAX}$	Maximum OVP Pin Sink Current		2			mA
FCP-Single Protocol Section						
V_{DPL}	DP Low Level Threshold Voltage	BC1.2 Detection	0.23	0.25	0.27	V
V_{DNL}	DN Low Level Threshold Voltage	BC1.2 Detection	0.30	0.35	0.40	V
$t_{BC1.2}$	DP and DN High Debounce Time		1.0		1.5	S
R_{DP}	DP Resistance		300	500	700	kΩ
R_{DN}	DN Pull-Low Resistance		14.25	19.53	24.80	kΩ
t_{TOGGLE}	DN Low Debounce Time after BC1.2 Detection				1	ms
V_{DN_HI}	DN High Threshold Voltage		1			V
V_{DN_LO}	DN Low Threshold Voltage				0.5	V
T_{DN_FLT}	DN Detection Debounce Time[3]			50		µs
T_{START}	Minimum Low in the Beginning of Control Signal		20			ms
T_{5V_LS}	Low-Speed Mode - Period for Voltage Reset to 5 V		8	10	12	ms
T_{SV+_LS}	Low-Speed Mode - Period for Voltage Increase		13.3	15.3	17.3	ms
T_{5V_HS}	High-Speed Mode - Period for Voltage Reset to 5 V		77	102	127	µs
T_{SV+_HS}	High-Speed Mode - Period for Voltage Increase		157	182	206	µs
Pump Express Protocol Section						
t_{ON_CCA}	Current Control Pattern Timing On Time (A)		410	500	600	ms
t_{ON_CCB}	Current Control Pattern Timing On Time (B)		220	300	370	ms
t_{ON_CCC}	Current Control Pattern Timing On Time (C)		50	100	150	ms
t_{ON_CCD}	Current Control Pattern Timing Off Time (D)		50	100	150	ms
$V_{REF\_H\_PE}$	Current Sense High Threshold Voltage	Max. Current Control Low Current is 130 mA and Min. Current Control High Current is 350 mA	9.3	13.3	17.3	mV
V_{REF_Hys}	Hysteresis for Current Sense Low signal Detection			2		mV
T_{WDT}	Current Plug-Out Detection Debounce Time		180		240	ms

Notes:

2. Guaranteed for temperature range -5°C ~85°C.
3. Guaranteed by design

Typical Performance Characteristics

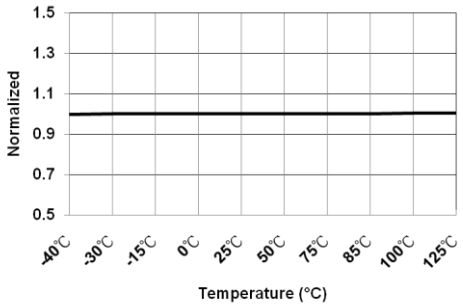


Figure 5. V_{DD} Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

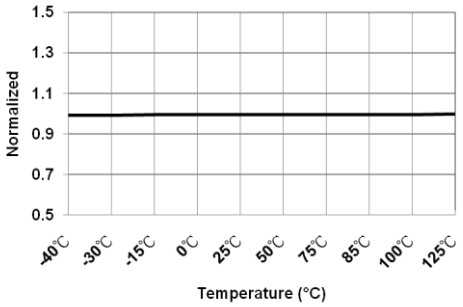


Figure 6. V_{DD} Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

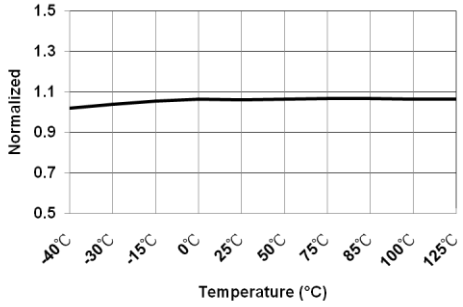


Figure 7. Operating Current Under 5 V ($I_{IN-OP-LV}$) vs. Temperature

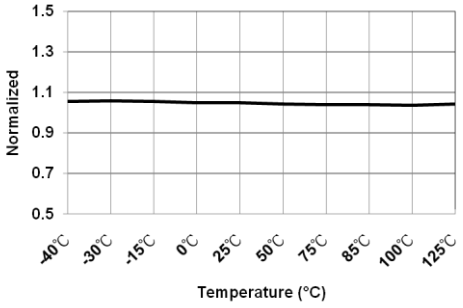


Figure 8. Operating Current Over 5 V ($I_{IN-OP-HV}$) vs. Temperature

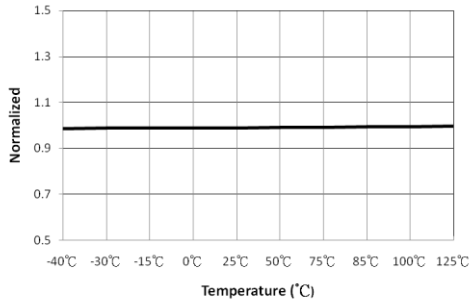


Figure 9. Voltage Difference between CSP and CSN at Mode 1 ($V_{CSP-CSN-M1}$) vs. Temperature

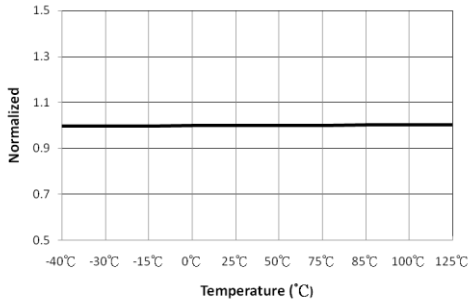


Figure 10. Voltage Difference between CSP and CSN at Mode 2 ($V_{CSP-CSN-M2}$) vs. Temperature

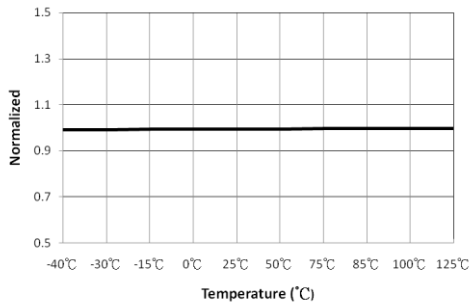


Figure 11. Voltage Difference between CSP and CSN Mode 2 and 12 V ($V_{CSP-CSN-M2-12V}$) vs. Temperature

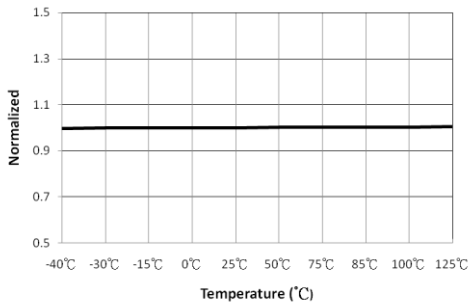


Figure 12. Voltage Difference between CSP and CSN at Mode 3 ($V_{CSP-CSN-M3}$) vs. Temperature

Typical Performance Characteristics

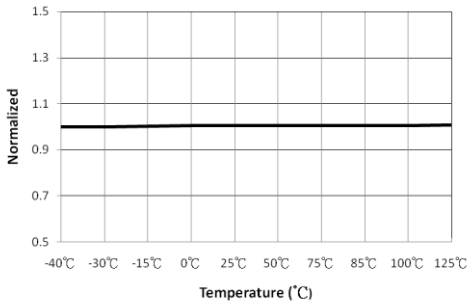


Figure 13. Voltage Difference between CSP and CSN at Mode 4 ($V_{CSP-CSN-M4}$) vs. Temperature

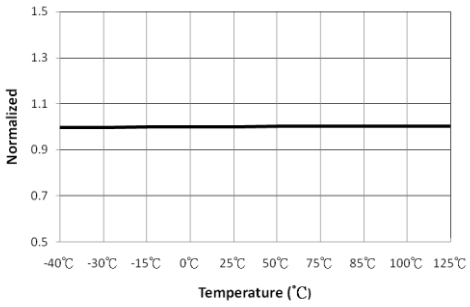


Figure 14. Voltage Difference between CSP and CSN at Mode 4 and 12 V ($V_{CSP-CSN-M4-12V}$)vs. Temperature

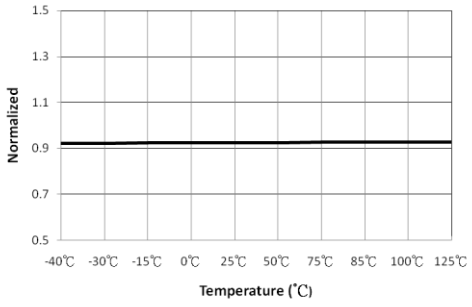


Figure 15. Voltage Difference between CSP and CSN to Enable Green Mode ($V_{CSP-CSN-Green-L}$) vs. Temperature

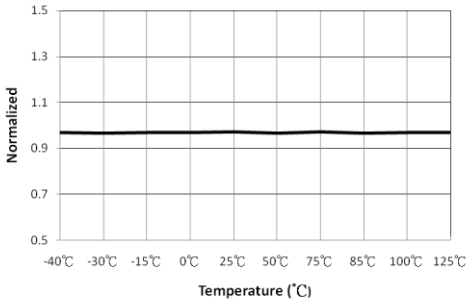


Figure 16. Voltage Difference between CSP and CSN to Disable Green Mode ($V_{CSP-CSN-Green-H}$) vs. Temperature

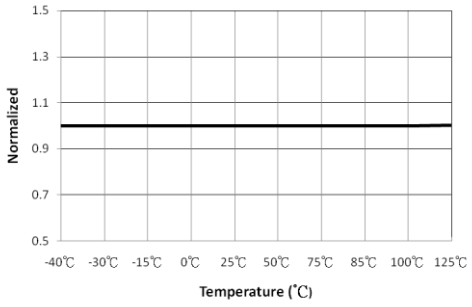


Figure 17. Reference Voltage for CV Regulation at 4 V (V_{CVR-4V}) vs. Temperature

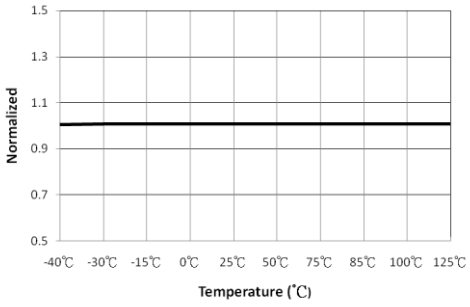


Figure 18. Reference Voltage for CV Regulation at 4.2 V ($V_{CVR-4.2}V$) vs. Temperature

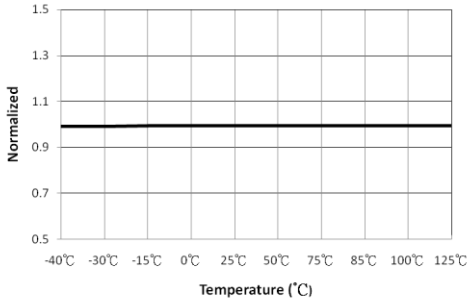


Figure 19.Reference Voltage for CV Regulation at 4.4 V ($V_{CVR-4.4V}$) vs. Temperature

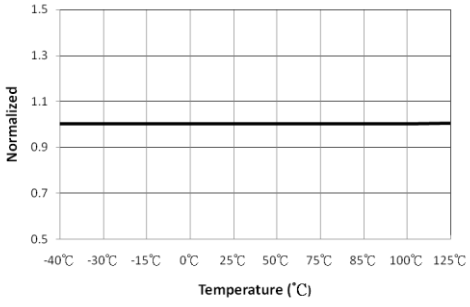


Figure 20. Reference Voltage for CV Regulation at 4.6 V ($V_{CVR-4.6V}$) vs. Temperature

Typical Performance Characteristics

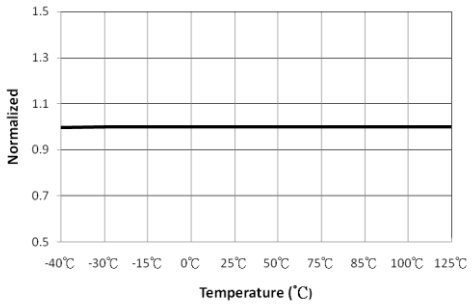


Figure 21. Reference Voltage for CV Regulation at 4.8 V ($V_{CVR-4.8V}$) vs. Temperature

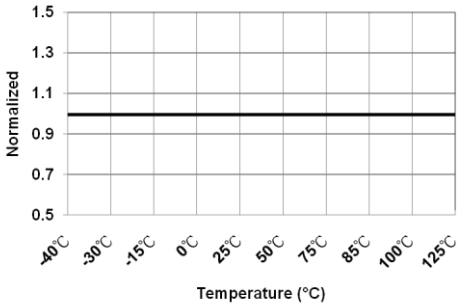


Figure 22. Reference Voltage for CV Regulation at 5 V (V_{CVR-5V}) vs. Temperature

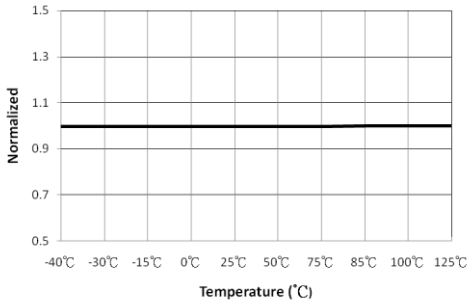


Figure 23. Reference Voltage for CV Regulation at 7 V (V_{CVR-7V}) vs. Temperature

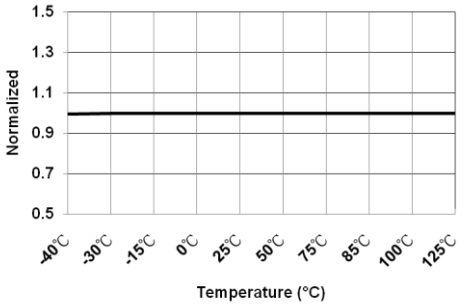


Figure 24. Reference Voltage for CV Regulation at 9 V (V_{CVR-9V}) vs. Temperature

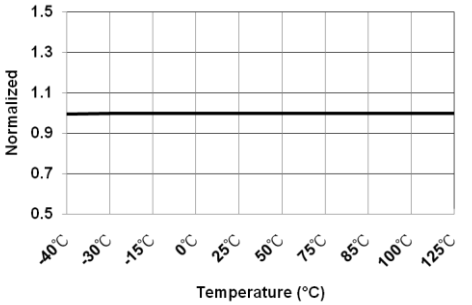


Figure 25. Reference Voltage for CV Regulation at 12 V ($V_{CVR-12V}$) vs. Temperature

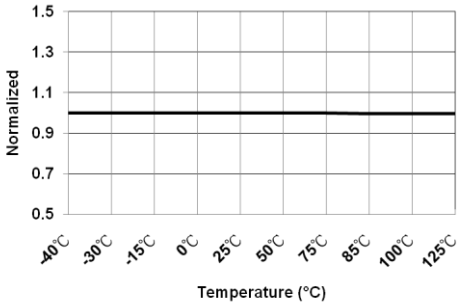


Figure 26. V_{IN} OVP Voltage Under 5 ($V_{IN-OVP-LV}$) vs. Temperature

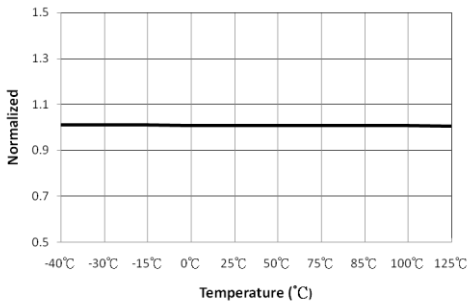


Figure 27. V_{IN} OVP Voltage at 7 V ($V_{IN-OVP-7V}$) vs. Temperature

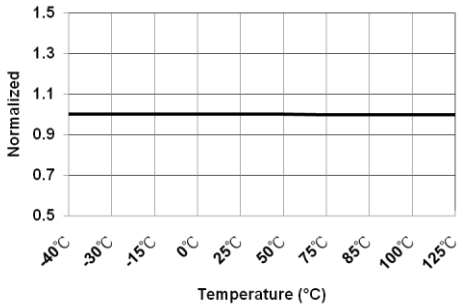


Figure 28. V_{IN} OVP Voltage at 9 V ($V_{IN-OVP-9V}$) vs. Temperature

Typical Performance Characteristics

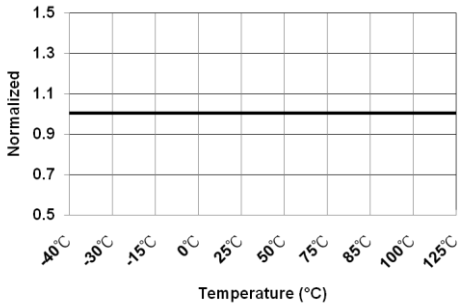


Figure 29. V_{IN} UVP Disable Voltage at 9 V ($V_{IN-UVP-H-9V}$) vs. Temperature

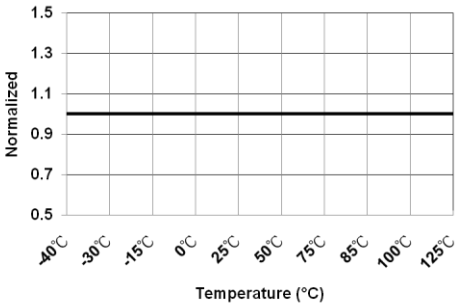


Figure 30. $V_{IN\ UVP}$ Enable Voltage at 12 V ($V_{IN-UVP-L-12V}$) vs. Temperature

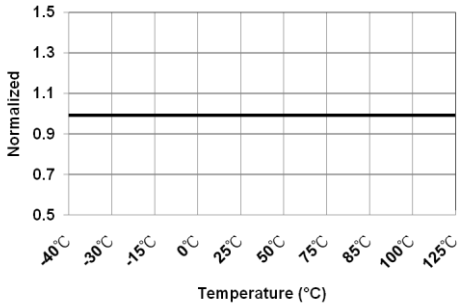


Figure 31. V_{IN} UVP Disable Voltage at 12 V ($V_{IN-UVP-H-12V}$) vs. Temperature

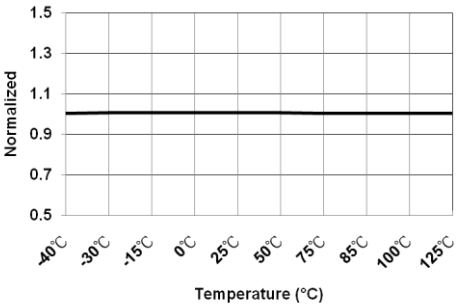


Figure 32. Charge Pump Disable Threshold Voltage (V_{IN-CP}) vs. Temperature

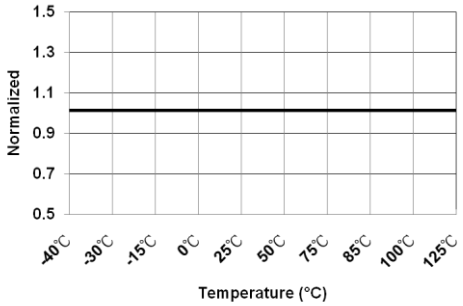


Figure 33. DP Low Level Threshold Voltage (V_{DPL}) vs. Temperature

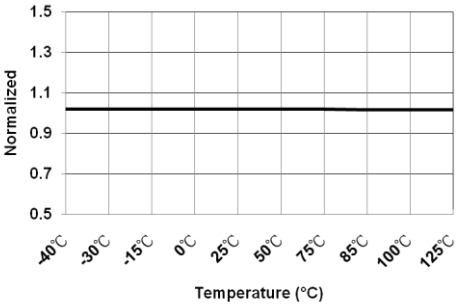


Figure 34. DN Low Level Threshold Voltage (V_{DNL}) vs. Temperature

Functional Description

The highly integrated secondary-side power Constant Voltage and Constant Current Controller FAN6100HM is compatible with MediaTek Pump Express™ Plus fast-charging and Fairchild's own FCP-Single communication protocol for quick charger applications. It can be an optimal solution for quick charger requirement. The FAN6100HM enables power supply's output voltage adjustment if it detects a protocol capable mobile phone and/ or tablet. When a compliant powered device is detected, the FAN6100HM will produce BC1.2 procedure then will be ready to acknowledge which protocol comes in. At that moment Output voltage is generated to 5 V as default and then changes to 7 V, 9 V or 12 V to meet quick charger requirements of HVDCP power supplies. These voltages are based on the capabilities of the downstream device. The downstream device requests an output voltage for the HVDCP power supply. If a non compliant powered device is detected, the controller disables adaptive output voltage to ensure safe operation with smart phones and tablets that support only 5 V.

The controller consists of two operational amplifiers for Constant Voltage (CV) and Constant Current (CC) regulation with adjustable references voltage. The CC control loop also incorporates a current sense amplifier with a gain of 10. Outputs of the CV and CC amplifiers are tied together in open drain configuration. FAN6100HM also incorporates an internal charge pump circuit to maintain CC regulation down to the power supply's output voltage, V_{BUS} of 2 V without an external voltage supply to the IC. Programmable cable voltage drop compensation allows precise CV regulation at the end of USB cable via adjusting one external resistor.

Protection functions of the FAN6100HM include adaptive V_{IN} Over-Voltage Protection (V_{IN} OVP) and adaptive V_{IN} Under-Voltage Protection (V_{IN} UVP).

Constant-Voltage Regulation Operation

Figure 35 shows the primary-side internal PWM control circuit of the FAN501A and secondary side regulator circuit of the FAN6100HM which consists of two operational amplifiers for Constant Voltage (CV) and Constant Current (CC) regulation with adjustable voltage references.

The constant voltage (CV) regulation is implemented in the same way as the conventional isolated power supply. Output voltage is sensed on the VREF pin via the resistor divider, R_{F1} and R_{F2} and compared with the internal reference voltage for constant voltage regulation (V_{CVR}) to generate a CV compensation signal (COMV) on the SFB pin. The compensation signal is transferred to the primary-side using an opto-coupler and applied to the PWM comparator through attenuator Av to determine the duty cycle.

Constant-Current Regulation Operation

The constant current (CC) regulation is implemented with sensing the output current. The output current is sensed via the current-sense resistor (R_{CS}) connected between the CSP and CSN pins and placed on the output ground return path. The sensed signal is amplified by internal current sensing amplifier $A_{V\text{-}CCR}$ before the amplified current feedback signal is fed into the positive terminal of the internal operational amplifier and compared with the internal reference voltage for constant current regulation (V_{CCR}) to generate a CC compensation signal (COMI) on the SFB pin. The compensation signal is transferred to the primary-side using an opto-coupler to the primary-side PWM controller.

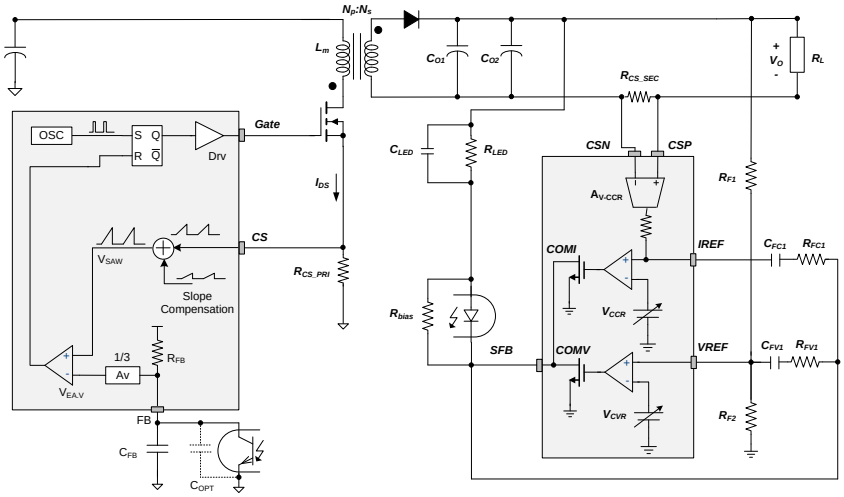


Figure 35. Internal PWM Control Circuit

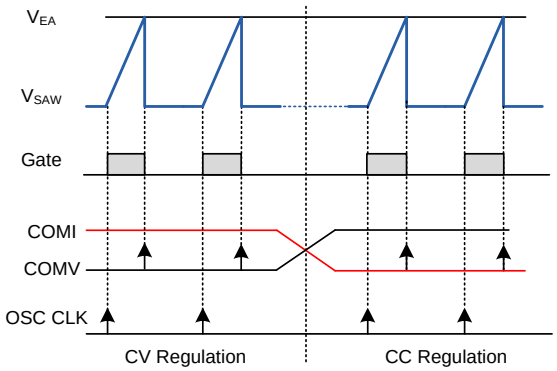


Figure 36. PWM Operation for CV and CC

V_{EA} is compared with an internal sawtooth waveform (V_{SAW}) by PWM comparators to determine the duty cycle. As seen in Figure 35, output of the comparator is used as a reset signal of flip-flop to determine the MOSFET turn-off instant. The lower signal, either COMV or COMI, is transferred to the primary-side to determine the duty cycle, as shown in Figure 36. During CV regulation, COMV is transferred to the primary-side to determine the duty cycle while COMI is saturated to HIGH. During CC regulation, COMI is transferred to the primary-side to determine the duty cycle while COMV is saturated to HIGH.

Green Mode Operation

FAN6100HM has Green Mode operation with low quiescent current consumption (< 850 µA). During green mode, the charge pump function is disabled to reduce power consumption. The FAN6100HM enters green mode when the amplified output current sensed signal is smaller than 47 mV. If amplified output current sensed signal increases to be greater than 63 mV, FAN6100HM leaves green mode and the charge pump function is enabled.

Once FAN6100HM enters green mode, the operating current is also reduced from 2.4 mA to 850 µA to minimize power consumption. It provides low power consumption by the green mode operation at no load.

Constant Current Mode Selection

FAN6100HM provides flexible output CC choice for a variety of power rating designs. The control signal is a logic level signal for constant current mode determined by QP and QN pin settings. The output constant current mode selection specifications are as follows:

Table 1. Mode Descriptions and Settings

Mode Description	Mode Setting
Mode 1	QP=0 and QN=0
Mode 2	QP=0 and QN=1
Mode 3	QP=1 and QN =0
Mode 4	QP=1 and QN =1

For mode 1 setting, it is fixative output CC 2 A for each output voltage level. The specifications are as follows:

Table 2. Mode 1 Specifications

Output Voltage	Rated Current
4 V	2 A
4.2 V	
4.4 V	
4.6 V	
4.8 V	
5 V	
7 V	
9 V	
12 V	

For Mode 2 setting, it is fixative CC output 2.5 A except for 12 V mode. The specifications are as follows:

Table 3. Mode 2 Specifications

Output Voltage	Rated Current
4 V	2.5 A
4.2 V	
4.4 V	
4.6 V	
4.8 V	
5 V	
7 V	
9 V	
12 V	1.87 A

For Mode 3 setting, it is fixative CC output 3 A for each output voltage level. The specifications are as follows:

Table 4. Mode 3 Specifications

Output Voltage	Rated Current
4 V	3 A
4.2 V	
4.4 V	
4.6 V	
4.8 V	
5 V	
7 V	
9 V	
12 V	

For Mode 4 setting, it is fixative CC output 3 A except for 12 V mode. The specifications are as follows:

Table 5. Mode 4 Specifications

Output Voltage	Rated Current
4 V	3 A
4.2 V	
4.4 V	
4.6 V	
4.8 V	
5 V	
7 V	
9 V	
12 V	2.25 A

Cable Voltage Drop Compensation

FAN6100HM incorporates programmable cable voltage drop compensation function via adjusting one external resistor to maintain constant voltage regulation at the end of USB cable.

Figure 37 shows the internal block of the cable voltage drop compensation function. Output current information is obtained from the amplified current sensing voltage. Depending on the weighting of the external resistor, the current signal is modulated to offset the CV loop reference voltage, V_{CVR}. Thus, output voltage is increased by this offset voltage on the CV loop reference to compensate for cable voltage drop.

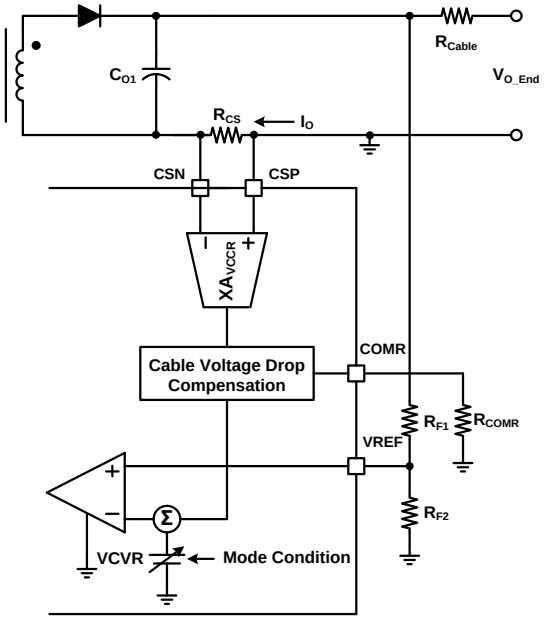


Figure 37. Cable Voltage Drop Compensation Block

Supply Voltage and Charge Pump Operation

Figure 38 shows the supply voltage circuit, including V_{DD} and the charge-pump circuit. FAN6100HM can withstand up to 20 V on the VIN pin and enable this pin to be connected directly to the output terminal of a power supply.

During startup, the charge-pump circuit is enabled when V_{IN} voltage is larger than 2 V and disabled after 40 ms from the V_{DD} voltage reaches V_{DD-ON} (3.65 V). The charge-pump circuit is used to boost the V_{DD} voltage to maintain normal operation for the controller when output voltage is low. The charge-pump stage includes a Low Dropout (LDO) pre-regulator and a charge-pump circuit. The LDO pre-regulator regulates the input voltage of charge-pump circuit to 2.7 V and then boosts up the V_{DD} voltage when VIN is lower than V_{IN-CP} (6.4 V) and out of Green Mode. When V_{IN} is greater than the value 6.2 V which subtract V_{IN-CP} from $V_{IN-CP-Hys}$ or lower than V_{IN-CP} (6.4 V) in Green Mode, the charge-pump circuit is disabled and the VIN voltage is fed directly to V_{DD}.

When charge-pump circuit is disabled, output capacitor supplies charging current to charge the hold-up capacitor C_{VDD}. The V_{DD} voltage is clamped at 5.4 V by internal Zener diode when the charge-pump circuit is disabled.

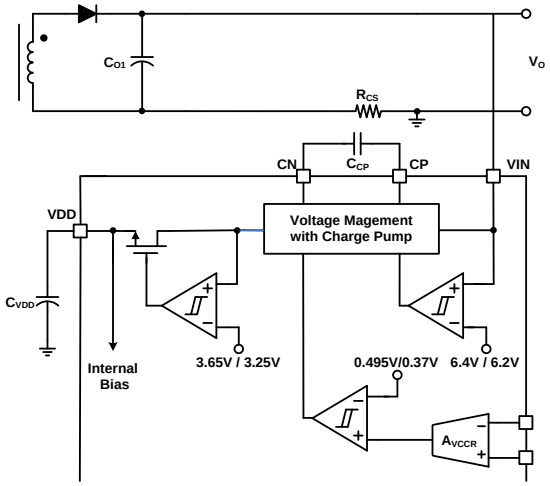


Figure 38. Supply Voltage Block

Output Bleeder Section

For HVDCP power supply applications, a discharge path on the output of the HVDCP power supply is necessary to ensure that a high output voltage level can transfer to a low output voltage level quickly during mode changes. This is especially critical under no-load condition where the natural decay rate of the output voltage is low. To enable output bleeder function when the mode changes from high output voltage to low output voltage can ensure short voltage transition time.

Figure 39 shows the internal block of output bleeder function. The FAN6100HM implements the output bleeder function to discharge the output voltage rapidly during mode changes. The BLD pin is connected to the output voltage terminal as the discharging path. When the high output voltage to low output voltage mode change signal is initiated, an internal switch is turned on to discharge the output voltage. The switch stays on until $t_{BLD-MAX}$ is reached. The BLD pin can withstand up to 20 V and enable this pin to be connected directly to the output terminal of a HVDCP power supply.

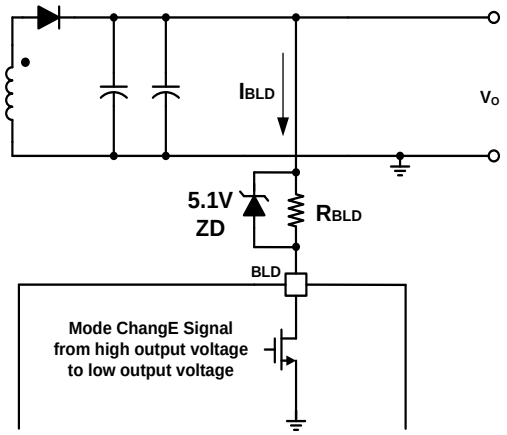


Figure 39. Output Bleeder Function

V_{IN} Over-Voltage-Protection (OVP)

Figure 40 shows the V_{IN} over-voltage protection (OVP) block, which is adaptive operated according to mode condition. Output voltage is sensed through the VIN pin for OVP detection. Once output voltage rises to V_{IN-OVP} by each mode and then V_{IN} OVP is triggered, where V_{IN} OVP occurs, the OVP pin is pulled down to ground through an internal switch until V_{DD-OFF} (3.25 V) is reached.

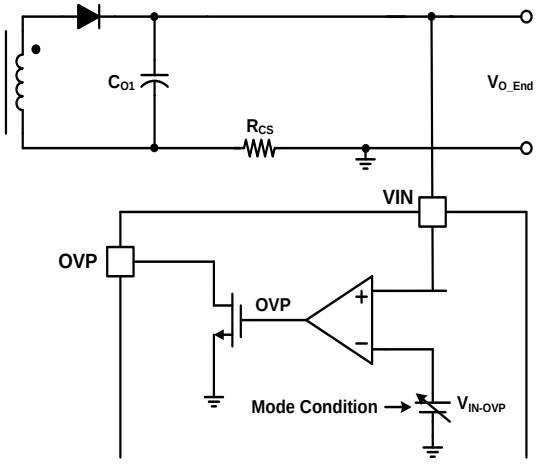


Figure 40. V_{IN} Over-Voltage-Protection

V_{IN} Under-Voltage-Protection (UVP)

Figure 41 shows the V_{IN} under-voltage protection (V_{IN} UVP) block. The output current is reduced to protect the system at 5 V, 7 V, 9 V and 12 V condition when V_{IN} UVP function is triggered. Once output voltage drops below $V_{IN-UVP-L}$, the CC reference voltage V_{CCR} is adjusted and modified by $A_{V-CCR-UVP}$. The output current can be calculated as:

$$I_{O\_CC} \le \frac{V_{CSP-CSN}}{R_{CS}} \cdot A_{V-CCR-UVP} \quad (1)$$

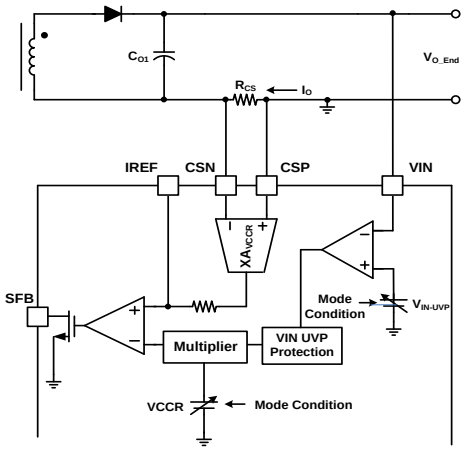


Figure 41. V_{IN} Under-Voltage Protection Block

Protocol Communication

(1) MediaTek Pump Express™ Plus Fast-Charging

FAN6100HM is compatible with MediaTek Pump Express™ Plus fast-charging which can permit receiving output voltage change signal by CSP and CSN pin signal. There are two kinds of output current control patterns, one is for output voltage growth, and another is for output voltage reduction, shown in Figure 42 and Figure 43 FAN6100HM monitors the output current control patterns by the CSP and CSN pins.

FAN6100HM not only support MediaTek Pump Express™ Plus fast-charging for 5 V to 12 V quick charger application but also support for 4 V to 5 V low output voltage charger solution.

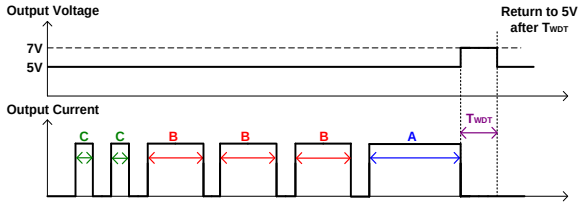


Figure 42. Output Current Control Pattern for Output Voltage Growth

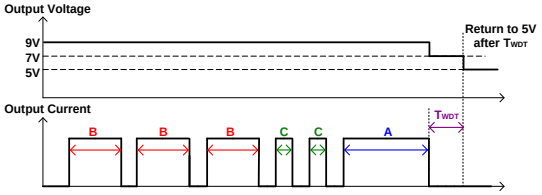


Figure 43. Output Current Control Pattern for Output Voltage Reduction

(2) Fairchild's FCP-Single Communication Protocol

FAN6100HM can be compatible with Fairchild's own FCP-Single communication protocol includes high-speed mode and low-speed mode to apply high-end processor and low-end processor application. For FCP-Single communication protocol detection, it uses the DN signal to determine output voltage of the HVDCP power supply. There are four types of the control signal for the output voltage adjustment, 1. Output voltage increase (SV+_HS) for high-speed mode detection 2. Output voltage returns to 5 V (S5V_HS) for high-speed mode detection 3. Output voltage increase (SV+_LS) for low-speed mode detection 4. Output voltage returns to 5 V (S5V_LS) for low-speed mode detection. Figure 44 shows FCP-Single communication protocol control signal waveform.

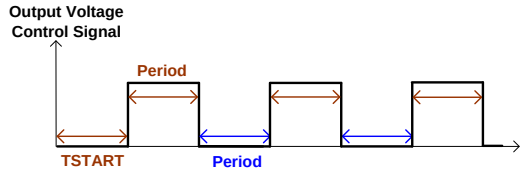


Figure 44.FCP-Single Communication Protocol Control Signal Waveform

Applications Information

Constant Current Mode Selection

For mode 1 setting, QP and QN should be connected to ground as low level signal.

For mode 2 setting, QP should be connected to ground as low level signal and QN can be open to generate high level signal.

For Mode 3 setting, QN should be connected to ground as low level signal and QP can be open to generate high level signal.

For Mode 4 setting, QP and QN should be open to generate high level signal.

Setting Output Voltage Sensing Resistor for VREF Pin

The output voltage can be derived by setting R_{F1} and R_{F2}, as calculated by:

$$V_O = V_{CVR} \cdot \frac{R_{F1} + R_{F2}}{R_{F2}} \quad (2)$$

Considering the low stand-by power request and the noise immunity for VREF, it is typical to select currents, which is flowing current through resistor divider, range from 100 µA up to 250 µA can be used.

Setting Secondary Side Output Constant Current Sensing Resistor

The constant current point (I_{O_CC}) can be set by selecting the current sensing resistor as:

$$I_{O\_CC} = \frac{V_{CSP-CSN}}{R_{CS}} \quad (3)$$

Setting Capacitance for V_{DD} and Charge-Pump Circuit

FAN6100HM can withstand up to 20 V on the VIN pin and enable this pin to be connected directly to the output terminal of a power supply. It is typical to use a 100 Ω resistor between the VIN pin and the output terminal of a power supply and then connect 470 nF capacitor on VIN pin if ESD immunity need to be enhanced.

The charge-pump circuit needs an external capacitor, C_{CP}, typically 220 nF~1 µF, as the energy storage element. To stabilize the operation of the clamping LDO stage, it is typical to use 1 µF capacitor to keep the LDO loop stable. The C_{VDD} typically 220 nF~1 µF, as the energy storage element.

Select Cable Drop Compensation Resistor

The external compensation resistor, R_{COMR}, can be calculated by:

$$R_{COMR} = \frac{R_{F2}}{R_{F1} + R_{F2}} \cdot \frac{R_{Cable}}{R_{CS}} \cdot \frac{1}{A_{V-CCR}} \cdot \frac{1}{K_{COMR-CDC}} \quad (4)$$

R_{F1} and R_{F2} = output feedback resistor divider derived from Eq. (2);

R_{Cable} = cable resistance;

R_{CS} = current sensing resistor derived from Eq. (3);

$K_{COMR-CDC}$ = cable compensation design parameter of the controller, which is 1.0 µA/V; and

A_{V-CCR} = derived from Eq. (3), 10 V/V.

Setting Bleeder Resistor

The BLD pin can withstand up to 20 V, and enables this pin to be connected directly to the output terminal of a HVDCP power supply. The output voltage should not be lower than 4.1 V at output voltage transition. For short transition time, adding a 2-step bleeder circuit, (5.1 V Zener diode, and one resistance (R_{BLD})) is recommended to avoid output voltage drop deeply.

The first step bleeder current is determined by internal constant current design, the type value is 240 mA. The second step bleeder discharging current (I_{BLD}) can be adjusted by external bleeder series resistor (R_{BLD}), calculated as:

$$I_{BLD} = \frac{V_O}{R_{BLD}} \quad (5)$$

where RBLD is bleeder resistor connected between the output side and the BLD pin.

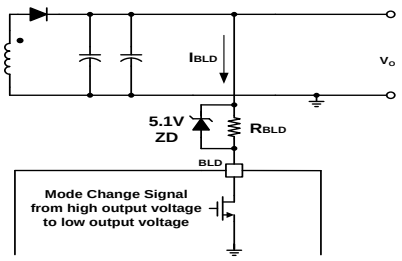


Figure 45. Output Bleeder Function

Typical Application Circuit

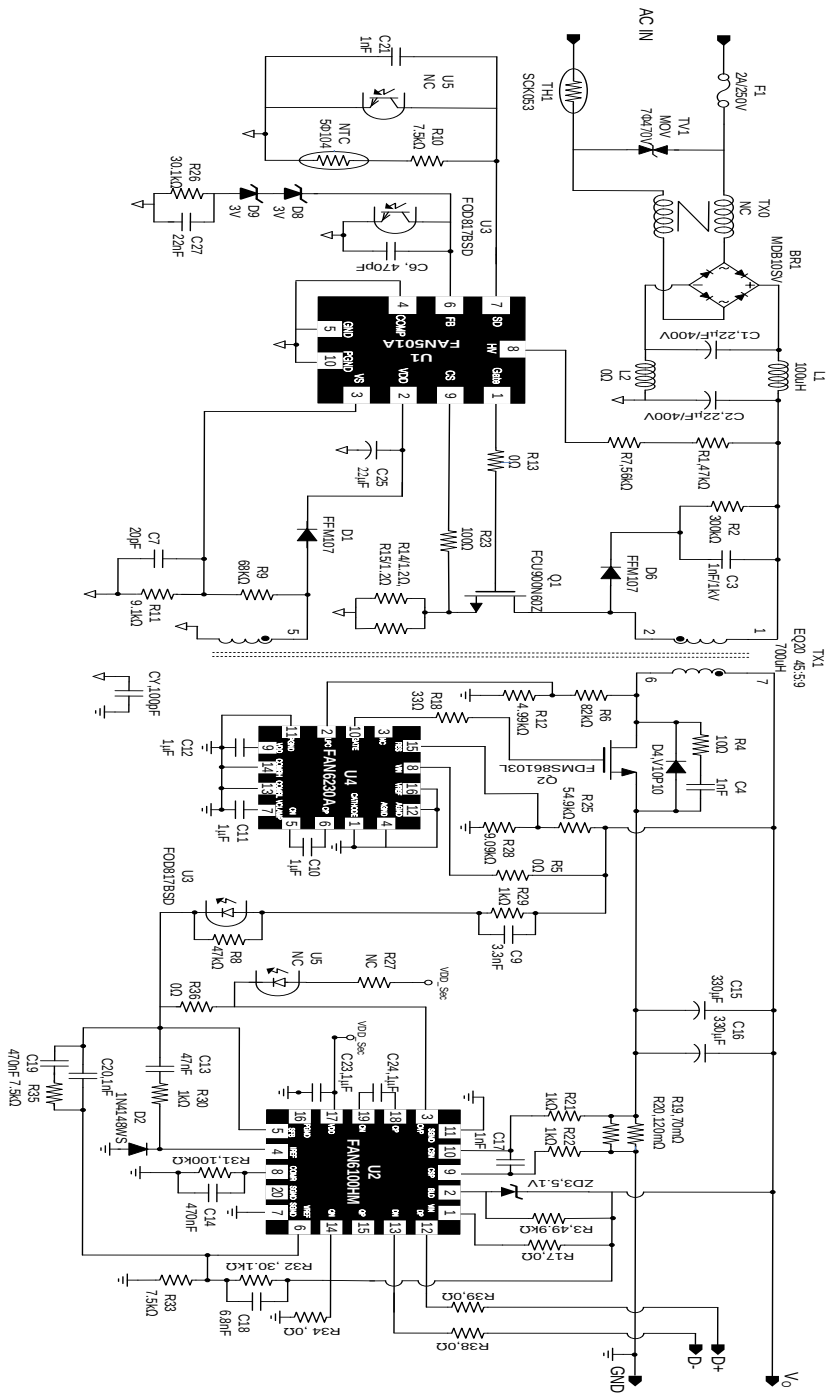


Figure 46. Schematic of Typical Application 24 W Circuit

Transformer Specification

Core: EQ20
Bobbin: EQ20

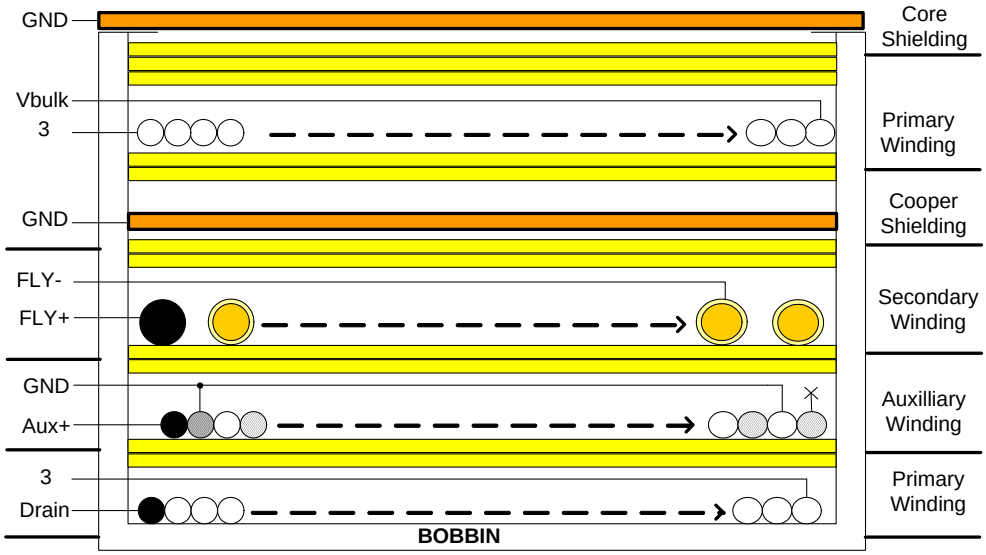


Figure 47.Transformer Diagram

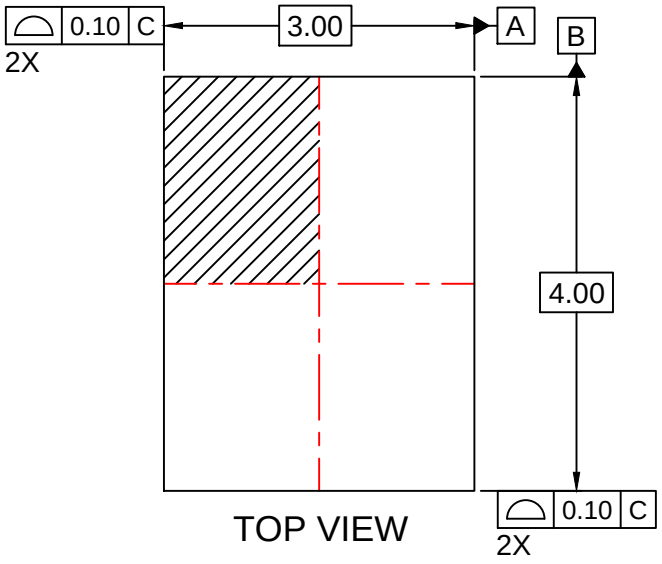
Table 6. Transformer Winding and Specification

Winding	Terminal		Wire	Turns	Isolation Layer
	Start Pin	End Pin			Turns
N1-1	4	3	0.32 mm×1	30	2
N2	2	1	0.18 mm×2	9	2
	1	x	0.18 mm×2	9	
N3	Fly+	FLY-	0.75 mm×1	5	2
N3	1	x	Copper-Foil	1	2
N1-2	3	5	0.32 mm×1	15	2
CORE - EQ20					
Bobbin – EQ20					

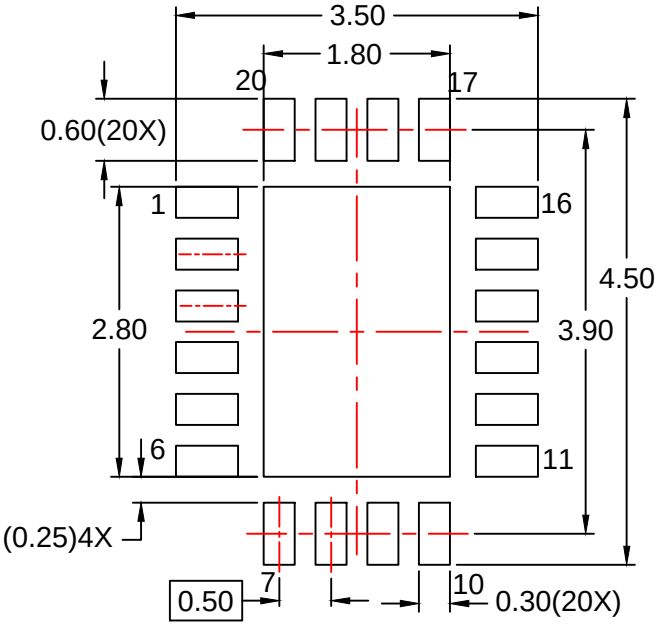
Inductance	1-2	700 µH± 7%	100 kHz
Effective Leakage	1-2	<20 µH Maximum	Short Other Pin

Table 7. System Performance

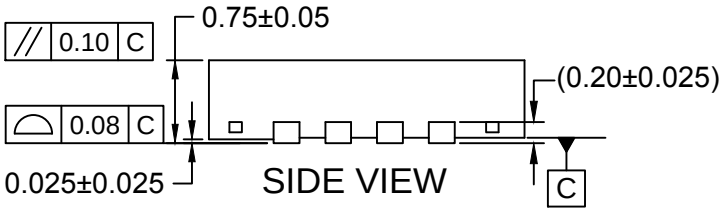
Vo	V_{IN}	Standby Power	Output Loading					Average Efficiency
			0.2 A	0.5 A	1 A	1.5 A	2 A	
5 V	115 V_{AC}	15.5 mW	82.55%	85.20%	85.41%	86.51%	87.43%	86.14%
	230 V_{AC}	16.1 mW	79.45%	82.81%	84.39%	87.60%	87.51%	85.58%
9 V	115 V_{AC}	33.3 mW	86/88%	87.78%	88.41%	88.59%	89.14%	88.48%
	230 V_{AC}	34.4 mW	83.18%	85.94%	88.83%	90.23%	89.64%	88.66%
12 V	115 V_{AC}	52.0 mW	83.59%	84.55%	88.00%	88.93%	89.45%	87.73%
	230 V_{AC}	55.0 mW	83.62%	86.34%	88.83%	89.45%	90.71%	88.83%



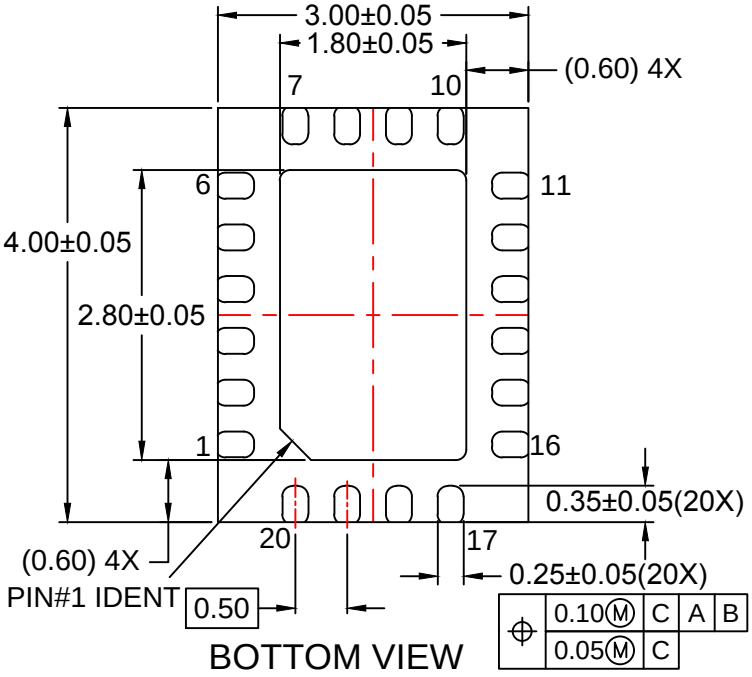
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

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C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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Rev. I74