



FDMS8020

N-Channel PowerTrench[®] MOSFET 30 V, 131 A, 2.5 mΩ

Features

- Max $r_{DS(on)}$ = 2.5 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 26\text{ A}$
- Max $r_{DS(on)}$ = 3.6 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 21.5\text{ A}$
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

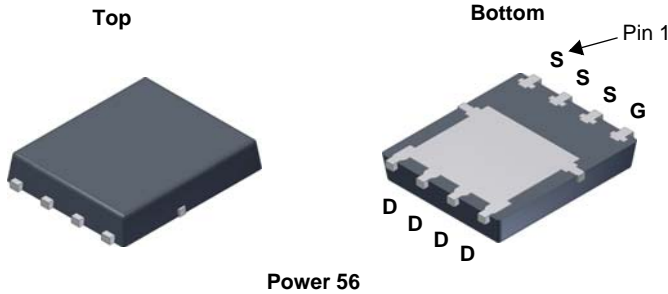


General Description

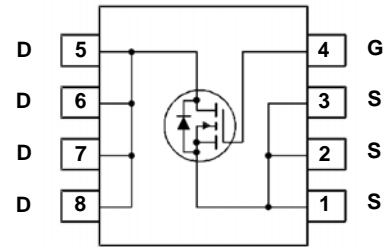
This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- VRM Vcore Switching For Desktop And Server
- OringFET / Load Switching
- DC-DC Conversion
- Motor Bridge Switch



Power 56



MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	± 20	V
I_D	Drain Current -Continuous $T_C = 25\text{ °C}$ (Note 6)	131	A
	-Continuous $T_C = 100\text{ °C}$ (Note 6)	83	
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	26	
	-Pulsed (Note 5)	507	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	93	mJ
P_D	Power Dissipation $T_C = 25\text{ °C}$	65	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.9	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8020	FDMS8020	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		14		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1.0	1.5	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 26\text{ A}$		2.0	2.5	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 21.5\text{ A}$		2.6	3.6	
		$V_{GS} = 10\text{ V}$, $I_D = 26\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		2.9	3.7	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 26\text{ A}$		154		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		2855	3800	pF
C_{oss}	Output Capacitance			1050	1400	pF
C_{rss}	Reverse Transfer Capacitance			115	175	pF
R_g	Gate Resistance			0.9		Ω

Switching Characteristics

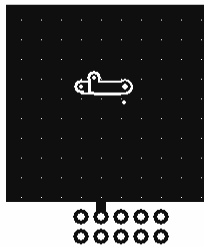
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 26\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		12	22	ns	
t_r	Rise Time			5.7	12	ns	
$t_{d(off)}$	Turn-Off Delay Time			32	52	ns	
t_f	Fall Time			4	10	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		43	61	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	$V_{DD} = 15\text{ V}$, $I_D = 26\text{ A}$		21	29	nC
Q_{gs}	Gate to Source Charge				7.3		nC
Q_{gd}	Gate to Drain "Miller" Charge				6.0		nC

Drain-Source Diode Characteristics

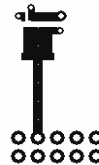
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.1\text{ A}$ (Note 2)		0.68	1.1	V
		$V_{GS} = 0\text{ V}$, $I_S = 26\text{ A}$ (Note 2)		0.78	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 26\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		37	58	ns
Q_{rr}	Reverse Recovery Charge			18	33	nC
t_{rr}	Reverse Recovery Time	$I_F = 26\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$		30	48	ns
Q_{rr}	Reverse Recovery Charge			36	57	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) $50\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $125\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3. Starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 0.3\text{ mH}$, $I_{AS} = 25\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$.

4. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

5. Pulsed I_D please refer to SOA curve for more details.

6. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

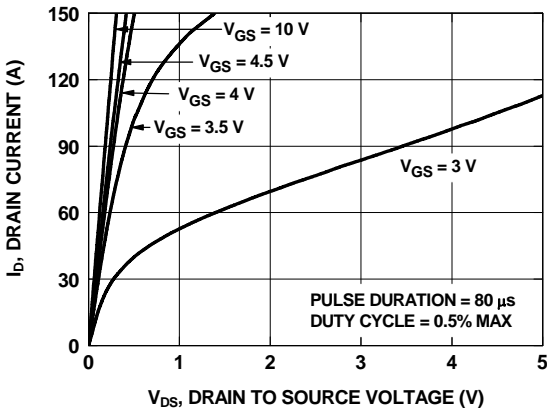


Figure 1. On-Region Characteristics

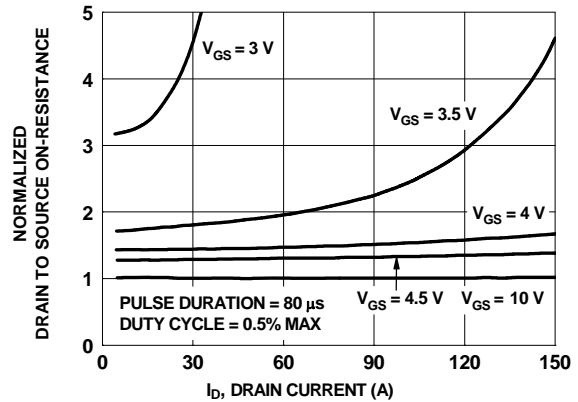


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

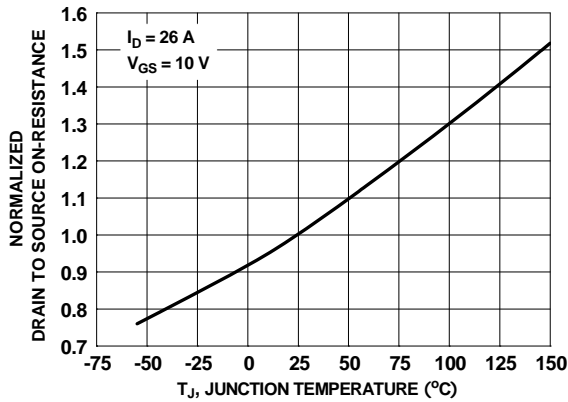


Figure 3. Normalized On-Resistance vs. Junction Temperature

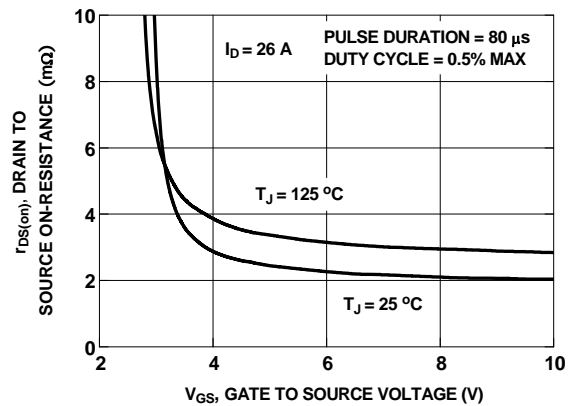


Figure 4. On-Resistance vs. Gate to Source Voltage

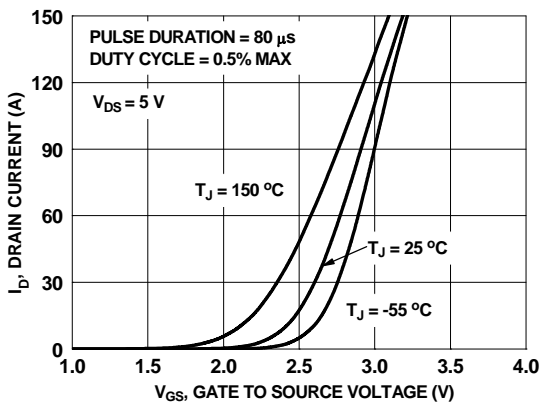


Figure 5. Transfer Characteristics

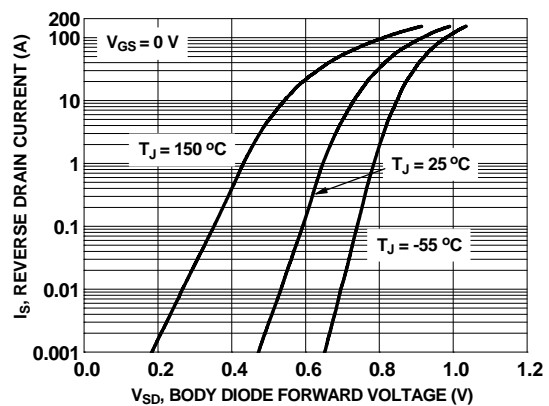


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

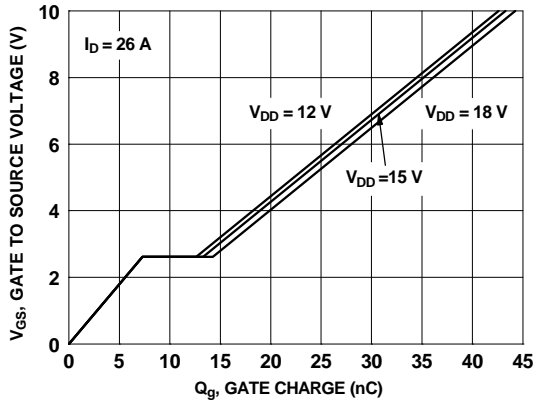


Figure 7. Gate Charge Characteristics

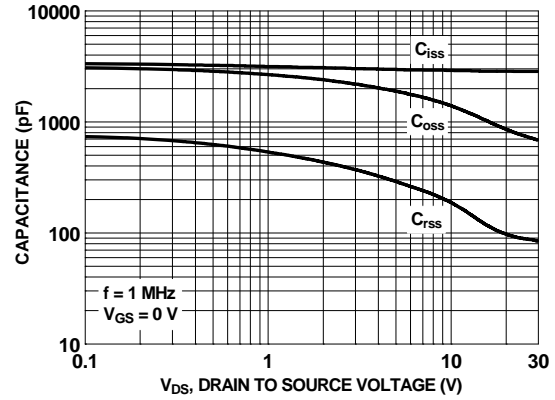


Figure 8. Capacitance vs. Drain to Source Voltage

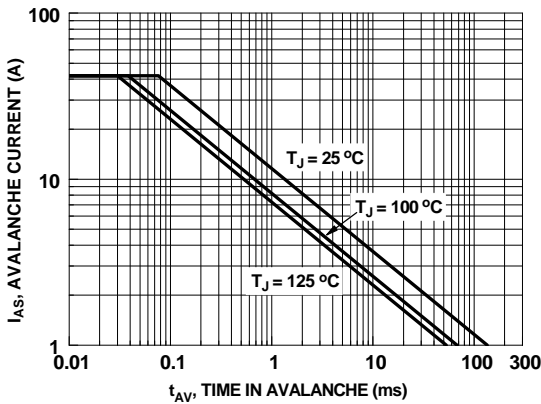


Figure 9. Unclamped Inductive Switching Capability

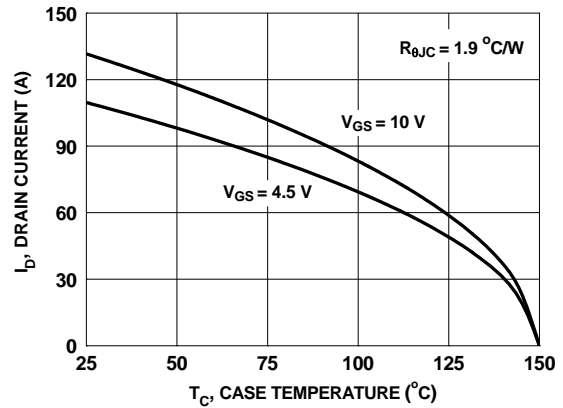


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

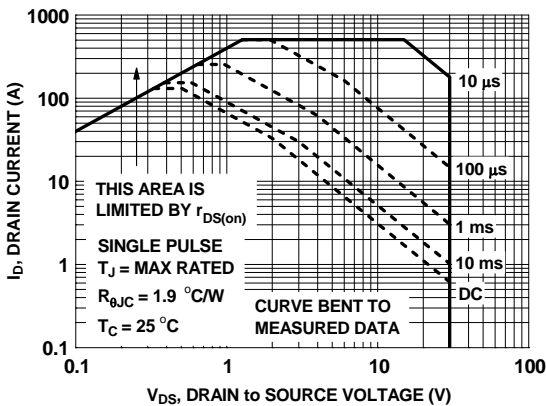


Figure 11. Forward Bias Safe Operating Area

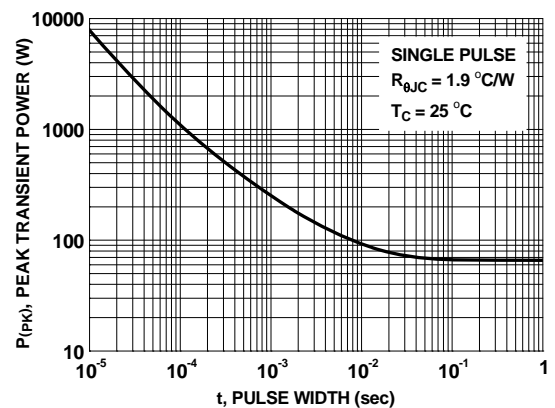


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

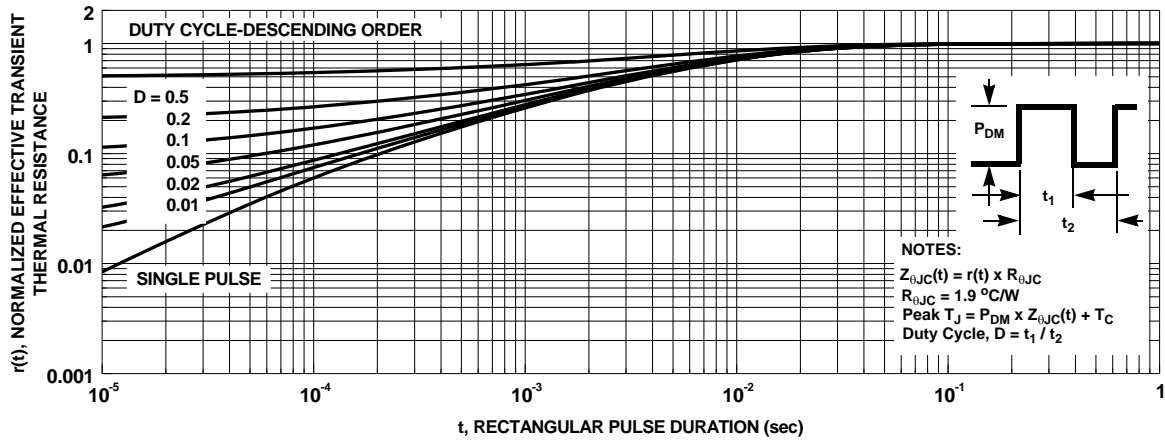
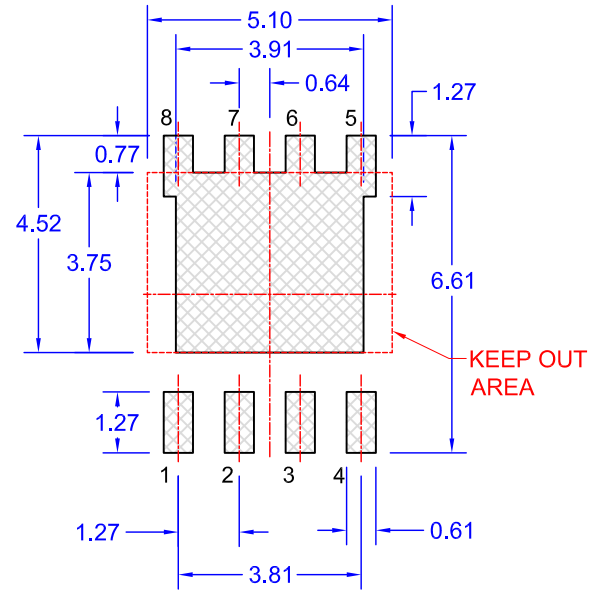


Figure 13. Junction-to-Case Transient Thermal Response Curve



TOP VIEW



LAND PATTERN RECOMMENDATION



SIDE VIEW

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F. DRAWING FILE NAME: PQFN08AREV10





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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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