



# FDMC8884

## N-Channel PowerTrench<sup>®</sup> MOSFET

30 V, 15 A, 19 mΩ

### Features

- Max  $r_{DS(on)}$  = 19 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 9.0\text{ A}$
- Max  $r_{DS(on)}$  = 30 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 7.2\text{ A}$
- High performance technology for extremely low  $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

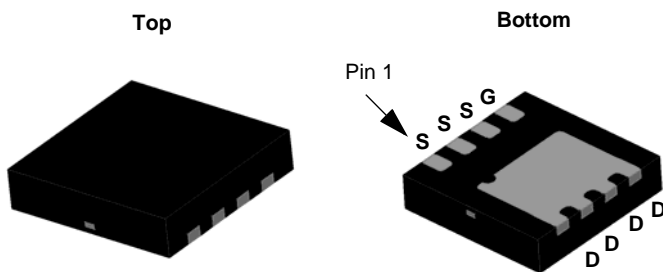


### General Description

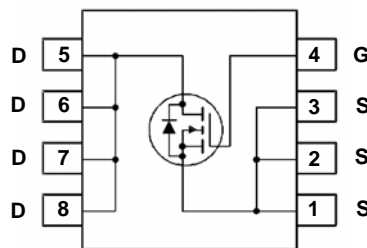
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### Application

- High side in DC - DC Buck Converters
- Notebook battery power management
- Load switch in Notebook



MLP 3.3x3.3



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous	$T_C = 25\text{ °C}$	15
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	9.0
	-Pulsed		40
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	24
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	18
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	2.3
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.6	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8884	FDMC8884	MLP 3.3x3.3	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		22		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 125\text{ }^\circ\text{C}$			1 250	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.4	1.9	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 9.0\text{ A}$		16	19	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 7.2\text{ A}$		22	30	
		$V_{GS} = 10\text{ V}, I_D = 9.0\text{ A}, T_J = 125\text{ }^\circ\text{C}$		22	30	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}, I_D = 9.0\text{ A}$		24		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		513	685	pF
$C_{oss}$	Output Capacitance			110	150	pF
$C_{rss}$	Reverse Transfer Capacitance			76	115	pF
$R_g$	Gate Resistance			1.4	2.1	$\Omega$

**Switching Characteristics**

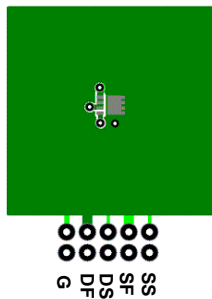
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 9.0\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		6	12	ns
$t_r$	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			15	27	ns
$t_f$	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 10\text{ V}$	$V_{DD} = 15\text{ V},$ $I_D = 9.0\text{ A}$	10	14	nC
	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$		5.0	7.0	nC
$Q_{gs}$	Total Gate Charge			1.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2.2		nC

**Drain-Source Diode Characteristics**

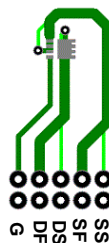
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 9.0\text{ A}$ (Note 2)		0.86	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 1.6\text{ A}$ (Note 2)		0.76	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 9.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		13	18	ns
$Q_{rr}$	Reverse Recovery Charge			3	10	nC

NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 53  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper

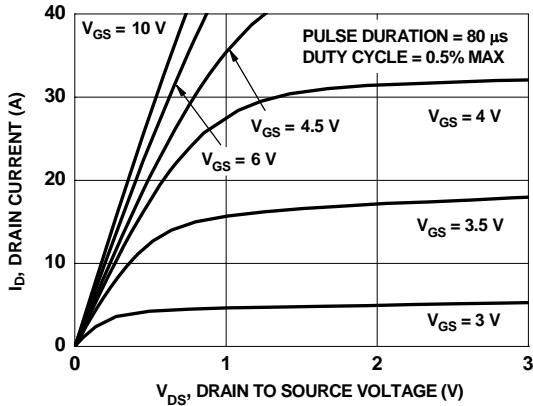


b. 125  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

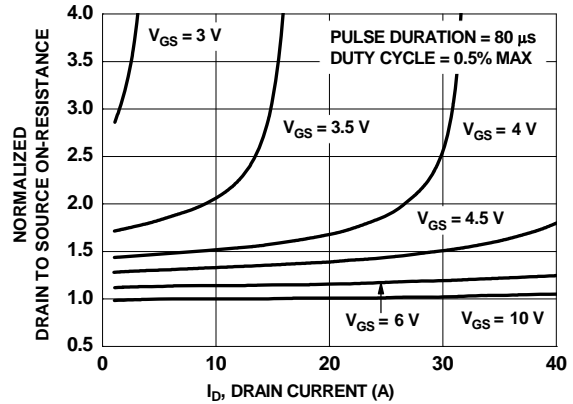
2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

3.  $E_{AS}$  of 24 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 7\text{ A}$ ,  $V_{DD} = 30\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 3\text{ mH}$ ,  $I_{AS} = 4\text{ A}$ .

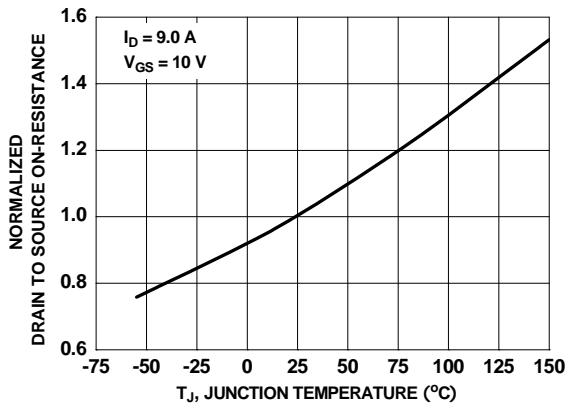
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



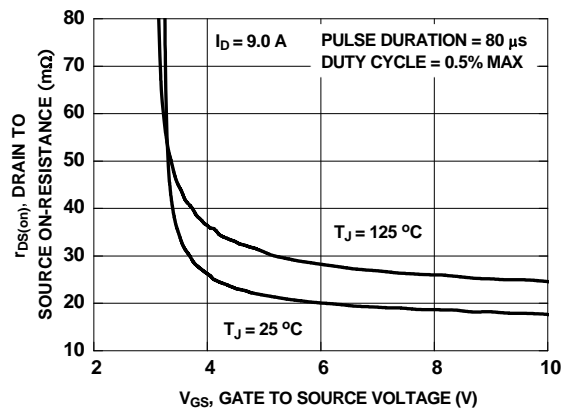
**Figure 1. On-Region Characteristics**



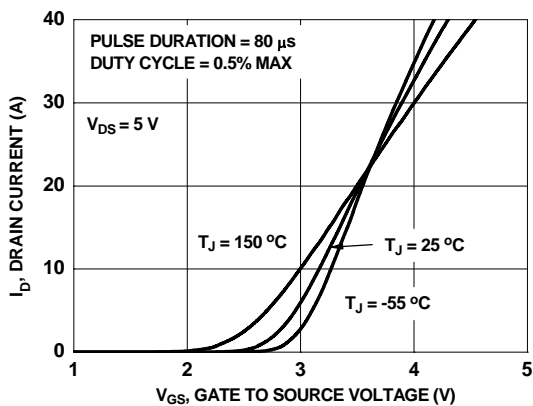
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



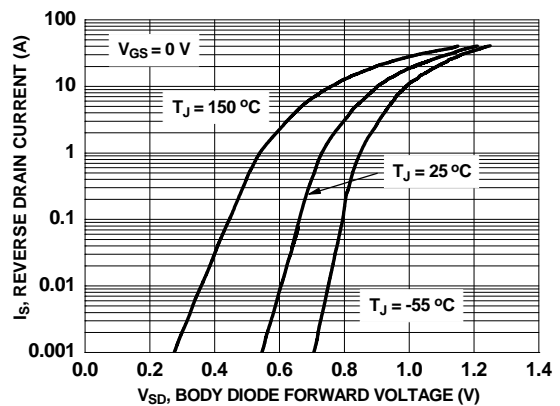
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

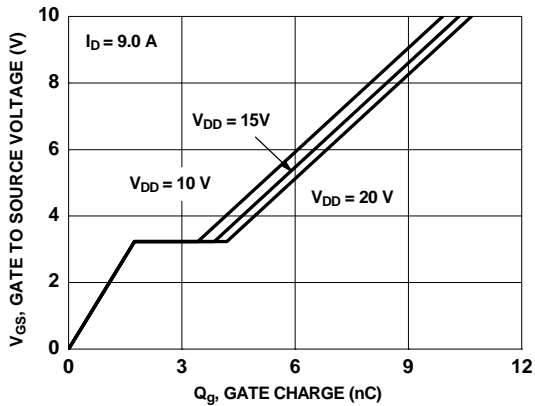


**Figure 5. Transfer Characteristics**

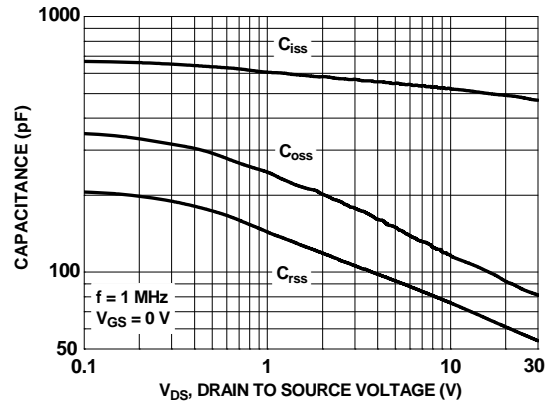


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

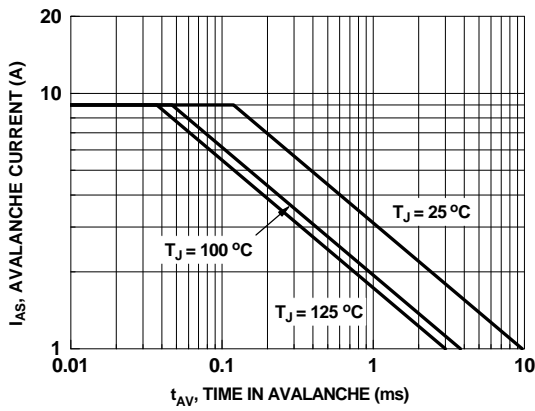
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



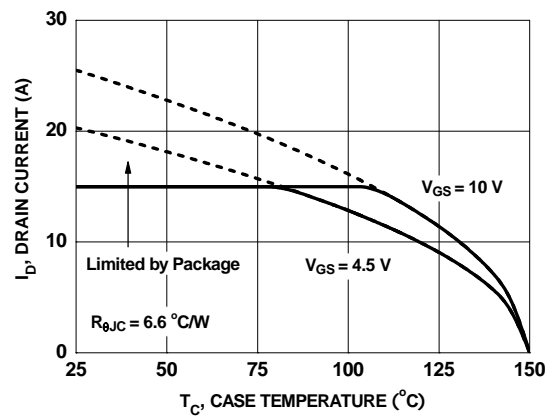
**Figure 7. Gate Charge Characteristics**



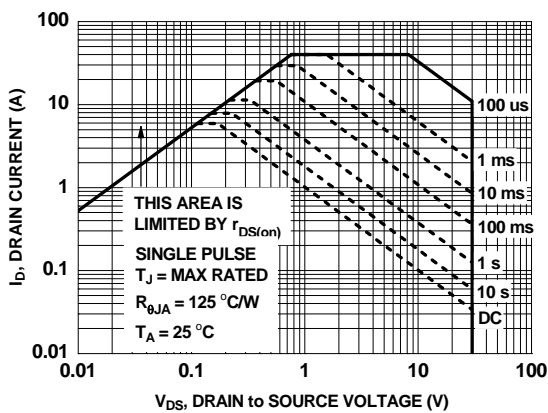
**Figure 8. Capacitance vs Drain to Source Voltage**



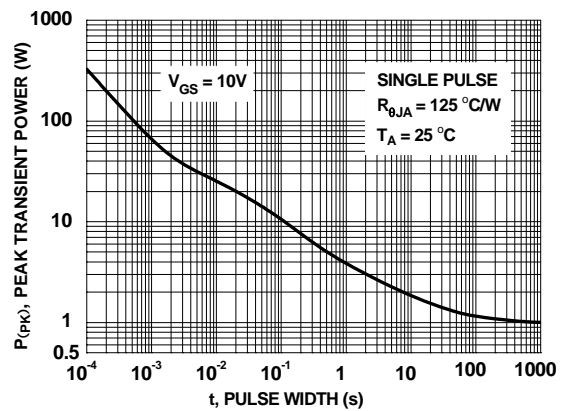
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

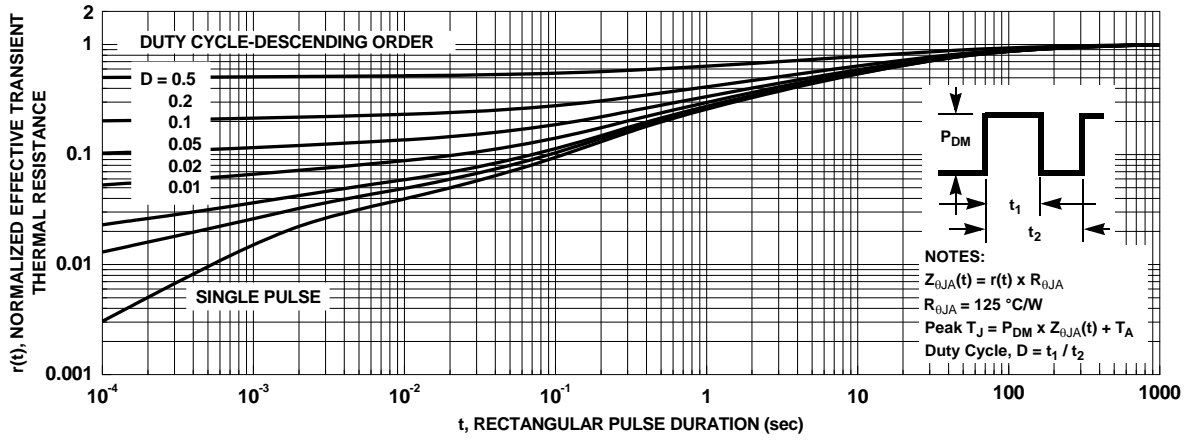


**Figure 11. Forward Bias Safe Operating Area**

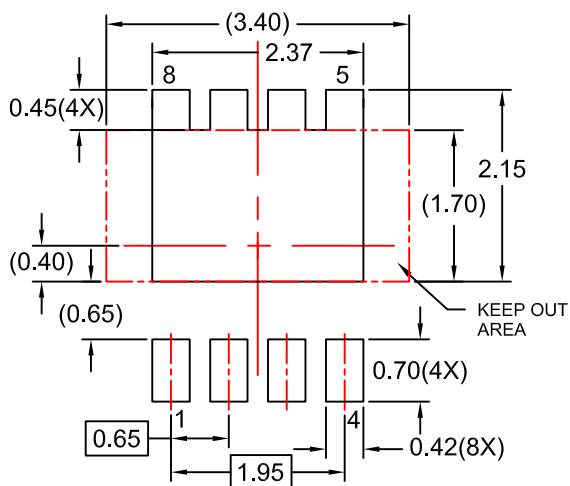
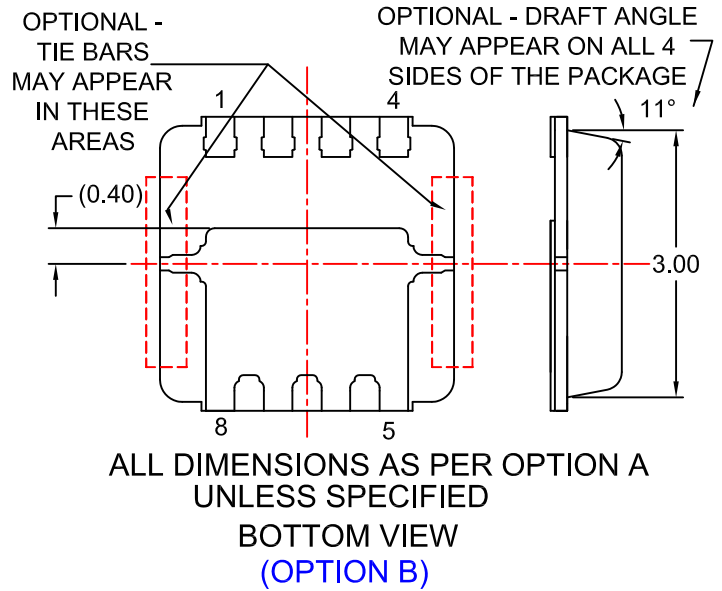
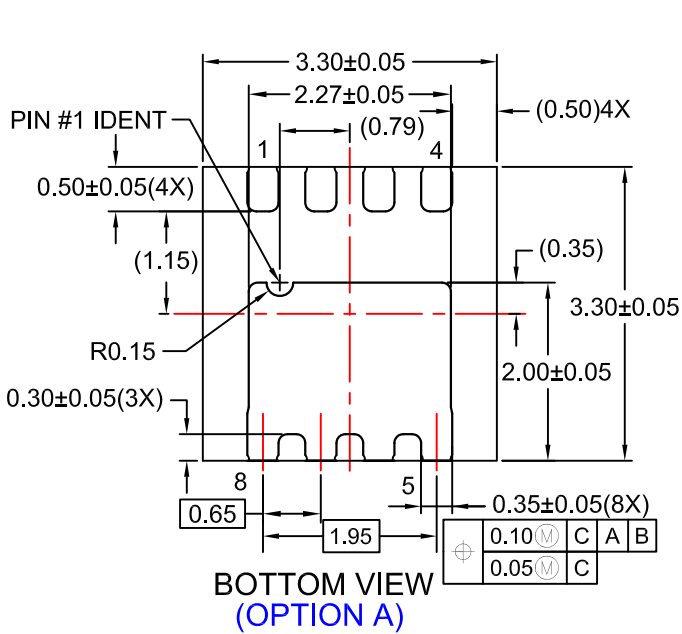
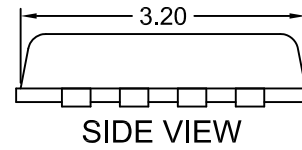
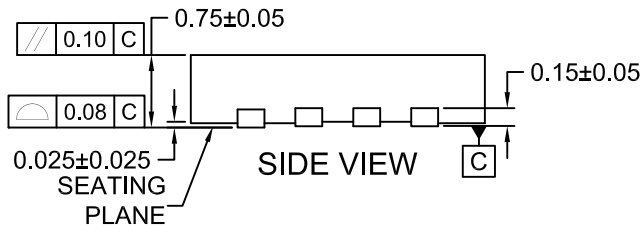
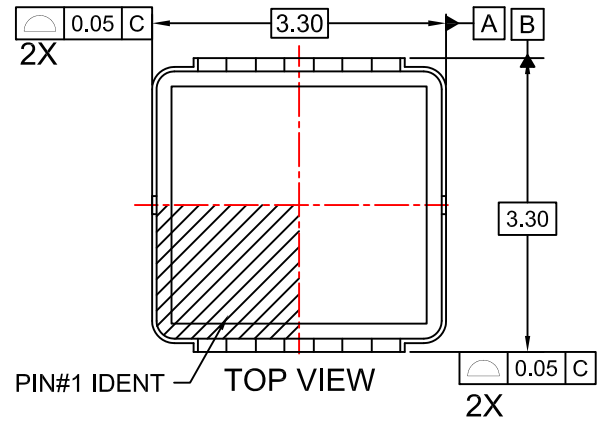
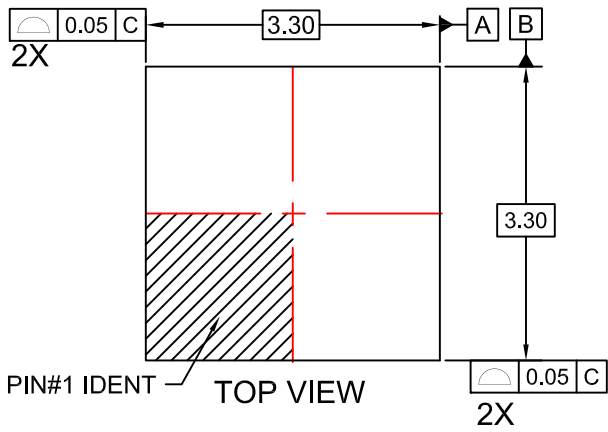


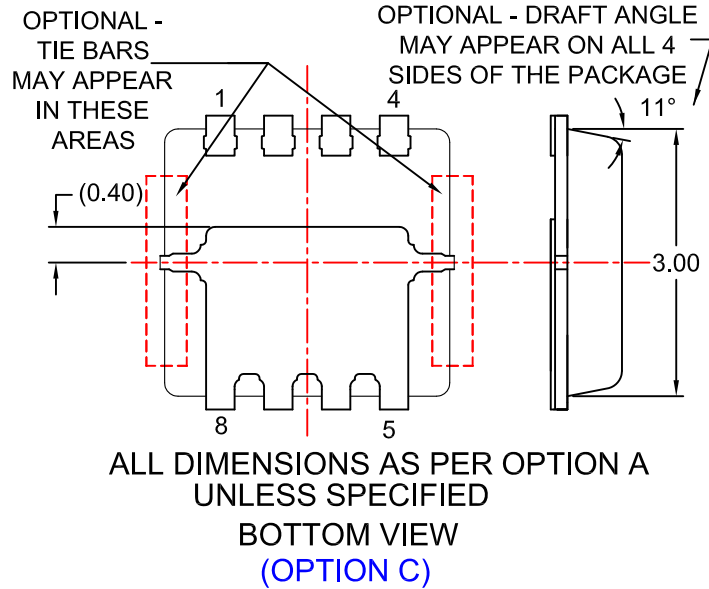
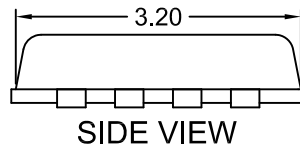
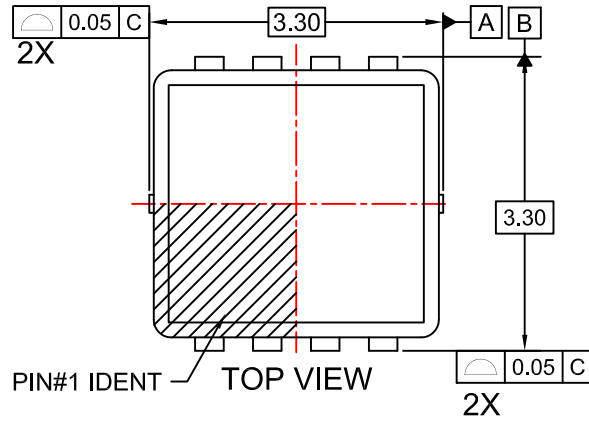
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**

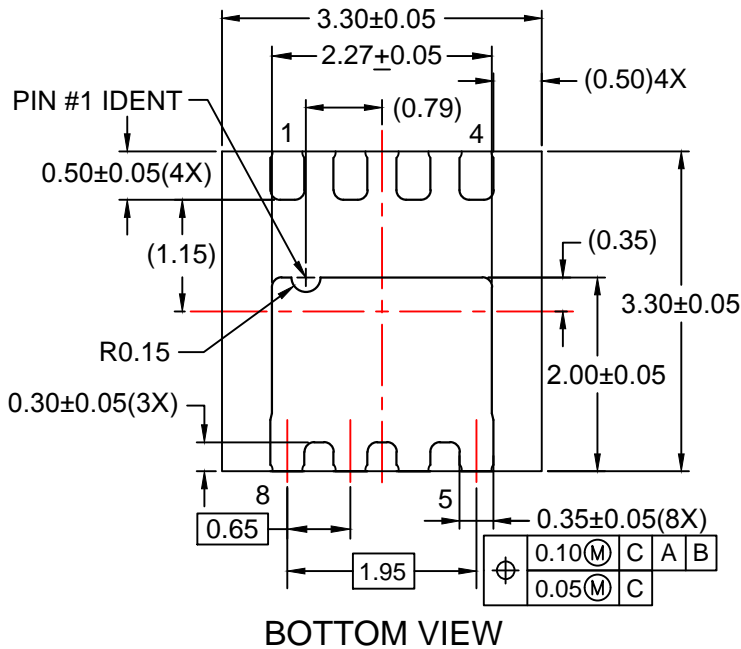
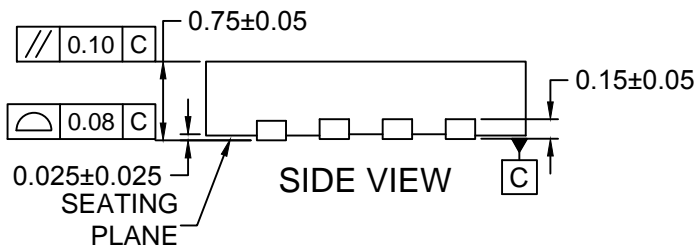
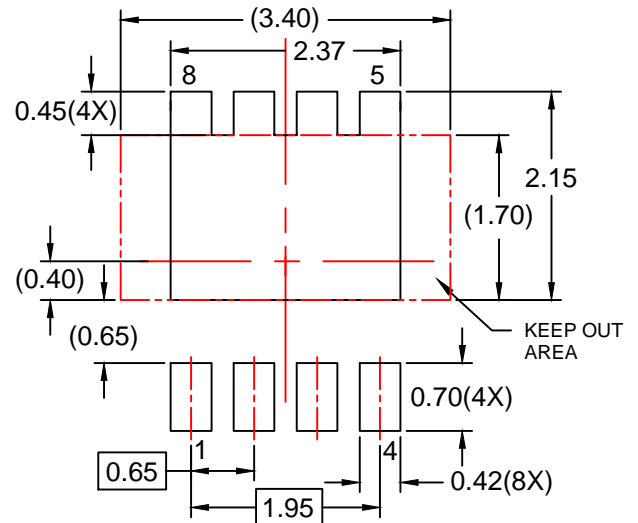
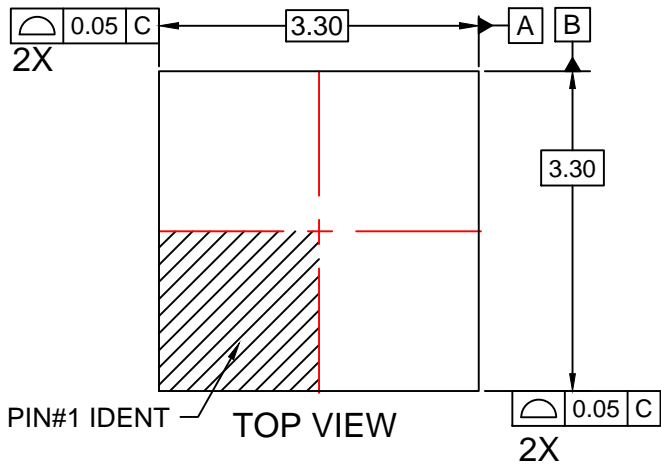




**NOTES:**

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.
- F. DRAWING FILENAME: MKT-MLP08Wrev3.
- G. OPTION A - SAWN MLP, OPTIONS B & C - PUNCH MLP.





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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