

# MOSFET – N-Channel, POWERTRENCH®

**30 V, 16 A, 14.3 mohm**

## FDMC8882

### Description

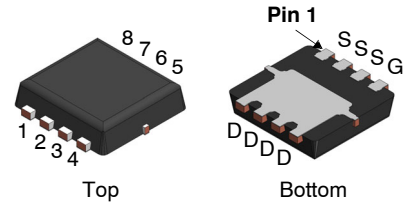
This N-Channel MOSFET is produced using **onsemi**'s advanced POWETRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### Features

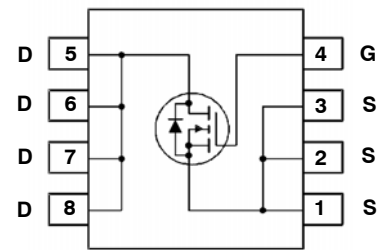
- Max  $R_{DS(on)}$  = 14.3 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 10.5\text{ A}$
- Max  $R_{DS(on)}$  = 22.5 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 8.3\text{ A}$
- High Performance Technology for Extremely Low  $R_{DS(on)}$
- Termination is Lead-Free
- RoHS Compliant

### Applications

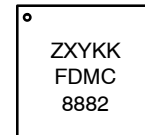
- High Side in DC-DC Buck Converters
- Notebook Battery Power Management
- Load Switch in Notebook



WDFN8 3.3x3.3, 0.65P  
 CASE 511DR



### MARKING DIAGRAM



- Z = Assembly Plant Code
- XY = Date Code (Year & Week)
- KK = Lot Traceability Code
- FDMC8882 = Specific Device Code

### ORDERING INFORMATION

| Device   | Package            | Shipping†             |
|----------|--------------------|-----------------------|
| FDMC8882 | WDFN8<br>(Pb-Free) | 3000 /<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDMC8882

## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol         | Parameter  |                              | Ratings                               | Unit             |   |
|----------------|--|------------------------------|---------------------------------------|------------------|---|
| $V_{DS}$       | Drain to Source Voltage                          |                              | 30                                    | V                |   |
| $V_{GS}$       | Gate to Source Voltage                           |                              | $\pm 20$                              | V                |   |
| $I_D$          | Drain Current                                    | Continuous (Package Limited) | $T_C = 25^\circ\text{C}$              | 16               | A |
|                |  | Continuous (Silicon Limited) | $T_C = 25^\circ\text{C}$              | 34               |   |
|                |  | Continuous                   | $T_A = 25^\circ\text{C}$<br>(Note 1a) | 10.5             | A |
|                |  | Pulsed                       | -                                     | 40               |   |
| $P_D$          | Power Dissipation                                |                              | $T_C = 25^\circ\text{C}$              | 18               | W |
|                | Power Dissipation                                |                              | $T_A = 25^\circ\text{C}$<br>(Note 1a) | 2.3              |   |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range |                              | -55 to +150                           | $^\circ\text{C}$ |   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

| Symbol          | Parameter   | Ratings | Unit                      |
|-----------------|---|---------|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case              | 6.6     | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 53      |                           |

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------------|-----|-----|-----|------|
|--------|-----------|-----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|                                      |   |  |    |    |           |                            |
|--------------------------------------|---|--|----|----|-----------|----------------------------|
| $BV_{DSS}$                           | Drain-to-Source Breakdown Voltage         | $I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$                          | 30 | -  | -         | V                          |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$             | -  | 25 | -         | $\text{mV}/^\circ\text{C}$ |
| $I_{DSS}$                            | Zero Gate Voltage Drain Current           | $V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$                          | -  | -  | 1         | $\mu\text{A}$              |
|                                      |   | $V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^\circ\text{C}$ | -  | -  | 250       |                            |
| $I_{GSS}$                            | Gate-to-Source Leakage Current            | $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$                      | -  | -  | $\pm 100$ | nA                         |

### ON CHARACTERISTICS

|  |  |  |     |      |      |                            |
|--|--|--|-----|------|------|----------------------------|
| $V_{GS(th)}$                           | Gate-to-Source Threshold Voltage                         | $V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$                               | 1.2 | 1.9  | 2.5  | V                          |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate-to-Source Threshold Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$             | -   | -5   | -    | $\text{mV}/^\circ\text{C}$ |
| $R_{DS(on)}$                           | Static Drain-to-Source On Resistance                     | $V_{GS} = 10 \text{ V}, I_D = 10.5 \text{ A}$                          | -   | 12.4 | 14.3 | $\text{m}\Omega$           |
|  |  | $V_{GS} = 4.5 \text{ V}, I_D = 8.3 \text{ A}$                          | -   | 16.0 | 22.5 |                            |
|  |  | $V_{GS} = 10 \text{ V}, I_D = 10.5 \text{ A}, T_J = 125^\circ\text{C}$ | -   | 17.4 | -    |                            |
| $g_{FS}$                               | Forward Transconductance                                 | $V_{DS} = 5 \text{ V}, I_D = 10.5 \text{ A}$                           | -   | 33   | -    | S                          |

### DYNAMIC CHARACTERISTICS

|           |                              |  |   |     |     |             |
|-----------|------------------------------|--|---|-----|-----|-------------|
| $C_{iss}$ | Input Capacitance            | $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ | - | 710 | 945 | $\text{pF}$ |
| $C_{oss}$ | Output Capacitance           |  | - | 140 | 185 | $\text{pF}$ |
| $C_{rss}$ | Reverse Transfer Capacitance |  | - | 90  | 135 | $\text{pF}$ |
| $R_g$     | Gate Resistance              |  | - | 1.0 | -   | $\Omega$    |

# FDMC8882

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Symbol                           | Parameter                     | Test Conditions  | Min | Typ | Max | Unit |
|----------------------------------|-------------------------------|--|-----|-----|-----|------|
| <b>SWITCHING CHARACTERISTICS</b> |                               |  |     |     |     |      |
| $t_{d(on)}$                      | Turn-On Delay Time            | $V_{DD} = 15\text{ V}$ , $I_D = 10.5\text{ A}$ , $V_{GS} = 10\text{ V}$ ,<br>$R_{GEN} = 6\ \Omega$ | –   | 7   | 14  | ns   |
| $t_r$                            | Rise Time                     |  | –   | 3   | 10  |      |
| $t_{d(off)}$                     | Turn-Off Delay Time           |  | –   | 17  | 30  |      |
| $t_f$                            | Fall Time                     |  | –   | 2   | 10  |      |
| $Q_{g(tot)}$                     | Total Gate Charge             | $V_{GS} = 0\text{ V to }10\text{ V}$ , $V_{DD} = 15\text{ V}$ , $I_D = 10.5\text{ A}$              | –   | 14  | 20  | nC   |
|                                  | Total Gate Charge             | $V_{GS} = 0\text{ V to }4.5\text{ V}$ , $V_{DD} = 15\text{ V}$ , $I_D = 10.5\text{ A}$             | –   | 7   | 10  |      |
| $Q_{gs}$                         | Gate-to-Source Charge         | $V_{DD} = 15\text{ V}$ , $I_D = 10.5\text{ A}$   | –   | 2.3 | –   |      |
| $Q_{gd}$                         | Gate-to-Drain “Miller” Charge | $V_{DD} = 15\text{ V}$ , $I_D = 10.5\text{ A}$   | –   | 2.8 | –   |      |

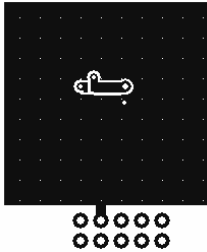
## DRAIN-SOURCE DIODE CHARACTERISTICS

|          |                                       |  |   |      |     |    |
|----------|---------------------------------------|--|---|------|-----|----|
| $V_{SD}$ | Source-to-Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}$ , $I_S = 10.5\text{ A}$ (Note 2)     | – | 0.88 | 1.2 | V  |
|          |                                       | $V_{GS} = 0\text{ V}$ , $I_S = 1.9\text{ A}$ (Note 2)      | – | 0.76 | 1.2 |    |
| $t_{rr}$ | Reverse Recovery Time                 | $I_F = 10.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ | – | 16   | 28  | ns |
| $Q_{rr}$ | Reverse Recovery Charge               |  | – | 4.4  | 10  | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- 53°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



- 125°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

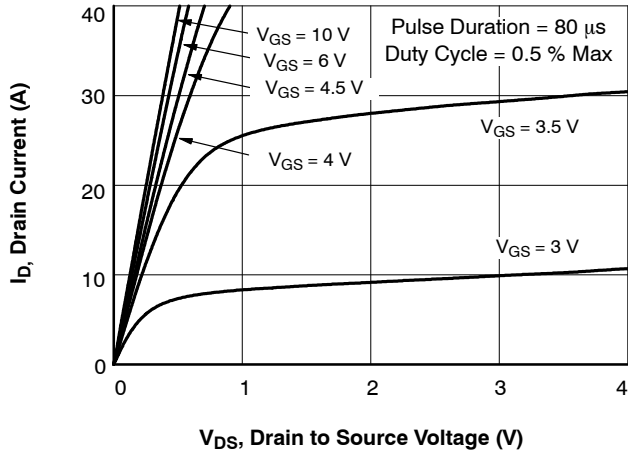


Figure 1. On-Region Characteristics

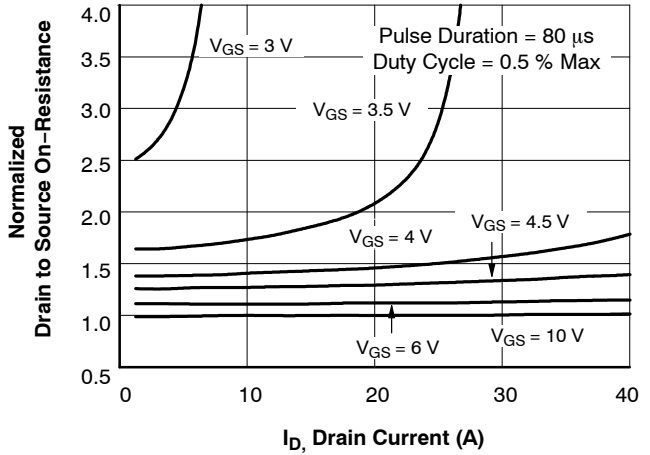


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

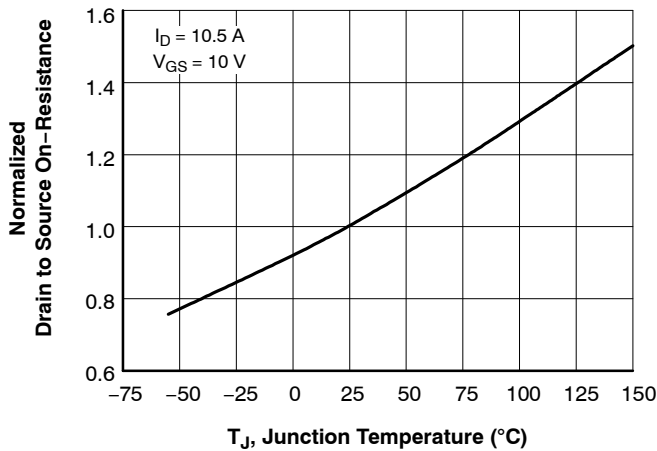


Figure 3. Normalized On-Resistance vs. Junction Temperature

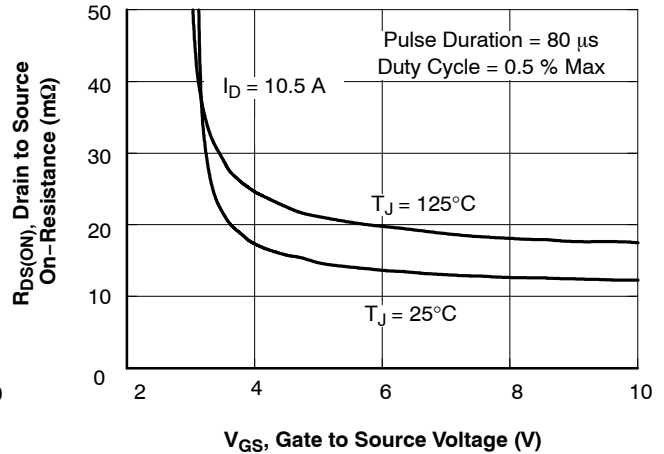


Figure 4. On-Resistance vs. Gate to Source Voltage

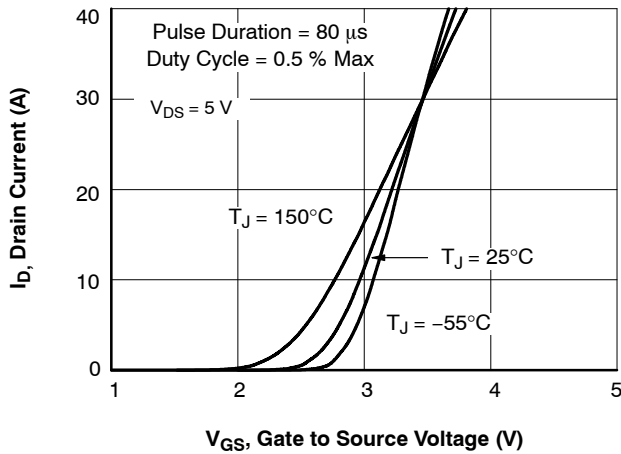


Figure 5. Transfer Characteristics

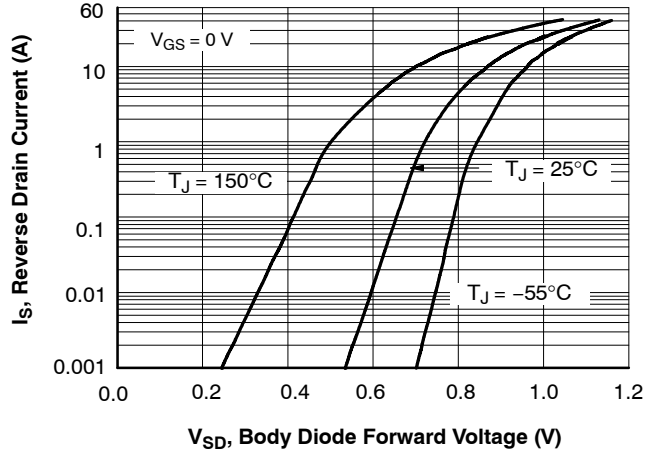


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

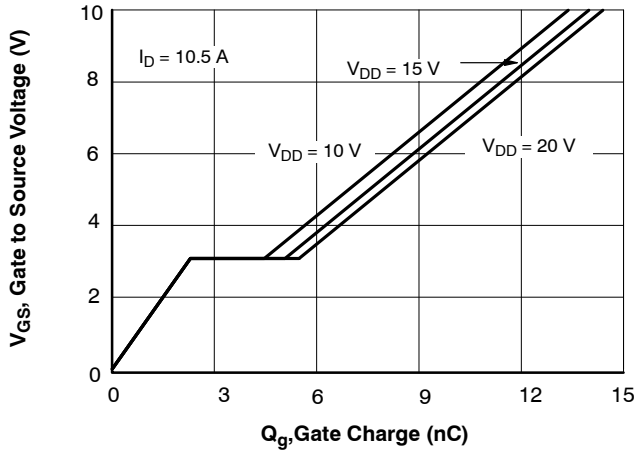


Figure 7. Gate Charge Characteristics

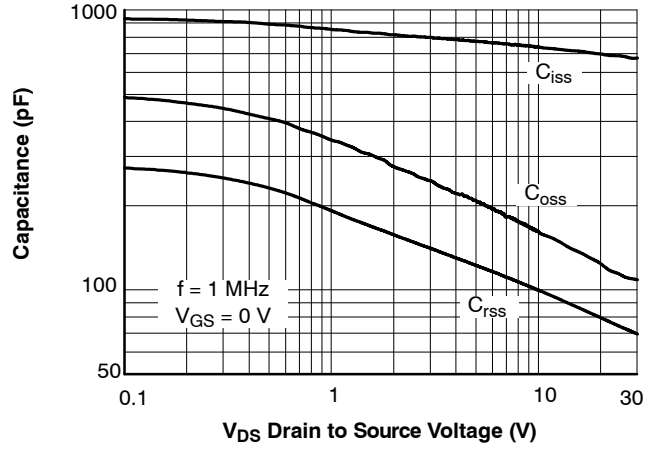


Figure 8. Capacitance vs Drain to Source Voltage

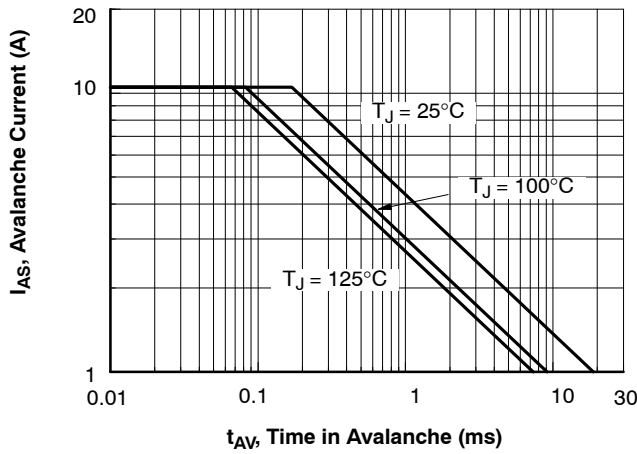


Figure 9. Unclamped Inductive Switching Capability

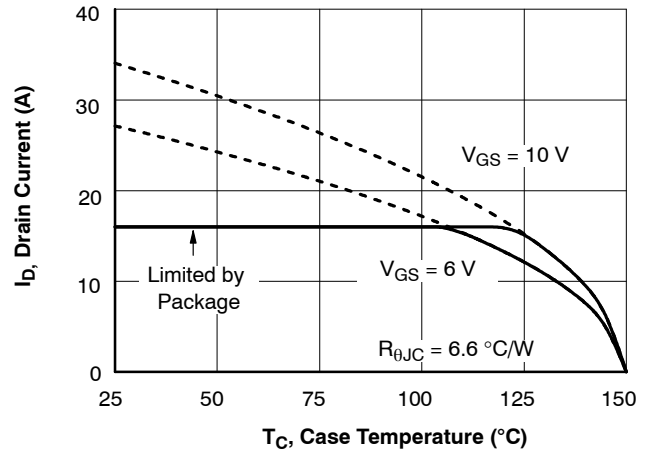


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

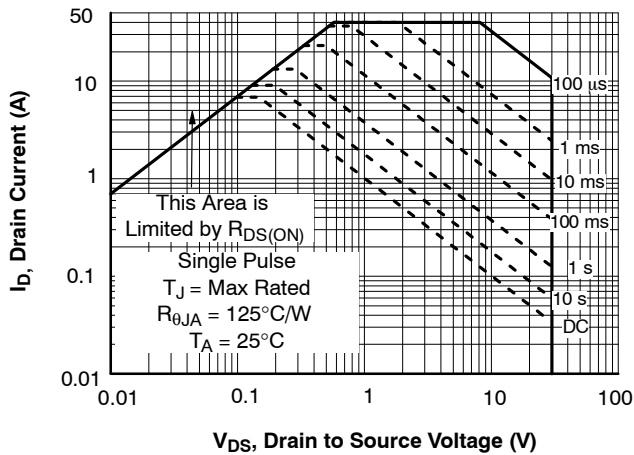


Figure 11. Forward Bias Safe Operating Area

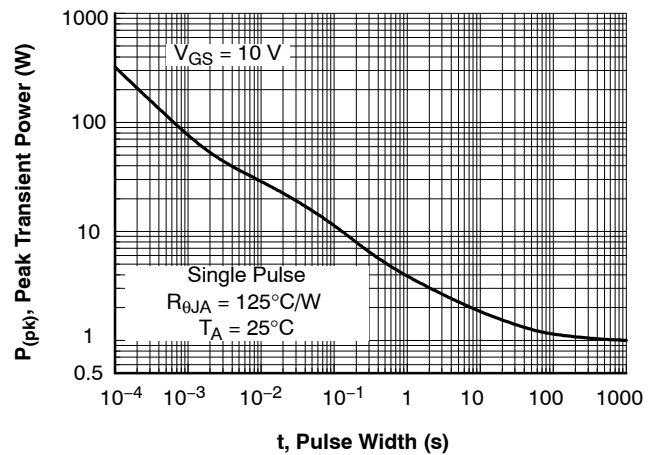


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

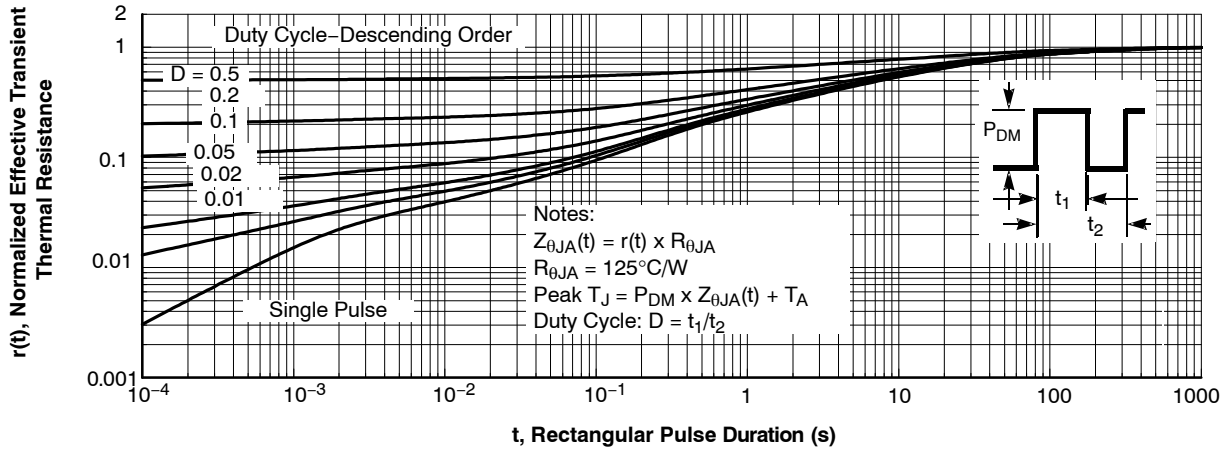
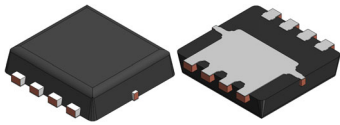


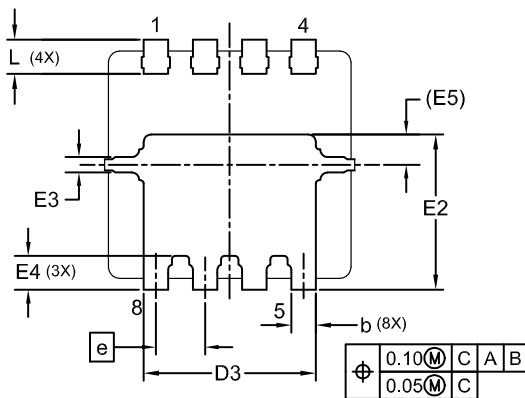
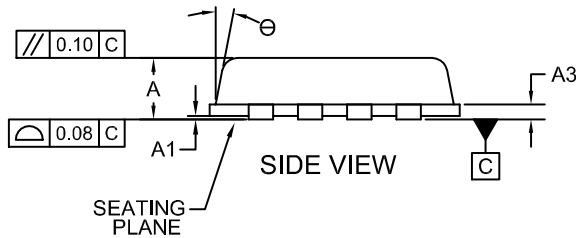
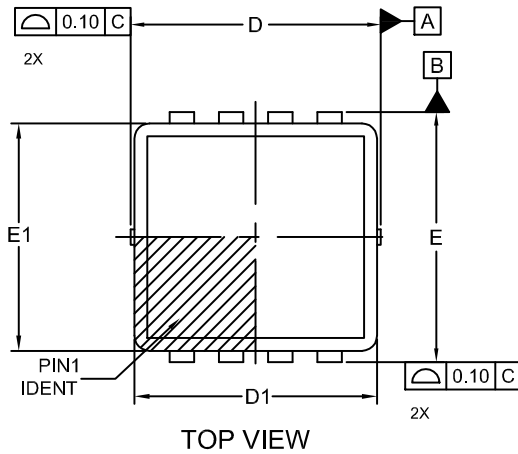
Figure 13. Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**WDFN8 3.3x3.3, 0.65P**  
CASE 511DR  
ISSUE B

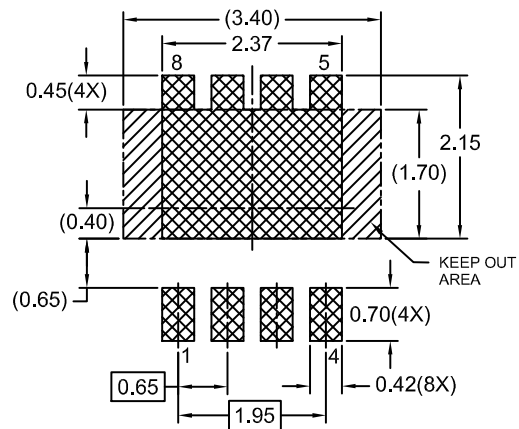
DATE 02 FEB 2022



| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN         | NOM  | MAX  |
| A   | 0.70        | 0.75 | 0.80 |
| A1  | 0.00        | -    | 0.05 |
| A3  | 0.15        | 0.20 | 0.25 |
| b   | 0.27        | 0.32 | 0.37 |
| D   | 3.20        | 3.30 | 3.40 |
| D1  | 3.10        | 3.20 | 3.30 |
| D3  | 2.17        | 2.27 | 2.37 |
| E   | 3.20        | 3.30 | 3.40 |
| E1  | 2.90        | 3.00 | 3.10 |
| E2  | 1.95        | 2.05 | 2.15 |
| E3  | 0.15        | 0.20 | 0.25 |
| E4  | 0.30        | 0.40 | 0.50 |
| E5  | 0.40 REF    |      |      |
| e   | 0.65 BSC    |      |      |
| L   | 0.30        | 0.40 | 0.50 |
| Θ   | 0°          | -    | 12°  |

**NOTES:**

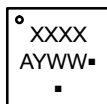
- A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
- C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.



**RECOMMENDED LAND PATTERN**

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM\***



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

(Note: Microdot may be in either location)

|                         |                             |  |
|-------------------------|-----------------------------|--|
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| <b>DESCRIPTION:</b>     | <b>WDFN8 3.3x3.3, 0.65P</b> | <b>PAGE 1 OF 1</b>   |

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