

# **MOSFET** – Dual N-Channel, POWERTRENCH®

60 V, 8.2 A, 17 m $\Omega$ 

# **FDMC89521L**

#### **General Description**

This device includes two 60 V N-Channel MOSFETs in a dual Power 33 (3 mm x 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

#### **Features**

- Max  $r_{DS(on)} = 17 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 8.2 \text{ A}$
- Max  $r_{DS(on)} = 27 \text{ m}\Omega$  at  $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 6.7 \text{ A}$
- Termination is Lead-free
- These Devices are RoHS Compliant

# **Applications**

- Battery Protection
- Load Switching
- Bridge Topologies

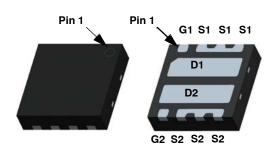
# MOSFET MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Units
VDS	Drain to Source Voltage	60	V
Vgs	Gate to Source Voltage	±20	V
I <sub>D</sub>		8.2 40	Α
Eas	Single Pulse Avalanche Energy (Note 3)	32	mJ
P <sub>D</sub>	Power Dissipation T <sub>C</sub> = 25°C	16	W
5	Power Dissipation $T_A = 25^{\circ}C$ (Note 1a)	1.9	
TJ, TSTG	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
RеJC	Thermal Resistance, Junction-to-Case	8.0	°C/W
R <sub>θ</sub> JA	Thermal Resistance, Junction-to-Ambient (Note 1a)	65	°C/W
R <sub>θ</sub> JA	Thermal Resistance, Junction-to-Ambient (Note 1b)	155	°C/W



Power 33

WDFN8 3x3, 0.65P CASE 511DG

#### **MARKING DIAGRAM**

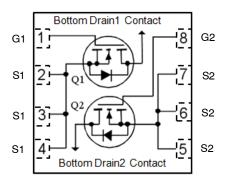


\$Y = onsemi Logo &Z = Assembly Plant Code &2 = Numeric Date Code

&K = Lot Code

FDMC89521L = Specific Device Code

#### **PIN ASSIGNMENT**



**N-Channel MOSFET** 

# **ORDERING INFORMATION**

See detailed ordering and shipping information on page 6 of this data sheet.

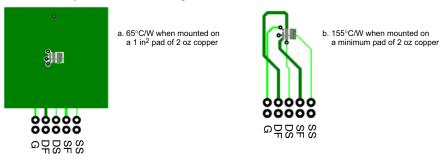
# **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = 25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min.	Тур.	Max.	Unit
OFF CHARA	CTERISTICS				-	
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25°C		30		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA
ON CHARAC	CTERISTICS					
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25°C		-6		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8.2 A		13	17	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.7 A		21	27	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8.2 A, T <sub>J</sub> = 125°C		20	26	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 8.2 A		28		S
YNAMIC C	HARACTERISTICS			•		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V		1228	1635	pF
C <sub>oss</sub>	Output Capacitance	f = 1 MHz		243	325	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1		10	15	pF
$R_g$	Gate Resistance			0.7		Ω
WITCHING	CHARACTERISTICS					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_D = 8.2 \text{ A},$		7.9	16	ns
t <sub>r</sub>	Rise Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$		2.1	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	7		18	33	ns
t <sub>f</sub>	Fall Time	7		1.7	10	ns
Qg	Total Gate Charge	$V_{GS}$ = 0 V to 10 V, $V_{DD}$ = 30 V, $I_D$ = 8.2 A	17	24	nC	
		$V_{GS} = 0 \text{ V to } 4.5 \text{ V}, V_{DD} = 30 \text{ V}, I_D = 8.2 \text{ A}$		7.9	12	nC
Q <sub>gs</sub>	Gate to Source Charge	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 8.2 A		3.8		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			1.9		nC
	IRCE DIODE CHARACTERISTICS	•		•		
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 8.2 A (Note 2)		0.85	1.3	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.6 A (Note 2)		0.75	1.2	1
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 8.2 A, di/dt = 100 A/μs		25	40	ns
Q <sub>rr</sub>	Reverse Recovery Charge	7		11	20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- 2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%. 3. E<sub>AS</sub> of 32 mJ is based on starting T<sub>J</sub> = 25°C, L = 1 mH, I<sub>AS</sub> = 8 A, V<sub>DD</sub> = 54 V, V<sub>GS</sub> = 10 V. 100% tested at L = 3 mH, I<sub>AS</sub> = 5.4 A.

# TYPICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

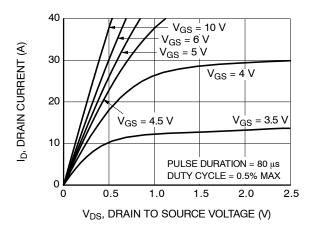


Figure 1. On-Region Characteristics

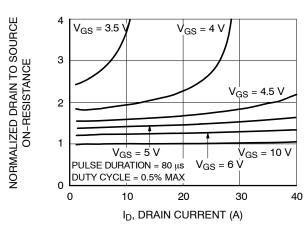


Figure 2. Normalized On–Resistance vs.
Drain Current and Gate Voltage

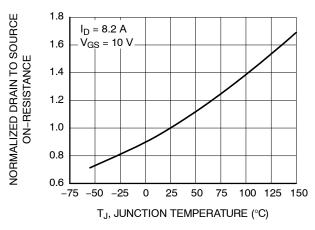


Figure 3. Normalized On–Resistance vs. Junction Temperature

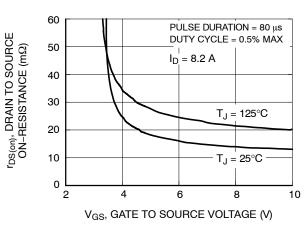


Figure 4. On-Resistance vs. Gate to Source Voltage

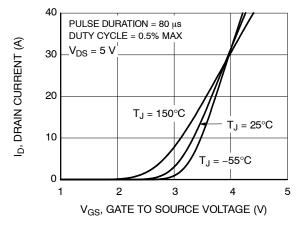


Figure 5. Transfer Characteristics

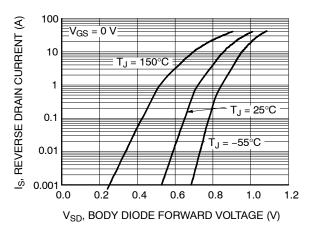


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# TYPICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted) (continued)

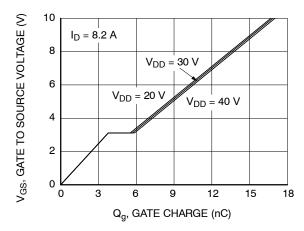


Figure 7. Gate Charge Characteristics

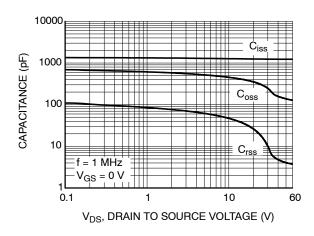


Figure 8. Capacitance vs. Drain to Source Voltage

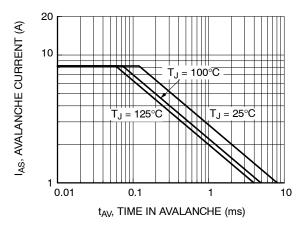


Figure 9. Unclamped Inductive Switching Capability

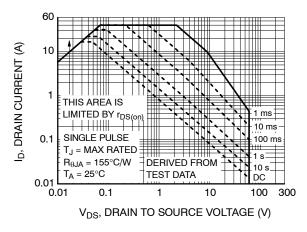


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

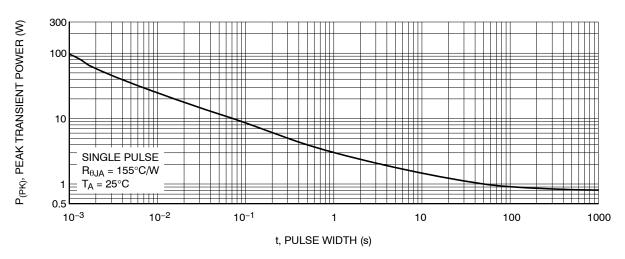


Figure 11. Single Pulse Maximum Power Dissipation

# TYPICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted) (continued)

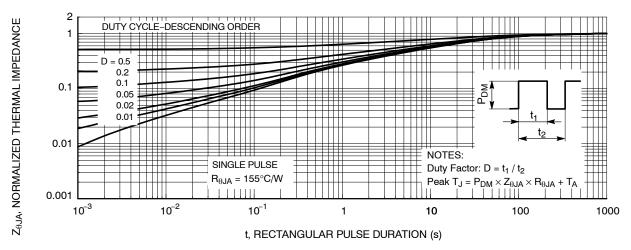


Figure 12. Junction-to-Case Transient Thermal Response Curve

#### **ORDERING INFORMATION**

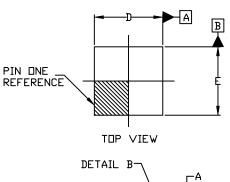
Device	Device Marking	Package Type	Shipping <sup>†</sup>
FDMC89521L	FDMC89521L	WDFN8 3x3, 0.65P (Pb-Free)	3000 / Tape & Reel

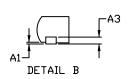
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

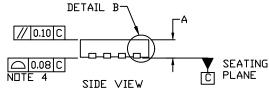
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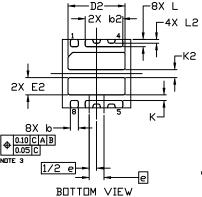
#### WDFN8 3x3, 0.65P CASE 511DG ISSUE A

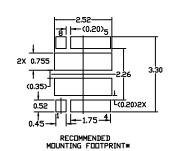
**DATE 12 FEB 2019** 











For additional information on our Pb-Free strategy and soldering details, please download the IIN Semiconductor Soldering and Mounting Techniques Reference Manual, SILDERRH/D.

#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. DIMENSION 6 APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS			
DIM	MIN.	N□M.	MAX.	
Α	0.70	0.75	0.80	
A1	0.00		0.05	
A3	0.20 REF			
ھ	0.30	0.35	0.40	
p2	1.65 REF			
D	2.90	3.00	3.10	
D2	2.45	2.50	2.55	
E	2.90	3.00	3.10	
E2	1.40	1.50	1.60	
e	0.65 BSC			
К	0.25			
K2	0.35 REF			
L	0.27	0.32	0.37	
L2	0.163 REF			

# GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code A = Assembly Location

Y = Year WW = Work Week ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN8 3x3, 0.65P		PAGE 1 OF 1	

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