

# Digital FET, N-Channel

## FDV303N

### General Description

These N-Channel enhancement mode field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. This very high density process is tailored to minimize on-state resistance at low gate drive conditions. This device is designed especially for application in battery circuits using either one lithium or three cadmium or NMH cells. It can be used as an inverter or for high-efficiency miniature discrete DC/DC conversion in compact portable electronic devices like cellular phones and pagers. This device has excellent on-state resistance even at gate drive voltages as low as 2.5 V.

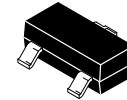
### Features

- 25 V, 0.68 A Continuous, 2 A Peak
  - ◆  $R_{DS(ON)} = 0.45 \Omega @ V_{GS} = 4.5 V$
  - ◆  $R_{DS(ON)} = 0.6 \Omega @ V_{GS} = 2.7 V$
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits,  $V_{GS(th)} < 1 V$
- Gate-Source Zener for ESD Ruggedness, > 6 kV Human Body Model
- Compact Industry Standard SOT-23 Surface Mount Package
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant



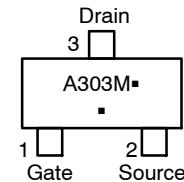
**ON Semiconductor®**

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SOT-23 (TO-236)  
CASE 318-08  
STYLE 21

### MARKING DIAGRAM



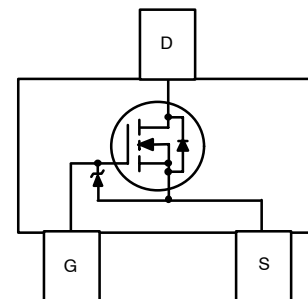
A or blank = One/two character Location Code  
303 = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\* Location code can be blank or with characters indicating manufacturing location

\* Date Code orientation and overbar may vary depending upon manufacturing location.

### PIN ASSIGNMENT



SOT-23

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDV303N

## MOSFET MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDV303N	Units
$V_{DSS}$	Drain–Source Voltage, Power Supply Voltage	25	V
$V_{GSS}$	Gate–Source Voltage, $V_{IN}$	8	V
$I_D$	Drain/Output Current – Continuous – Pulsed	0.68 2	A
$P_D$	Maximum Power Dissipation	0.35	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	–55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL–STD–883D Human Body Model (100 pf / 1500 $\Omega$ )	6.0	kV

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Units
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient	357	$^\circ\text{C}/\text{W}$

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
FDV303N	SOT–23 Case 318–08	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# FDV303N

**ELECTRICAL CHARACTERISTICS**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		26		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$			1	$\mu\text{A}$
					10	$\mu\text{A}$
$I_{GSS}$	Gate - Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA

**ON CHARACTERISTICS** (Note 1)

$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-2.6		mV/ $^\circ\text{C}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.65	0.8	1	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$ $T_J = 125^\circ\text{C}$		0.33	0.45	$\Omega$
				0.52	0.8	
			$V_{GS} = 2.7\text{ V}, I_D = 0.2\text{ A}$	0.44	0.6	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 2.7\text{ V}, V_{DS} = 5\text{ V}$	0.5			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 0.5\text{ A}$		1.45		S

**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		50		pF
$C_{oss}$	Output Capacitance			28		pF
$C_{rss}$	Reverse Transfer Capacitance			9		pF

**SWITCHING CHARACTERISTICS** (Note 1)

$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 6\text{ V}, I_D = 0.5\text{ A}, V_{GS} = 4.5\text{ V}, R_{GEN} = 50\ \Omega$		3	6	ns
$t_r$	Turn - On Rise Time			8.5	18	ns
$t_{D(off)}$	Turn - Off Delay Time			17	30	ns
$t_f$	Turn - Off Fall Time			13	25	ns
$Q_g$	Total Gate Charge	$V_{DS} = 5\text{ V}, I_D = 0.5\text{ A}, V_{GS} = 4.5\text{ V}$		1.64	2.3	nC
$Q_{gs}$	Gate-Source Charge			0.38		nC
$Q_{gd}$	Gate-Drain Charge			0.45		nC

**DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			0.3		A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.5\text{ A}$ (Note 1)		0.83	1.2	V

1. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%.

TYPICAL CHARACTERISTICS

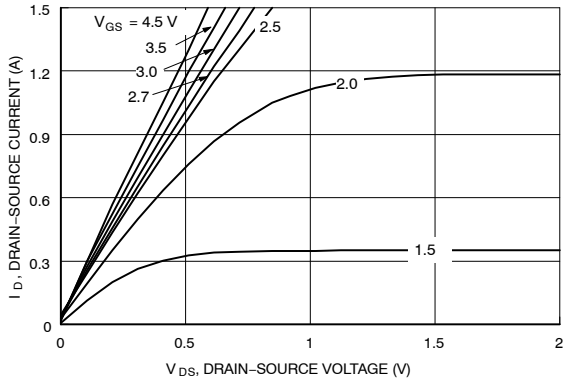


Figure 1. On-Region Characteristics

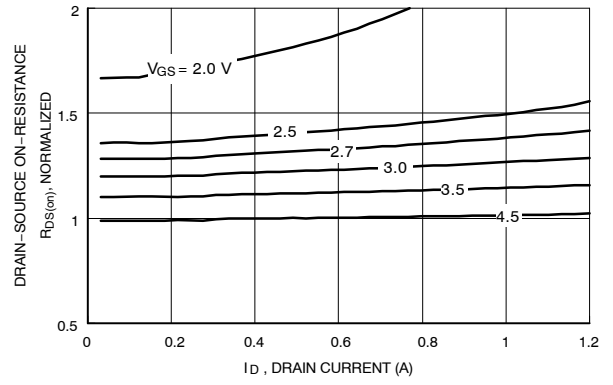


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

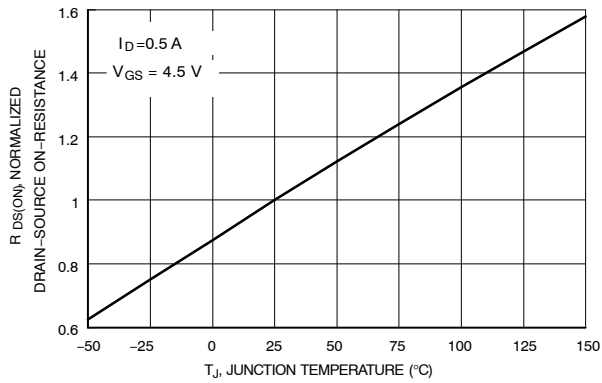


Figure 3. On-Resistance Variation with Temperature

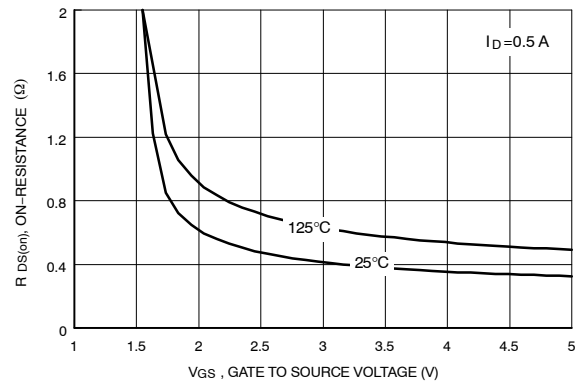


Figure 4. On Resistance Variation with Gate-To-Source Voltage

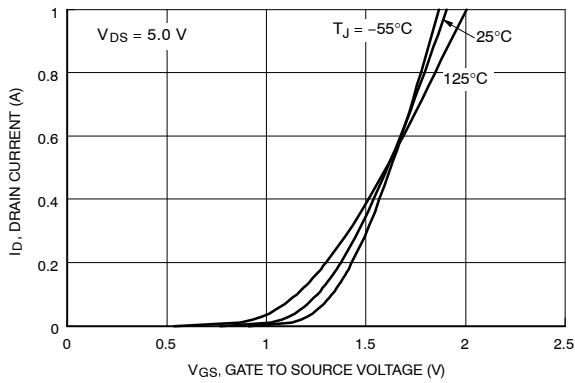


Figure 5. Transfer Characteristics

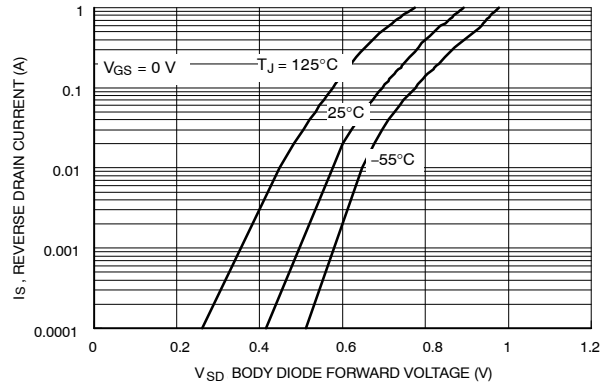


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  Unless Otherwise Noted (continued)

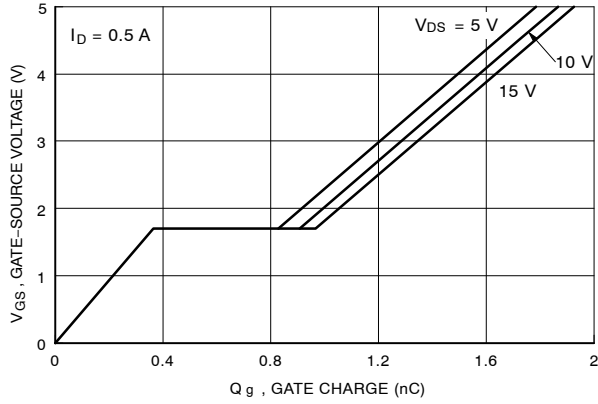


Figure 7. Gate Charge Characteristics

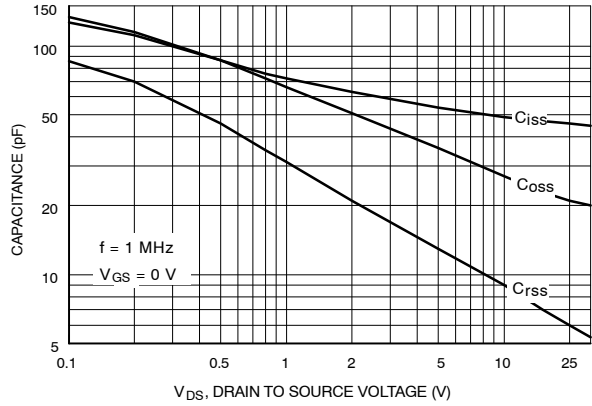


Figure 8. Capacitance Characteristics

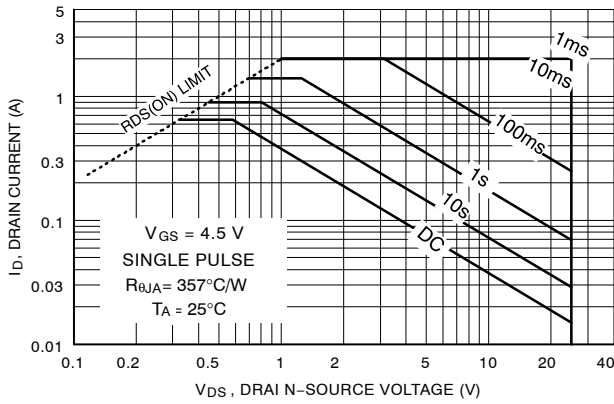


Figure 9. Maximum Safe Operating Area

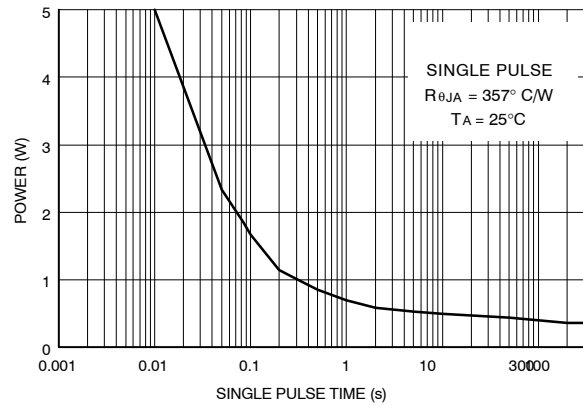


Figure 10. Single Pulse Maximum Power Dissipation

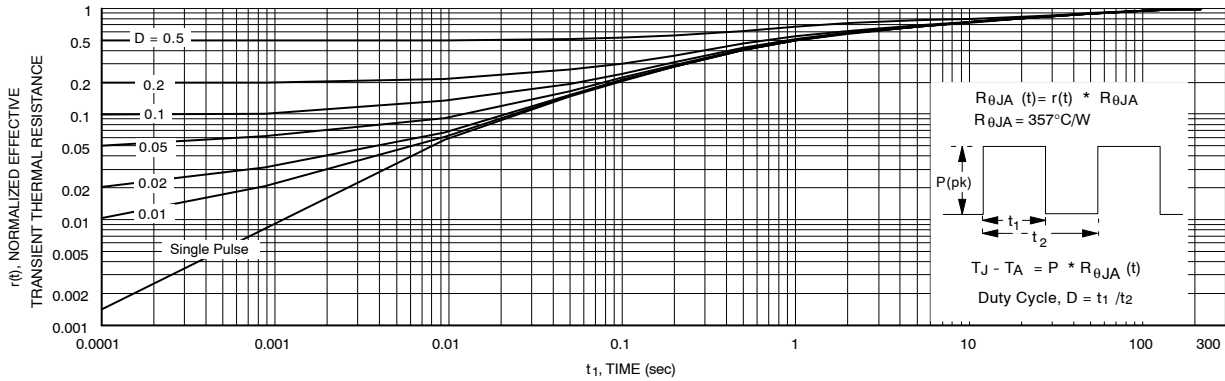


Figure 11. Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**SOT-23 (TO-236)**  
CASE 318  
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H <sub>E</sub>	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



**SOT-23 (TO-236)**  
**CASE 318**  
**ISSUE AT**

DATE 01 MAR 2023

- |   |   |   |   |   |   |
|---|---|---|---|---|---|
| STYLE 1 THRU 5:<br>CANCELLED                            | STYLE 6:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR | STYLE 7:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR       | STYLE 8:<br>PIN 1. ANODE<br>2. NO CONNECTION<br>3. CATHODE  |   |   |
| STYLE 9:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE      | STYLE 10:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE     | STYLE 11:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE-ANODE | STYLE 12:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE       | STYLE 13:<br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE           | STYLE 14:<br>PIN 1. CATHODE<br>2. GATE<br>3. ANODE          |
| STYLE 15:<br>PIN 1. GATE<br>2. CATHODE<br>3. ANODE      | STYLE 16:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE | STYLE 17:<br>PIN 1. NO CONNECTION<br>2. ANODE<br>3. CATHODE | STYLE 18:<br>PIN 1. NO CONNECTION<br>2. CATHODE<br>3. ANODE | STYLE 19:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE-ANODE | STYLE 20:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE          |
| STYLE 21:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN       | STYLE 22:<br>PIN 1. RETURN<br>2. OUTPUT<br>3. INPUT   | STYLE 23:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE         | STYLE 24:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE           | STYLE 25:<br>PIN 1. ANODE<br>2. CATHODE<br>3. GATE          | STYLE 26:<br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION |
| STYLE 27:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE | STYLE 28:<br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE     |   |   |   |   |

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