

# MOSFET – Dual, N-Channel, POWERTRENCH®

30 V, 12 mΩ and 23.5 mΩ

## FDMC7200

### General Description

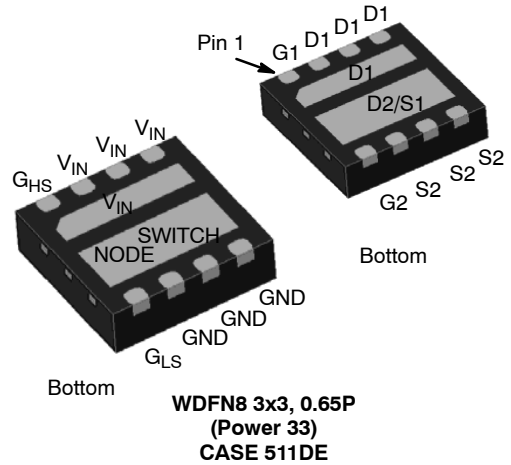
This device includes two specialized N-Channel MOSFETs in a dual Power 33 (3 mm x 3 mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

### Features

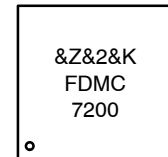
- Q1: N-Channel
  - ◆ Max  $R_{DS(on)}$  = 23.5 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 6\text{ A}$
  - ◆ Max  $R_{DS(on)}$  = 38 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 5\text{ A}$
- Q2: N-Channel
  - ◆ Max  $R_{DS(on)}$  = 12 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 8\text{ A}$
  - ◆ Max  $R_{DS(on)}$  = 18 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 7\text{ A}$
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load

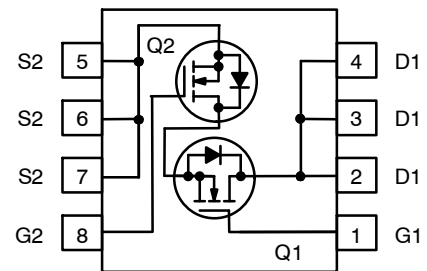


### MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = 2-Digit Date-Code
- &K = 2-Digit Lot Code
- FDMC7200 = Device Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

Device	Package	Shipping†
FDMC7200	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDMC7200

## MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Q1	Q2	Unit
$V_{DS}$	Drain to Source Voltage	30	30	V
$V_{GS}$	Gate to Source Voltage (Note 3)	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current – Continuous (Package Limited) $T_C = 25^\circ\text{C}$	8	8	A
	– Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$	20	40	
	– Continuous $T_A = 25^\circ\text{C}$	6 (Note 1a)	8 (Note 1b)	
	– Pulsed	40	40	
$P_D$	Power Dissipation $T_A = 25^\circ\text{C}$	1.9 (Note 1a)	2.2 (Note 1b)	W
	Power Dissipation $T_A = 25^\circ\text{C}$	0.7 (Note 1c)	0.9 (Note 1d)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 (Note 1a)	55 (Note 1b)	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	180 (Note 1c)	145 (Note 1d)	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	7.5	4	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	Q1	30	–	–	V
		$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	Q2	30	–	–	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1	–	14	–	$\text{mV}/^\circ\text{C}$
		$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	Q2	–	14	–	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	Q1	–	–	1	$\mu\text{A}$
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	Q2	–	–	1	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q1	–	–	100	nA
			Q2	–	–	100	

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	Q1	1.0	2.3	3.0	V
		$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	Q2	1.0	2.3	3.0	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1	–	–5	–	$\text{mV}/^\circ\text{C}$
		$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	Q2	–	–6	–	
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}, T_J = 125^\circ\text{C}$	Q1	–	19	23.5	m $\Omega$
			Q2	–	28	38	
		$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}, T_J = 125^\circ\text{C}$	Q1	–	10	12	
			Q2	–	13	18	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_D = 6 \text{ A}$ $V_{DD} = 5 \text{ V}, I_D = 8 \text{ A}$	Q1	–	29	–	S
			Q2	–	56	–	

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	Q1	–	495	660	pF
			Q2	–	1180	1570	
$C_{oss}$	Output Capacitance		Q1	–	145	195	pF
			Q2	–	330	440	
$C_{rss}$	Reverse Transfer Capacitance		Q1	–	20	30	pF
			Q2	–	30	45	

# FDMC7200

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
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### DYNAMIC CHARACTERISTICS

R <sub>g</sub>	Gate Resistance	f = 1 MHz	Q1	–	1.4	–	Ω
			Q2	–	1.4	–	

### SWITCHING CHARACTERISTICS

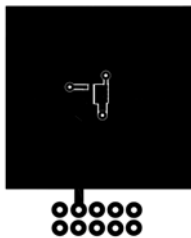
t <sub>d(on)</sub>	Turn-On Delay Time	Q1 V <sub>DD</sub> = 15 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω Q2 V <sub>DD</sub> = 15 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	Q1	–	11	20	ns
t <sub>r</sub>	Rise Time		Q1	–	3.1	10	
t <sub>d(off)</sub>	Turn-Off Delay Time		Q2	–	4	10	
t <sub>f</sub>	Fall Time		Q1	–	35	56	
			Q2	–	38	60	
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 6 A Q2: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 8 A	Q1	–	7.3	10	nC
			Q2	–	16	22	
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 4.5 V Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 6 A Q2: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 8 A	Q1	–	3.1	4.3	nC
			Q2	–	7	10	
Q <sub>gs</sub>	Gate to Source Charge	Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 6 A	Q1	–	1.8	–	nC
		Q2: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 8 A	Q2	–	4.1	–	
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 6 A	Q1	–	1	–	nC
		Q2: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 8 A	Q2	–	1.5	–	

### DRAIN-SOURCE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 6 A (Note 2) V <sub>GS</sub> = 0 V, I <sub>S</sub> = 8 A (Note 2)	Q1	–	0.8	1.2	V
			Q2	–	0.8	1.2	
t <sub>rr</sub>	Reverse Recovery Time	Q1 I <sub>F</sub> = 6 A, di/dt = 100 A/μS	Q1	–	13	24	ns
		Q2 I <sub>F</sub> = 8 A, di/dt = 100 A/μS	Q2	–	21	34	
Q <sub>rr</sub>	Reverse Recovery Charge	Q1 I <sub>F</sub> = 6 A, di/dt = 100 A/μS	Q1	–	2.3	10	nC
		Q2 I <sub>F</sub> = 8 A, di/dt = 100 A/μS	Q2	–	5.6	12	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

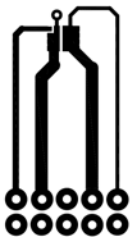
1. R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



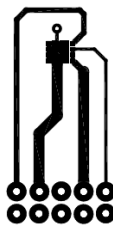
- a. 65°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



- b. 55°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



- c. 180°C/W when mounted on a minimum pad of 2 oz copper



- d. 145°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. As an N-ch device, the negative V<sub>gs</sub> rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

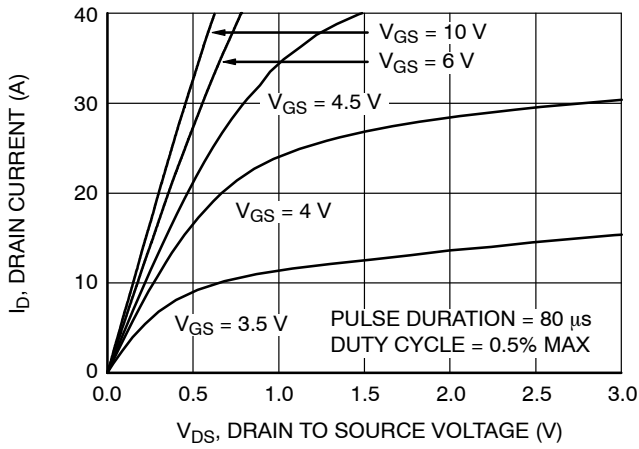


Figure 1. On Region Characteristics

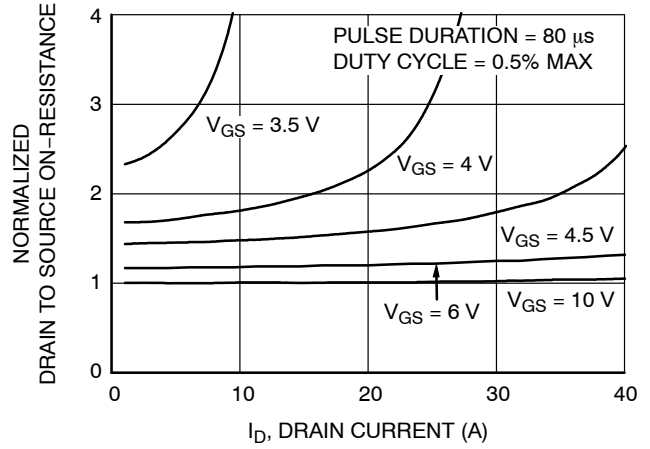


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

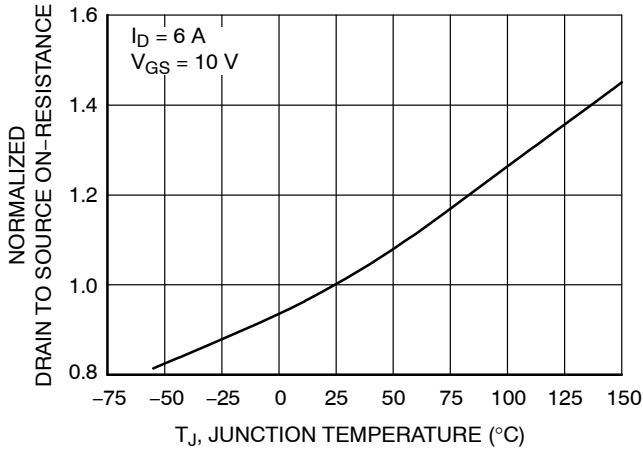


Figure 3. Normalized On Resistance vs. Junction Temperature

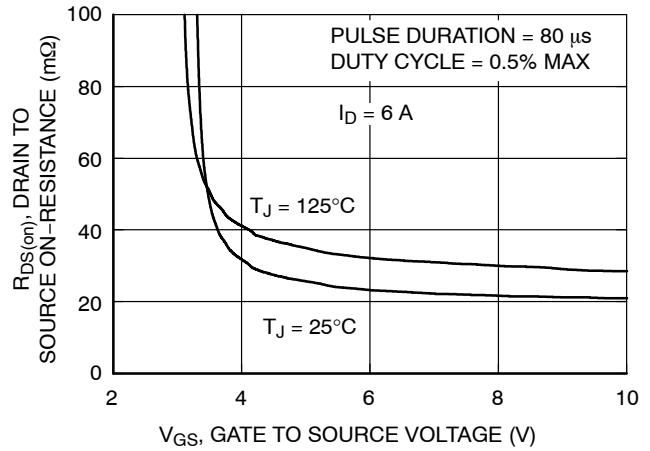


Figure 4. On-Resistance vs. Gate to Source Voltage

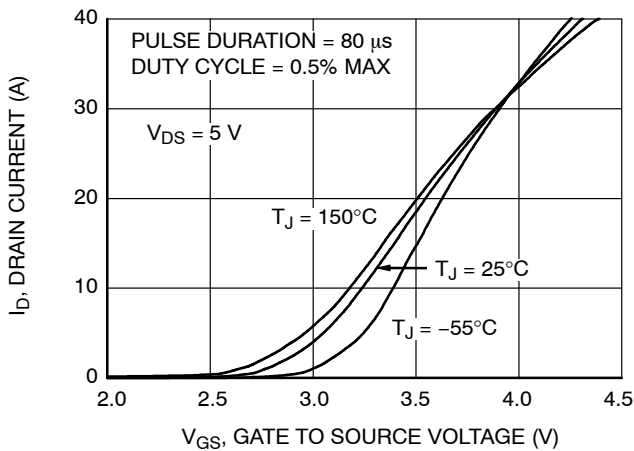


Figure 5. Transfer Characteristics

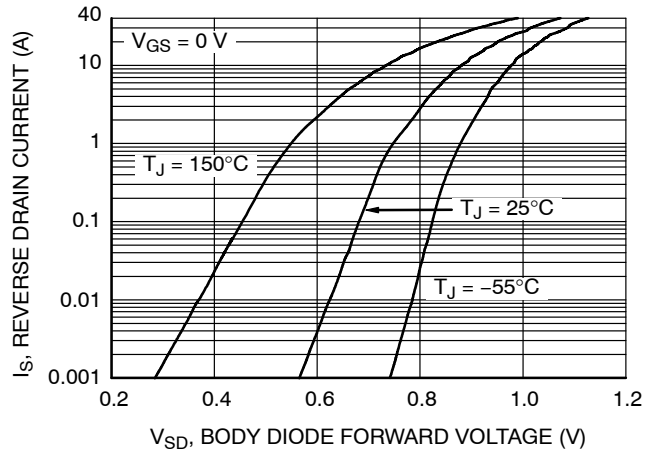


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

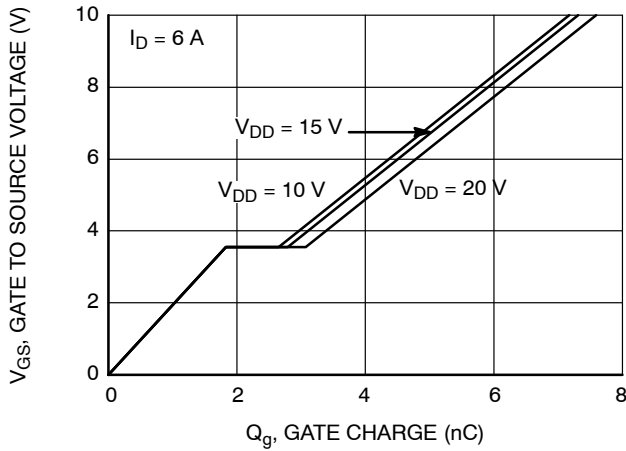


Figure 7. Gate Charge Characteristics

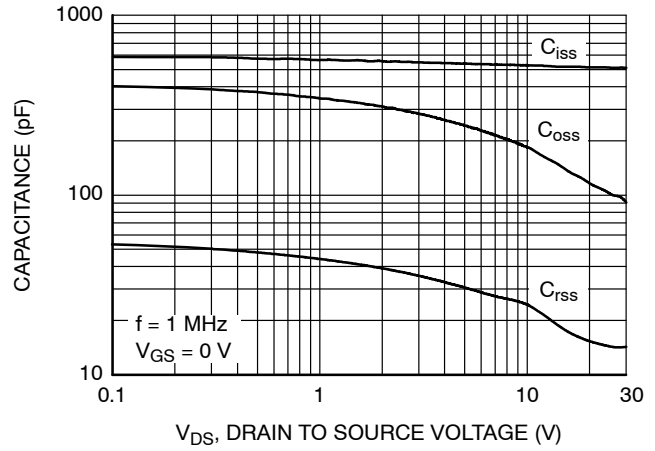


Figure 8. Capacitance vs. Drain to Source Voltage

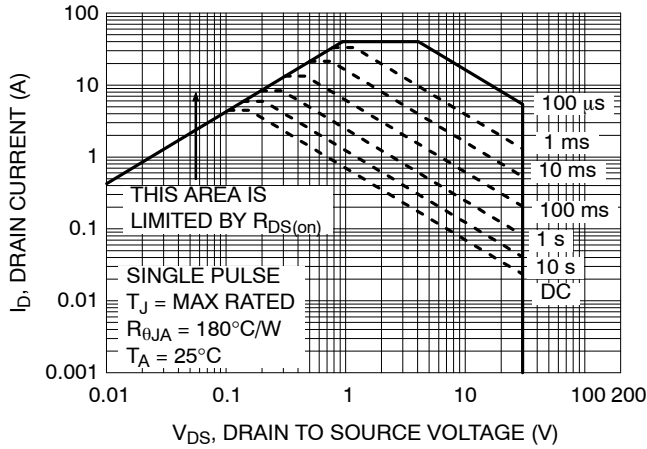


Figure 9. Forward Bias Safe Operating Area

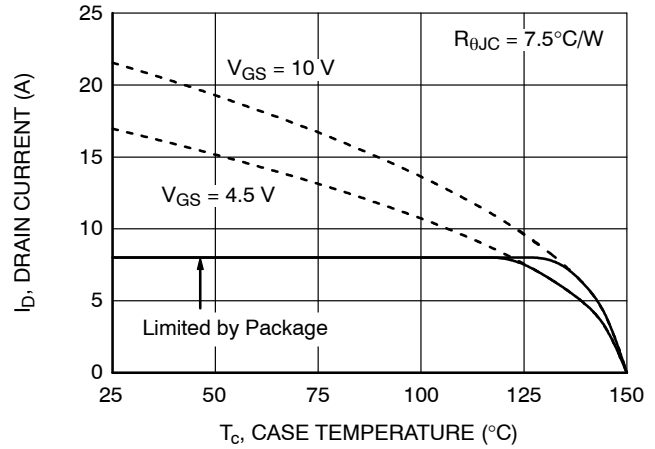


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

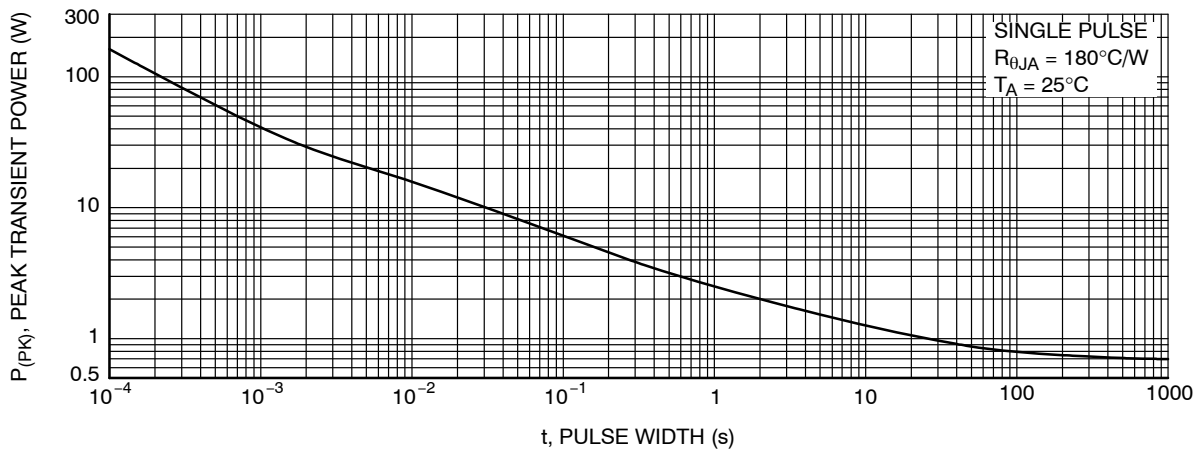


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

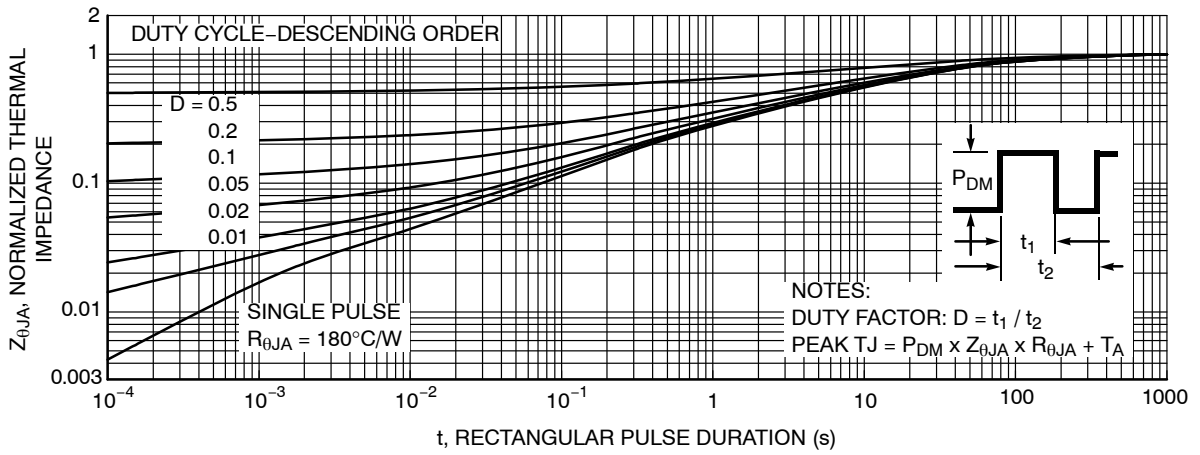


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

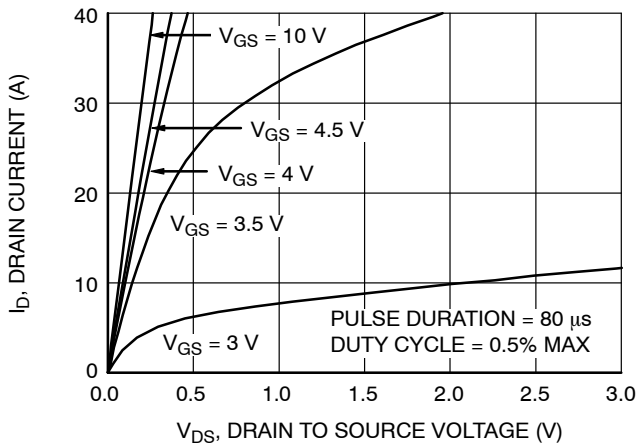


Figure 13. On-Region Characteristics

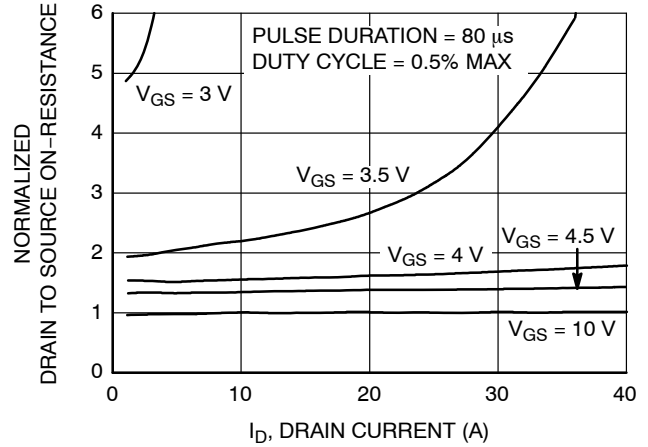


Figure 14. Normalized On-Resistance vs. Drain Current and Gate Voltage

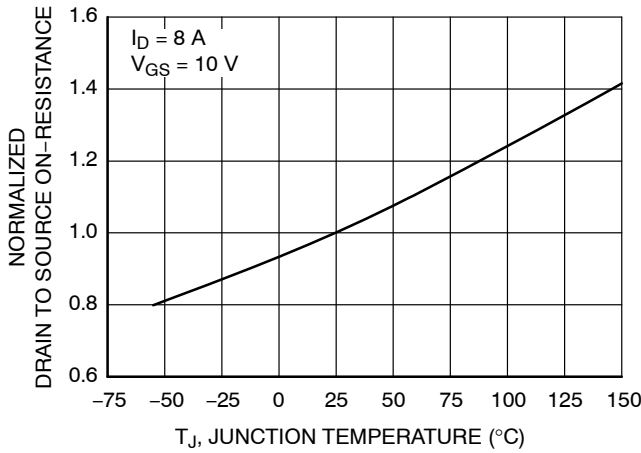


Figure 15. Normalized On Resistance vs. Junction Temperature

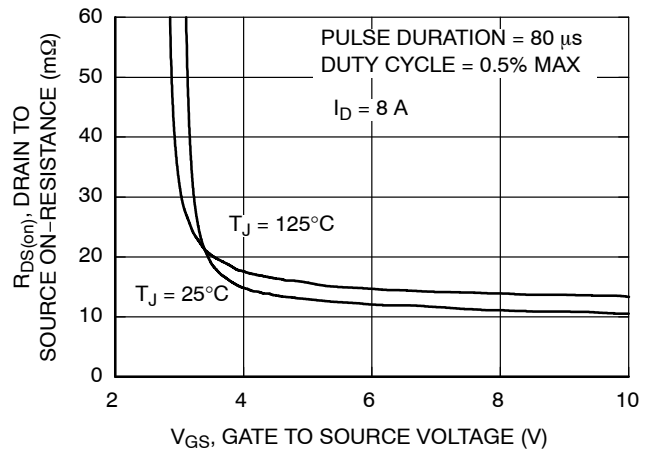


Figure 16. On-Resistance vs. Gate to Source Voltage

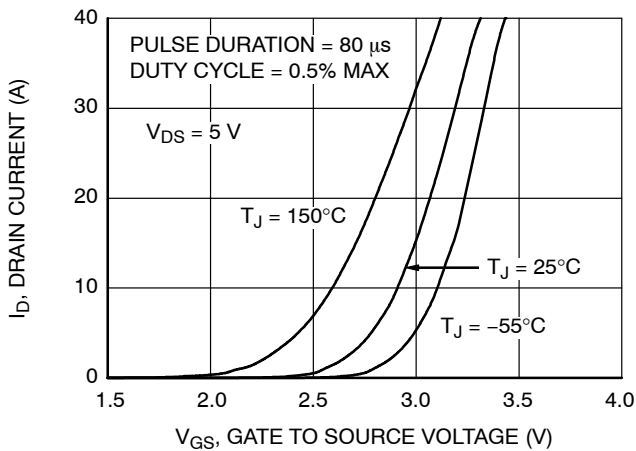


Figure 17. Transfer Characteristics

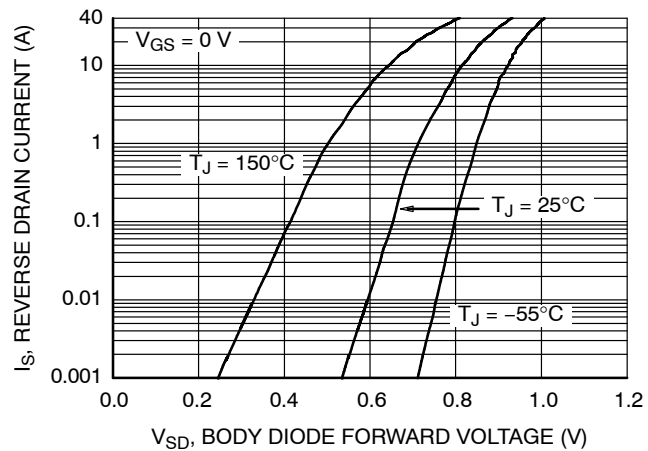


Figure 18. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

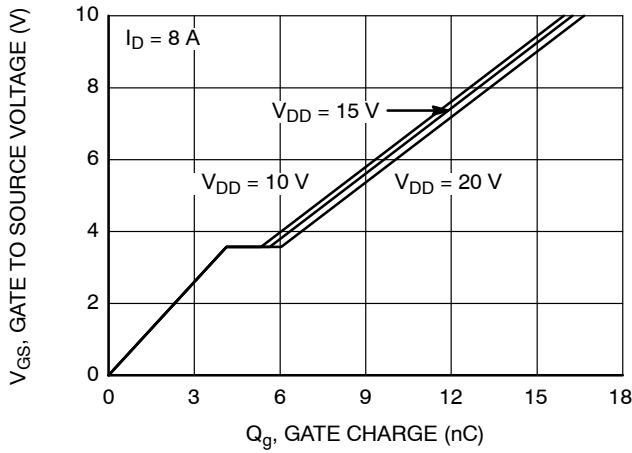


Figure 19. Gate Charge Characteristics

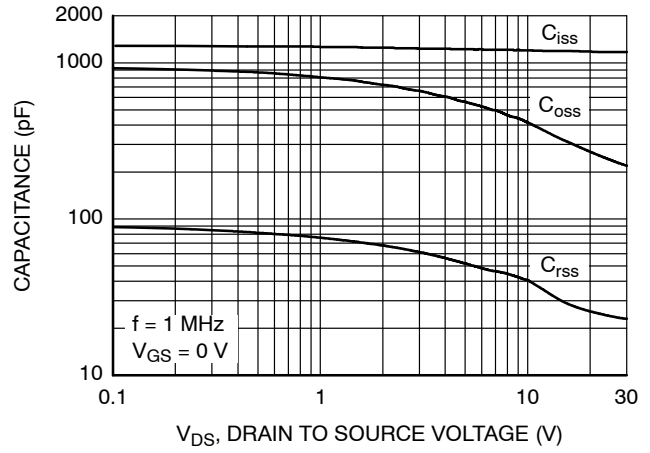


Figure 20. Capacitance vs. Drain to Source Voltage

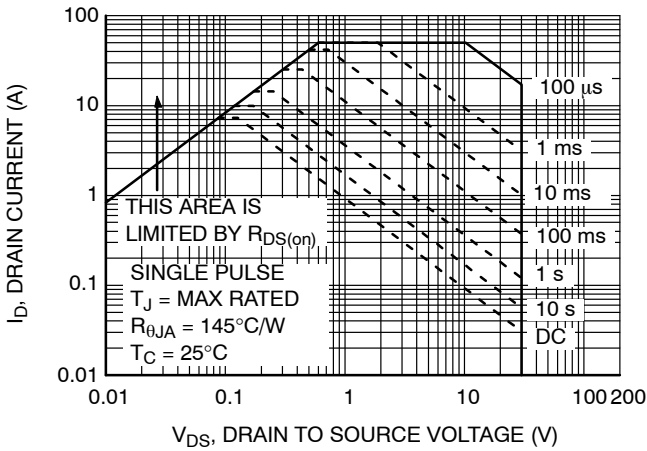


Figure 21. Forward Bias Safe Operating Area

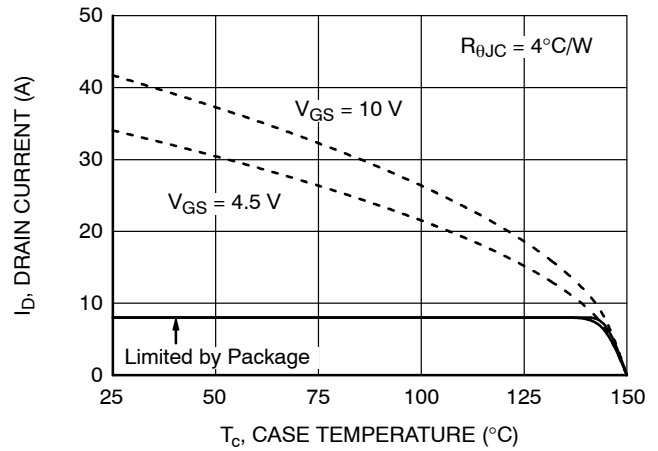


Figure 22. Maximum Continuous Drain Current vs. Case Temperature

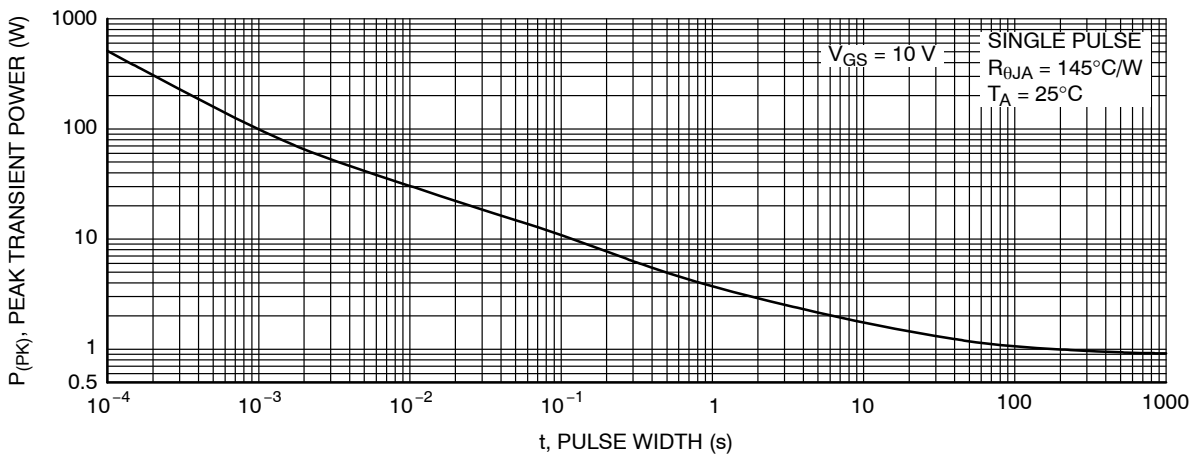


Figure 23. Single Pulse Maximum Power Dissipation



TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

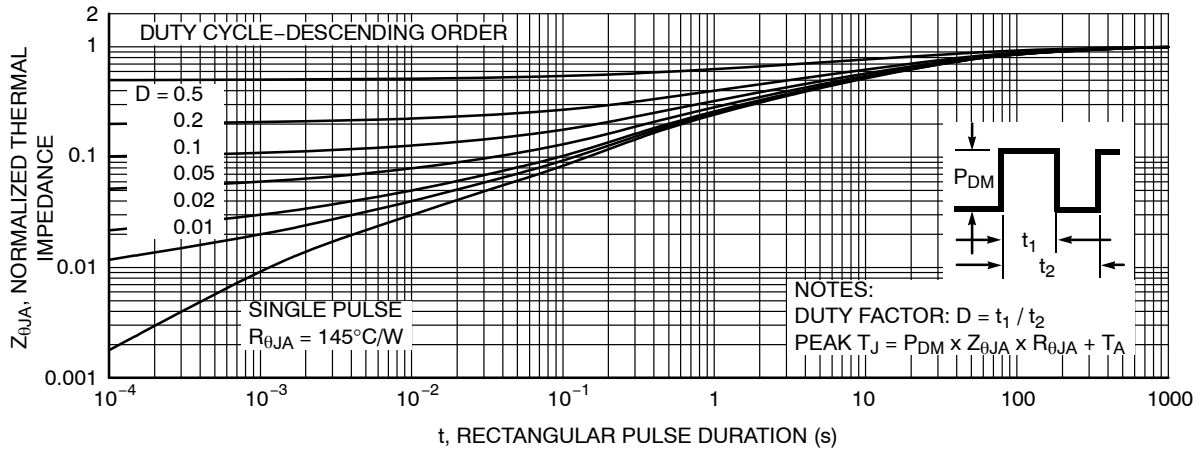


Figure 24. Junction-to-Ambient Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE

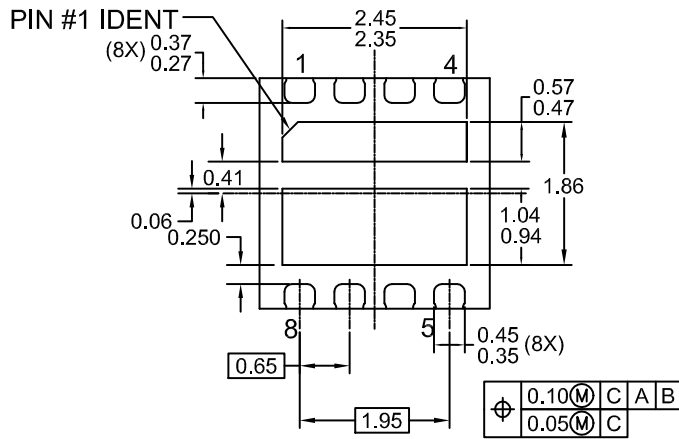
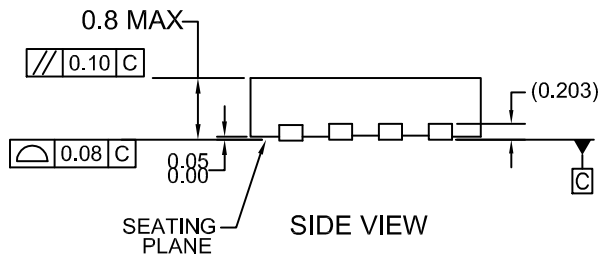
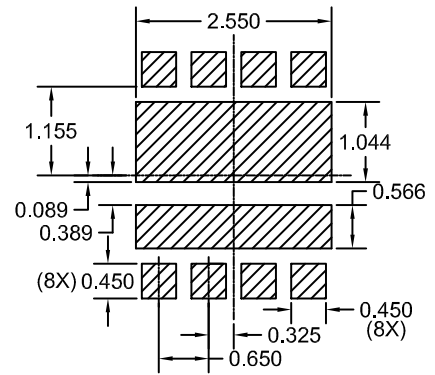
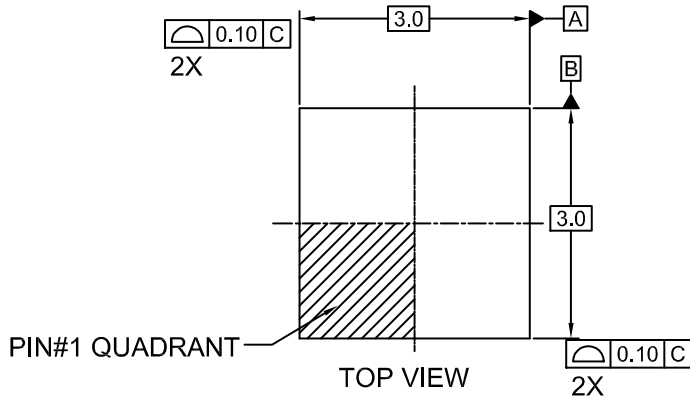
## PACKAGE DIMENSIONS

ON Semiconductor®



WDFN8 3x3, 0.65P  
CASE 511DE  
ISSUE O

DATE 31 AUG 2016



### NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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