EMI2180

Common Mode Filter with ESD Protection

Functional Description

The EMI2180 is an industry first Common Mode Filter tuned to MHL speed (CMF) with integrated ESD protection. Differential signaling I/Os can now have both common mode filtering and ESD protection in one package, instead of using separate devices for each function. In addition, traditional common mode chokes are coil–based, while the EMI2180 is silicon–based. This enables the EMI2180 to have a smaller footprint and profile. The EMI2180 protects against ESD pulses up to ±15 kV contact per the IEC61000–4–2 standard.

The EMI2180 is particularly well–suited for protecting systems using high–speed differential ports such as MHL, MHL to USB interface corresponding ports in removable storage, digital camcorders, DVD–RW drives; and other applications where ESD protection are required in a small footprint package.

The EMI2180 is available in a RoHS–compliant, WDFN-8 package.

Features

- Single Integrated Package for Common Mode Filter (CMF) and ESD Protection for MHL High Speed Data Lines
- High Differential Mode Bandwidth Cutoff Frequency for Best Signal Integrity
- Low Profile with Small Footprint in WDFN6 1.6 x 2.0 mm Package
- Provides ESD Protection to IEC61000–4–2 Level 4, ±15 kV Contact Discharge
- Low Channel Input Capacitance
- These Devices are Pb–Free and are RoHS Compliant

Applications

- I/O Ports, Display, MHL in Mobile Phones, Wireless Handsets and Cameras
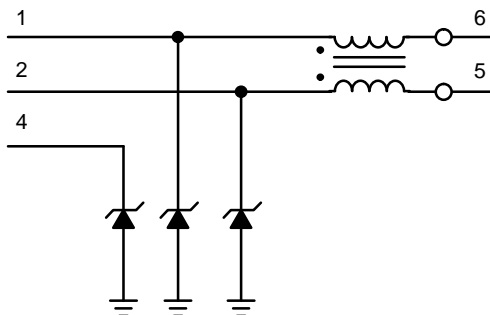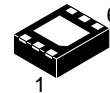- MHL to USB Interface
- High–Speed Differential Data Lines
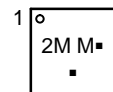

Figure 1. EMI2180 Electrical Schematic

ON Semiconductor®
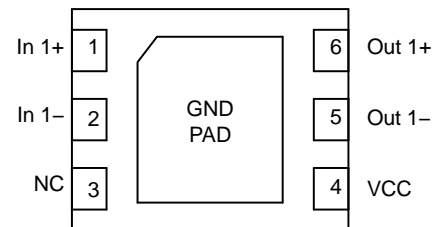
http://onsemi.com

MARKING DIAGRAM

WDFN6
CASE 511BV

2M = Specific Device Code
M = Date Code
▪ = Pb–Free Package

(*Note: Microdot may be in either location)

PIN CONNECTIONS

In 1+	1		6	Out 1+
In 1–	2	GND PAD	5	Out 1–
NC	3		4	VCC

(Top View)

ORDERING INFORMATION

Device	Package	Shipping[†]
EMI2180MTTBG	WDFN6 (Pb–Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

EMI2180

PIN FUNCTION DESCRIPTION

Pin Name	Pin No.	Type	Description
MHL_In+	1	I/O	CMF Channel 1+ to Connector (External)
MHL_In−	2	I/O	CMF Channel 1− to Connector (External)
MHL_Out+	6	I/O	CMF Channel 1+ to ASIC (Internal)
MHL_Out−	5	I/O	CMF Channel 1− to ASIC (Internal)
VCC	4	VCC	Supply Protection (External)
NC	3	NC	No Connect
GND	Belly Pad	GND	GND

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Operating Temperature Range	Top	−40 to +85	°C
Storage Temperature Range	Tstg	−65 to +150	°C
DC Voltage at any channel input	Vdc	−0.5 to 5.5	V
ESD Discharge IEC61000−4−2 Contact Discharge	V_{PP}	±15	kV
Maximum Lead Temperature for Soldering Purposes (1/8" from Case for 10 seconds)	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

EMI2180

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LEAK}	Channel Leakage Current	T_A = 25°C, V_{IN} = 5 V, V_N = 0 V			1.0	μA
V_F	Channel Negative Voltage	I_F = 10 mA, T_A = 25°C	0.1		1.5	V
C_{ID}	Channel ID Capacitance (Pin 4 to GND)	T_A = 25°C, At 1 MHz, V_N = 0 V		0.8	1.3	pF
C_{IN}	Channel Input Capacitance (Pins 1, 2 to GND)	T_A = 25°C, At 1 MHz, V_N = 0 V		2.0		pF
R_{CH}	Channel Resistance (Pins 1–6 and 2–5)	T_A = 25°C, At 1 MHz, V_N = 0 V		3.5	5.0	Ω
f_{3dB}	Differential Mode (Sdd21) Cut–off Frequency	50 Ω Source and Load Termination		4.0		GHz
f_{ATTN}	Common Mode (Scc21) Stop Band Attenuation	@ 75 MHz		3		dB
		@ 500 MHz		10		dB
		@ 1 GHz ~ 3 GHz		15		dB
f_{ATTN}	Mode–to–Mode Conversion (Sdc21, Scd21)	up to 6 GHz		40	35	dB
V_{ESD}	In–system ESD Withstand Voltage a) Contact discharge per IEC 61000–4–2 standard, Level 4 **(External Pins)** b) Contact discharge per IEC 61000–4–2 standard, Level 1 **(Internal Pins)**	(Notes 1 and 2)	±15 ±12			kV
V_{RWM}	Reverse Working Voltage	(Note 3)			5.0	V
V_{BR}	Breakdown Voltage	IT = 1 mA, (Note 4)	5.6		9.0	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
1. Standard IEC61000–4–2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330, V_N grounded.
2. These measurements performed with no external capacitor.
3. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level
4. V_{BR} is measured at pulse test current I_T.
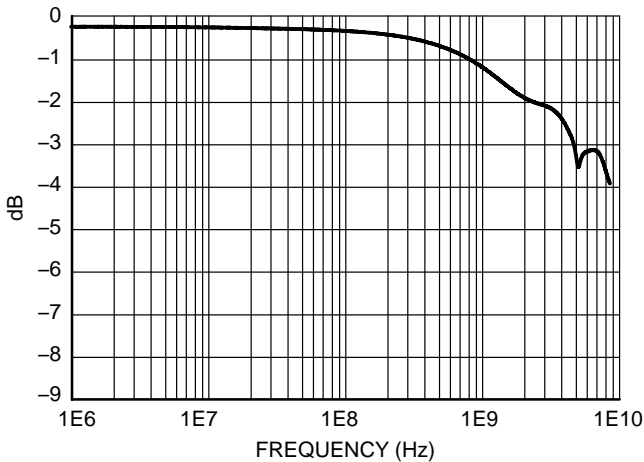
TYPICAL CHARACTERISTICS

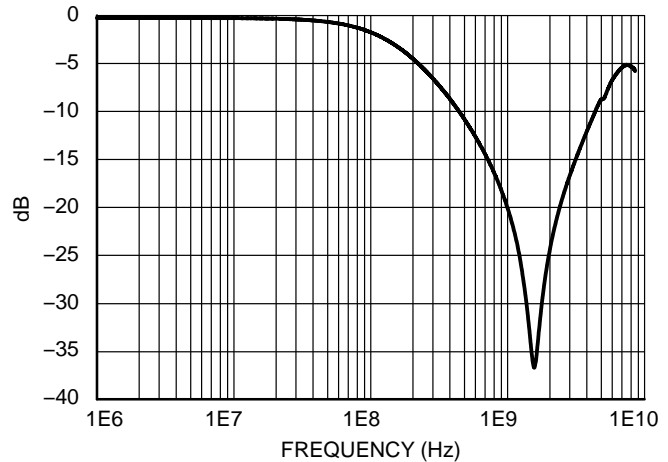Figure 2. Differential Mode Attenuation vs. Frequency

Figure 3. Common Mode Attenuation vs. Frequency

EMI2180

TRANSMISSION LINE PULSE (TLP) MEASUREMENTS

Transmission Line Pulse (TLP) provides current versus voltage (I–V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 4. TLP I–V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10 s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 5 where an 8 kV IEC61000–4–2 current waveform is compared with TLP current pulses at 8 and 16 A. A TLP curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. Typical TLP I–V curves for the EMI2180 are shown in Figure 6.
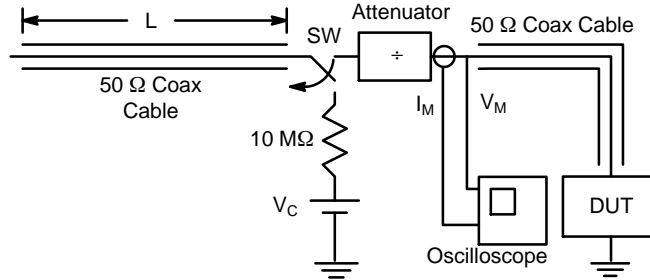
Figure 4. Simplified Schematic of a Typical TLP System
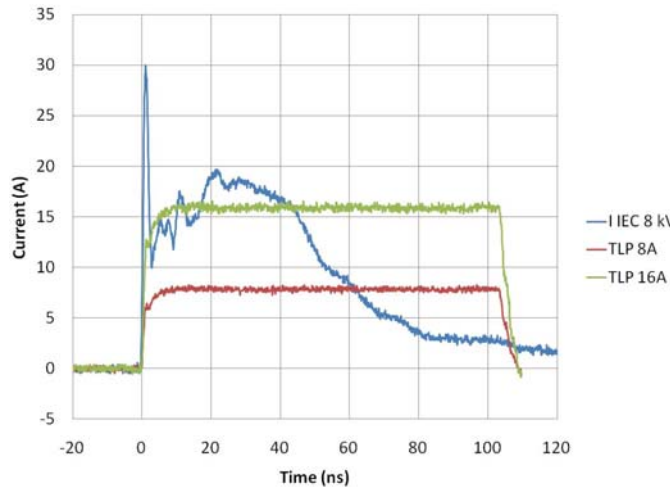
Figure 5. Comparison Between 8 kV IEC61000–4–2 and 8 A and 16 A TLP Waveforms
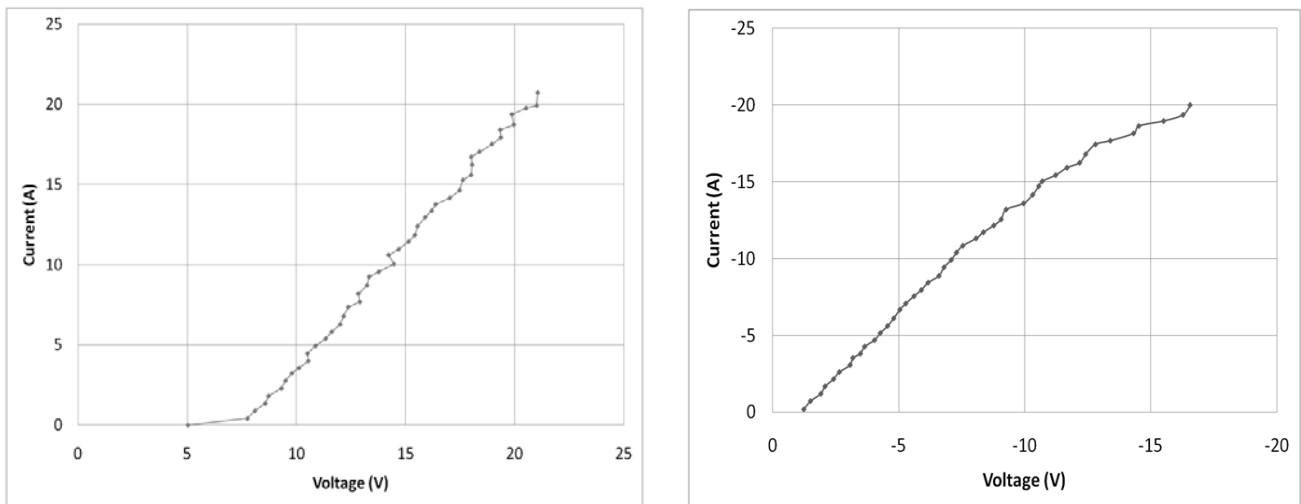
Figure 6. Positive and Negative TLP Waveforms

ESD VOLTAGE CLAMPING

   For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to On Semiconductor Application Notes AND8307/D and AND8308/D.

IEC61000−4−2 Spec.

Level	Test Volt-age (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

IEC61000−4−2 Waveform
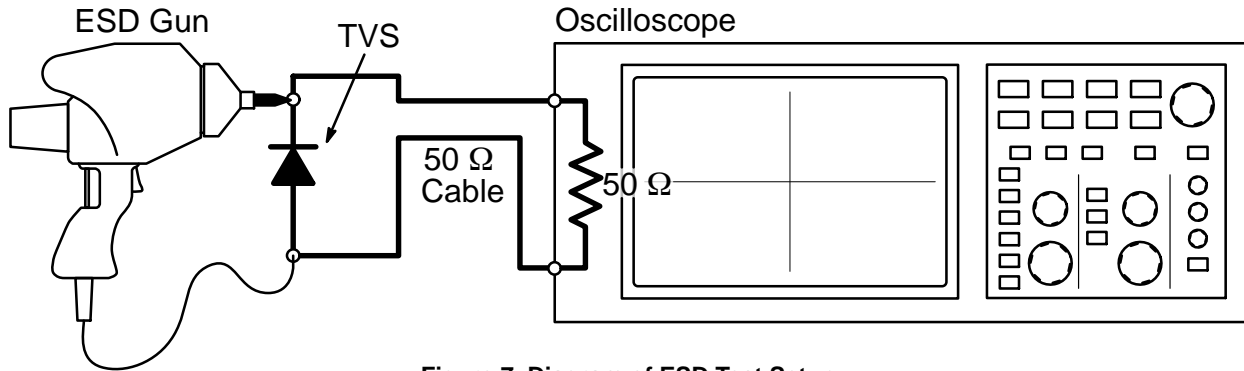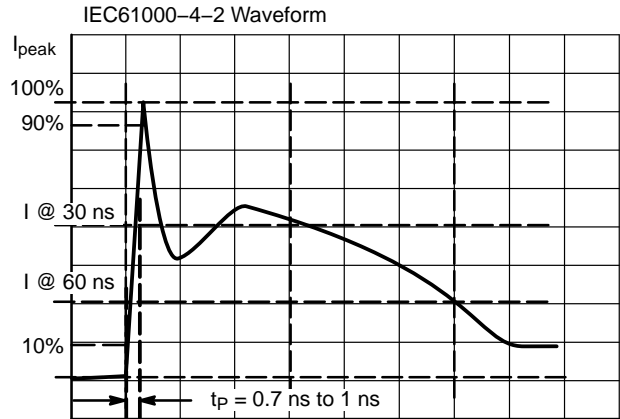
Figure 7. Diagram of ESD Test Setup
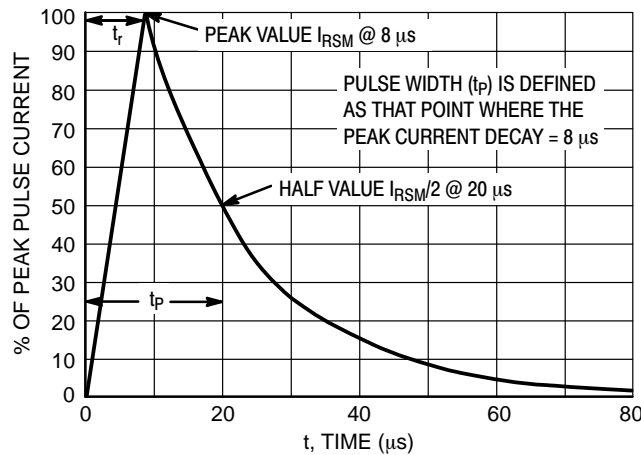
Figure 8. 8 x 20 μs Pulse Waveform
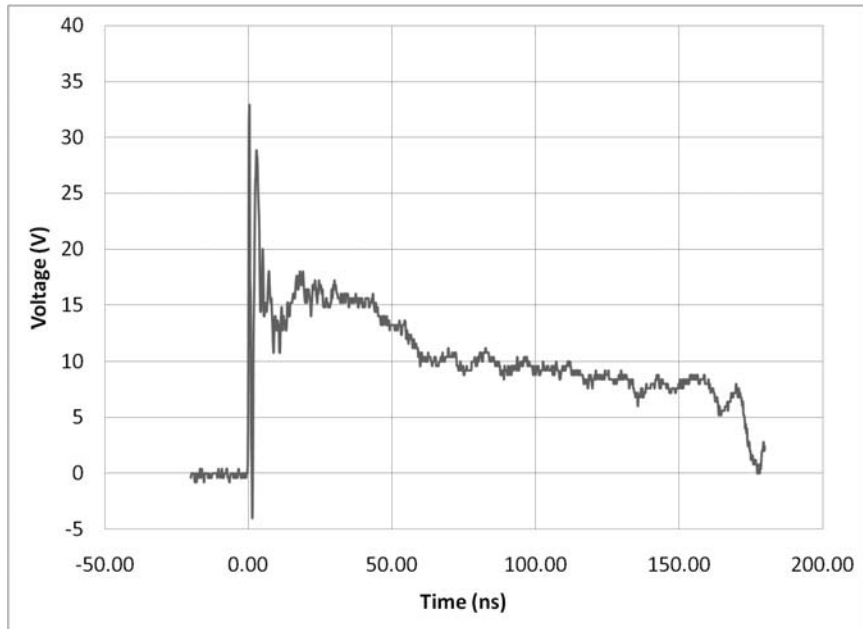
Figure 9. ESD Clamping Voltage +8 kV per IEC6100−4−2 (external to internal pin)
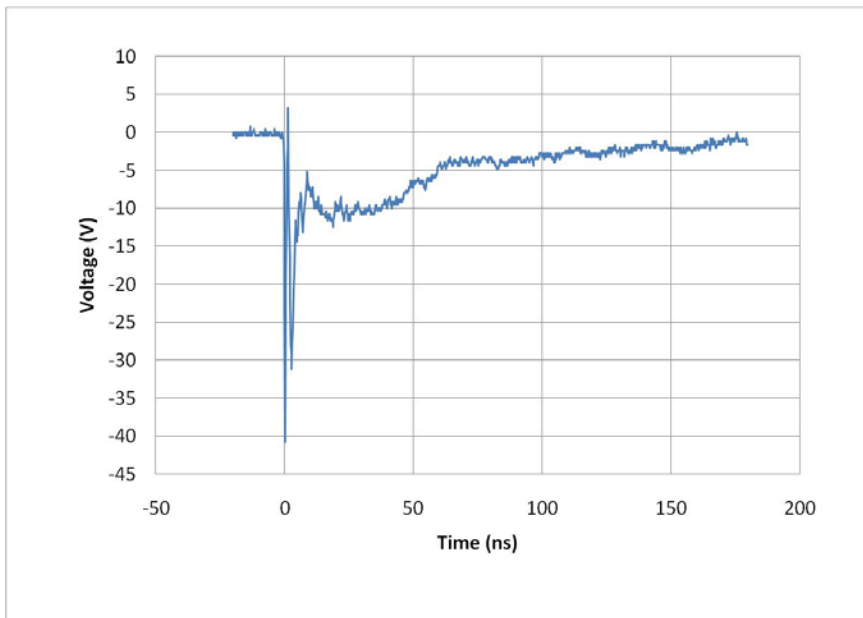
Figure 10. ESD Clamping Voltage −8 kV per IEC6100−4−2 (external to internal pin)
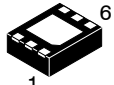
WDFN6 1.6x2.0, 0.5P
CASE 511BV
ISSUE O

DATE 17 MAY 2012

6

1

SCALE 4:1

TOP VIEW

D
A
B
E

PIN ONE
REFERENCE

2X | ⌒ | 0.10 | C

2X | ⌒ | 0.10 | C

DETAIL A
OPTIONAL
CONSTRUCTIONS

L
L
L1

SIDE VIEW

| ∥ | 0.05 | C |

| ⌒ | 0.05 | C |

NOTE 4

DETAIL B
(A3)
A
A1
C SEATING PLANE

DETAIL B
OPTIONAL
CONSTRUCTION

EXPOSED Cu
MOLD CMPD
A3
A1

BOTTOM VIEW

DETAIL A
D2
6X L
1
3
E2
K
6
4
6X b
e

| ⊕ | 0.10 | C | A | B |
| | 0.05 | C | NOTE 3 |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.60	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.40
D	1.60 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.95	1.15
e	0.50 BSC	
K	0.20	---
L	0.15	0.35
L1	---	0.10

**GENERIC
MARKING DIAGRAM***

1
XX M■

XX = Specific Device Code
M = Date Code
■ = Pb–Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, "G" or microdot "■", may or may not be present.

**RECOMMENDED
MOUNTING FOOTPRINT**

1.30
6X 0.43
1.15
2.30
6X 0.36
1
0.50 PITCH

DIMENSIONS: MILLIMETERS
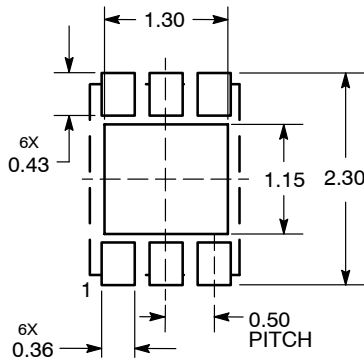
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	WDFN6, 1.6X2.0, 0.5P		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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