# MC74AC273, MC74ACT273

## Octal D Flip-Flop

The MC74AC273/74ACT273 has eight edge-triggered D–type flip–flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip–flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW–to–HIGH clock transition, is transferred to the corresponding flip–flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### Features

- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip–Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- Outputs Source/Sink 24 mA
- ′ACT273 Has TTL Compatible Inputs
- These are Pb–Free Devices
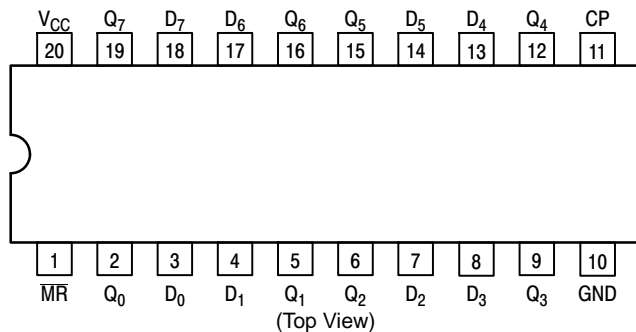


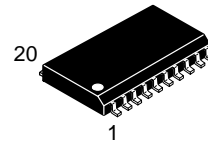**Pinout: 20–Lead Packages Conductors**

### MODE SELECT-FUNCTION TABLE

| Operating Mode | Inputs | | | Outputs |
|---|---|---|---|---|
| | MR | CP | $D_n$ | $Q_n$ |
| Reset (Clear) | L | X | X | L |
| Load ′1′ | H | ⌐ | H | H |
| Load ′0′ | H | ⌐ | L | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

**ON Semiconductor®**

**SOIC–20WB**
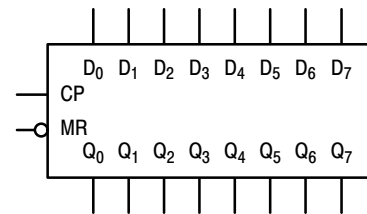**SUFFIX DW**
**CASE 751D**
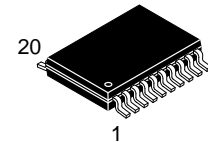
**TSSOP–20**
**SUFFIX DT**
**CASE 948E**

### PIN ASSIGNMENT

| PIN | FUNCTION |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| $\overline{MR}$ | Master Reset |
| CP | Clock Pulse Input |
| $Q_0$–$Q_7$ | Data Outputs |



**Logic Symbol**

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 6 of this data sheet.

# MC74AC273, MC74ACT273
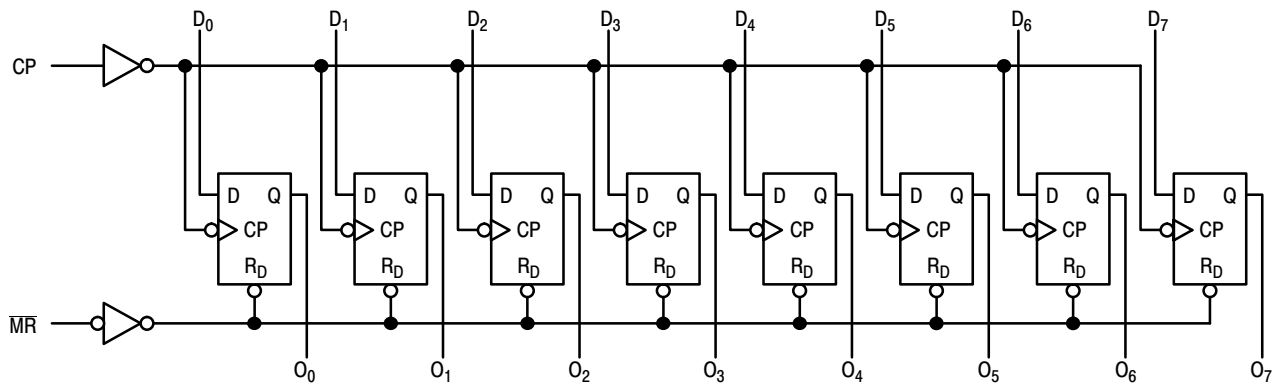


NOTE: That this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Figure 1. Logic Diagram**

**MAXIMUM RATINGS**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | −0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | | −0.5 to $V_{CC}$ +0.5 | V |
| $V_{OUT}$ | DC Output Voltage (Referenced to GND) (Note 1) | | −0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | DC Input Diode Current | | ±20 | mA |
| $I_{OK}$ | DC Output Diode Current | | ±50 | mA |
| $I_{OUT}$ | DC Output Sink/Source Current | | ±50 | mA |
| $I_{CC}$ | DC Supply Current, per Output Pin | | ±50 | mA |
| $I_{GND}$ | DC Ground Current, per Output Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | − 65 to + 150 | °C |
| $T_L$ | Lead temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | 140 | °C |
| $θ_{JA}$ | Thermal Resistance (Note 2) | SOIC<br>TSSOP | 65.8<br>110.7 | °C/W |
| MSL | Moisture Sensitivity | SOIC<br>TSSOP | Level 3<br>Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 30% – 35% | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 3)<br>Machine Model (Note 4)<br>Charged Device Model (Note 5) | > 2000<br>> 200<br>> 1000 | V |
| $I_{Latchup}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 85°C (Note 6) | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. $I_{OUT}$ absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD 51−7.
3. Tested to EIA/JESD22−A114−A.
4. Tested to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A.
6. Tested to EIA/JESD78.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 'AC | 2.0 | 5.0 | 6.0 | V |
| | | 'ACT | 4.5 | 5.0 | 5.5 | |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Ref. to GND) | | 0 | – | $V_{CC}$ | V |
| $t_r$, $t_f$ | Input Rise and Fall Time (Note 7)<br>'AC Devices except Schmitt Inputs | $V_{CC}$ @ 3.0 V | – | 150 | – | ns/V |
| | | $V_{CC}$ @ 4.5 V | – | 40 | – | |
| | | $V_{CC}$ @ 5.5 V | – | 25 | – | |
| $t_r$, $t_f$ | Input Rise and Fall Time (Note 8)<br>'ACT Devices except Schmitt Inputs | $V_{CC}$ @ 4.5 V | – | 10 | – | ns/V |
| | | $V_{CC}$ @ 5.5 V | – | 8.0 | – | |
| $T_A$ | Operating Ambient Temperature Range | | −40 | 25 | 85 | °C |
| $I_{OH}$ | Output Current – High | | – | – | −24 | mA |
| $I_{OL}$ | Output Current – Low | | – | – | 24 | mA |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
7. $V_{IN}$ from 30% to 70% $V_{CC}$; see individual Data Sheets for devices that differ from the typical input rise and fall times.
8. $V_{IN}$ from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

## DC CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | 74AC $T_A$ = +25°C | | 74AC $T_A$ = −40°C to +85°C | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum High Level Input Voltage | 3.0￼4.5￼5.5 | 1.5￼2.25￼2.75 | 2.1￼3.15￼3.85 | 2.1￼3.15￼3.85 | V | $V_{OUT}$ = 0.1 V or $V_{CC}$ − 0.1 V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 3.0￼4.5￼5.5 | 1.5￼2.25￼2.75 | 0.9￼1.35￼1.65 | 0.9￼1.35￼1.65 | V | $V_{OUT}$ = 0.1 V or $V_{CC}$ − 0.1 V |
| $V_{OH}$ | Minimum High Level Output Voltage | 3.0￼4.5￼5.5 | 2.99￼4.49￼5.49 | 2.9￼4.4￼5.4 | 2.9￼4.4￼5.4 | V | $I_{OUT}$ = −50 μA |
| | | 3.0￼4.5￼5.5 | −￼−￼− | 2.56￼3.86￼4.86 | 2.46￼3.76￼4.76 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$￼$I_{OH}$ −12 mA￼−24 mA￼−24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 3.0￼4.5￼5.5 | 0.002￼0.001￼0.001 | 0.1￼0.1￼0.1 | 0.1￼0.1￼0.1 | V | $I_{OUT}$ = 50 μA |
| | | 3.0￼4.5￼5.5 | −￼−￼− | 0.36￼0.36￼0.36 | 0.44￼0.44￼0.44 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$￼$I_{OL}$ 12 mA￼24 mA￼24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | − | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OLD}$ $I_{OHD}$ | †Minimum Dynamic Output Current | 5.5￼5.5 | −￼− | −￼− | 75￼−75 | mA | $V_{OLD}$ = 1.65 V Max￼$V_{OHD}$ = 3.85 V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | − | 8.0 | 80 | μA | $V_{IN}$ = $V_{CC}$ or GND |

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.
NOTE:　Note: $I_{IN}$ and $I_{CC}$ @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V $V_{CC}$.

## AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

| Symbol | Parameter | $V_{CC}$* (V) | 74AC $T_A$ = +25°C $C_L$ = 50 pF | | | 74AC $T_A$ = −40°C to +85°C $C_L$ = 50 pF | | Unit | Figure No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| $f_{max}$ | Maximum Clock Frequency | 3.3￼5.0 | 90￼140 | 125￼175 | −￼− | 75￼125 | −￼− | Mhz | 3–3 |
| $t_{PLH}$ | Propagation Delay Clock to Output | 3.3￼5.0 | 4.0￼3.0 | 7.0￼5.5 | 12.5￼9.0 | 3.0￼2.5 | 14.0￼10.0 | ns | 3–6 |
| $t_{PHL}$ | Propagation Delay Clock to Output | 3.3￼5.0 | 4.0￼3.0 | 7.0￼5.0 | 13.0￼10.0 | 3.5￼2.5 | 14.5￼11.0 | ns | 3–6 |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to Output | 3.3￼5.0 | 4.0￼3.0 | 7.0￼5.0 | 13.0￼10.0 | 3.5￼2.5 | 14.0￼10.5 | ns | 3–6 |

*Voltage Range 3.3 V is 3.3 V ±0.3 V. Voltage Range 5.0 V is 5.0 V ±0.5 V.

## AC OPERATING REQUIREMENTS

| Symbol | Parameter | $V_{CC}$* (V) | 74AC $T_A$ = +25°C $C_L$ = 50 pF | | 74AC $T_A$ = −40°C to +85°C $C_L$ = 50 pF | Unit | Figure No. |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | | |
| $t_s$ | Setup Time, HIGH or LOW Data to CP | 3.3￼5.0 | 3.5￼2.5 | 5.5￼4.0 | 6.0￼4.5 | ns | 3–9 |
| $t_h$ | Hold Time, HIGH or LOW Data to CP | 3.3￼5.0 | −2.0￼−1.0 | 0￼1.0 | 0￼1.0 | ns | 3–9 |
| $t_w$ | Clock Pulse Width HIGH or LOW | 3.3￼5.0 | 3.5￼2.5 | 5.5￼4.0 | 6.0￼4.5 | ns | 3–6 |
| $t_w$ | $\overline{MR}$ Pulse Width HIGH or LOW | 3.3￼5.0 | 2.0￼1.5 | 5.5￼4.0 | 6.0￼4.5 | ns | 3–6 |
| $t_{rec}$ | Recovery Time $\overline{MR}$ to CP | 3.3￼5.0 | 1.5￼1.0 | 3.5￼2.0 | 4.5￼3.0 | ns | 3–9 |

*Voltage Range 3.3 V is 3.3 V ±0.3 V. Voltage Range 5.0 V is 5.0 V ±0.5 V.

## DC CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | 74ACT $T_A$ = +25°C | | 74ACT $T_A$ = –40°C to +85°C | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | Guaranteed Limits | | |
| $V_{IH}$ | Minimum High Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 2.0<br>2.0 | 2.0<br>2.0 | V | $V_{OUT}$ = 0.1 V<br>or $V_{CC}$ – 0.1 V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 0.8<br>0.8 | 0.8<br>0.8 | V | $V_{OUT}$ = 0.1 V<br>or $V_{CC}$ – 0.1 V |
| $V_{OH}$ | Minimum High Level Output Voltage | 4.5<br>5.5 | 4.49<br>5.49 | 4.4<br>5.4 | 4.4<br>5.4 | V | $I_{OUT}$ = –50 µA |
| | | 4.5<br>5.5 | –<br>– | 3.86<br>4.86 | 3.76<br>4.76 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OH}$   –24 mA<br>    –24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 4.5<br>5.5 | 0.001<br>0.001 | 0.1<br>0.1 | 0.1<br>0.1 | V | $I_{OUT}$ = 50 µA |
| | | 4.5<br>5.5 | –<br>– | 0.36<br>0.36 | 0.44<br>0.44 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>   24 mA<br>$I_{OL}$   24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | – | ±0.1 | ±1.0 | µA | $V_I$ = $V_{CC}$, GND |
| $\Delta I_{CCT}$ | Additional Max. $I_{CC}$/Input | 5.5 | 0.6 | – | 1.5 | mA | $V_I$ = $V_{CC}$ – 2.1 V |
| $I_{OLD}$<br>$I_{OHD}$ | †Minimum Dynamic Output Current | 5.5<br>5.5 | –<br>– | –<br>– | 75<br>–75 | mA | $V_{OLD}$ = 1.65 V Max<br>$V_{OHD}$ = 3.85 V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | – | 8.0 | 80 | µA | $V_{IN}$ = $V_{CC}$ or GND |

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

## AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

| Symbol | Parameter | $V_{CC}$* (V) | 74ACT $T_A$ = +25°C $C_L$ = 50 pF | | | 74ACT $T_A$ = –40°C to +85°C $C_L$ = 50 pF | | Unit | Figure No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| $f_{max}$ | Maximum Clock Frequency | 5.0 | 125 | 200 | – | 125 | – | MHz | 3–3 |
| $t_{PHL}$ | Propagation Delay Clock to Output | 5.0 | 3.0 | 6.0 | 10 | 2.5 | 11.0 | ns | 3–6 |
| $t_{PLH}$ | Propagation Delay Clock to Output | 5.0 | 3.0 | 6.5 | 11 | 2.5 | 12.0 | ns | 3–6 |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to Output | 5.0 | 3.0 | 7.0 | 11 | 2.5 | 11.5 | ns | 3–6 |

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## AC OPERATING REQUIREMENTS

| Symbol | Parameter | $V_{CC}$* (V) | 74ACT $T_A$ = +25°C $C_L$ = 50 pF | | 74ACT $T_A$ = –40°C to +85°C $C_L$ = 50 pF | Unit | Figure No. |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | Guaranteed Minimum | | |
| $t_s$ | Setup Time, HIGH or LOW – Data to CP | 5.0 | 3.0 | 4.5 | 5.0 | ns | 3–9 |
| $t_h$ | Hold Time, HIGH or LOW – Data to CP | 5.0 | –2.5 | 2.0 | 2.0 | ns | 3–9 |
| $t_w$ | Clock Pulse Width – HIGH or LOW | 5.0 | 2.5 | 4.0 | 4.5 | ns | 3–6 |
| $t_w$ | $\overline{MR}$ Pulse Width – HIGH or LOW | 5.0 | 2.5 | 4.0 | 4.5 | ns | 3–6 |
| $t_{rec}$ | Recovery Time – $\overline{MR}$ to CP | 5.0 | –1.0 | 2.0 | 3.0 | ns | 3–6 |

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## CAPACITANCE

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0 V |
| $C_{PD}$ | Power Dissipation Capacitance | 50 | pF | $V_{CC}$ = 5.0 V |

# MC74AC273, MC74ACT273

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC74AC273DWG | SOIC−20WB (Pb−Free) | 38 Units / Rail |
| MC74AC273DWR2G | SOIC−20WB (Pb−Free) | 1000 / Tape & Reel |
| MC74AC273DTR2G | TSSOP−20 (Pb−Free) | 2500 / Tape & Reel |
| MC74ACT273DWG | SOIC−20WB (Pb−Free) | 38 Units / Rail |
| MC74ACT273DWR2G | SOIC−20WB (Pb−Free) | 1000 / Tape & Reel |
| MC74ACT273DTR2G | TSSOP−20 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS

**SOIC−20WB**  **TSSOP−20**



```
AC273
AWLYYWWG
```

```
AC
273
ALYW■
   ■
```

```
ACT273
AWLYYWWG
```

```
ACT
273
ALYW■
   ■
```
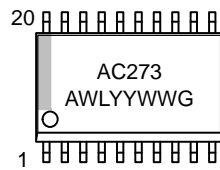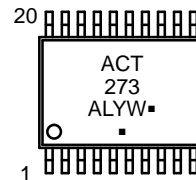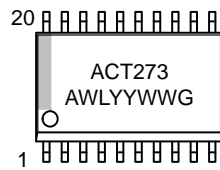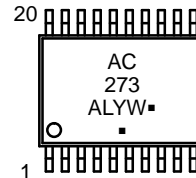
A          = Assembly Location
WL, L    = Wafer Lot
YY, Y    = Year
WW, W   = Work Week
G or ■    = Pb−Free Package
(Note: Microdot may be in either location)

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**onsemi**
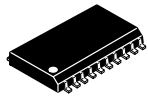
**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015

**SCALE 1:1**

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
| --- | --- | --- |
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0 ° | 7 ° |

**RECOMMENDED SOLDERING FOOTPRINT\***

20X
0.52

20X
1.30

11.00

1.27
PITCH
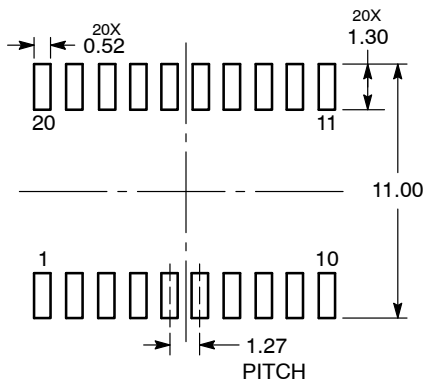
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM\***

XXXXXXXXXX
XXXXXXXXXX
AWLYYWWG
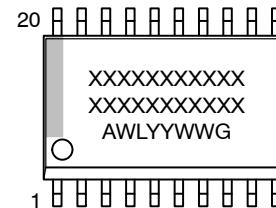
| | |
| --- | --- |
| XXXXX | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

\*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**TSSOP−20 WB**
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
|-----|------|------|------|------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

**SECTION N−N**

**DETAIL E**

**SEATING PLANE**

**SOLDERING FOOTPRINT**

7.06

0.65 PITCH

16X 0.36

16X 1.26

DIMENSIONS: MILLIMETERS

## GENERIC MARKING DIAGRAM*

XXXX
XXXX
ALYW▪

A  = Assembly Location
L  = Wafer Lot
Y  = Year
W  = Work Week
▪  = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪ ", may or may not be present.

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|---|---|---|---|
| DESCRIPTION: | TSSOP−20 WB | | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

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