MOSFET – N & P-Channel, POWERTRENCH®

20 V

FDC6420C

	V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
Q1	20 V	70 mΩ @ 4.5 V	3.0 A
		95 mΩ @ 2.5 V	
Q2	−20 V	125 mΩ @ −4.5 V	−2.2 A
		190 mΩ @ −2.5 V	

General Description

These N & P−Channel MOSFETs are produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize on−state resistance and yet maintain superior switching performance.

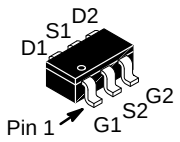
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO−8 and TSSOP−8 packages are impractical.

Features

- *Q1* 3.0 A, 20 V
  - $R_{DS(on)}$ = 70 mΩ @ V_{GS} = 4.5 V
  - $R_{DS(on)}$ = 95 mΩ @ V_{GS} = 2.5 V
- *Q2* −2.2 A, −20 V
  - $R_{DS(on)}$ = 125 mΩ @ V_{GS} = −4.5 V
  - $R_{DS(on)}$ = 190 mΩ @ V_{GS} = −2.5 V
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- SUPERSOT™ −6 Package: Small Footprint (72% Smaller than SO−8); Low Profile (1 mm Thick)
- This is a Pb−Free Device

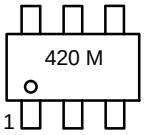
Applications

- DC−DC Converter
- Load Switch
- LCD Display Inverter



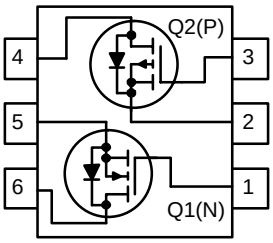
TSOT23 6−Lead
(SUPERSOT−6)
CASE 419BL

MARKING DIAGRAM



420 = Device Code
M = Date Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

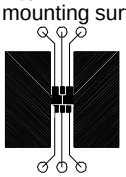
Symbol	Parameter		Q1	Q2	Unit
V_{DSS}	Drain−Source Voltage		20	−20	V
V_{GSS}	Gate−Source Voltage		±12	±12	V
I_D	Drain Current – Continuous (Note 1a)		3.0	−2.2	A
	Drain Current – Pulsed		12	−6	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.96		W
		(Note 1b)	0.9		
		(Note 1c)	0.7		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

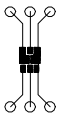
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	60	°C/W

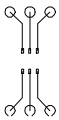
1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 130°C/W when mounted on a 0.125 in^2 pad of 2 oz. copper.



b. 140°C/W when mounted on a 0.004 in^2 pad of 2 oz. copper.



c. 180°C/W when mounted on a minimum pad.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain–Source Breakdown Voltage	Q1	V_{GS} = 0 V, I_D = 250 μA	20	–	–	V
		Q2	V_{GS} = 0 V, I_D = −250 μA	−20	–	–	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	Q1	I_D = 250 μA, Ref. to 25°C	–	13	–	mV/°C
		Q2	I_D = −250 μA, Ref. to 25°C	–	−11	–	
I_{DSS}	Zero Gate Voltage Drain Current	Q1	V_{DS} = 16 V, V_{GS} = 0 V	–	–	1	μA
		Q2	V_{DS} = −16 V, V_{GS} = 0 V	–	–	−1	
I_{GSSF}	Gate–Body Leakage, Forward	Q1	V_{GS} = 12 V, V_{DS} = 0 V	–	–	100	nA
		Q2	V_{GS} = 12 V, V_{DS} = 0 V	–	–	100	
I_{GSSR}	Gate–Body Leakage, Reverse	Q1	V_{GS} = −12 V, V_{DS} = 0 V	–	–	−100	nA
		Q2	V_{GS} = −12 V, V_{DS} = 0 V	–	–	−100	
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	Q1	V_{DS} = V_{GS}, I_D = 250 μA	0.5	0.9	1.5	V
		Q2	V_{DS} = V_{GS}, I_D = −250 μA	−0.6	−1.0	−1.5	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	Q1	I_D = 250 μA, Ref. to 25°C	–	−3	–	mV/°C
		Q2	I_D = −250 μA, Ref. to 25°C	–	−3	–	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.) (continued)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 2)							
$R_{DS(on)}$	Static Drain–Source On–Resistance	Q1	V_{GS} = 4.5 V, I_D = 3.0 A	–	50	70	mΩ
			V_{GS} = 2.5 V, I_D = 2.5 A	–	66	95	
			V_{GS} = 4.5 V, I_D = 3.0 A, T_J = 125°C	–	71	106	
		Q2	V_{GS} = −4.5 V, I_D = −2.2 A	–	100	125	
			V_{GS} = −2.5 V, I_D = −1.8 A	–	145	190	
			V_{GS} = −4.5 V, I_D = −2.2 A, T_J = 125°C	–	137	184	
$I_{D(on)}$	On–State Drain Current	Q1	V_{GS} = 4.5 V, V_{DS} = 5 V	12	–	–	A
		Q2	V_{GS} = −4.5 V, V_{DS} = −5 V	−6	–	–	
g_{FS}	Forward Transconductance	Q1	V_{DS} = 5 V, I_D = 2.5 A	–	10	–	S
		Q2	V_{DS} = −5 V, I_D = −2.0 A	–	6	–	
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	Q1	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	–	324	–	pF
		Q2	V_{DS} = −10 V, V_{GS} = 0 V, f = 1.0 MHz	–	337	–	
C_{oss}	Output Capacitance	Q1	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	–	82	–	
		Q2	V_{DS} = −10 V, V_{GS} = 0 V, f = 1.0 MHz	–	88	–	
C_{rss}	Reverse Transfer Capacitance	Q1	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	–	42	–	
		Q2	V_{DS} = −10 V, V_{GS} = 0 V, f = 1.0 MHz	–	51	–	
SWITCHING CHARACTERISTICS (Note 2)							
$t_{d(on)}$	Turn–On Delay Time	Q1	For *Q1*: V_{DS} = 10 V, I_{DS} = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω For *Q2*: V_{DS} = −10 V, I_{DS} = −1 A, V_{GS} = −4.5 V, R_{GEN} = 6 Ω	–	5	10	ns
		Q2		–	9	18	
t_r	Turn–On Rise Time	Q1		–	7	14	
		Q2		–	12	22	
$t_{d(off)}$	Turn–Off Delay Time	Q1		–	13	23	
		Q2		–	10	20	
t_f	Turn–Off Fall Time	Q1		–	1.6	3	
		Q2		–	5	10	
Q_g	Total Gate Charge	Q1	For *Q1*: V_{DS} = 10 V, I_{DS} = 3.0 A, V_{GS} = 4.5 V For *Q2*: V_{DS} = −10 V, I_{DS} = −2.2 A, V_{GS} = −4.5 V	–	3.3	4.6	nC
		Q2		–	3.7	–	
Q_{gs}	Gate–Source Charge	Q1		–	0.95	–	
		Q2		–	0.68	–	
Q_{gd}	Gate–Drain Charge	Q1		–	0.7	–	
		Q2		–	1.3	–	
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain–Source Diode Forward Current	Q1		–	–	0.8	A
		Q2		–	–	−0.8	
V_{SD}	Drain–Source Diode Forward Voltage	Q1	V_{GS} = 0 V, I_S = 0.8 A (Note 2)	–	0.7	1.2	V
		Q2	V_{GS} = 0 V, I_S = 0.8 A (Note 2)	–	−0.8	−1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS: N−CHANNEL

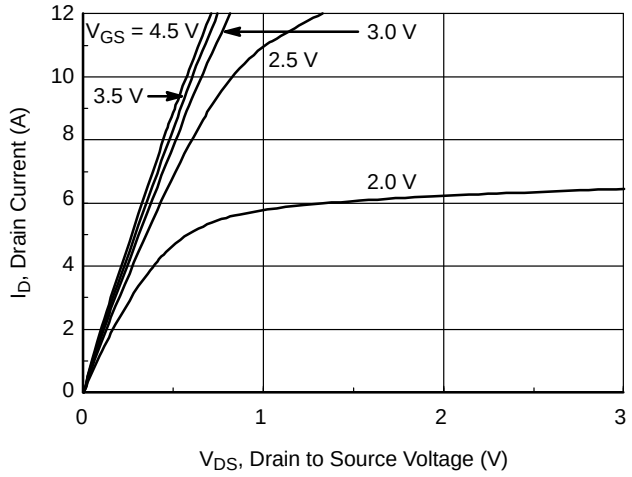


Figure 1. On−Region Characteristics

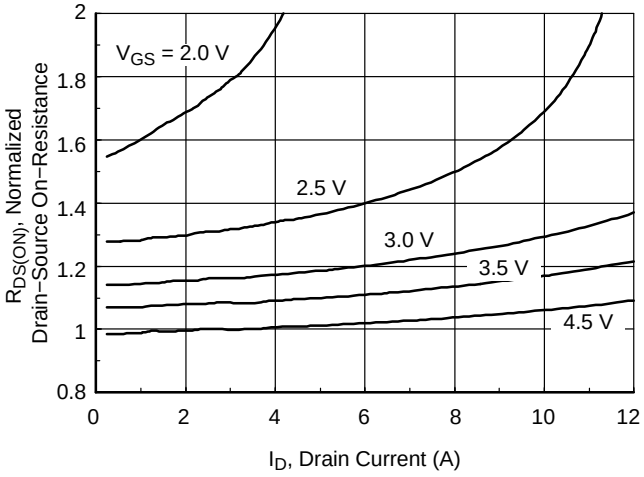


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

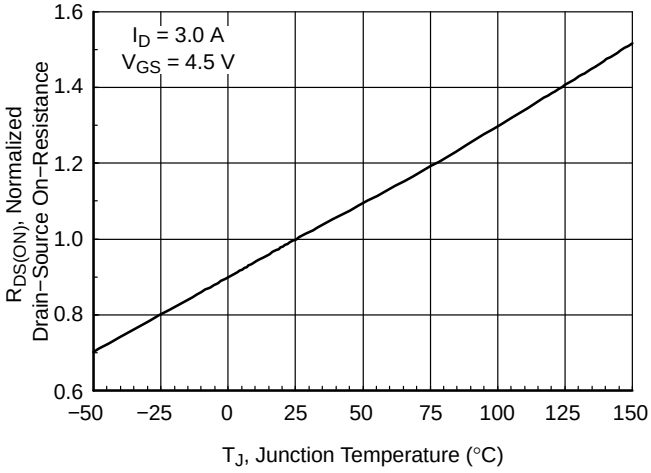


Figure 3. On−Resistance Variation with Temperature

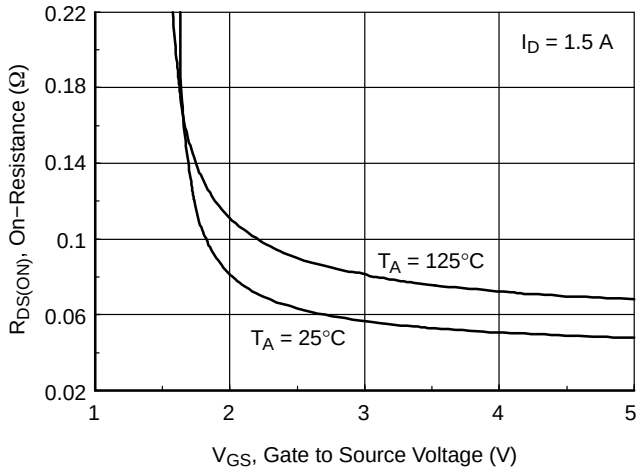


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

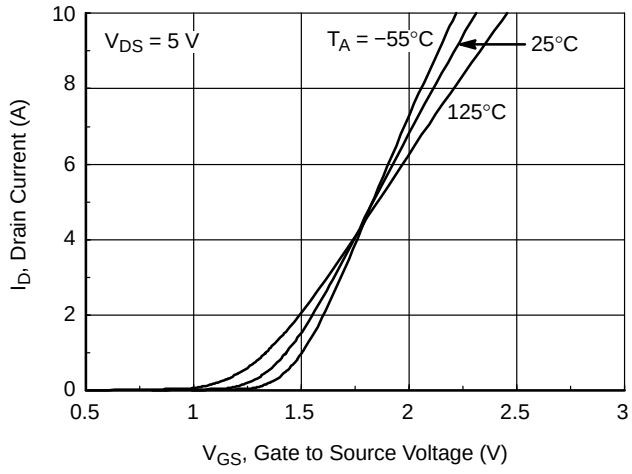


Figure 5. Transfer Characteristics

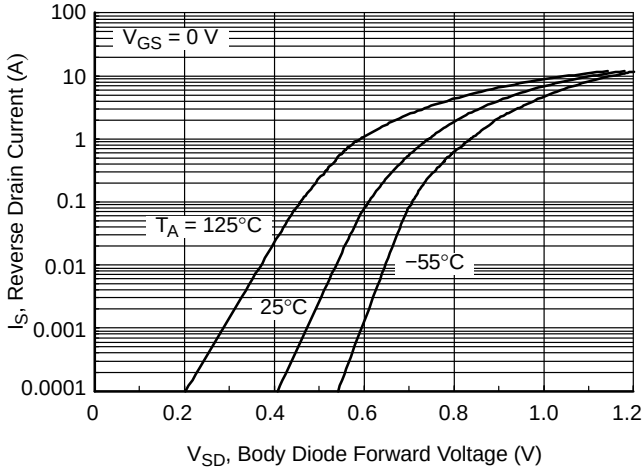


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: N−CHANNEL (continued)

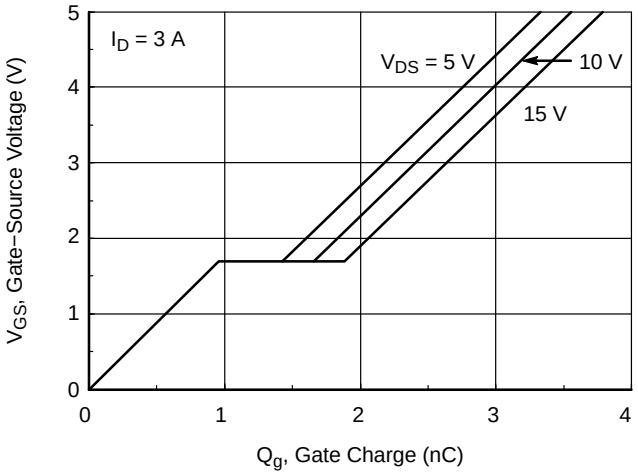


Figure 7. Gate Charge Characteristics

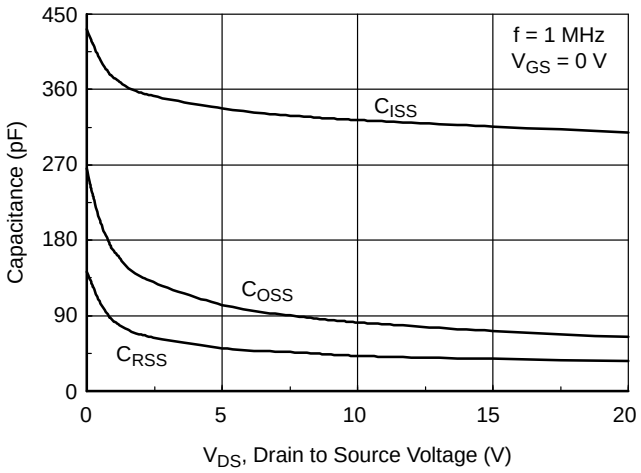


Figure 8. Capacitance Characteristics

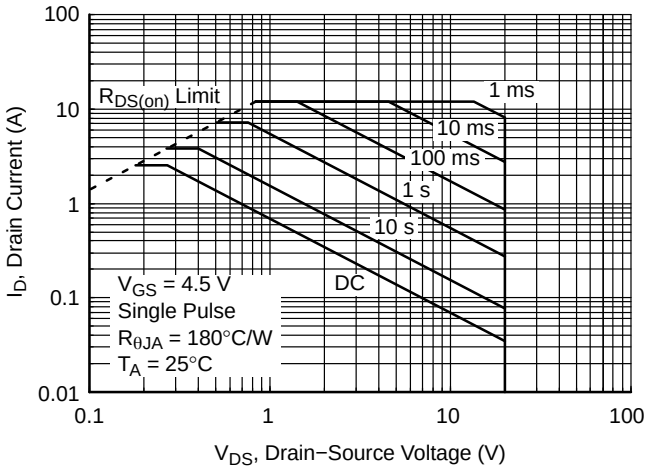


Figure 9. Maximum Safe Operating Area

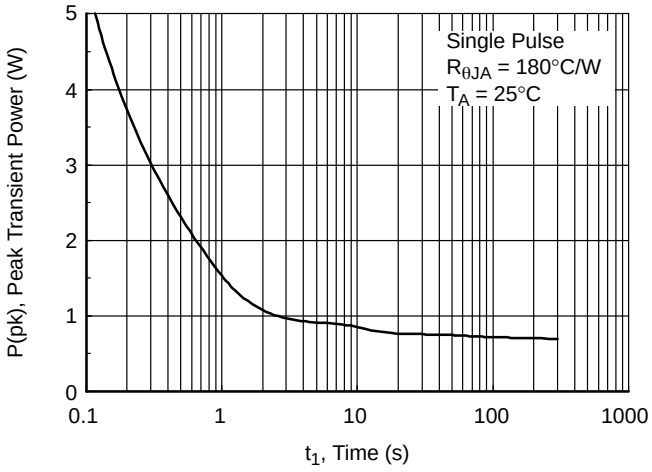


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS: P−CHANNEL

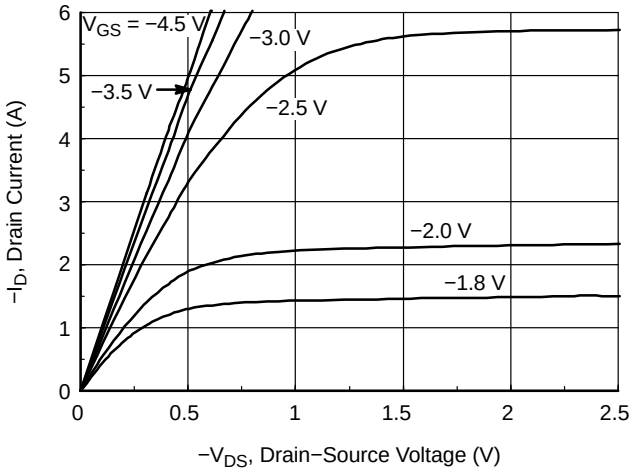


Figure 11. On−Region Characteristics

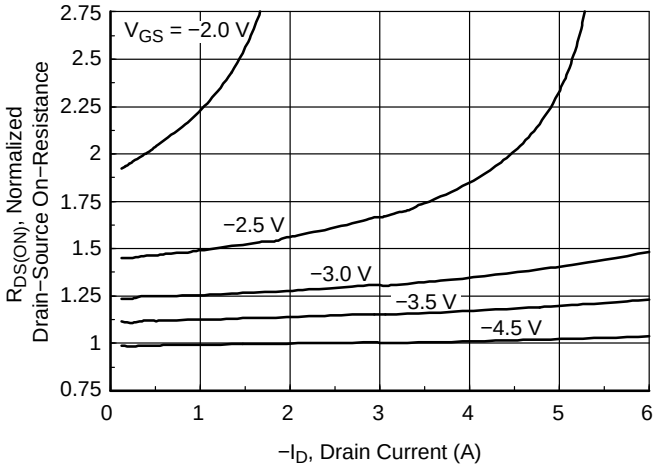


Figure 12. On−Resistance Variation with Drain Current and Gate Voltage

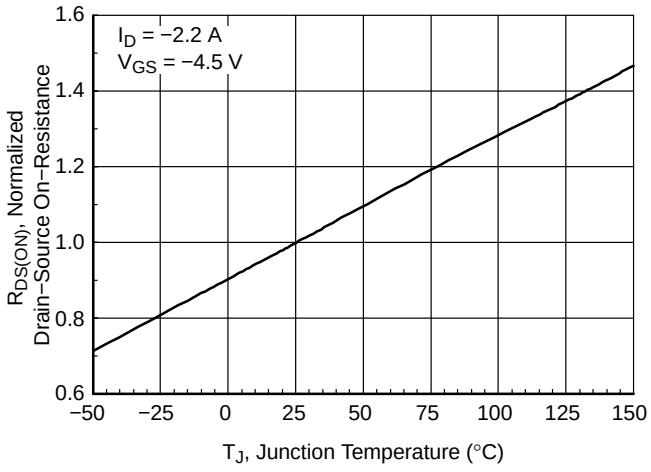


Figure 13. On−Resistance Variation with Temperature

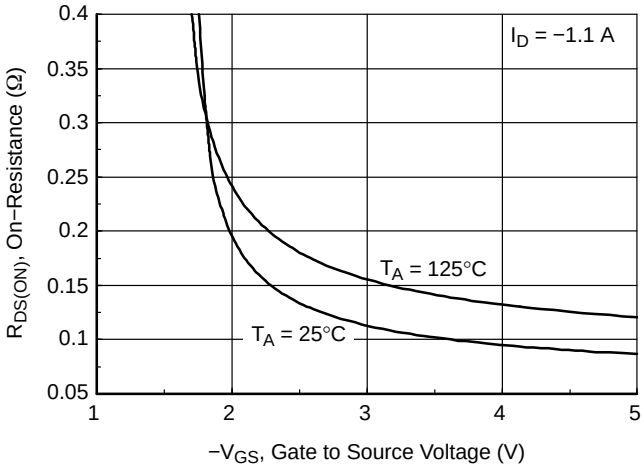


Figure 14. On−Resistance Variation with Gate−to−Source Voltage

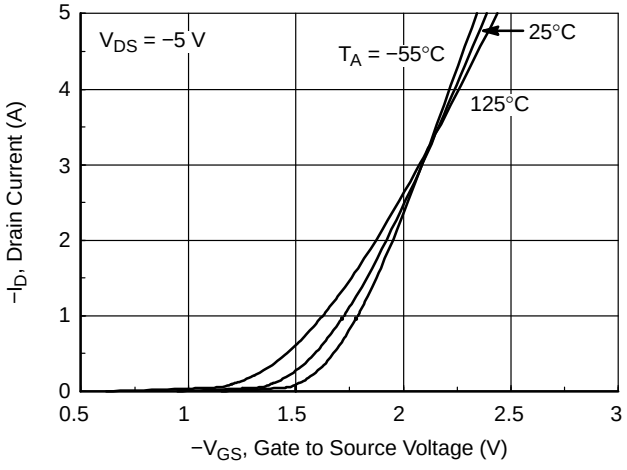


Figure 15. Transfer Characteristics

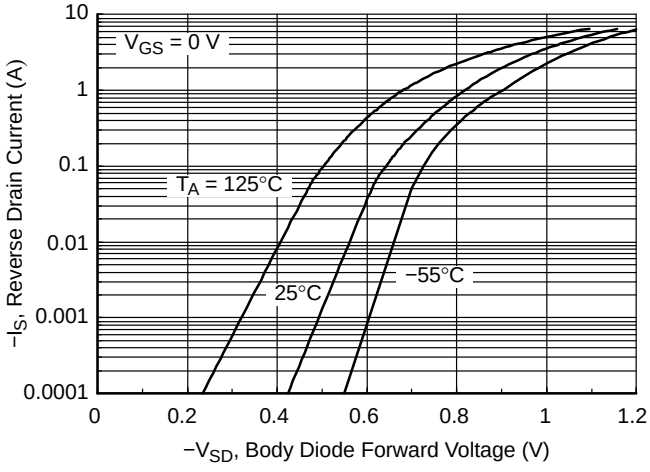


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: P−CHANNEL (continued)

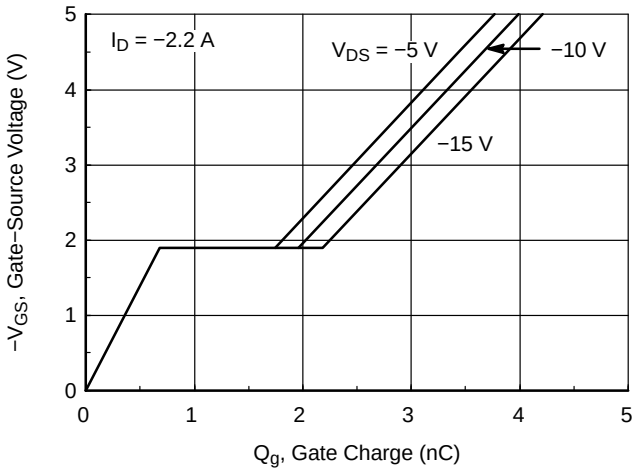


Figure 17. Gate Charge Characteristics

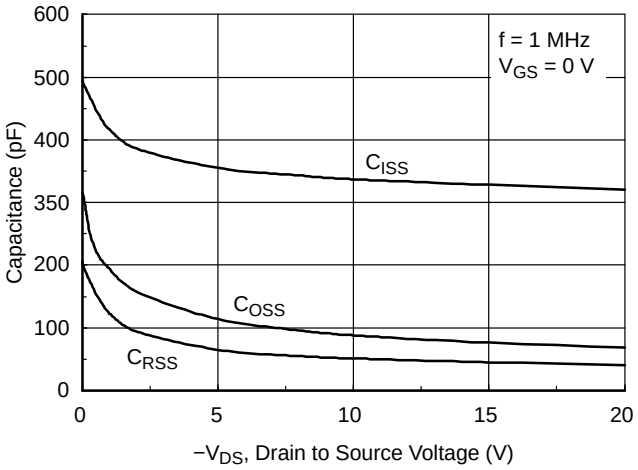


Figure 18. Capacitance Characteristics

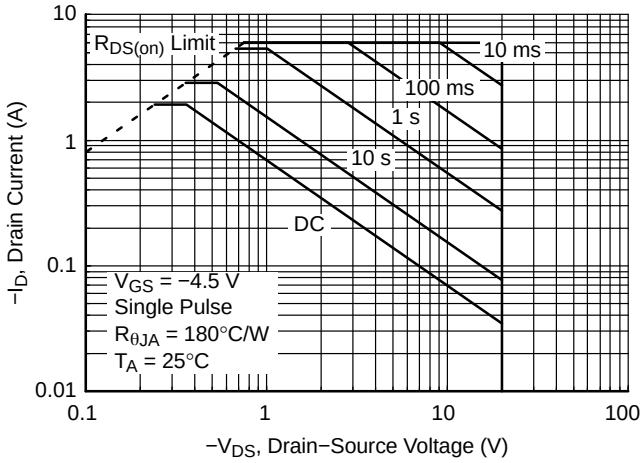


Figure 19. Maximum Safe Operating Area

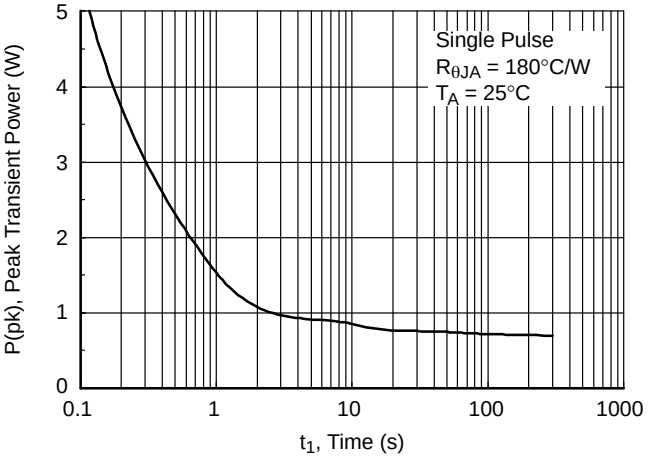


Figure 20. Single Pulse Maximum Power Dissipation

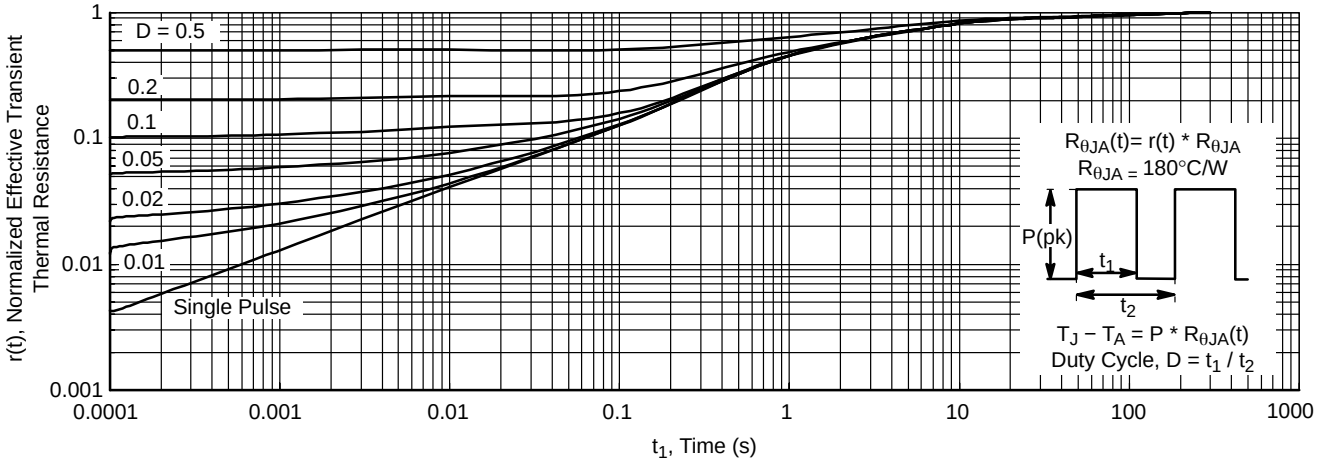


Figure 21. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

PACKAGE MARKING AND ORDERING INFORMATION

Device Order Number	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDC6420C	420	TSOT23 6−Lead (SUPERSOT−6) (Pb−Free)	7”	8 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

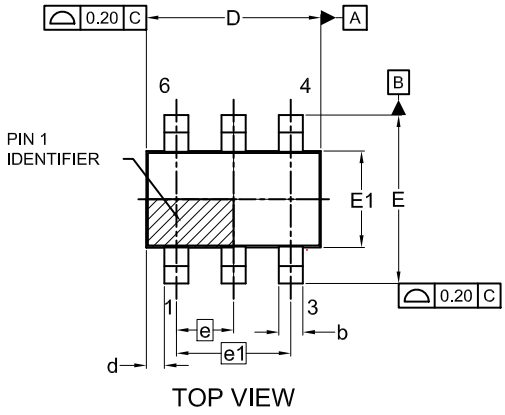
ON Semiconductor®

1

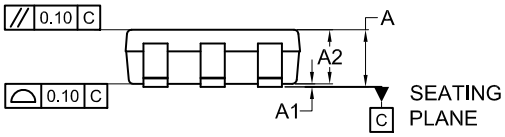
SCALE 2:1

TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

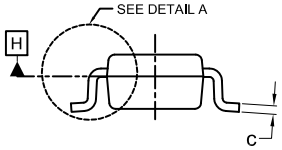


TOP VIEW

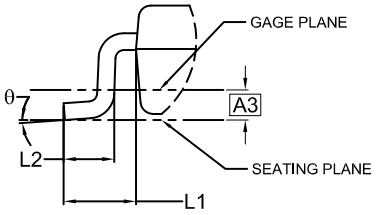


FRONT VIEW

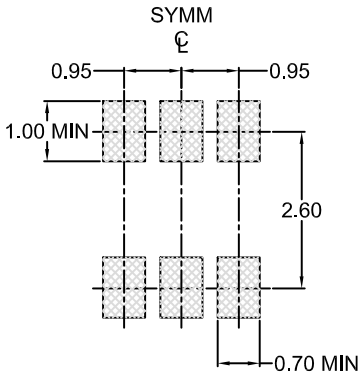
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

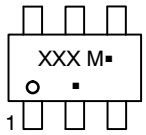
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSOT23 6−Lead**	**PAGE 1 OF 1**

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