

# M62333P/FP, M62338P/FP

R03DS0038EJ0500

## 8-bit 3ch I<sup>2</sup>C BUS D/A Converter with Buffer Amplifiers

Rev.5.00

Jun 03, 2011

### Description

The M62333/M62338 is an integrated circuit semiconductor of CMOS structure with 3 channels of built in D/A converters with output buffer operational amplifiers.

The input is 2-wires serial method is used for the transfer format of digital data to allow connection with a microcomputer with minimum wiring.

The output buffer operational amplifier employs AB class output circuit with sync and source drive capacity of 1.0 mA or more, and it operates in the whole voltage range from V<sub>CC</sub> to ground.

The M62333 and the M62338 differ only in their slave address.

### Features

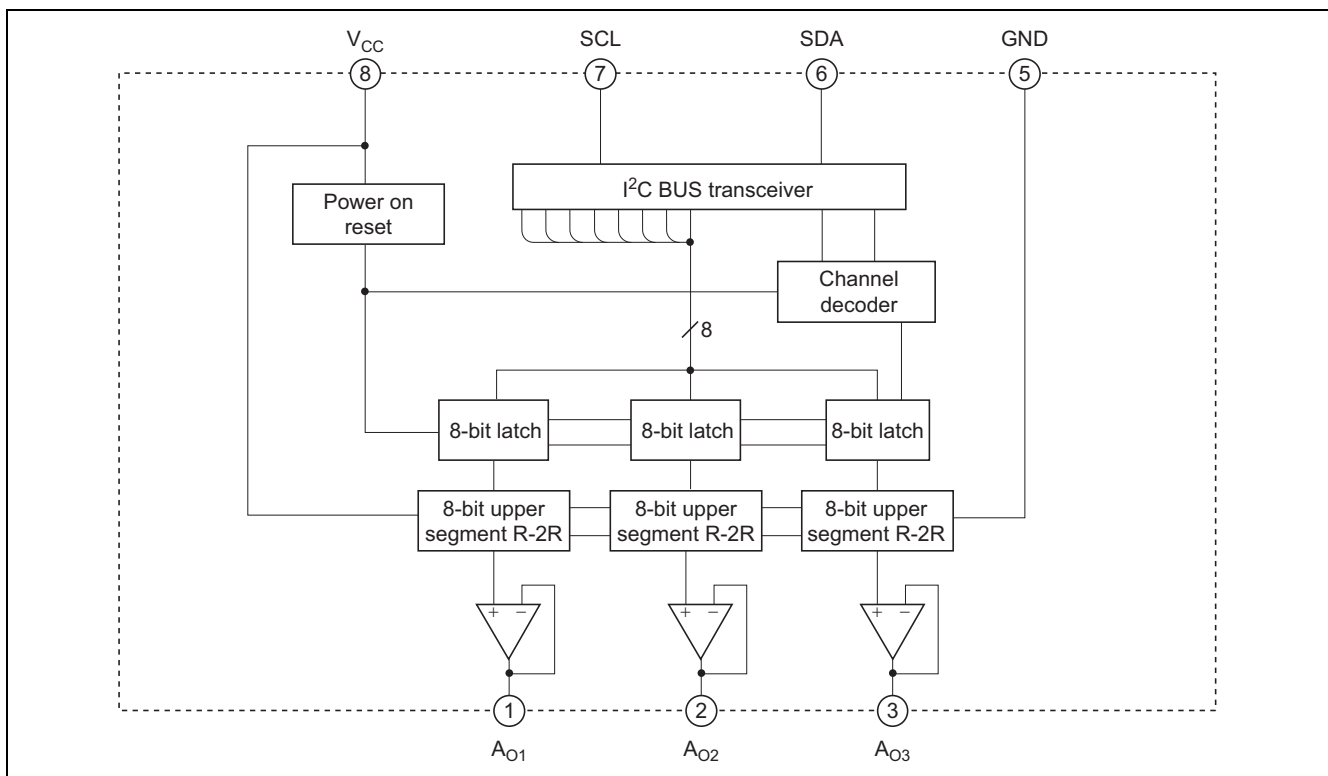
- Digital data transfer format: I<sup>2</sup>C BUS serial data method
- Output buffer operational amplifier: It operates in the whole voltage range from V<sub>CC</sub> to ground.
- High output current drive capacity: ±1.0 mA over

### Application

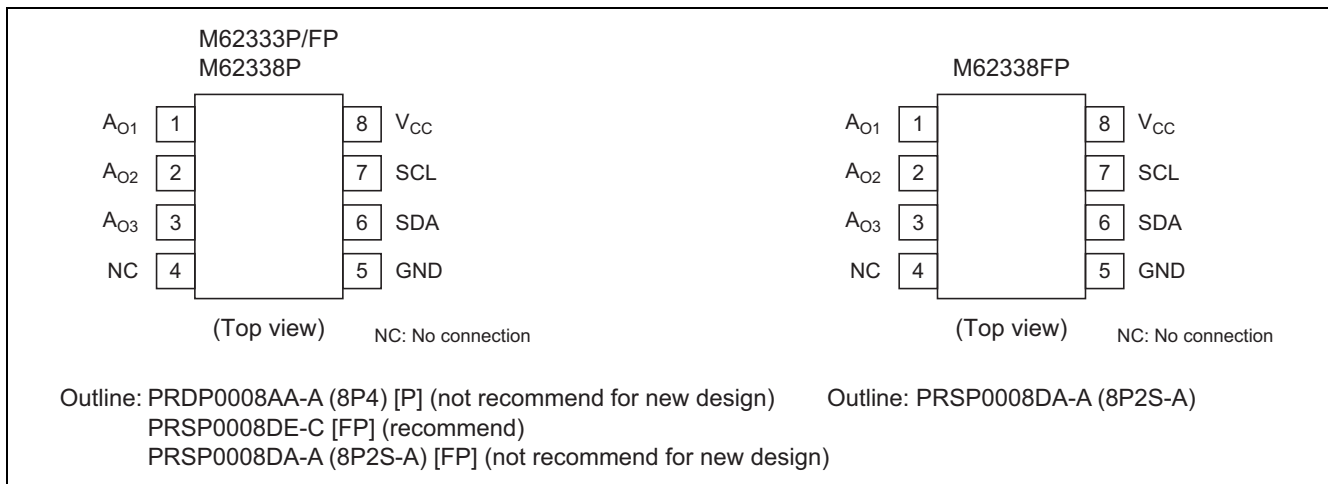
Conversion from digital data to analog control data for home-use and industrial equipment.

Signal gain control or automatic adjustment of Display-monitor or CTV.

### Block Diagram



## Pin Arrangement



## Pin Description

Pin No.	Pin Name	Function
6	SDA	Serial data input terminal
7	SCL	Serial clock input terminal
1	A <sub>01</sub>	8-bit resolution D/A converter output terminal
2	A <sub>02</sub>	
3	A <sub>03</sub>	
8	V <sub>CC</sub>	Power supply terminal
5	GND	GND terminal

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	-0.3 to 7.0	V
Input voltage	$V_{in}$	-0.3 to $V_{CC} + 0.3$	V
Output voltage	$V_O$	-0.3 to $V_{CC} + 0.3$	V
Power dissipation	$P_d$	417 (P) / 272 (FP)	mW
Operating temperature	$T_{opr}$	-20 to 85	°C
Storage temperature	$T_{stg}$	-40 to 125	°C

## Electrical Characteristics

( $V_{CC} = +5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_a = -20\text{ to }85^\circ\text{C}$  unless otherwise noted)

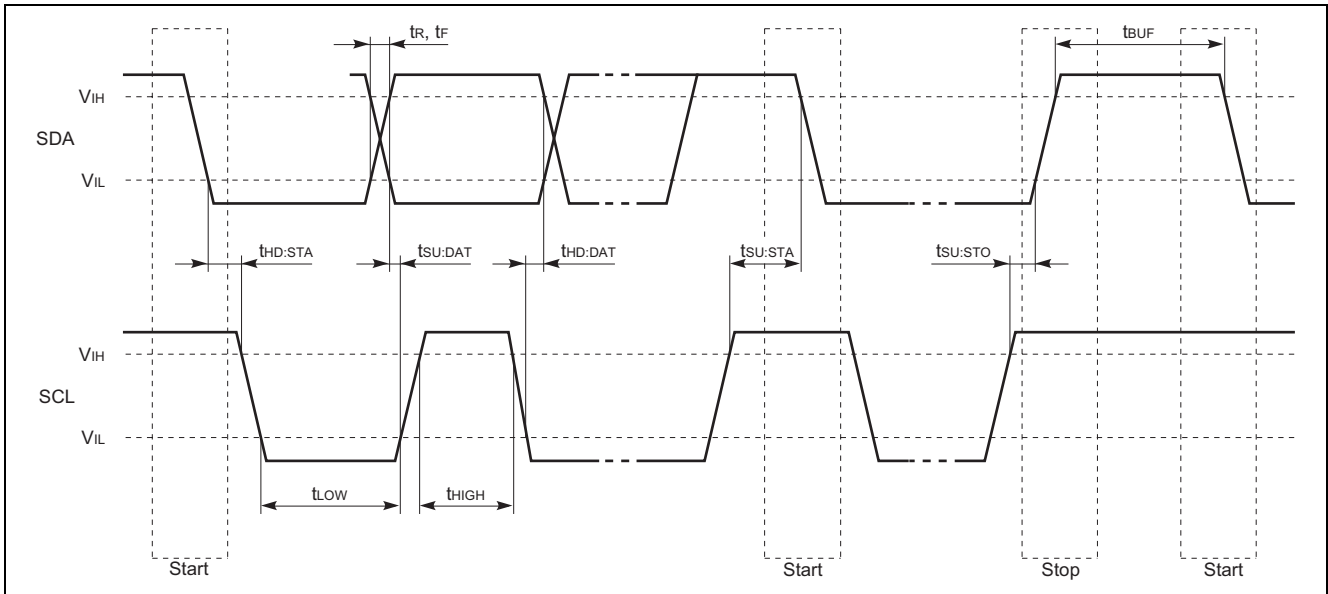
Item	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Supply voltage	$V_{CC}$	2.7	5.0	5.5	V	
Supply current	$I_{CC}$	0	0.9	2.7	mA	CLK = 500 kHz operation, $I_{AO} = 0\ \mu\text{A}$ Data: 6Ah (at maximum current)
		0	0.6	1.8	mA	SDA = SCL = GND, $I_{AO} = 0\ \mu\text{A}$
Output low voltage (SDA)	$V_{OL}$	—	—	0.4	V	$I_{sink} = 3\text{ mA}$
Input leak current	$I_{ILK}$	-10	—	10	$\mu\text{A}$	$V_{IN} = 0\text{ to }V_{CC}$
Input low voltage	$V_{IL}$	—	—	$0.2 V_{CC}$	V	
Input high voltage	$V_{IH}$	$0.8 V_{CC}$	—	—	V	
Buffer amplifier output voltage range	$V_{AO}$	0.1	—	$V_{CC} - 0.1$	V	$I_{AO} = \pm 100\ \mu\text{A}$
		0.2	—	$V_{CC} - 0.2$	V	$I_{AO} = \pm 500\ \mu\text{A}$
Buffer amplifier output drive range	$I_{AO}$	-1.0	—	1.0	mA	Upper side saturation voltage = 0.3 V Lower side saturation voltage = 0.2 V
Differential nonlinearity	$S_{DL}$	-1.0	—	1.0	LSB	$V_{CC} = 5.12\text{ V}$ (20 mV/LSB) without load ( $I_{AO} = 0$ )
Nonlinearity	$S_L$	-1.5	—	1.5	LSB	
Zero code error	$S_{ZERO}$	-2.0	—	2.0	LSB	
Full scale error	$S_{FULL}$	-2.0	—	2.0	LSB	
Output capacitance load	$C_O$	—	—	0.1	$\mu\text{F}$	
Buffer amplifier output impedance	$R_O$	—	5.0	—	$\Omega$	

## I<sup>2</sup>C BUS Line Characteristics

Item	Symbol	Min	Max	Unit
SCL clock frequency	$t_{SCL}$	0	100	kHz
Time the bus must be free before a new transmission can start	$t_{BUF}$	4.7	—	$\mu$ s
Hold time START condition (After this period, the first clock pulse is generated)	$t_{HD:STA}$	4.0	—	$\mu$ s
Low period of the clock	$t_{LOW}$	4.7	—	$\mu$ s
High period of the clock	$t_{HIGH}$	4.0	—	$\mu$ s
Set-up time for START condition (Only relevant for a repeated START condition)	$t_{SU:STA}$	4.7	—	$\mu$ s
Hold time DATA	$t_{HD:DAT}$	0	—	$\mu$ s
Set-up time DATA	$t_{SU:DAT}$	250	—	ns
Rise time of both SDA and SCL lines	$t_R$	—	1000	ns
Fall time of both SDA and SCL lines	$t_F$	—	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	—	$\mu$ s

Note: Transmitter must internally provide at least a hold time to bridge the undefined region (300 ns Max) of the falling edge of SCL.

### Timing Chart



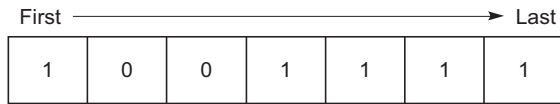
## I<sup>2</sup>C BUS Format

STA	Slave address	W	A	Sub address	A	DAC data	A	STP
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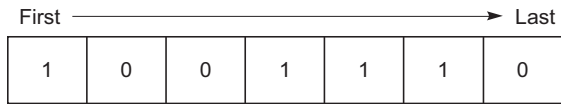
Note: STA: start condition, A: affirmation bit, W: write (SDA = Low), STP: stop condition

- Slave address

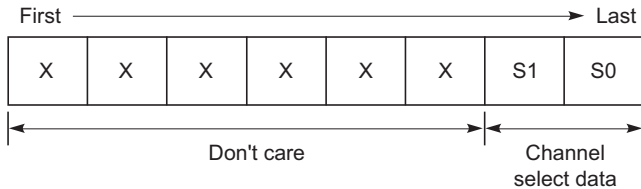
M62333



M62338



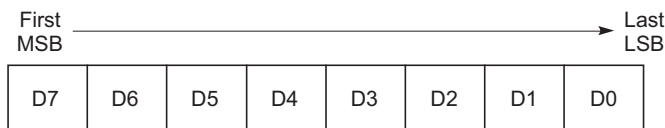
- Sub address



Channel select data

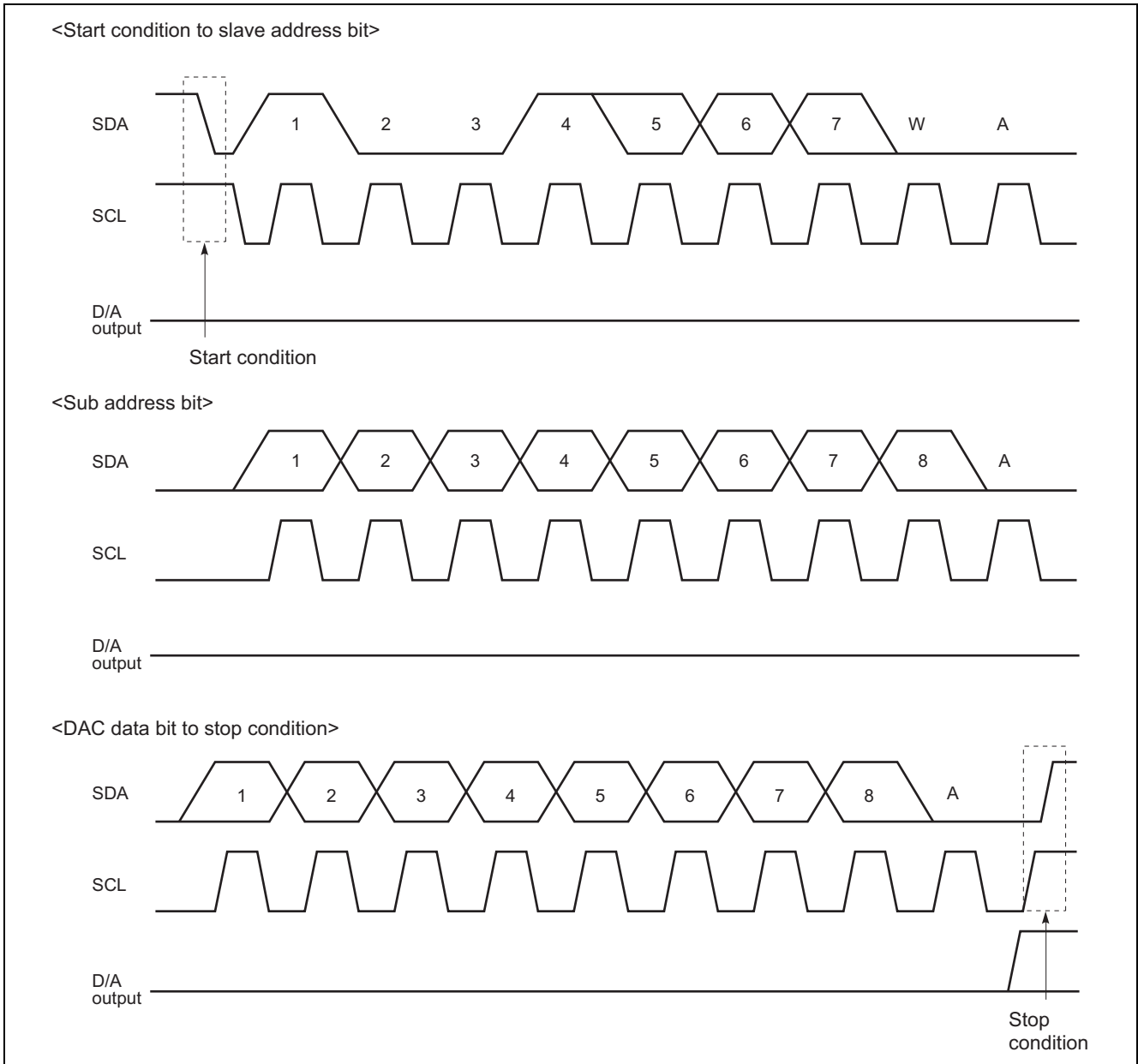
S1	S0	Channel Selection
0	0	ch1 selection
0	1	ch2 selection
1	0	ch3 selection
1	1	Don't care

- DAC data



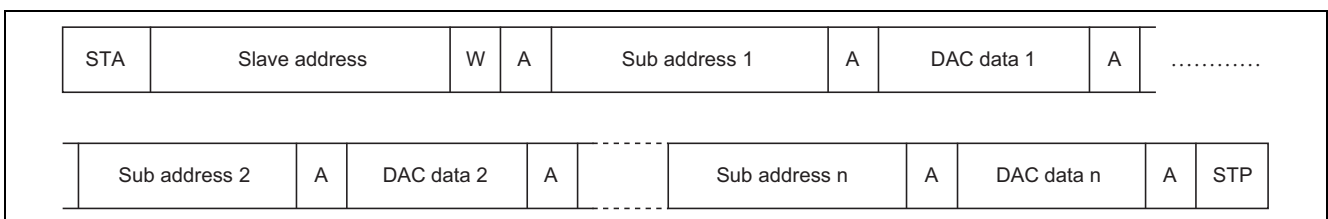
D7	D6	D5	D4	D3	D2	D1	D0	DAC output
0	0	0	0	0	0	0	0	$V_{CC} / 256 \times 1$
0	0	0	0	0	0	0	1	$V_{CC} / 256 \times 2$
0	0	0	0	0	0	1	0	$V_{CC} / 256 \times 3$
0	0	0	0	0	0	1	1	$V_{CC} / 256 \times 4$
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	$V_{CC} / 256 \times 255$
1	1	1	1	1	1	1	1	$V_{CC}$

### Timing Chart (Model)



- Start condition With SCL at High, SDA line goes from High to Low
- Stop condition With SCL at High, SDA line goes from Low to High  
(Under normal circumstances, SDA is changed when SCL is Low)
- Acknowledge bit The receiving IC has to pull down SDA line whenever receive slave data.  
(The transmitting IC releases the SDA line just then transmit 8-bit data.)

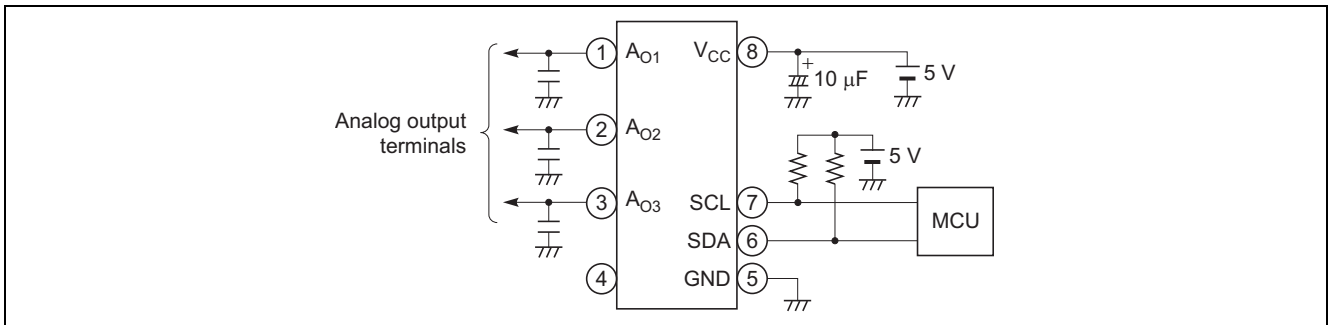
### Digital Data Formats



## Precaution for Use

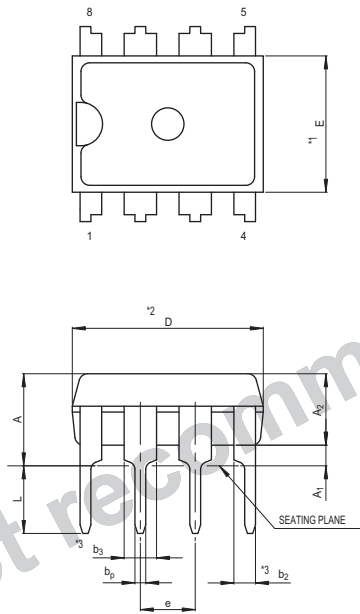
- Supply voltage terminal ( $V_{CC}$ ) is also used for D/A converter upper reference voltage setting. If ripple or spike is input this terminal, accuracy of D/A conversion is down. So, when use this device, please connect capacitor among  $V_{CC}$  to GND for stable D/A conversion.
- This IC's output amplifier has an advantage to capacitive load. So it's no problem at device action when connect capacitor (0.1  $\mu\text{F}$  Max) among output to GND for every noise eliminate.
- Purchase of Renesas's I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components an I<sup>2</sup>C system, provided that the system conforms to I<sup>2</sup>C Standard Specification as defined by Philips.

## Application Example



Package Dimensions

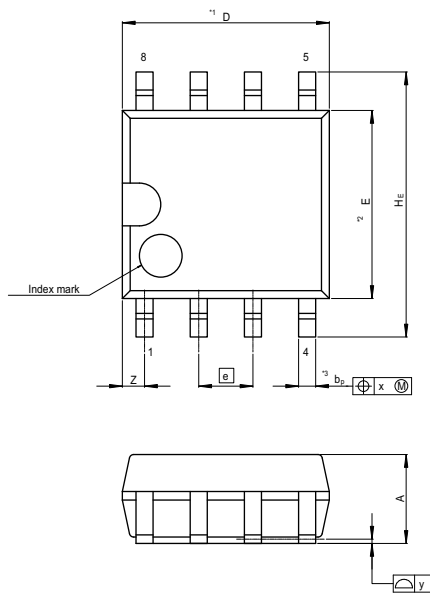
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP8-6.3x8.84-2.54	PRDP0008AA-A	8P4	0.5g



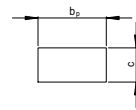
NOTE)  
 1. DIMENSIONS \*\*1\* AND \*\*2\* DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	7.32	7.62	7.92
D	8.7	8.9	9.1
E	6.15	6.3	6.45
A	—	—	4.5
A1	0.51	—	—
A2	—	3.3	—
bp	0.4	0.5	0.6
b2	0.9	1.0	1.3
b3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

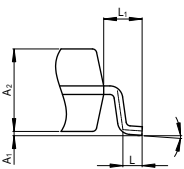
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x4.85-1.27	PRSP0008DE-C	—	0.1g



NOTE)  
 1. DIMENSIONS \*\*1\* (Nom)\* AND \*\*2\* DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section (Ni/Pd/Au plating)

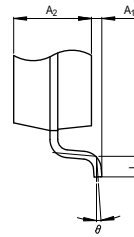
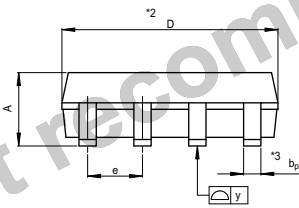
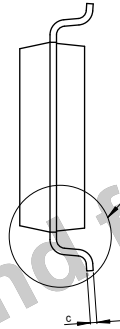
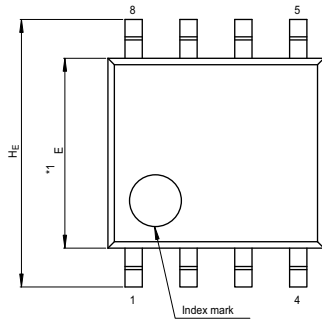


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.65	4.85	5.05
E	4.2	4.4	4.6
A2	—	1.85	—
A1	0.00	0.1	0.20
A	—	—	2.03
bp	0.34	0.4	0.46
b1	—	—	—
c	0.15	0.20	0.25
c1	—	—	—
θ	0°	—	8°
HE	5.7	6.2	6.5
Ⓧ	1.12	1.27	1.42
x	—	—	0.12
y	—	—	0.10
Z	—	—	0.75
L	0.25	0.45	0.65
L1	—	0.90	—



M62333P/FP, M62338P/FP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x5-1.27	PRSP0008DA-A	8P2S-A	0.07g



NOTE)  
 1. DIMENSIONS \*\*1\* AND \*\*2\* DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A <sub>2</sub>	—	1.5	—
A <sub>1</sub>	0.05	—	—
A	—	—	1.9
b <sub>p</sub>	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H <sub>E</sub>	5.9	6.2	6.5
e	1.12	1.27	1.42
y	—	—	0.1
L	0.2	0.4	0.6

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