RAA730500
Monolithic Programmable Analog IC

R02DS0008EJ0120
Rev.1.20
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Overview

The RAA730500 is a monolithic programmable analog IC with a range of on-chip circuits such as configurable amplifiers, a synchronous detection amplifier, a general-purpose operational amplifier, D/A converters, and a temperature sensor, allowing the RAA730500 to be used as an analog front-end device for processing minute sensor signals. The RAA730500 uses a Serial Peripheral Interface (SPI) to allow external devices to control each on-chip circuit, enabling a more compact package and a reduction in the number of control pins. The compact package used by the RAA730500—a 48-pin LQFP—in turns enables a more compact set design.

Features

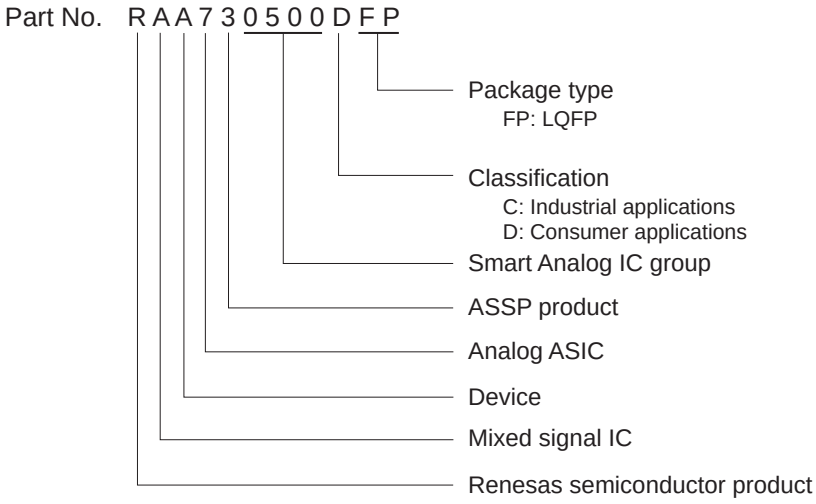
- On-chip configurable amplifier × 3 ch
- On-chip synchronous detection amplifier × 1 ch
- On-chip general-purpose operational amplifier × 1 ch
- On-chip low-pass filter × 1 ch
- On-chip high-pass filter × 1 ch
- On-chip D/A converter × 4 ch
- On-chip variable output voltage regulator × 1 ch
- On-chip reference voltage generator × 1 ch
- On-chip temperature sensor × 1 ch
- On-chip SPI × 1 ch
- Includes a low-current mode.
- Operating voltage range: 3.0 V ≤ V_{DD} ≤ 5.5 V
- Operating temperature range: -40°C ≤ T_A ≤ 105°C
- Package: 48-pin plastic LQFP (fine pitch) (7 × 7)

Applications

- Home appliances
- Industrial equipment
- Healthcare equipment

Ordering Information

Pin count	Package	Part Number
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	RAA730500CFP, RAA730500DFP



How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, electronic circuits.

- To gain a general understanding of functions:
  →Read this manual in the order of the CONTENTS.
- To check the revised points :
  →The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what: " field.

Conventions

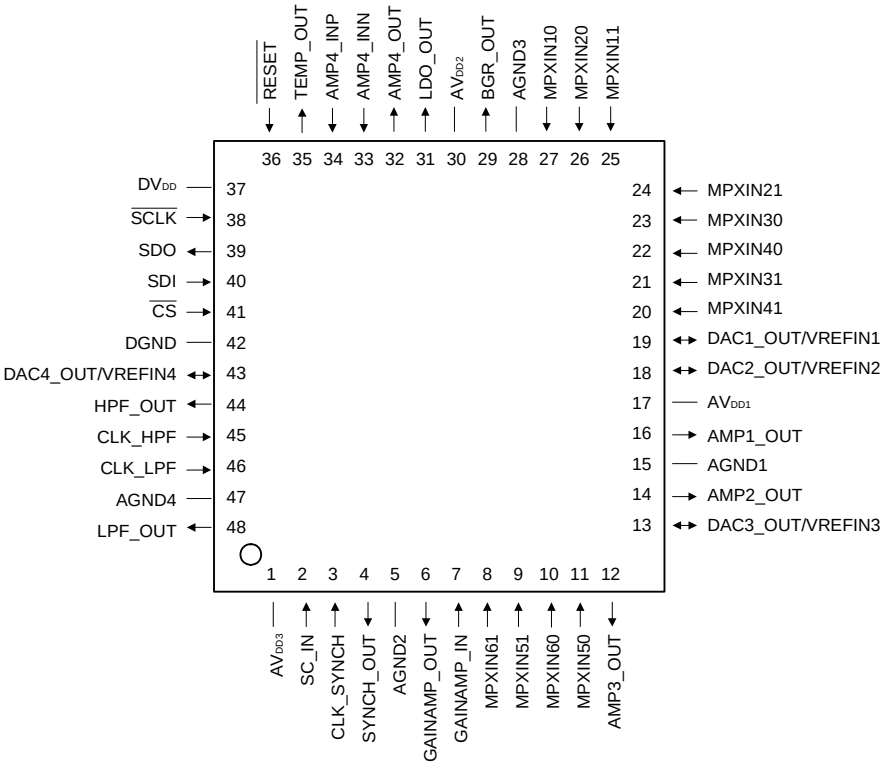
Data significance	: Higher digits on the left and lower digits on the right
Active low representations	: $\overline{\text{xxx}}$ (overscore over pin and signal name)
Note	: Footnote for item marked with Note in the text
Caution	: Information requiring particular attention
Remark	: Supplementary information
Numerical representations	: Binary ...xxxx or xxxxB Decimal ...xxxx Hexadecimal ...xxxxH

Contents

1. Pin Configuration

1.1 Pin Layout

48-pin plastic LQFP (fine pitch) (7 × 7)



Cautions 1. Make the potential of AGND1, AGND2, AGND3, AGND4, and DGND the same.

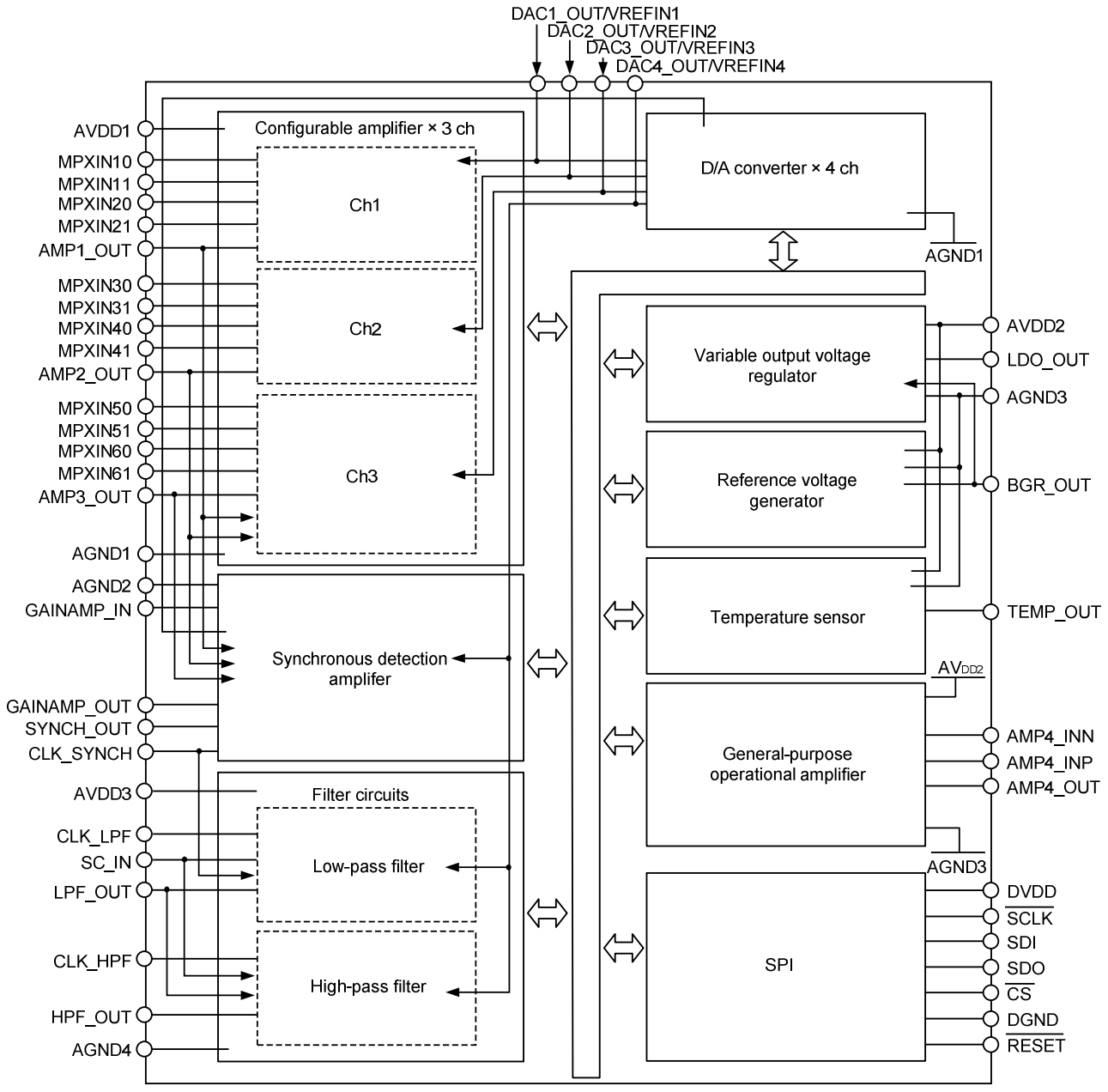
2. Make the potential of AV_{DD1}, AV_{DD2}, AV_{DD3}, and DV_{DD} the same.

3. Connect the LDO_OUT pin to AGND3 via a capacitor (4.7 µF: recommended).

4. Connect the BGR_OUT pin to AGND3 via a capacitor (0.1 µF: recommended).

5. Connect the DAC4_OUT/VREFIN4 pin to AGND1 via a capacitor (470 pF: recommended).

1.2 Block Diagram



1.3 Pin Functions

Table 1-1. Pin Functions (1/2)

Pin No.	Pin Name	I/O	Pin Functions
1	AV_{DD3}	–	Power supply pin for low-pass filter and high-pass filter
2	SC_IN	Input	Input pin for filter signal processing
3	CLK_SYNCH	Input	Pin for inputting synchronous detector control clock
4	SYNCH_OUT	Output	Synchronous detector output pin
5	AGND2	–	GND pin for synchronous detection amplifier
6	GAINAMP_OUT	Output	Output pin for synchronous detection amplifier
7	GAINAMP_IN	Input	Synchronous detection amplifier input pin
8	MPXIN61	Input	Multiplexer 6 input pin 1 (Configurable amplifier Ch3 input pin1 (+))
9	MPXIN51	Input	Multiplexer 5 input pin 1 (Configurable amplifier Ch3 input pin1 (–))
10	MPXIN60	Input	Multiplexer 6 input pin 0 (Configurable amplifier Ch3 input pin0 (+))
11	MPXIN50	Input	Multiplexer 5 input pin 0 (Configurable amplifier Ch3 input pin0 (–))
12	AMP3_OUT	Output	Configurable amplifier Ch3 output pin
13	DAC3_OUT/ VREFIN3	Input/ output	D/A converter Ch3 output pin/configurable amplifier Ch3 reference voltage input pin
14	AMP2_OUT	Output	Configurable amplifier Ch2 output pin
15	AGND1	–	GND pin for configurable amplifiers Ch1 to Ch3
16	AMP1_OUT	Output	Configurable amplifier Ch1 output pin
17	AV_{DD1}	–	Power supply pin for configurable amplifiers Ch1 to Ch3
18	DAC2_OUT/ VREFIN2	Input/ output	D/A converter Ch2 output pin/configurable amplifier Ch2 reference voltage input pin
19	DAC1_OUT/ VREFIN1	Input/ output	D/A converter Ch1 output pin/configurable amplifier Ch1 reference voltage input pin
20	MPXIN41	Input	Multiplexer 4 input pin 1 (Configurable amplifier Ch2 input pin 1 (+))
21	MPXIN31	Input	Multiplexer 3 input pin 1 (Configurable amplifier Ch2 input pin 1 (–))
22	MPXIN40	Input	Multiplexer 4 input pin 0 (Configurable amplifier Ch2 input pin 0 (+))
23	MPXIN30	Input	Multiplexer 3 input pin 0 (Configurable amplifier Ch2 input pin 0 (–))
24	MPXIN21	Input	Multiplexer 2 input pin 1 (Configurable amplifier Ch1 input pin 1 (+))
25	MPXIN11	Input	Multiplexer 1 input pin 1 (Configurable amplifier Ch1 input pin 1 (–))
26	MPXIN20	Input	Multiplexer 2 input pin 0 (Configurable amplifier Ch1 input pin 0 (+))
27	MPXIN10	Input	Multiplexer 1 input pin 0 (Configurable amplifier Ch1 input pin 0 (–))
28	AGND3	–	GND pin for variable output voltage regulator, general-purpose operational amplifier and reference voltage generator
29	BGR_OUT	Output	Reference voltage generator output pin
30	AV_{DD2}	–	Power supply pin for variable output voltage regulator, reference voltage generator, general-purpose operational amplifier and D/A converter
31	LDO_OUT	Output	Variable output voltage regulator output pin
32	AMP4_OUT	Output	General-purpose operational amplifier output pin
33	AMP4_INN	Input	Pin for inputting inverted signal to general-purpose operational amplifier
34	AMP4_INP	Input	Pin for inputting non-inverted signal to general-purpose operational amplifier
35	TEMP_OUT	Output	Temperature sensor output pin

Table 1-1. Pin Functions (2/2)

Pin No.	Pin Name	I/O	Pin Functions
36	$\overline{\text{RESET}}$	Input	External reset input pin
37	DV_{DD}	–	Power supply pin for SPI
38	$\overline{\text{SCLK}}$	Input	Serial clock input pin for SPI
39	SDO	Output	Serial data output pin for SPI
40	SDI	Input	Serial data input pin for SPI
41	$\overline{\text{CS}}$	Input	Chip select input pin for SPI
42	DGND	–	GND pin for SPI
43	DAC4_OUT/ VREFIN4	Input/ output	D/A converter Ch4 output pin and pin for inputting reference voltage to synchronous detection amplifier, low-pass filter, and high-pass filter
44	HPF_OUT	Output	High-pass filter output pin
45	CLK_HPF	Input	Pin for inputting high-pass filter control clock
46	CLK_LPF	Input	Pin for inputting low-pass filter control clock
47	AGND4	–	GND pin for low-pass filter and high-pass filter
48	LPF_OUT	Output	Low-pass filter output pin

1.4 Connection of Unused Pins

Table 1-2. Connection of Unused Pins

Pin Name	I/O	Recommended Connection of Unused Pins
SC_IN	Input	Directly connect to AGND4.
CLK_SYNCH	Input	Leave open.
SYNCH_OUT	Output	
GAINAMP_OUT	Output	
GAINAMP_IN	Input	Directly connect to AGND2.
MPXIN61	Input	Directly connect to AGND1.
MPXIN51	Input	
MPXIN60	Input	
MPXIN50	Input	
AMP3_OUT	Output	Leave open.
DAC3_OUT/VREFIN3	Input/output	
AMP2_OUT	Output	
AMP1_OUT	Output	
DAC2_OUT/VREFIN2	Input/output	
DAC1_OUT/VREFIN1	Input/output	
MPXIN41	Input	Directly connect to AGND1.
MPXIN31	Input	
MPXIN40	Input	
MPXIN30	Input	
MPXIN21	Input	
MPXIN11	Input	
MPXIN20	Input	
MPXIN10	Input	
AMP4_OUT	Output	Leave open.
AMP4_INN	Input	Directly connect to AGND3.
AMP4_INP	Input	
TEMP_OUT	Output	Leave open.
$\overline{\text{SCLK}}$	Input	
SDO	Output	
SDI	Input	
$\overline{\text{CS}}$	Input	
DAC4_OUT/VREFIN4	Input/output	
HPF_OUT	Output	
CLK_HPF	Input	
CLK_LPF	Input	
LPF_OUT	Output	
LDO_OUT	Output	
BGR_OUT	Output	
$\overline{\text{RESET}}$	Input	Connect to DV_{DD} directly or via a resistor.

1.5 Pin I/O Circuits

Figure 1-1. Pin I/O Circuit Type (1/4)

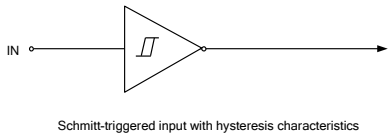
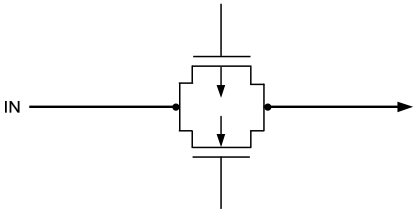
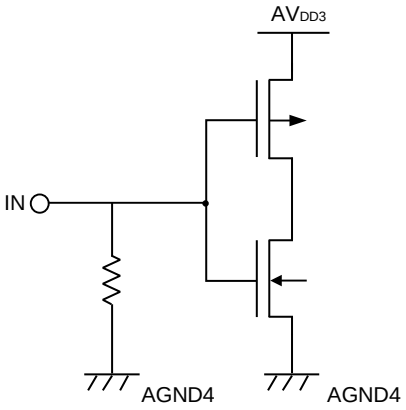
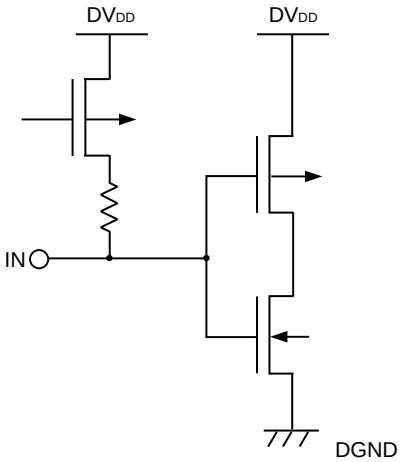
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
$\overline{\text{RESET}}$	 Schmitt-triggered input with hysteresis characteristics	MPXIN10 MPXIN11 MPXIN20 MPXIN21 MPXIN30 MPXIN31 MPXIN40 MPXIN41 MPXIN50 MPXIN51 MPXIN60 MPXIN61 SC_IN GAINAMP_IN	
CLK_SYNCH CLK_LPF CLK_HPF		$\overline{\text{SCLK}}$ SDI $\overline{\text{CS}}$	

Figure 1-1. Pin I/O Circuit Type (2/4)

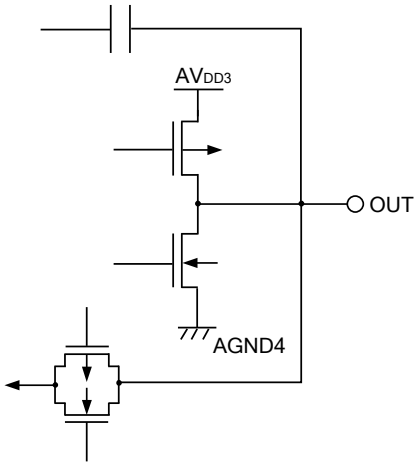
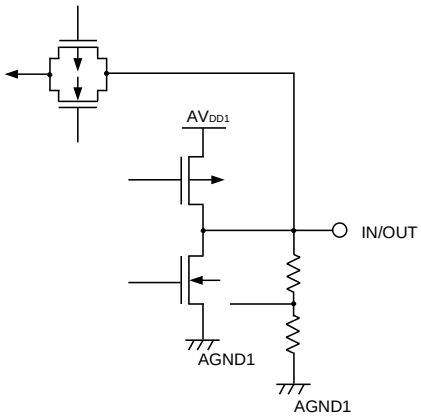
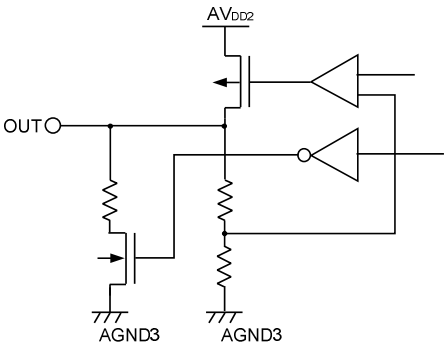
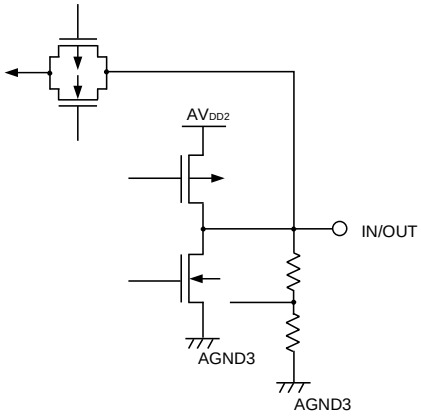
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
LPF_OUT HPF_OUT		DAC1_OUT/ VREFIN1 DAC2_OUT/ VREFIN2 DAC3_OUT/ VREFIN3	
LDO_OUT		DAC4_OUT/ VREFIN4	

Figure 1-1. Pin I/O Circuit Type (3/4)

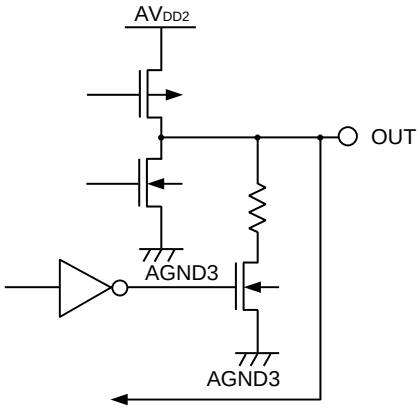
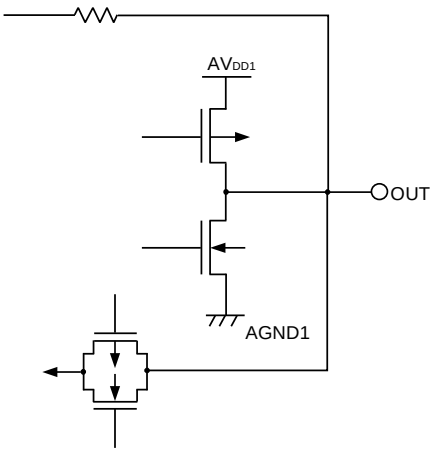
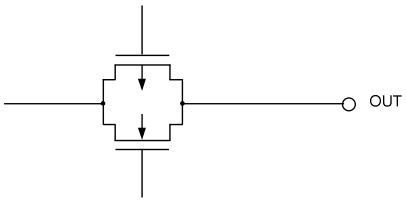
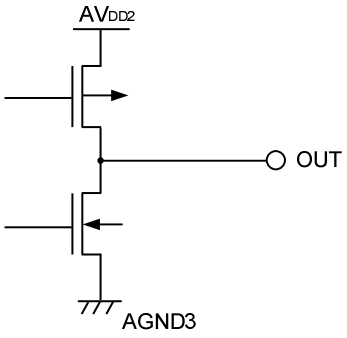
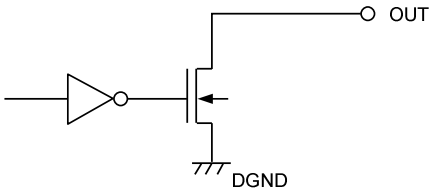
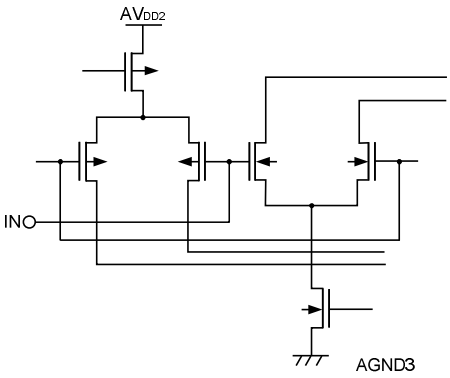
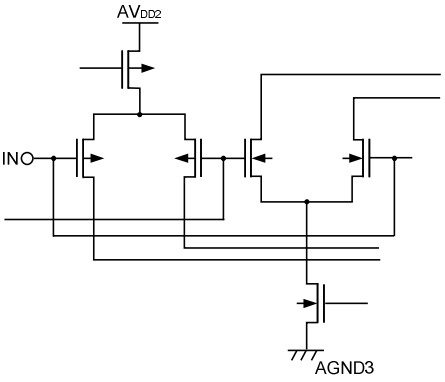
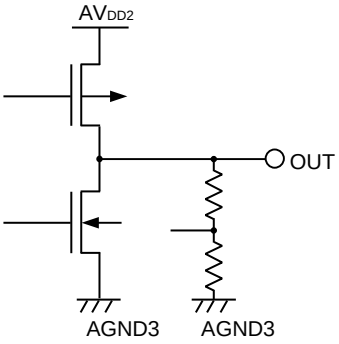
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
BGR_OUT		GAINAMP_OUT AMP3_OUT	
AMP1_OUT AMP2_OUT SYNCH_OUT		AMP4_OUT	

Figure 1-1. Pin I/O Circuit Type (4/4)

Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
SDO		AMP4_INP	
AMP4_INN		TEMP_OUT	

2. Configurable Amplifiers

The RAA730500 has three on-chip configurable amplifier channels.

2.1 Overview of Configurable Amplifier Features

By specifying settings in the SPI control registers, the configurable amplifiers can be used to realize the following features:

- Single-channel operation
  - Non-inverting amplifier
    - The gain can be specified between 9.5 dB and 40.1 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function
  - Inverting amplifier
    - The gain can be specified between 6 dB and 40 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function
  - Differential amplifier
    - The gain can be specified between 6 dB and 40 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function
  - Transimpedance amplifier
    - The feedback resistance can be specified between 20 kΩ and 640 kΩ in 6 steps
    - Four operating modes are available
    - Includes a power-off function
- Multiple-channel operation
  - Instrumentation amplifier
    - The gain can be specified between 20 dB and 54 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function

<R> And also, the DACn_OUT output signals can be used as the reference voltage for each configurable amplifier. If D/A converter is powered off, the external reference voltage is to be input to DACn_OUT/VREFINn pin. For details about use of D/A converter, see **5. D/A Converter**.

Remark n = 1 to 3

2.2 Block Diagram

Figure 2-1. Block Diagram of Configurable Amplifier Ch1

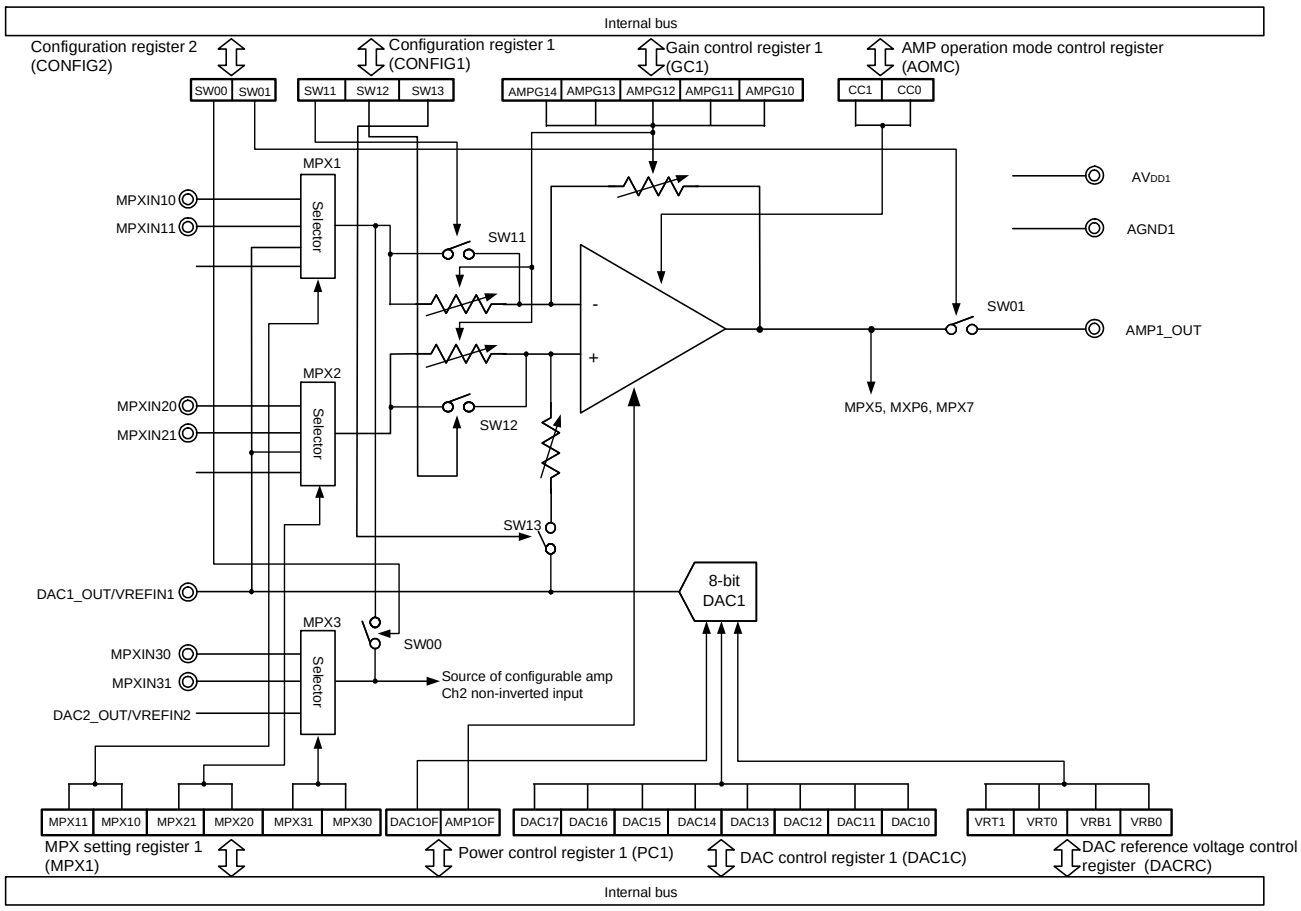


Figure 2-2. Block Diagram of Configurable Amplifier Ch2

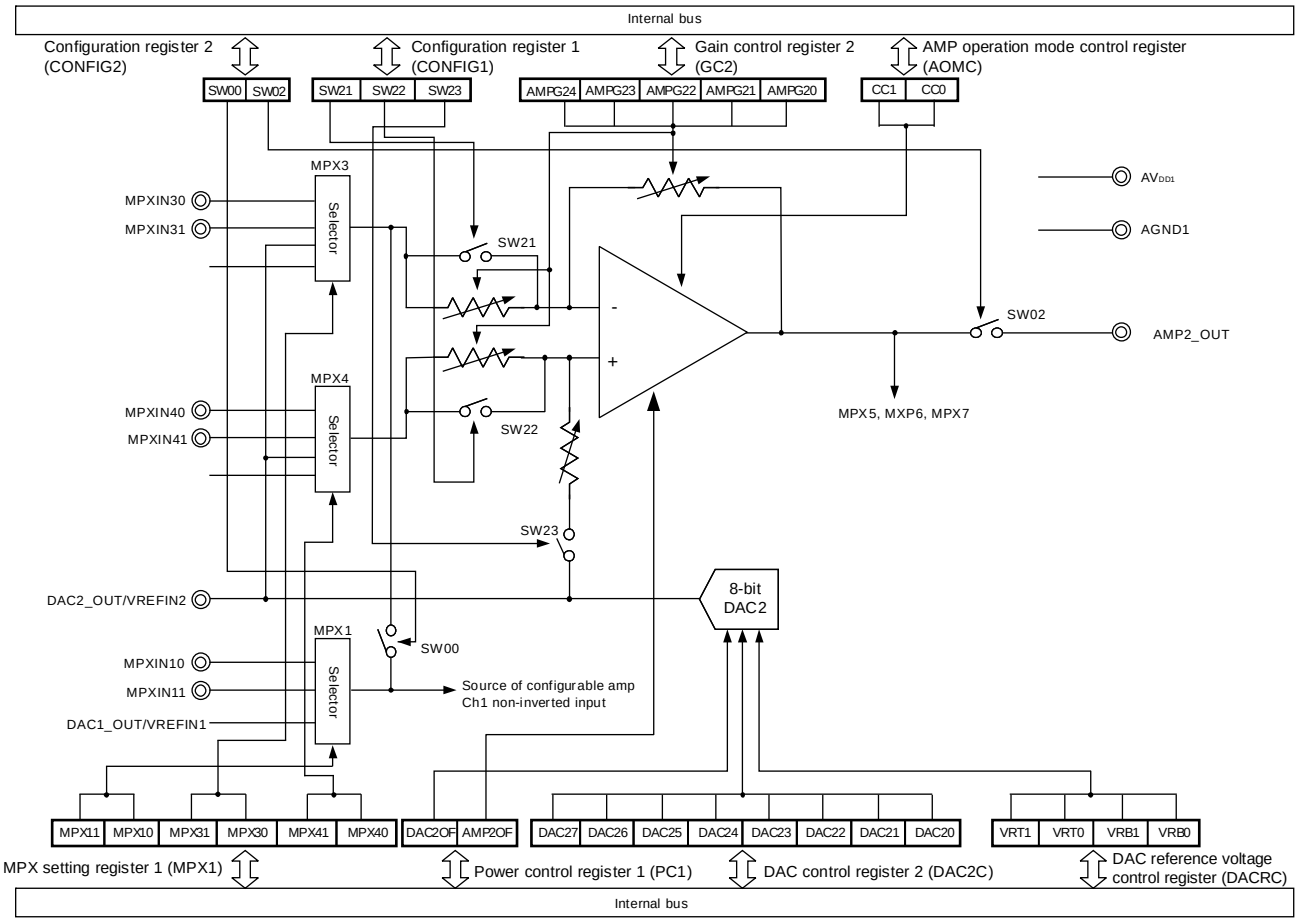
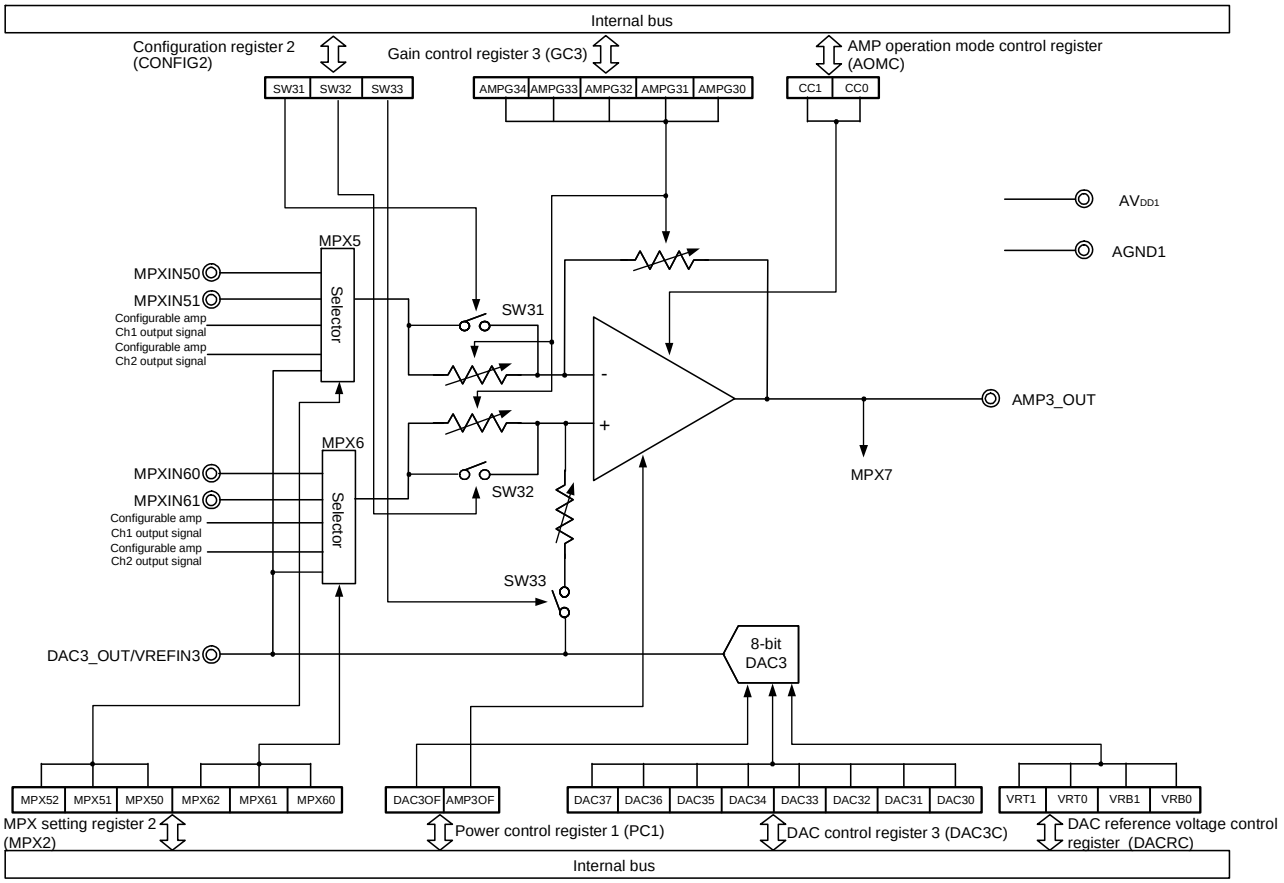


Figure 2-3. Block Diagram of Configurable Amplifier Ch3



2.3 Registers Controlling the Configurable Amplifiers

The configurable amplifiers are controlled by the following 9 registers:

- Configuration register 1 (CONFIG1)
- Configuration register 2 (CONFIG2)
- MPX setting register 1 (MPX1)
- MPX setting register 2 (MPX2)
- Gain control register 1 (GC1)
- Gain control register 2 (GC2)
- Gain control register 3 (GC3)
- AMP operation mode control register (AOMC)
- Power control register 1 (PC1)

(1) Configuration register 1 (CONFIG1)

This register is used to turn on or off each switch of configurable amplifiers Ch1 and Ch2.
Reset signal input clears this register to 00H.

Address: 00H After reset: 00H R/W

	7	6	5	4	3	2	1	0
CONFIG1	0	SW11	SW12	SW13	0	SW21	SW22	SW23

SW11	Control of SW11
0	Turn off SW11.
1	Turn on SW11.

SW12	Control of SW12
0	Turn off SW12.
1	Turn on SW12.

SW13	Control of SW13
0	Turn off SW13.
1	Turn on SW13.

SW21	Control of SW21
0	Turn off SW21.
1	Turn on SW21.

SW22	Control of SW22
0	Turn off SW22.
1	Turn on SW22.

SW23	Control of SW23
0	Turn off SW23.
1	Turn on SW23.

Remark Bits 7 and 3 can be set to 1, but this has no effect on the function.

(2) Configuration register 2 (CONFIG2)

This register is used to turn on or off each switch of configurable amplifiers Ch1 to Ch3.
Reset signal input clears this register to 00H.

Address: 01H After reset: 00H R/W

	7	6	5	4	3	2	1	0
CONFIG2	0	SW31	SW32	SW33	0	SW02	SW01	SW00

SW31	Control of SW31
0	Turn off SW31.
1	Turn on SW31.

SW32	Control of SW32
0	Turn off SW32.
1	Turn on SW32.

SW33	Control of SW33
0	Turn off SW33.
1	Turn on SW33.

SW02	Control of SW02
0	Turn off SW02.
1	Turn on SW02.

SW01	Control of SW01
0	Turn off SW01.
1	Turn on SW01.

SW00	Control of SW00
0	Turn off SW00.
1	Turn on SW00.

Remark Bits 7 and 3 can be set to 1, but this has no effect on the function.

(3) MPX setting register 1 (MPX1)

This register is used to control MPX1, MPX2, MPX3, and MPX4.
This register is used to select the signal input to configurable amplifiers Ch1 and Ch2.
Reset signal input clears this register to 00H.

Address: 03H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX1	MPX11	MPX10	MPX21	MPX20	MPX31	MPX30	MPX41	MPX40

MPX11	MPX10	Source of configurable amplifier Ch1 inverted input
0	0	MPXIN10 pin
0	1	MPXIN11 pin
1	0	D/A converter Ch1 output signal or VREFIN1 pin
1	1	Open pin

MPX21	MPX20	Source of configurable amplifier Ch1 non-inverted input
0	0	MPXIN20 pin
0	1	MPXIN21 pin
1	0	D/A converter Ch1 output signal or VREFIN1 pin
1	1	Open pin

MPX31	MPX30	Source of configurable amplifier Ch2 inverse input
0	0	MPXIN30 pin
0	1	MPXIN31 pin
1	0	D/A converter Ch2 output signal or VREFIN2 pin
1	1	Open pin

MPX41	MPX40	Source of configurable amplifier Ch2 non-inverted input
0	0	MPXIN40 pin
0	1	MPXIN41 pin
1	0	D/A converter Ch2 output signal or VREFIN2 pin
1	1	Open pin

(4) MPX setting register 2 (MPX2)

This register is used to control MPX5 and MPX6.
This register is used to select the signal input to configurable amplifier Ch3.
Reset signal input clears this register to 00H.

Address: 04H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX2	0	MPX52	MPX51	MPX50	0	MPX62	MPX61	MPX60

MPX52	MPX51	MPX50	Source of configurable amplifier Ch3 inverse input
0	0	0	MPXIN50 pin
0	0	1	MPXIN51 pin
0	1	0	Configurable amplifier Ch1 output signal
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch3 output signal or VREFIN3 pin
Other than above			Setting prohibited

MPX62	MPX61	MPX60	Source of configurable amplifier Ch3 non-inverted input
0	0	0	MPXIN60 pin
0	0	1	MPXIN61 pin
0	1	0	Output signal of configurable amplifier Ch1
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch3 output signal or VREFIN3 pin
Other than above			Setting prohibited

Remark Bits 7 and 3 can be set to 1, but this has no effect on the function.

(5) Gain control register 1 (GC1)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch1.
The value to specify depends on the configuration of configurable amplifier Ch1.
When using configurable amplifiers Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 1 (GC1) to 03H.
Reset signal input clears this register to 00H.

Address: 06H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC1	0	0	0	AMPG14	AMPG13	AMPG12	AMPG11	AMPG10

Table 2-1. Gain of Configurable Amplifier Ch1 (Non-Inverting Amplifier)

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Gain of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

Remark Bits 7 to 5 are fixed at 0 of read only.

Table 2-2. Gain of Configurable Amplifier Ch1 (Inverting Amplifier and Differential Amplifier)

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Gain of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Table 2-3. Feedback Resistance of Configurable Amplifier Ch1 (Transimpedance Amplifier)

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Feedback Resistance of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

(6) Gain control register 2 (GC2)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch2.
The value to specify depends on the configuration of configurable amplifier Ch2.
When using configurable amplifiers Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 2 (GC2) to 03H.
Reset signal input clears this register to 00H.

Address: 07H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC2	0	0	0	AMPG24	AMPG23	AMPG22	AMPG21	AMPG20

Table 2-4. Gain of Configurable Amplifier Ch2 (Non-Inverting Amplifier)

AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Gain of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

Remark Bits 7 to 5 are fixed at 0 of read only.

Table 2-5. Gain of Configurable Amplifier Ch2 (Inverting Amplifier and Differential Amplifier)

AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Gain of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Table 2-6. Feedback Resistance of Configurable Amplifier Ch2 (Transimpedance Amplifier)

AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Feedback Resistance of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

(7) Gain control register 3 (GC3)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch3.
The value to specify depends on the configuration of configurable amplifier Ch3.
When using configurable amplifiers Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 1 (GC1) and gain control register 2 (GC2) to 03H, respectively.
Reset signal input clears this register to 00H.

Address: 08H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC3	0	0	0	AMPG34	AMPG33	AMPG32	AMPG31	AMPG30

Table 2-7. Gain of Configurable Amplifier Ch3 (Non-Inverting Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

Remark Bits 7 to 5 are fixed at 0 of read only.

Table 2-8. Gain of Configurable Amplifier Ch3 (Inverting Amplifier and Differential Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Table 2-9. Feedback Resistance of Configurable Amplifier Ch3 (Transimpedance Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Feedback Resistance of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

Table 2-10. Gain of Configurable Amplifier Ch3 (Instrumentation Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	20 dB
0	0	0	0	1	22 dB
0	0	0	1	0	24 dB
0	0	0	1	1	26 dB
0	0	1	0	0	28 dB
0	0	1	0	1	30 dB
0	0	1	1	0	32 dB
0	0	1	1	1	34 dB
0	1	0	0	0	36 dB
0	1	0	0	1	38 dB
0	1	0	1	0	40 dB
0	1	0	1	1	42 dB
0	1	1	0	0	44 dB
0	1	1	0	1	46 dB
0	1	1	1	0	48 dB
0	1	1	1	1	50 dB
1	0	0	0	0	52 dB
1	0	0	0	1	54 dB
Other than above					Setting prohibited

(8) AMP operation mode control register (AOMC)

This register is used to specify the operating mode of configurable amplifiers Ch1 to Ch3.
Reset signal input clears this register to 00H.

Address: 09H After reset: 00H R/W

	7	6	5	4	3	2	1	0
AOMC	0	0	0	0	0	0	CC1	CC0

CC1	CC0	Operating mode of configurable amplifiers Ch1 to Ch3
0	0	High-speed mode
0	1	Mid-speed mode 2
1	0	Mid-speed mode 1
1	1	Low-speed mode

Remark 1. Bits 5 to 2 can be set to 1, but this has no effect on the function.
2. Bits 7 and 6 are fixed at 0 of read only.

<R> **(9) Power control register 1 (PC1)**

This register is used to enable or disable operation of the configurable amplifiers, the general-purpose operational amplifier, and the D/A converters.
Use this register to stop unused functions to reduce power consumption and noise.
When using one of configurable amplifier channels Ch1 to Ch3, be sure to set the control bit that corresponds to the channel (bits 0 to 2) to 1.
Reset signal input clears this register to 00H.

Address: 11H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	AMP4OF	AMP3OF	AMP2OF	AMP1OF

AMP3OF	Operation of configurable amplifier Ch3
0	Stop operation of configurable amplifier Ch3.
1	Enable operation of configurable amplifier Ch3.

AMP2OF	Operation of configurable amplifier Ch2
0	Stop operation of configurable amplifier Ch2.
1	Enable operation of configurable amplifier Ch2.

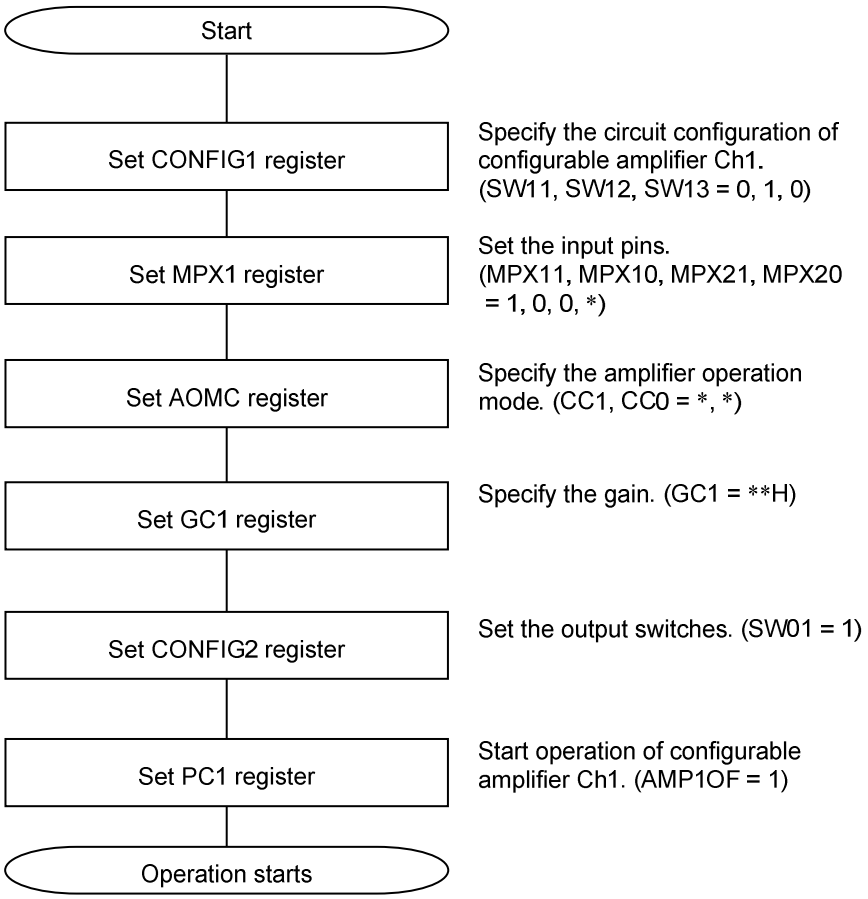
AMP1OF	Operation of configurable amplifier Ch1
0	Stop operation of configurable amplifier Ch1.
1	Enable operation of configurable amplifier Ch1.

2.4 Procedure for Operating the Configurable Amplifiers

(1) Procedure when using the amplifiers as non-inverting amplifiers

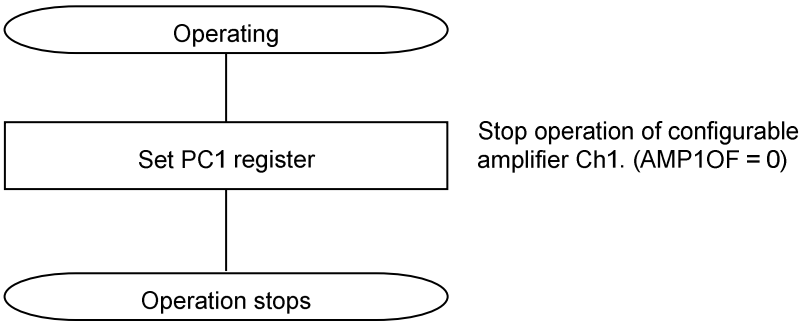
When using the configurable amplifiers as non-inverting amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (non-inverting amplifier)

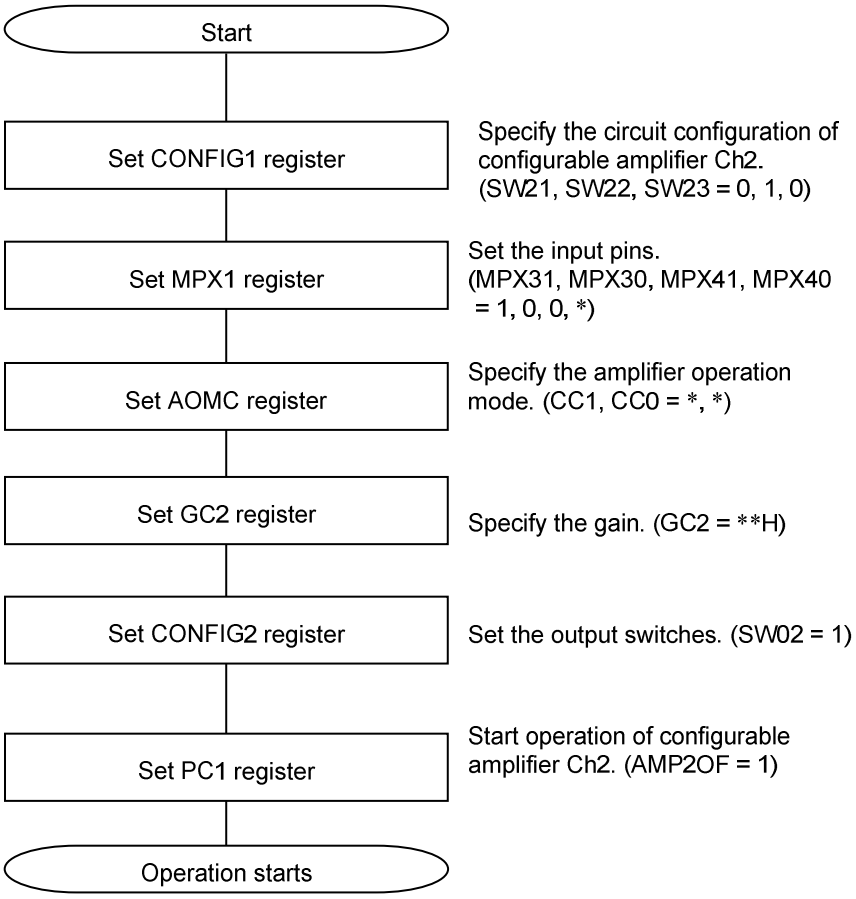


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (non-inverting amplifier)

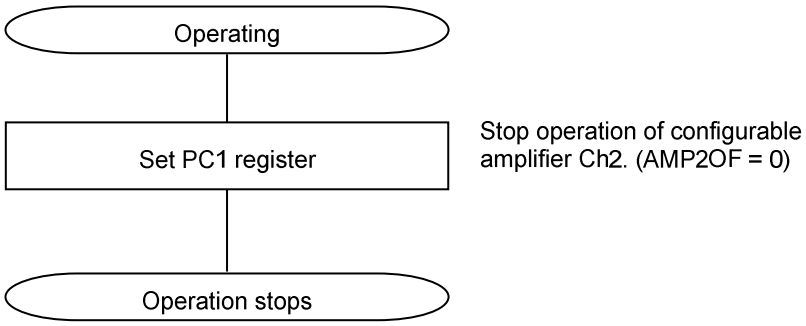


Example of procedure for starting configurable amplifier Ch2 (non-inverting amplifier)

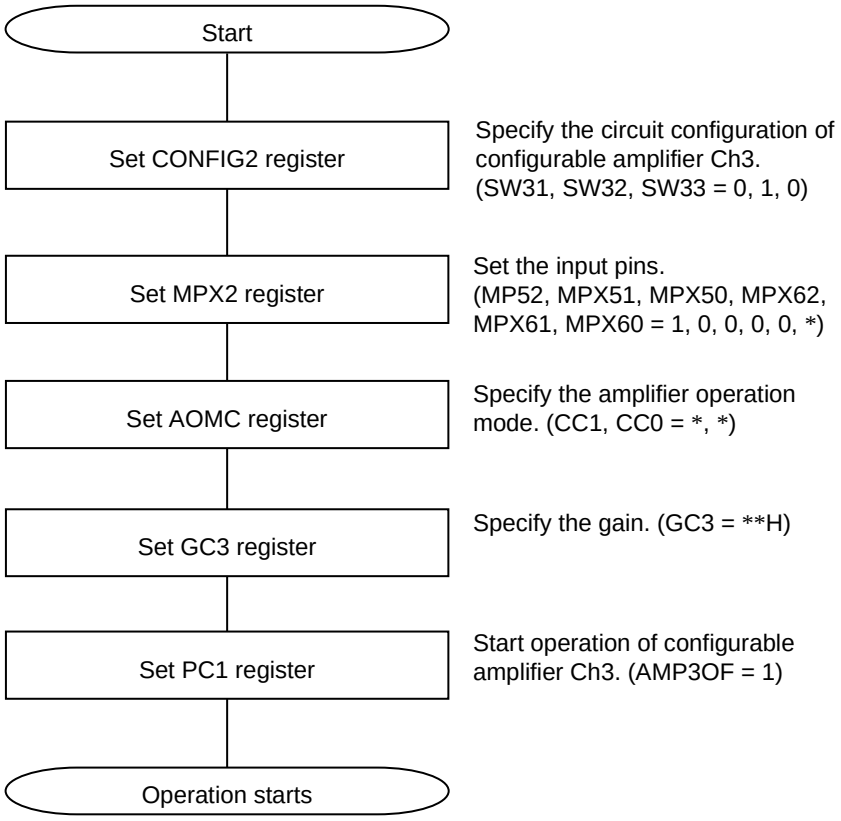


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (non-inverting amplifier)

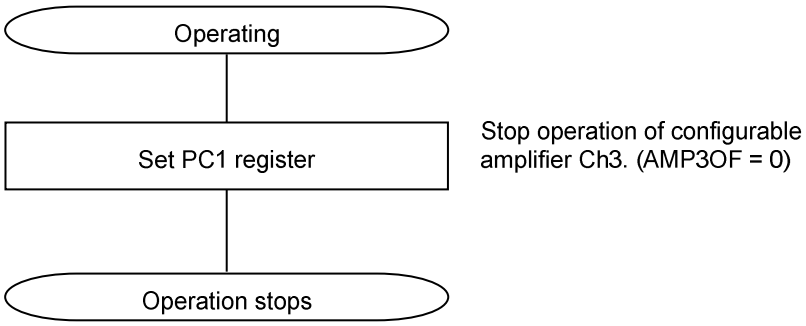


Example of procedure for starting configurable amplifier Ch3 (non-inverting amplifier)



Remark *: don't care

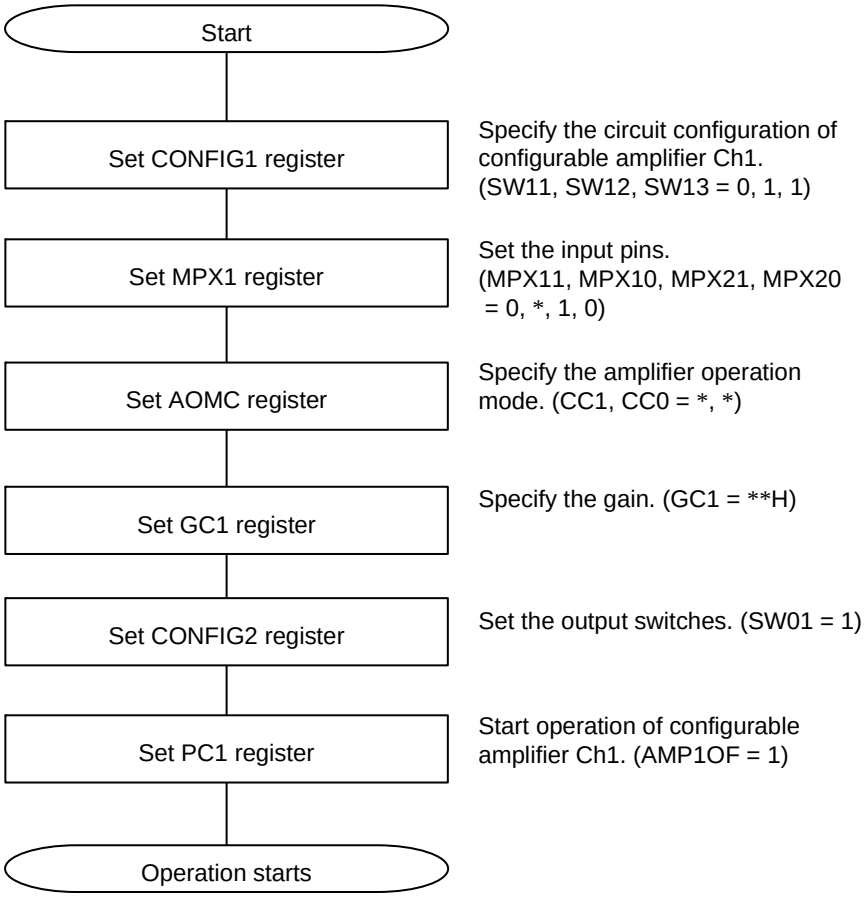
Example of procedure for stopping configurable amplifier Ch3 (non-inverting amplifier)



(2) Procedure when using the amplifiers as inverting amplifiers

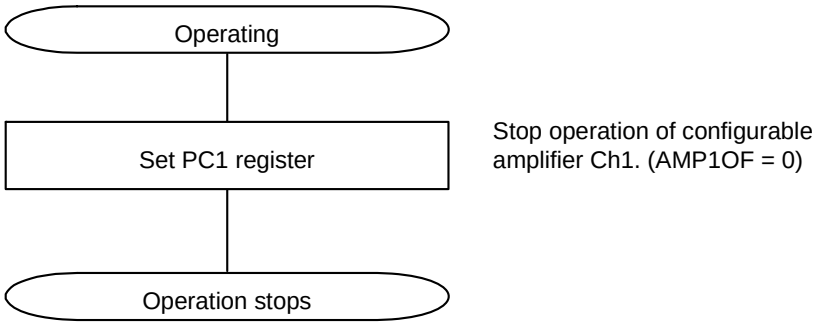
When using the configurable amplifiers as inverting amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (inverting amplifier)

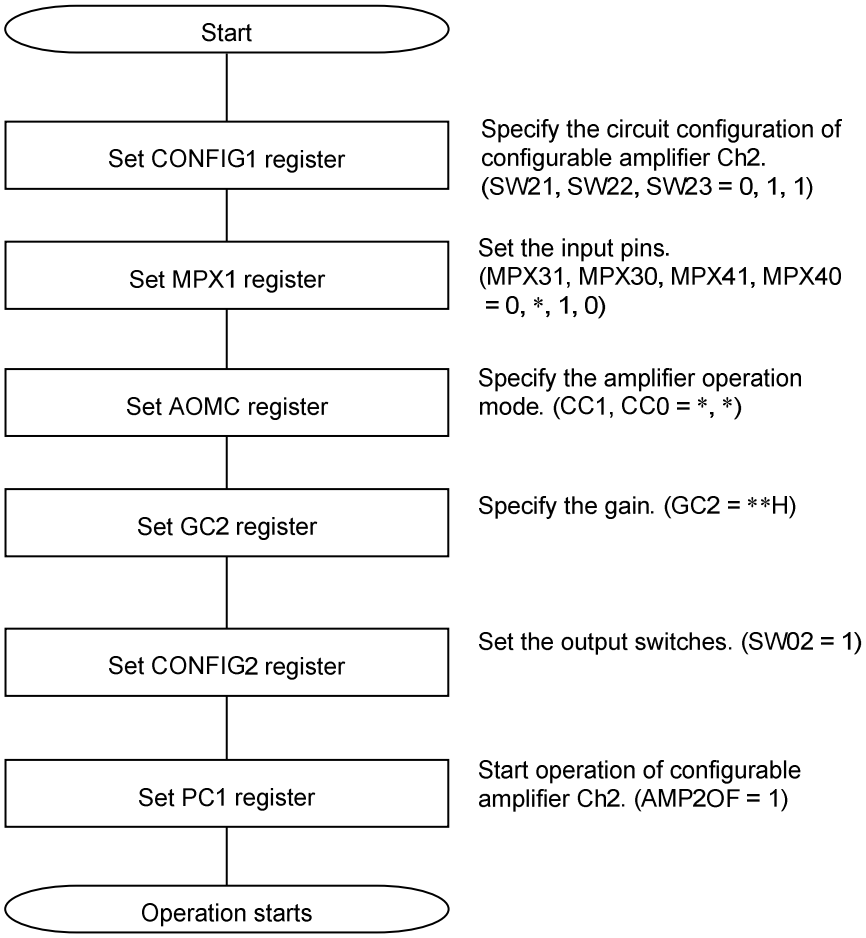


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (inverting amplifier)

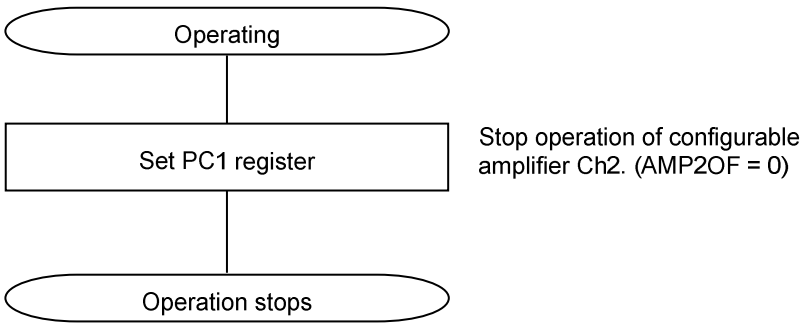


Example of procedure for starting configurable amplifier Ch2 (inverting amplifier)

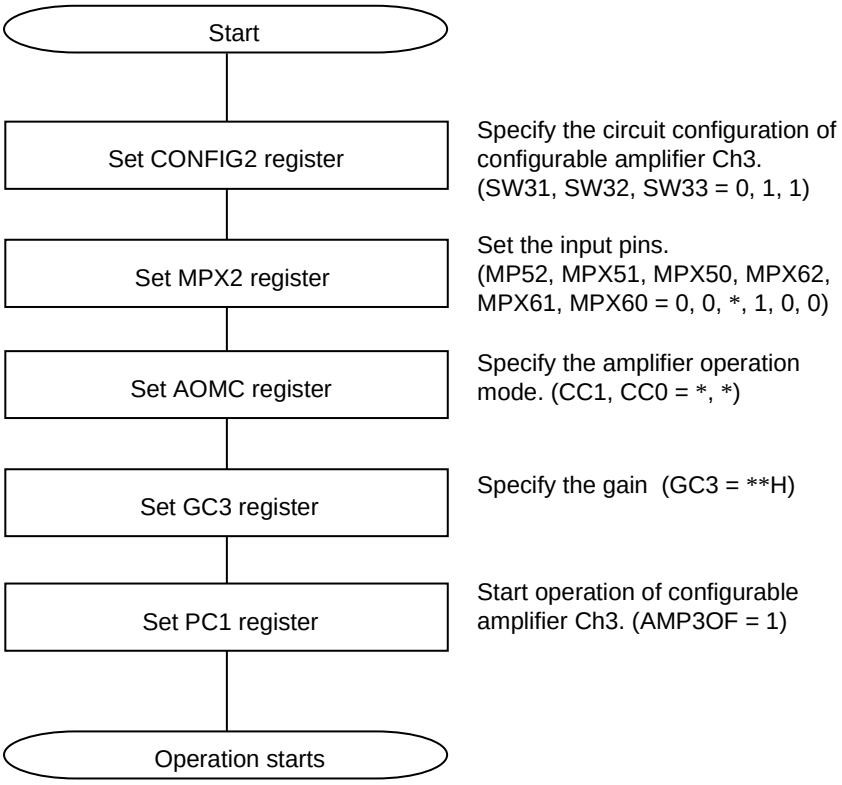


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (inverting amplifier)

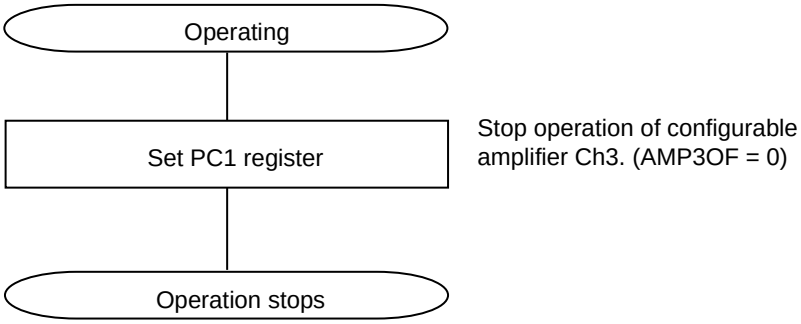


Example of procedure for starting configurable amplifier Ch3 (inverting amplifier)



Remark *: don't care

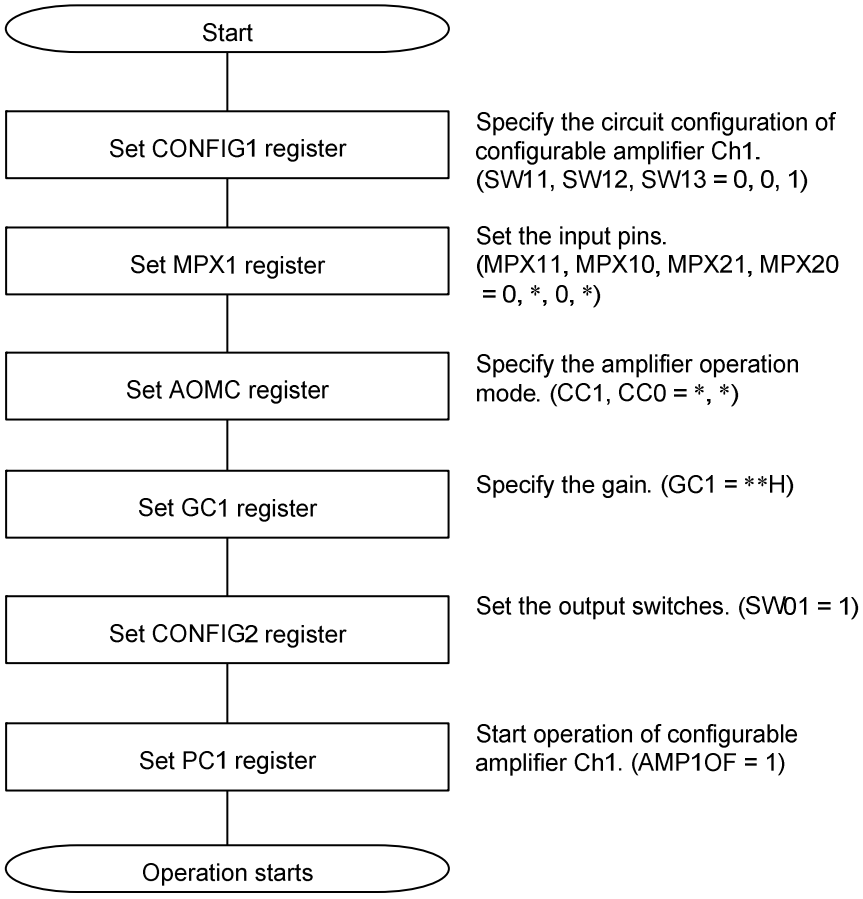
Example of procedure for stopping configurable amplifier Ch3 (inverting amplifier)



(3) Procedure when using the amplifiers as differential amplifiers

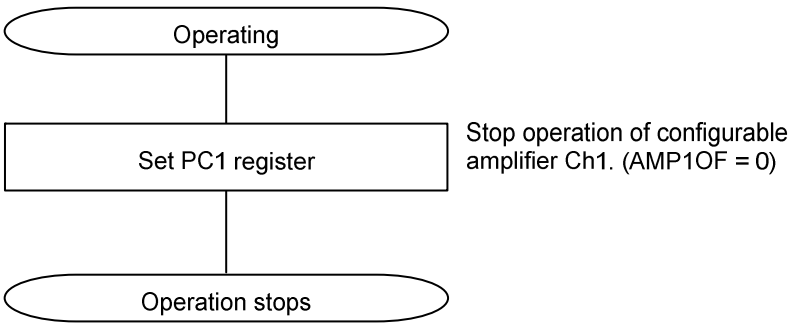
When using the configurable amplifiers together as a differential amplifier, follow the procedures below to start and stop the amplifier.

Example of procedure for starting configurable amplifier Ch1 (differential amplifier)

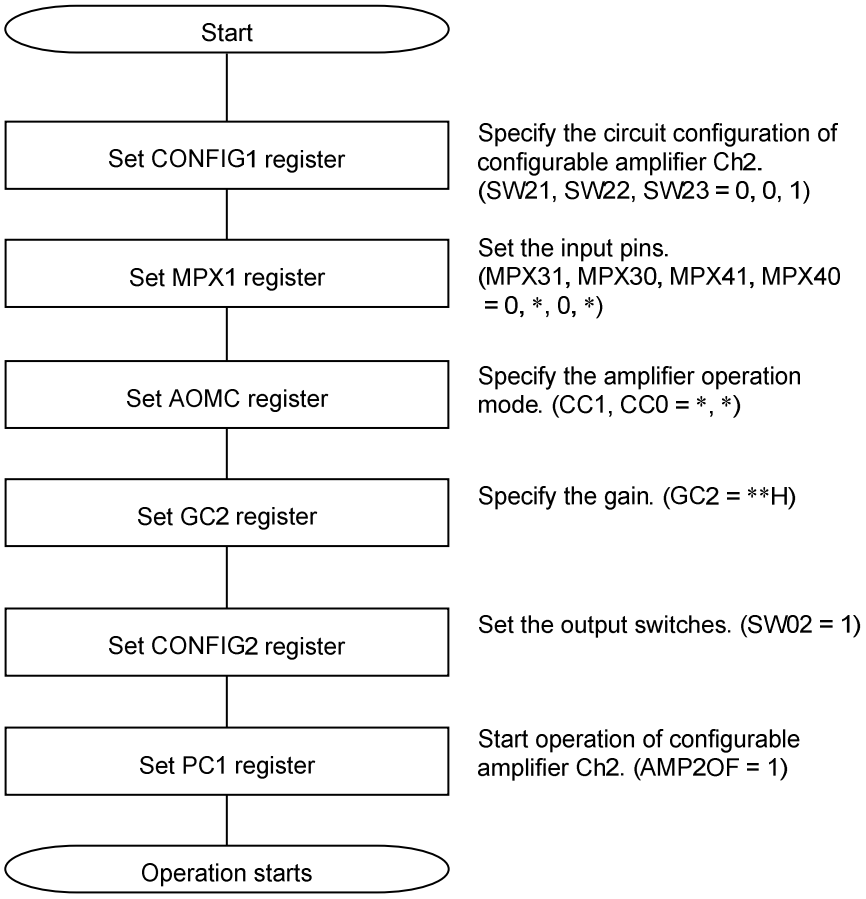


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (differential amplifier)

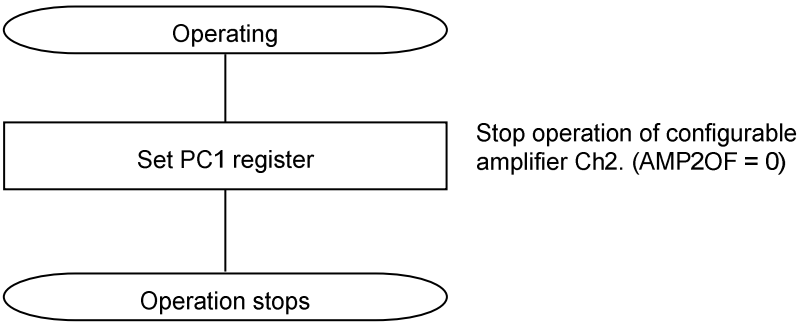


Example of procedure for starting configurable amplifier Ch2 (differential amplifier)

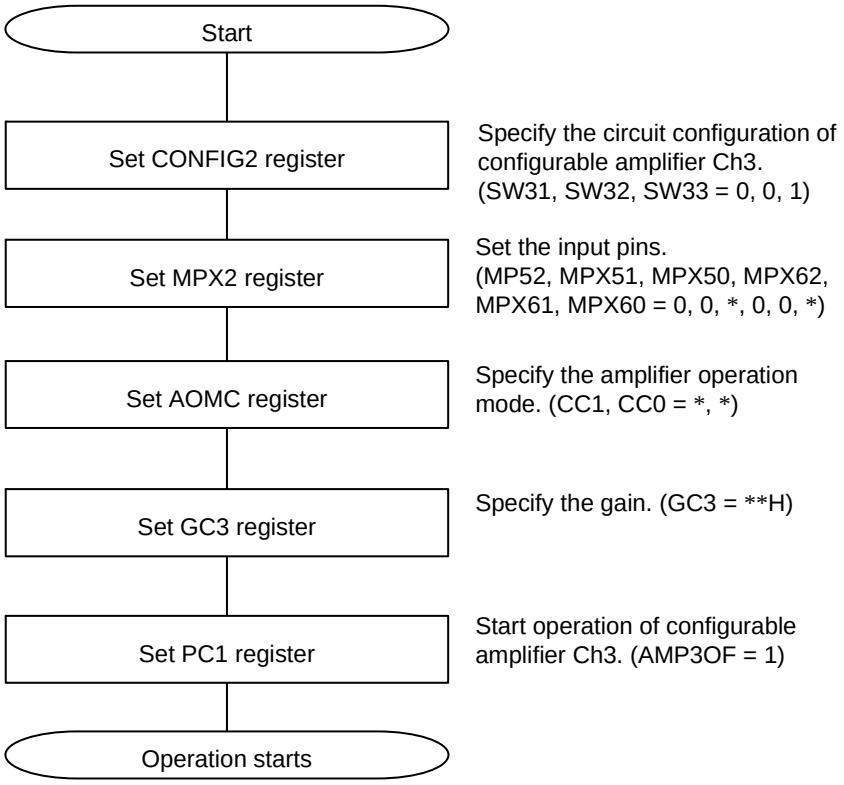


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (differential amplifier)

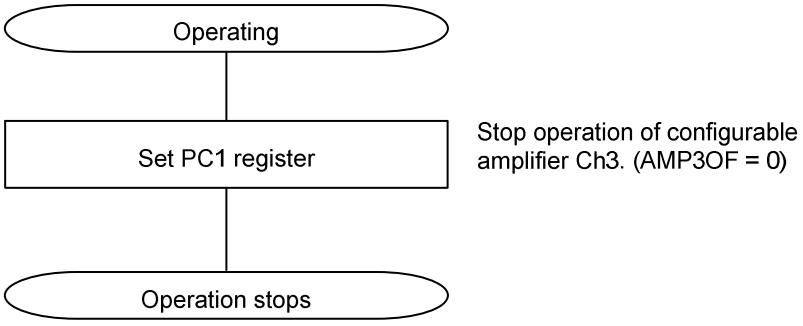


Example of procedure for starting configurable amplifier Ch3 (differential amplifier)



Remark *: don't care

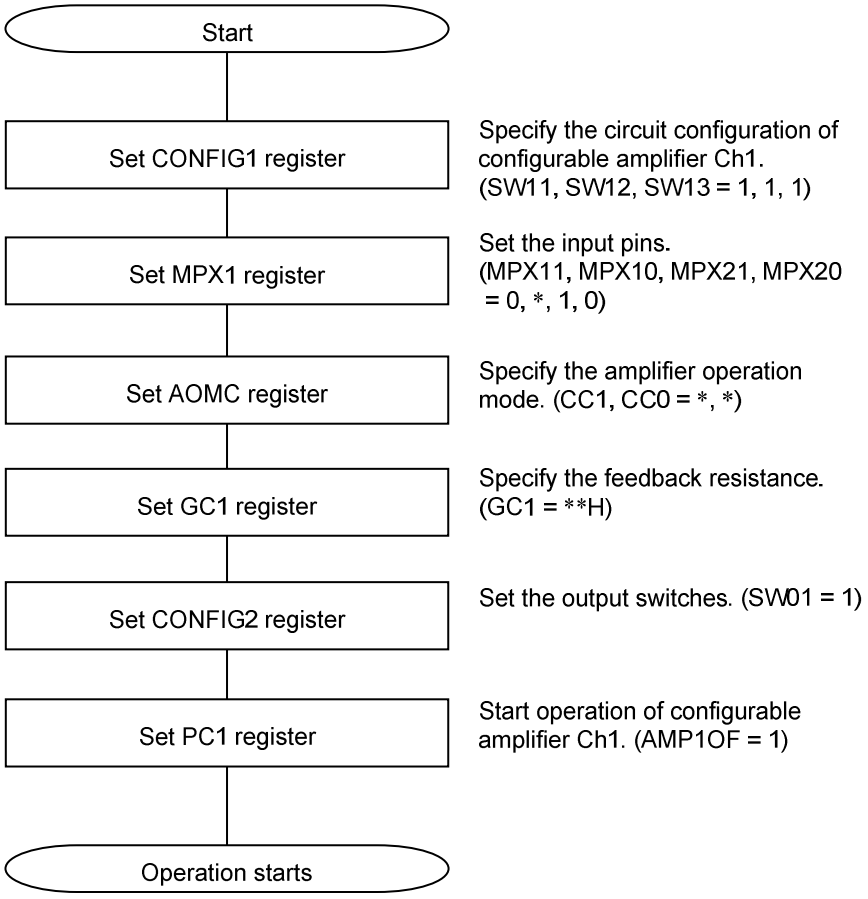
Example of procedure for stopping configurable amplifier Ch3 (differential amplifier)



(4) Procedure when using the amplifiers as a transimpedance amplifier

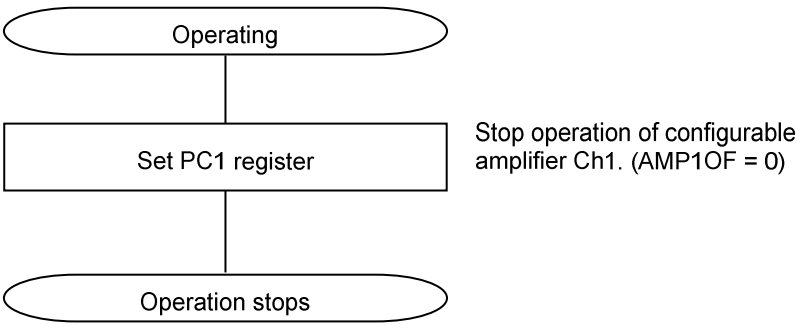
When using the configurable amplifiers as transimpedance amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (transimpedance amplifier)

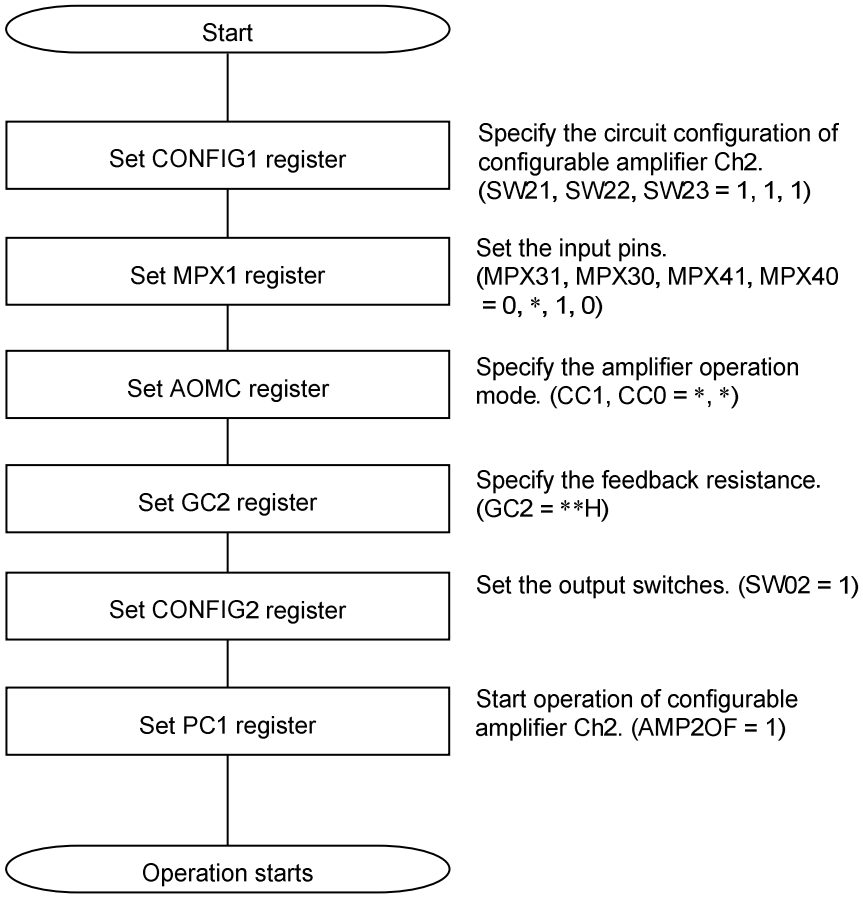


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (transimpedance amplifier)

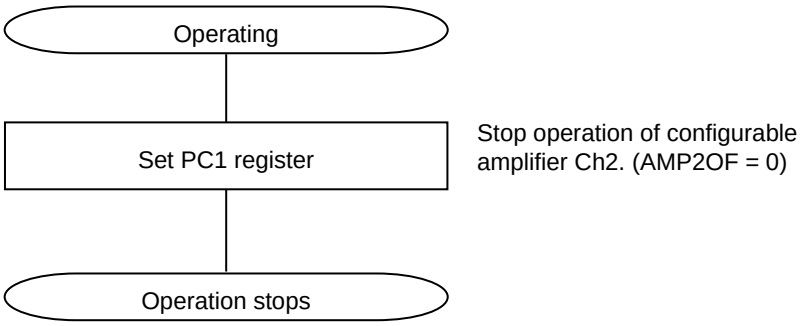


Example of procedure for starting configurable amplifier Ch2 (transimpedance amplifier)

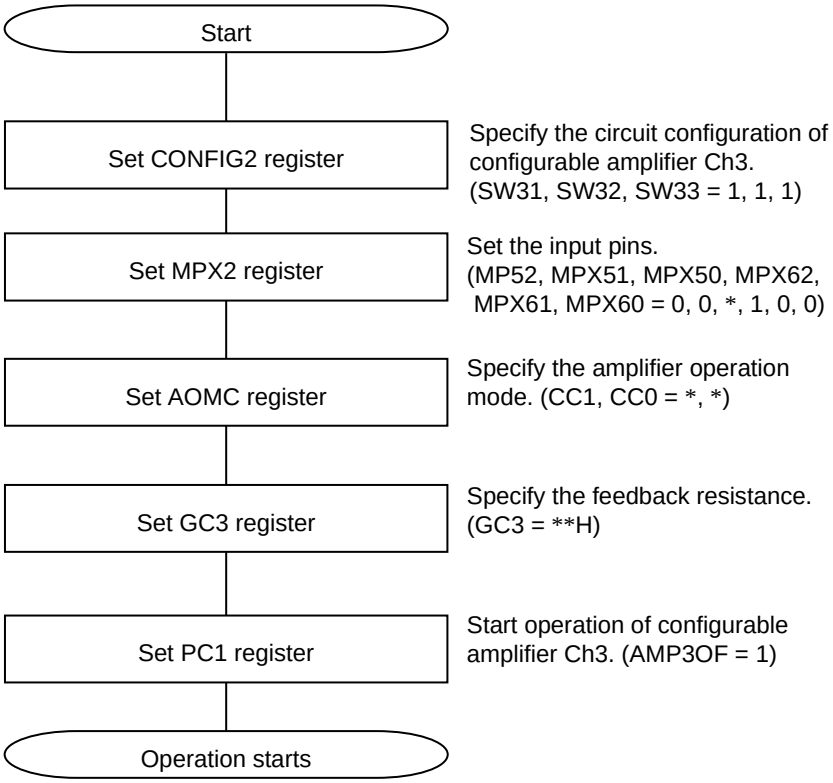


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (transimpedance amplifier)

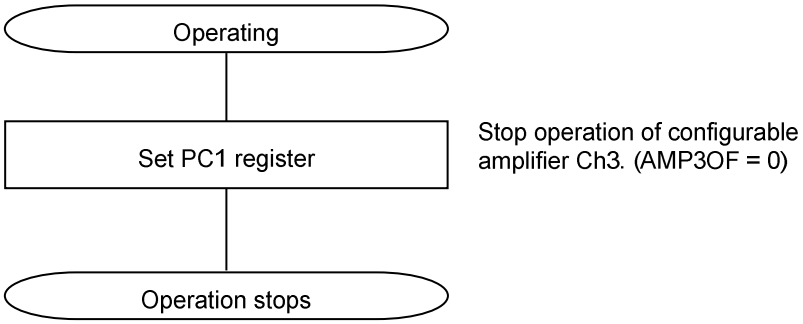


Example of procedure for starting configurable amplifier Ch3 (transimpedance amplifier)



Remark *: don't care

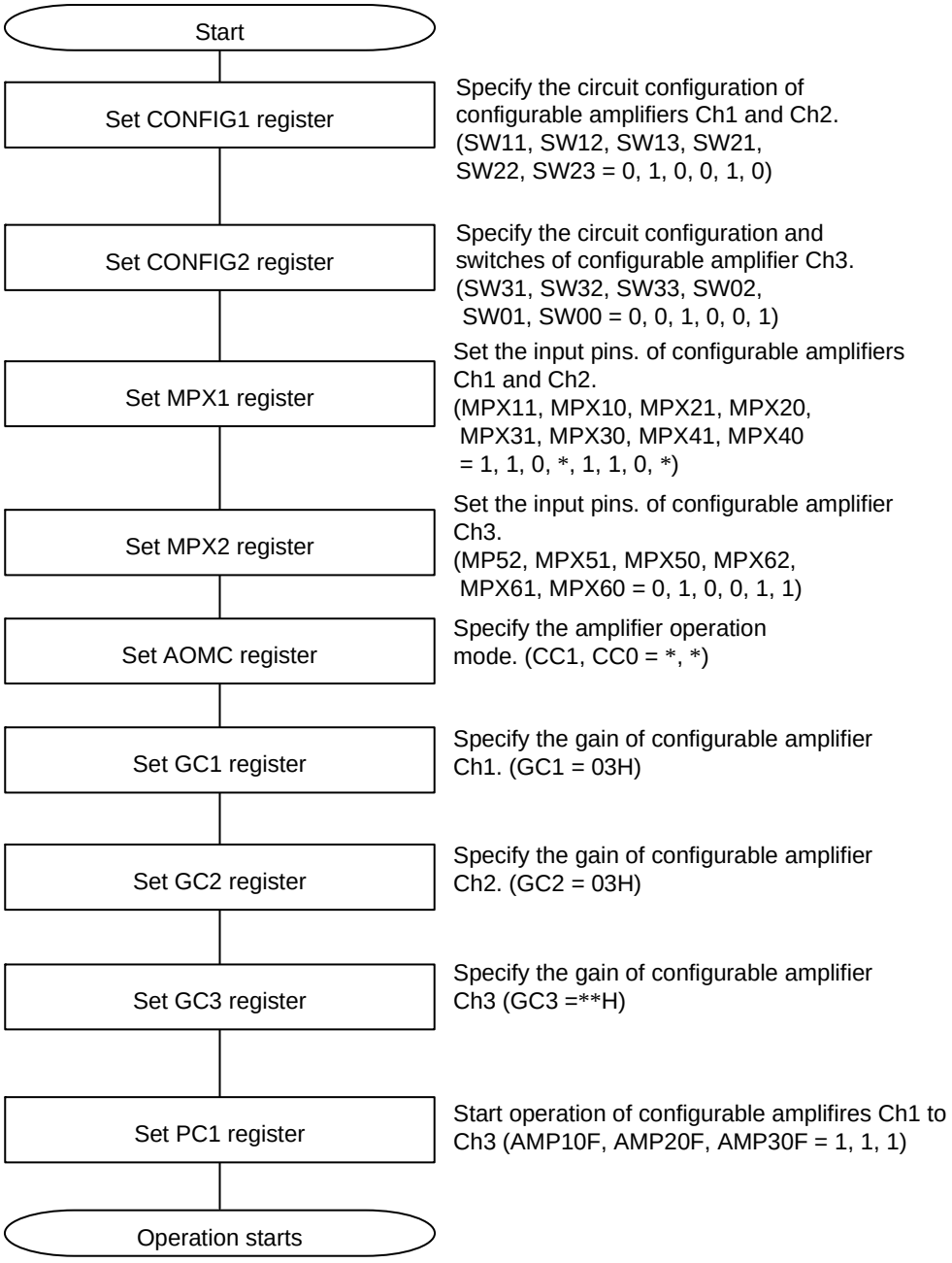
Example of procedure for stopping configurable amplifier Ch3 (transimpedance amplifier)



(5) Procedure when using the amplifiers as an instrumentation amplifier

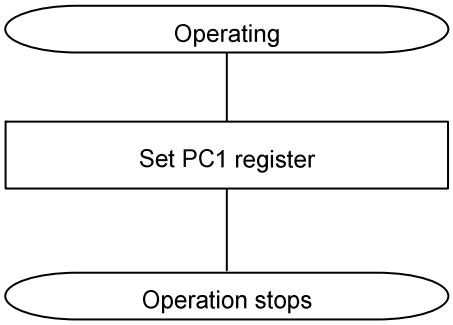
When using the configurable amplifiers together as an instrumentation amplifier, follow the procedures below to start and stop the amplifier.

Example of procedure for starting configurable amplifiers (instrumentation amplifier)



Remark *: don't care

Example of procedure for stopping configurable amplifiers (instrumentation amplifier)



Stop operation of configurable amplifiers Ch1 to Ch3.
(AMP1OF, AMP2OF, AMP3OF = 0, 0, 0)

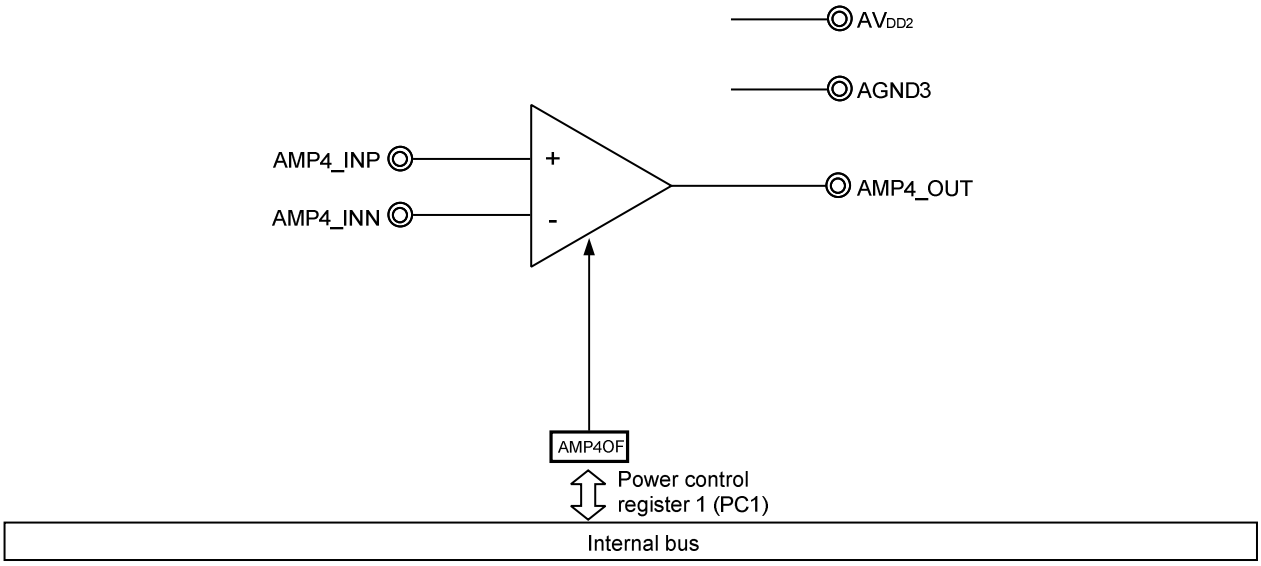
3. General-Purpose Operational Amplifier

The RAA730500 has one on-chip general-purpose operational amplifier-purpose channel.

3.1 Overview of General-Purpose Operational Amplifier Features

- Rail-to-rail I/O
- Includes a power-off function.

3.2 Block Diagram



3.3 Registers Controlling the General-purpose operational amplifier

The general-purpose operational amplifier is controlled by power control register 1 (PC1).

(1) Power control registers 1 (PC1)

This register is used to enable or disable operation of the configurable amplifiers, the general-purpose operational amplifier, and the D/A converters. Use this register to stop unused functions to reduce power consumption and noise. When using the general-purpose operational amplifier, be sure to set bit 3 to 1.
Reset signal input clears this register to 00H.

Address: 11H After reset: 00H R/W

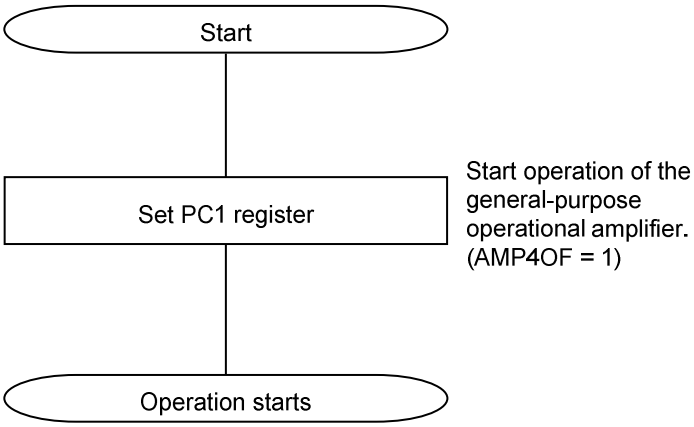
	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	AMP4OF	AMP3OF	AMP2OF	AMP1OF

AMP4OF	Operation of general-purpose operational amplifier
0	Stop operation of the general-purpose operational amplifier.
1	Enable operation of the general-purpose operational amplifier.

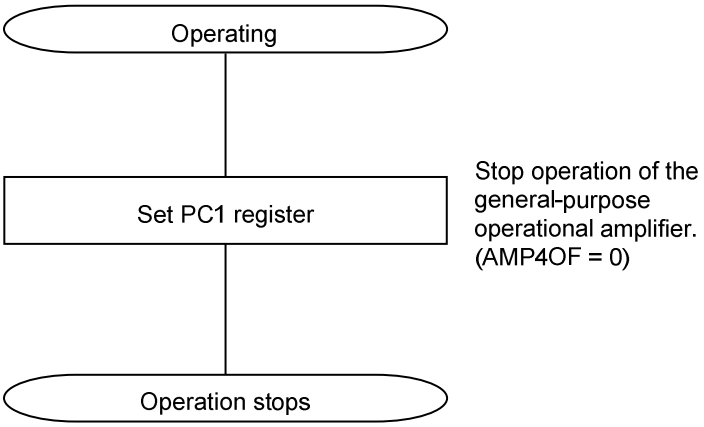
3.4 Procedure for Operating the General-purpose operational amplifier

Follow the procedures below to start and stop the general-purpose operational amplifier.

Example of procedure for starting the general-purpose operational amplifier



Example of procedure for stopping the general-purpose operational amplifier



4. Synchronous Detection Amplifier

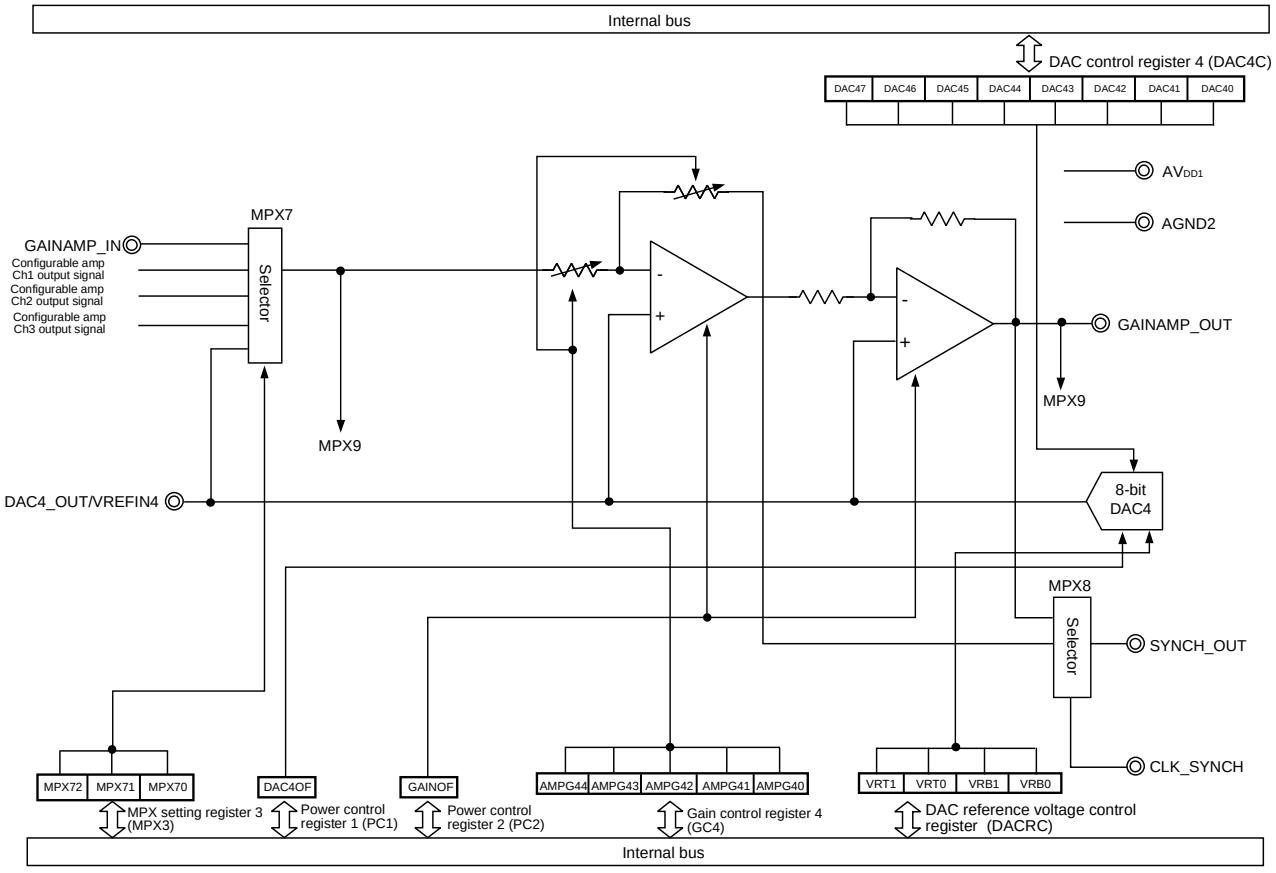
The RAA730500 has one on-chip gain adjustment amplifier channel with synchronous detection function as a synchronous detection amplifier. A synchronous detection amplifier has two output pins (GAINAMP_OUT pin, SYNCH_OUT pin). The output from SYNCH_OUT pin can be inverted output or non-inverted output according to the input of CLK_SYNCH pin.

<R> 4.1 Overview of Synchronous Detection Amplifier Features

- Rail-to-rail I/O
- The gain can be specified between 6 dB and 40 dB in 18 steps.
- Includes a power-off function.
- Includes a synchronous detector.
  - CLK_SYNCH = H: Inverted output signal (SYNCH_OUT pin)
  - CLK_SYNCH = L: Non-inverted output signal (SYNCH_OUT pin)

And also, the DAC4_OUT output signals can be used as the reference voltage for synchronous detection amplifier. If D/A converter is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin. For details about use of D/A converter, see **5. D/A Converter**.

4.2 Block Diagram



4.3 Registers Controlling the Synchronous Detection Amplifier

The synchronous detection amplifier is controlled by the following 3 registers:

- MPX setting register 3 (MPX3)
- Gain control register 4 (GC4)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX9, MPX10, and MPX11.
When selecting the signal to be input to the synchronous detection amplifier, use bits 2 to 0.
Reset signal input clears this register to 00H.

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of synchronous detection amplifier input
0	0	0	GAINAMP_IN pin
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFN4 pin
Other than above			Setting prohibited

Remark Bits 7 and 6 are fixed at 0 of read only.

(2) Gain control register 4 (GC4)

This register is used to specify the gain of the synchronous detection amplifier.
Reset signal input clears this register to 00H.

Address: 0AH After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC4	0	0	0	AMP44	AMP43	AMP42	AMP41	AMP40

AMP44	AMP43	AMP42	AMP41	AMP40	Gain
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Remark Bits 7 to 5 are fixed at 0 of read only.

(3) Power control register 2 (PC2)

This register is used to enable or disable operation of the synchronous detection amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.
When using the synchronous detection amplifier, be sure to set bit 4 to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

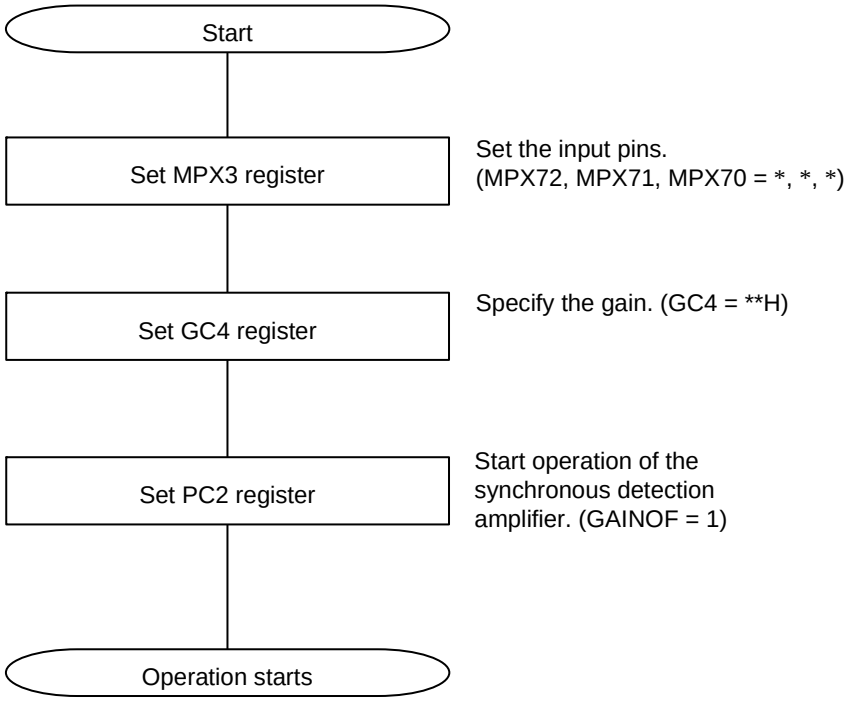
GAINOF	Operation of synchronous detection amplifier
0	Stop operation of the synchronous detection amplifier.
1	Enable operation of the synchronous detection amplifier.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

4.4 Procedure for Operating the Synchronous Detection Amplifier

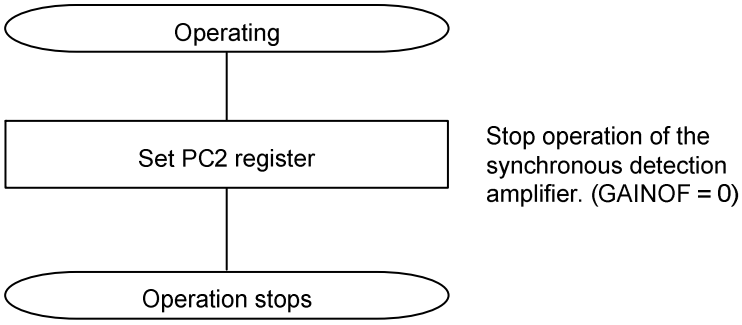
Follow the procedures below to start and stop the synchronous detection amplifier.

Example of procedure for starting the synchronous detection amplifier



Remark *: don't care

Example of procedure for stopping the synchronous detection amplifier



5. D/A Converters

The RAA730500 has four on-chip D/A converter channels.

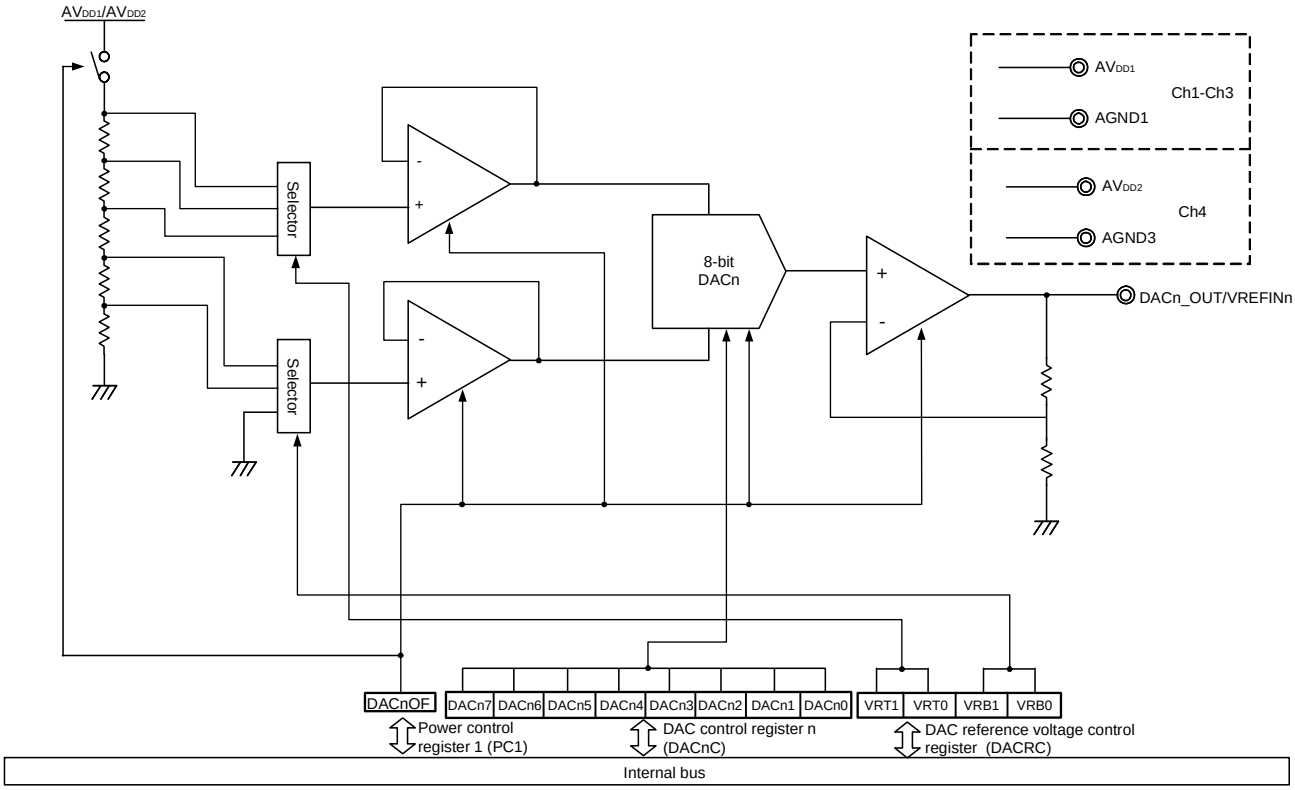
<R> 5.1 Overview of D/A Converter Features

The D/A converters are 8-bit resolution converters that convert digital input signals into analog signals.
The D/A converters have the following features:

- 8-bit resolution (× 4 ch: Ch1 to Ch4)
- R-2R ladder method
- Analog output voltage: Output voltage can be calculated with the equation shown below.
  Output voltage = {(Reference voltage upper limit – Reference voltage lower limit) × m/256}
  + Reference voltage lower limit (m = 0 to 255: Value set to DACnC register)
- Controls the reference voltage for the configurable amplifiers, synchronous detection amplifiers, low-pass filter, and high-pass filter
- Includes a power-off function.

Remark n = 1 to 4

5.2 Block Diagram



Remark n = 1 to 4

5.3 Registers Controlling the D/A Converters

The D/A converters are controlled by the following 3 registers:

- DAC reference voltage control register (DACRC)
- DAC control registers 1, 2, 3, 4 (DAC1C, DAC2C, DAC3C, DAC4C)
- Power control register 1 (PC1)

<R> **(1) DAC reference voltage control register (DACRC)**

This register is used to specify the upper (VRT) and lower (VRB) limits of the reference voltage for D/A converter channels Ch1 to Ch4.
When selecting the upper limit of the reference voltage, use bits 3 and 2. When selecting the lower limit of the reference voltage, use bits 1 and 0.
Reset signal input clears this register to 00H.

Address: 0CH After reset: 00H R/W

	7	6	5	4	3	2	1	0
DACRC	0	0	0	0	VRT1	VRT0	VRB1	VRB0

VRT1	VRT0	Reference voltage upper limit (Typ.)
0	0	AV_{DD1}
0	1	$AV_{DD1} \times 4/5$
1	0	$AV_{DD1} \times 3/5$
1	1	AV_{DD1}

VRB1	VRB0	Reference voltage lower limit (Typ.)
0	0	AGND1
0	1	$AV_{DD1} \times 1/5$
1	0	$AV_{DD1} \times 2/5$
1	1	AGND1

Remark Bits 7 to 4 are fixed at 0 of read only.

(2) DAC control registers 1, 2, 3, 4 (DAC1C, DAC2C, DAC3C, DAC4C)

This register is used to specify the analog voltage to be output to the DACn_OUT pin. The DACn_OUT output signal can be used as the reference voltage for the configurable amplifiers, synchronous detection amplifier, low-pass filter, and high-pass filter.
Reset signal input sets this register to 80H.

Address: 0DH (n = 1), 0EH (n = 2), 0FH (n = 3), 10H (n = 4) After reset: 80H R/W

	7	6	5	4	3	2	1	0
DACnC	DACn7	DACn6	DACn5	DACn4	DACn3	DACn2	DACn1	DACn0

Remark 1. n = 1 to 4

2. To calculate the output voltage, see **5. 1 Overview of D/A converter features**.

(3) Power control register 1 (PC1)

This register is used to enable or disable operation of the configurable amplifiers, the general-purpose operational amplifier, and the D/A converters. Use this register to stop unused functions to reduce power consumption and noise. When using one of D/A converter channels Ch1 to Ch4, be sure to set the control bit that corresponds to the channel (bits 7 to 4) to 1.
Reset signal input clears this register to 00H.

Address: 11H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	AMP4OF	AMP3OF	AMP2OF	AMP1OF

DAC4OF	Operation of D/A converter Ch4
0	Stop operation of D/A converter Ch4.
1	Enable operation of D/A converter Ch4.

DAC3OF	Operation of D/A converter Ch3
0	Stop operation of D/A converter Ch3.
1	Enable operation of D/A converter Ch3.

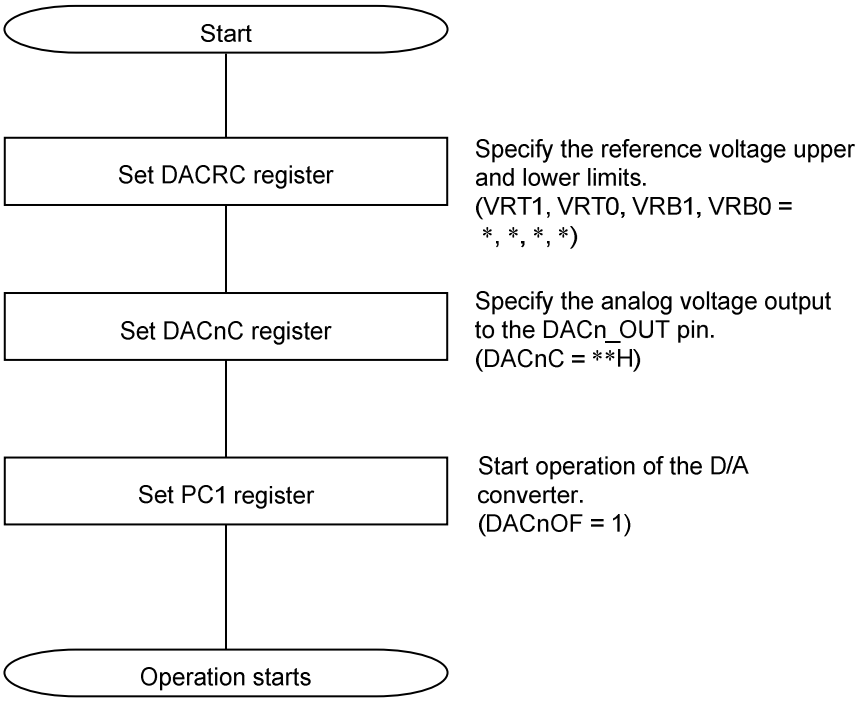
DAC2OF	Operation of D/A converter Ch2
0	Stop operation of D/A converter Ch2.
1	Enable operation of D/A converter Ch2.

DAC1OF	Operation of D/A converter Ch1
0	Stop operation of D/A converter Ch1.
1	Enable operation of D/A converter Ch1.

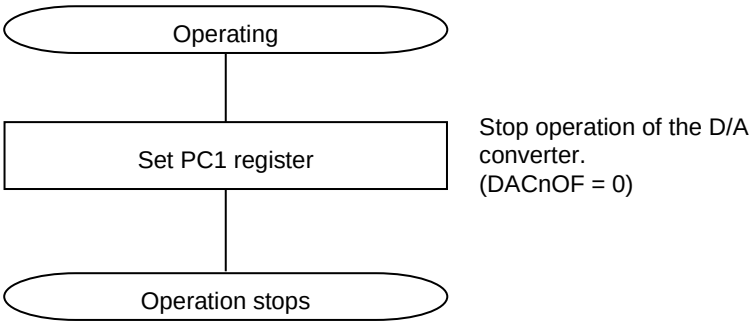
5.4 Procedure for Operating the D/A Converters

Follow the procedures below to start and stop the D/A converters.

Example of procedure for starting the D/A converters



Example of procedure for stopping the D/A converters



Remark *: don't care
n = 1 to 4

5.5 Notes on Using D/A Converters

Observe the following points when using the D/A converters:

(1) Only a very small current can flow from the DACn_OUT pin because the output impedance of the D/A converters is high. If the load input impedance is low, insert a follower amplifier between the load and the DACn_OUT pin. Also, make sure that the wiring between the pin and the follower amplifier or load is as short as possible (because of the high output impedance). If it is not possible to keep the wiring short, take measures such as surrounding the pin with a ground pattern.

(2) If inputting an external reference power supply to the VREFINn pin, be sure to set the DACnOF bit to 0.

Remark n = 1 to 4

6. Low-Pass Filter

The RAA730500 has one on-chip switched-capacitor low-pass filter channel.

<R> 6.1 Overview of Low-Pass Filter Features

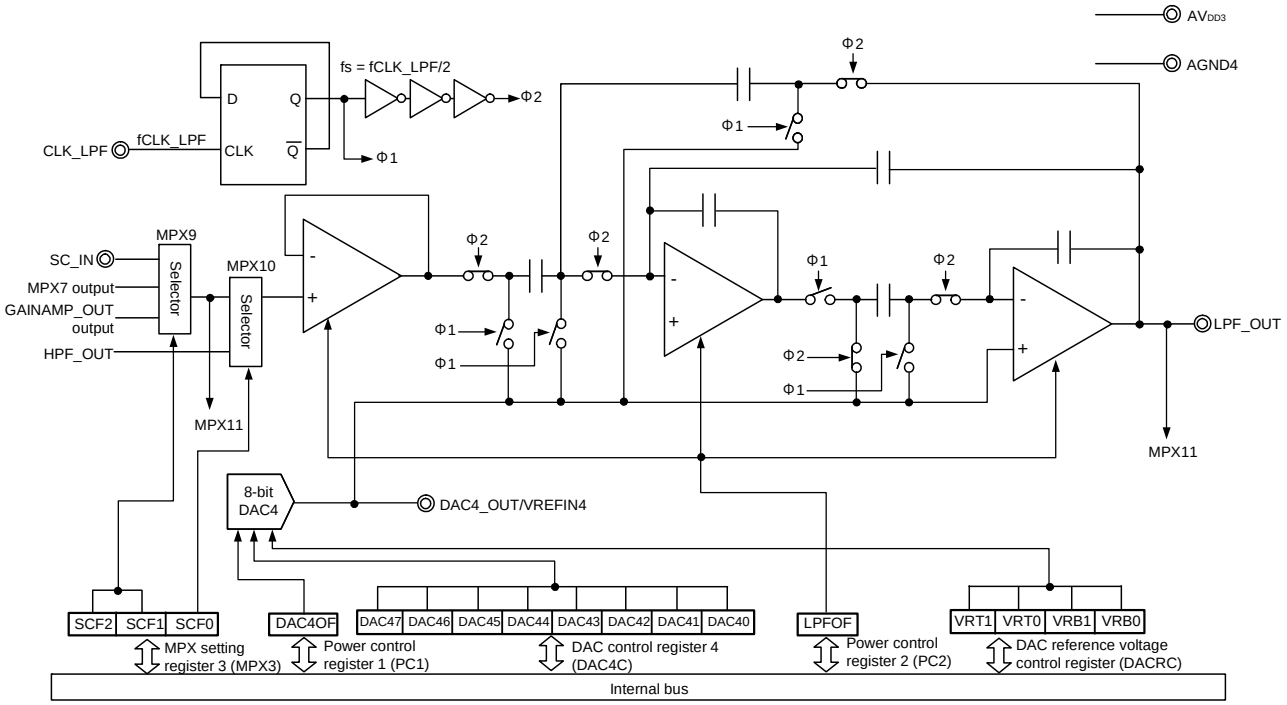
- Butterworth characteristics (Q value = 0.702)
- Cutoff frequency (fc) range: 9 Hz to 4.5 kHz
- External input clock frequency (f_{CLK_LPF}) range: $f_C \times 2/0.009$ = 2 kHz to 1 MHz
- Includes a power-off function.

And also, the DAC4_OUT output signals can be used as the reference voltage for low-pass filter. If D/A converter is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin. For details about use of D/A converter, see **5 D/A Converter**.

Remarks 1. The internal control clock (fs) of the low-pass filter has a duty of 50%, so the external input clock is divided by two at the internal D flip-flop before being used for the low-pass filter. If the internal control clock frequency (fs) is 100 kHz, therefore, input a 200 kHz clock signal to the CLK_LPF pin.

2. The phase of the signal input to the low-pass filter inverts after passing through the low-pass filter.

6.2 Block Diagram



6.3 Registers Controlling the Low-Pass Filter

The low-pass filter is controlled by the following 2 registers:

- MPX setting register 3 (MPX3)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX9, MPX10, and MPX11.
When selecting the signal to be input to the filter circuits, use bits 5 and 4.
When switching the order in which signals are processed by the low-pass and high-pass filters, use bit 3.
Reset signal input clears this register to 00H.

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

SCF2	SCF1	Source of input to filter circuits
0	0	SC_IN pin
0	1	MPX7 output signal
1	0	Synchronous detection amplifier output signal
1	1	Setting prohibited

SCF0	Specification of the order of filter signal processing
0	The MPX9 output signal passes the low-pass filter and then is input to the high-pass filter.
1	The MPX9 output signal passes the high-pass filter and then is input to the low-pass filter.

Remark Bits 7 and 6 are fixed at 0 of read only.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the synchronous detection amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using the low-pass filter, be sure to set bit 3 to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

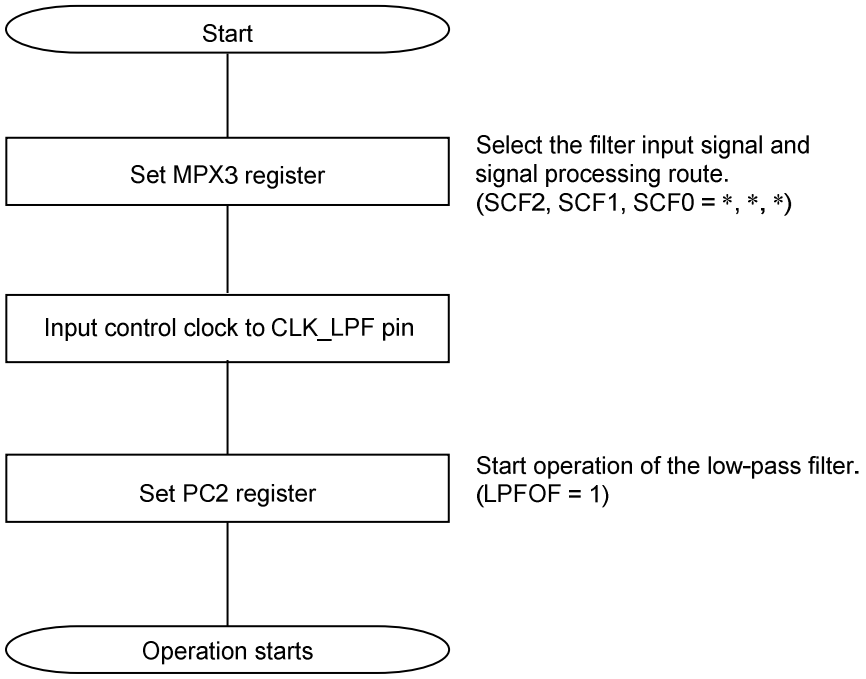
LPFOF	Operation of low-pass filter
0	Stop operation of the low-pass filter.
1	Enable operation of the low-pass filter.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

6.4 Procedure for Operating the Low-Pass Filter

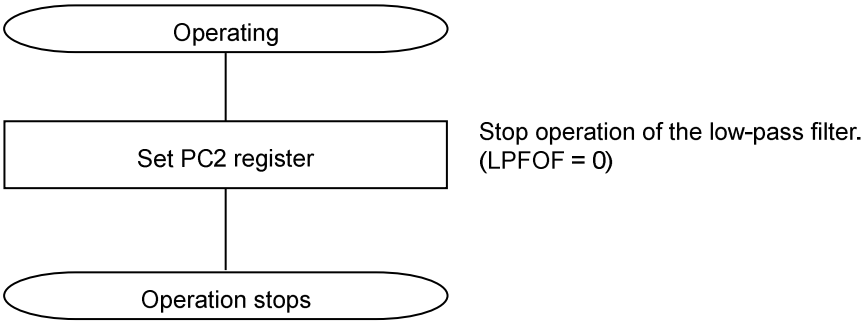
Follow the procedures below to start and stop the low-pass filter.

Example of procedure for starting the low-pass filter



Remark *: don't care

Example of procedure for stopping the low-pass filter



7. High-Pass Filter

The RAA730500 has one on-chip switched-capacitor high-pass filter channel.

<R> 7.1 Overview of High-Pass Filter Features

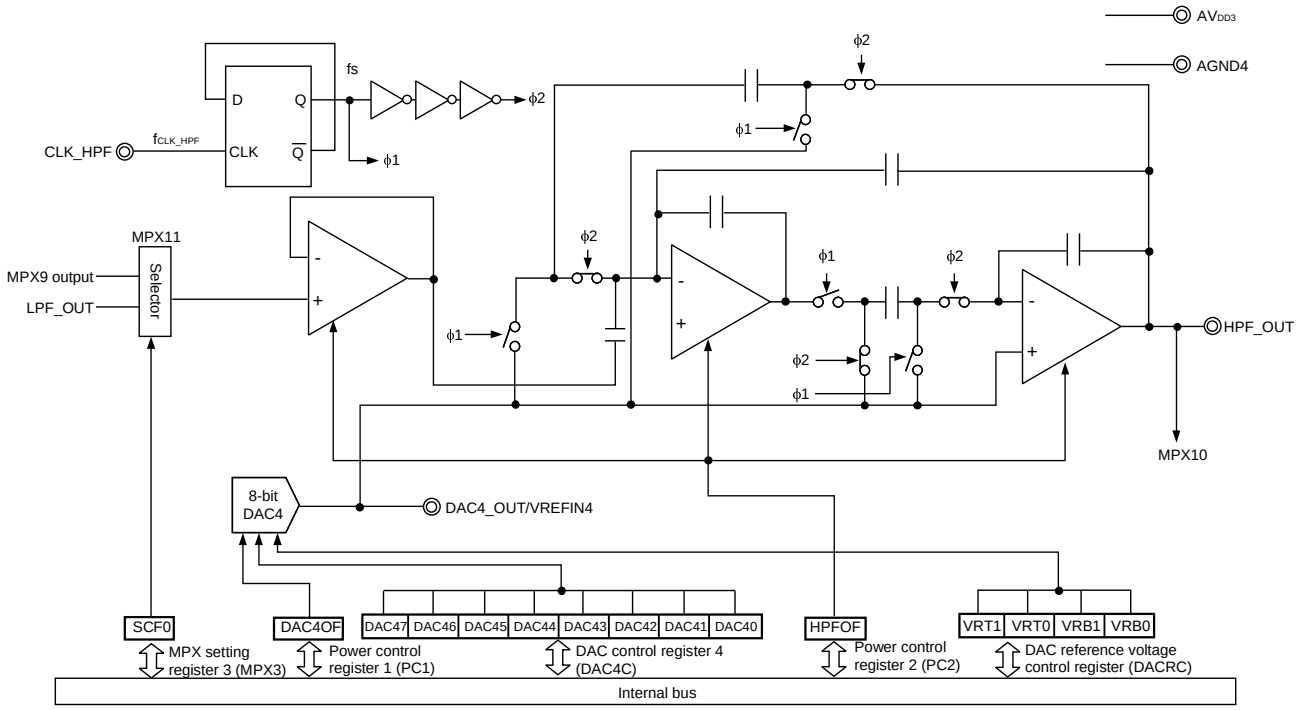
- Butterworth characteristics (Q value = 0.702)
- Cutoff frequency (fc) range: 8 to 800 Hz
- External input clock frequency (f_{CLK_HPF}) range: $f_C \times 2/0.008$ = 2 to 200 kHz
- Includes a power-off function.

And also, the DAC4_OUT output signals can be used as the reference voltage for high-pass filter. If D/A converter is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin. For details about use of D/A converter, see **5. D/A Converter**.

Remarks 1. The internal control clock (fs) of the high-pass filter has a duty of 50%, so the external input clock is divided by two at the internal D flip-flop before being used for the low-pass filter. If the internal control clock frequency (fs) is 100 kHz, therefore, input a 200 kHz clock signal to the CLK_HPF pin.

2. The phase of the signal input to the high-pass filter inverts after passing through the low-pass filter.

7.2 Block Diagram



7.3 Registers Controlling the High-Pass Filter

The high-pass filter is controlled by the following 2 registers:

- MPX setting register 3 (MPX3)
- Power control register 2 (PC2)

<R> **(1) MPX setting register 3 (MPX3)**

This register is used to control MPX7, MPX9, MPX10, and MPX11.
When selecting the signal to be input to the filter circuits, use bits 5 and 4.
When switching the order in which signals are processed by the low-pass and high-pass filters, use bit 3.
Reset signal input clears this register to 00H.

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

SCF2	SCF1	Source of input to filter circuits
0	0	SC_IN pin
0	1	MPX7 output signal
1	0	Synchronous detection amplifier output signal
1	1	Setting prohibited

SCF0	Specification of the order of filter signal processing
0	The MPX9 output signal passes the low-pass filter and then is input to the high-pass filter.
1	The MPX9 output signal passes the high-pass filter and then is input to the low-pass filter.

Remark Bits 7 and 6 are fixed at 0 of read only.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the synchronous detection amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using the high-pass filter, be sure to set bit 2 to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

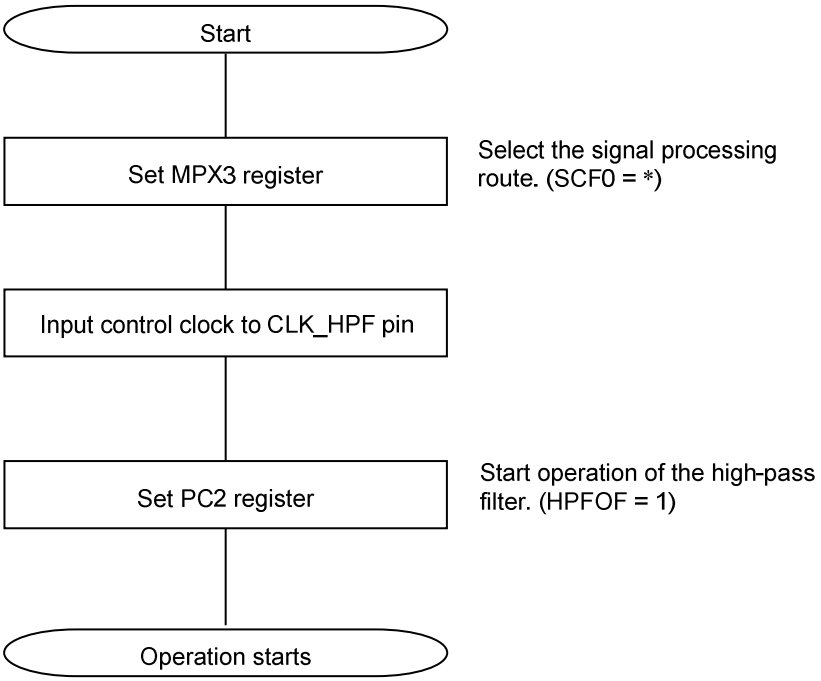
HPFOF	Operation of high-pass filter
0	Stop operation of the high-pass filter.
1	Enable operation of the high-pass filter.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

7.4 Procedure for Operating the High-Pass Filter

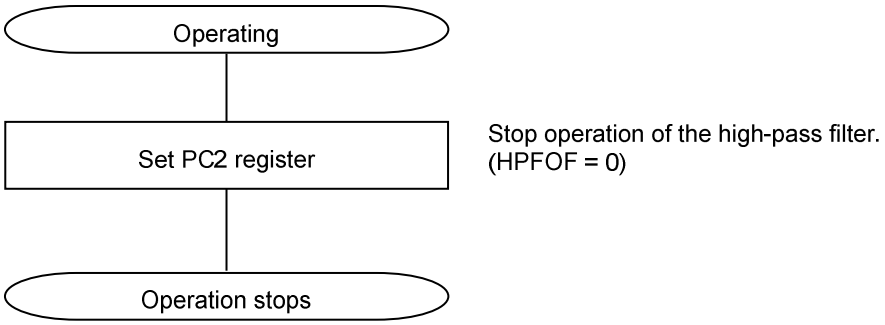
Follow the procedures below to start and stop the high-pass filter.

Example of procedure for starting the high-pass filter



Remark *: don't care

Example of procedure for stopping the high-pass filter



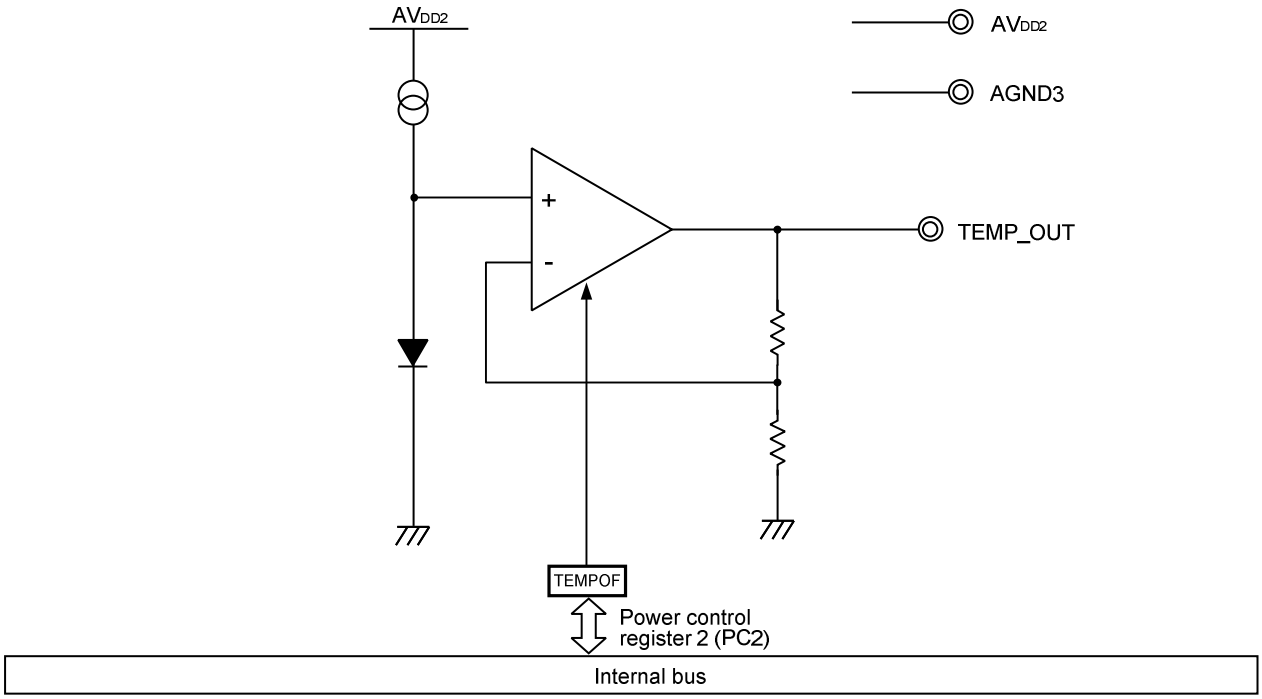
8. Temperature Sensor

The RAA730500 has one on-chip temperature sensor channel.

8.1 Overview of Temperature Sensor Features

- Output voltage temperature coefficient: -5mV/°C (Typ.)
- Includes a power-off function.

8.2 Block Diagram



8.3 Registers Controlling the Temperature Sensor

The temperature sensor is controlled by the following register:

- Power control register 2 (PC2)

(1) Power control register 2 (PC2)

This register is used to enable or disable operation of the synchronous detection amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When selecting the signal to be input to the temperature sensor, be sure to set bit 0 to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00 R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

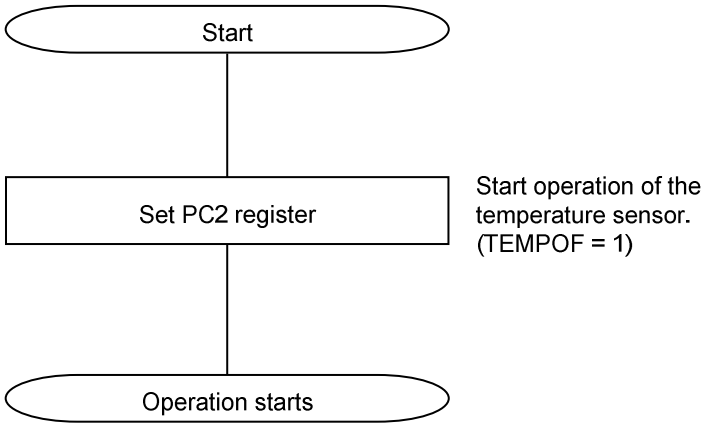
TEMPOF	Operation of temperature sensor
0	Stop operation of the temperature sensor.
1	Enable operation of the temperature sensor.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

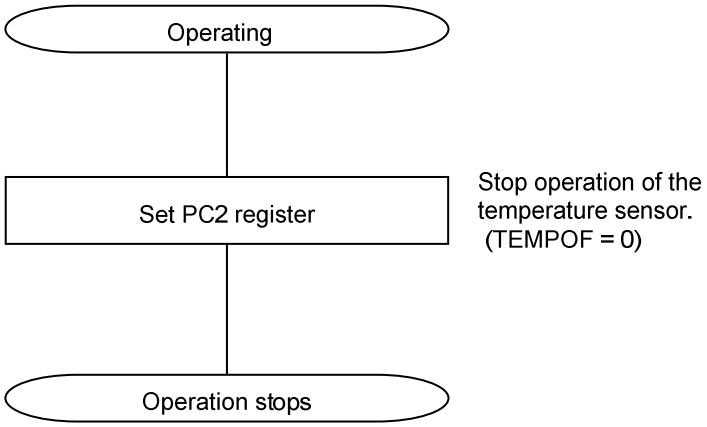
8.4 Procedure for Operating the Temperature Sensor

Follow the procedures below to start and stop the temperature sensor.

Example of procedure for starting the temperature sensor



Example of procedure for stopping the temperature sensor



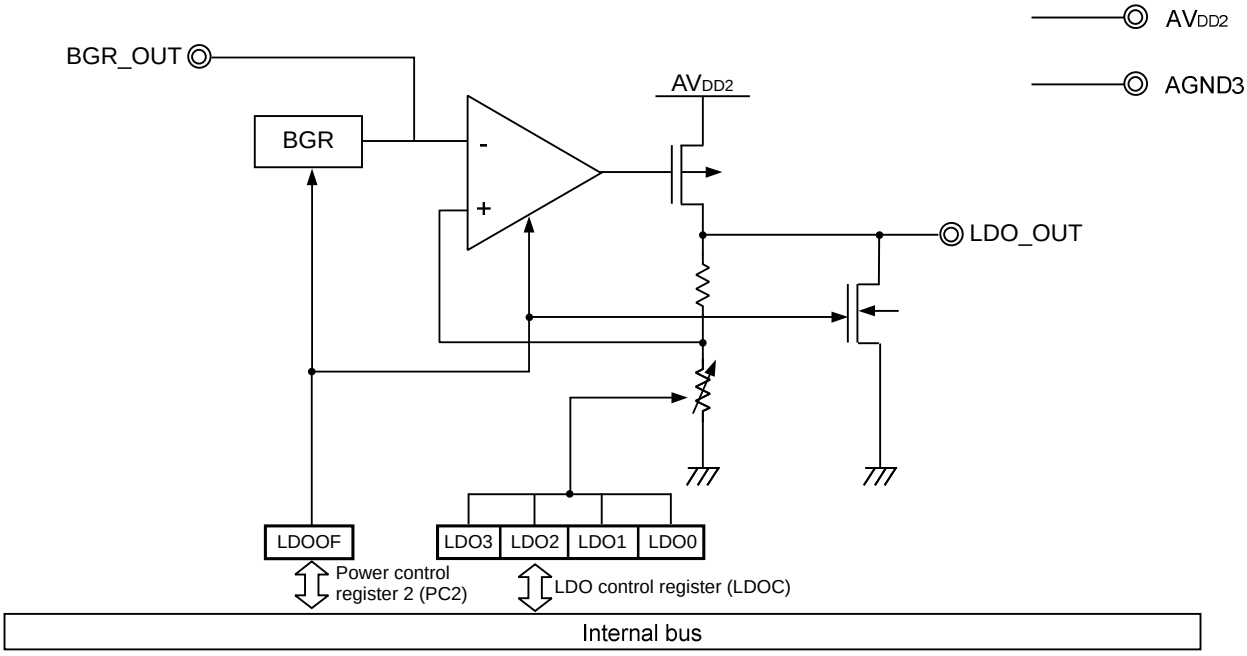
9. Variable Output Voltage Regulator

The RAA730500 has one on-chip variable output voltage regulator channel. This is a series regulator that generates a voltage of 3.3 V (default) from a supplied voltage of 5 V.

9.1 Overview of Variable Output Voltage Regulator Features

- Output voltage range: 2.0 to 3.3 V (Typ.)
- Output current: 15 mA (Max.)
- Includes a power-off function.

9.2 Block Diagram



9.3 Registers Controlling the Variable Output Voltage Regulator

The variable output voltage regulator is controlled by the following 2 registers:

- LDO control register (LDOC)
- Power control register 2 (PC2)

(1) LDO control register (LDOC)

This register is used to specify the output voltage of the variable output voltage regulator.
Reset signal input sets this register to 0DH.

Address: 0BH After reset: 0DH R/W

	7	6	5	4	3	2	1	0
LDOC	0	0	0	0	LDO3	LDO2	LDO1	LDO0

LDO3	LDO2	LDO1	LDO0	Output Voltage of Variable Output Voltage Regulator (Typ.)
0	0	0	0	2.0 V
0	0	0	1	2.1 V
0	0	1	0	2.2 V
0	0	1	1	2.3 V
0	1	0	0	2.4 V
0	1	0	1	2.5 V
0	1	1	0	2.6 V
0	1	1	1	2.7 V
1	0	0	0	2.8 V
1	0	0	1	2.9 V
1	0	1	0	3.0 V
1	0	1	1	3.1 V
1	1	0	0	3.2 V
1	1	0	1	3.3 V Note
Other than above				Setting prohibited

Note Output voltage of 3.3 V is available when the power supply voltage is 4 V or more.

Remark Bits 7 to 4 are fixed at 0 of read only.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the synchronous detection amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using the variable output voltage regulator and reference voltage generator, be sure to set bit 1 to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

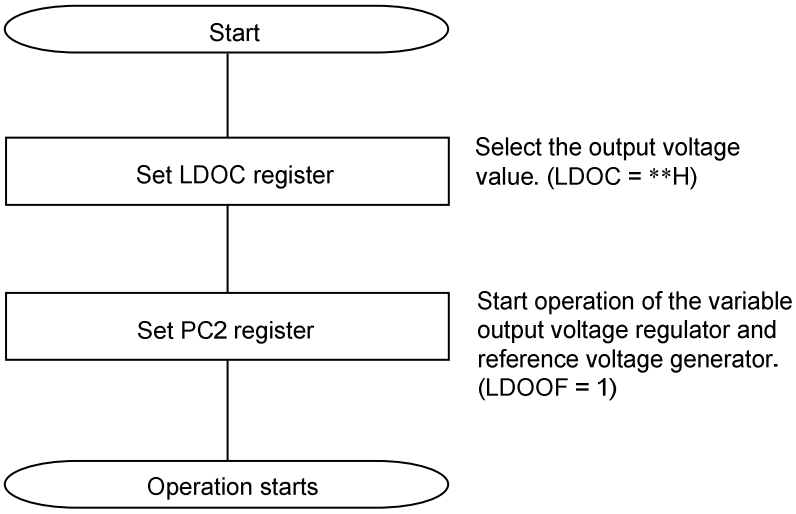
LDOOF	Operation of variable output voltage regulator and reference voltage generator
0	Stop operation of the variable output voltage regulator and reference voltage generator.
1	Enable operation of the variable output voltage regulator and reference voltage generator.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

9.4 Procedure for Operating the Variable Output Voltage Regulator

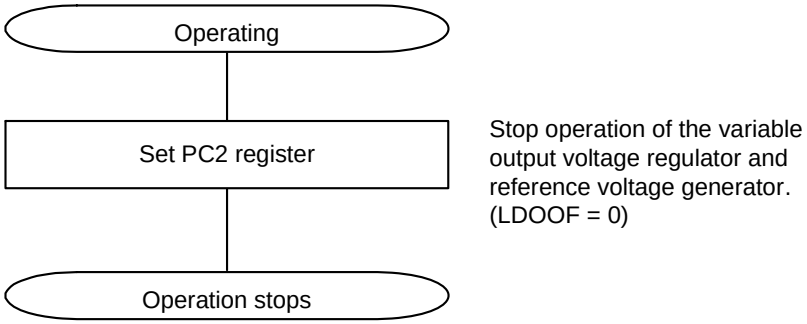
Follow the procedures below to start and stop the variable output voltage regulator and reference voltage generator.

Example of procedure for starting the variable output voltage regulator and reference voltage generator



Remark *: don't care

Example of procedure for stopping the variable output voltage regulator and reference voltage generator



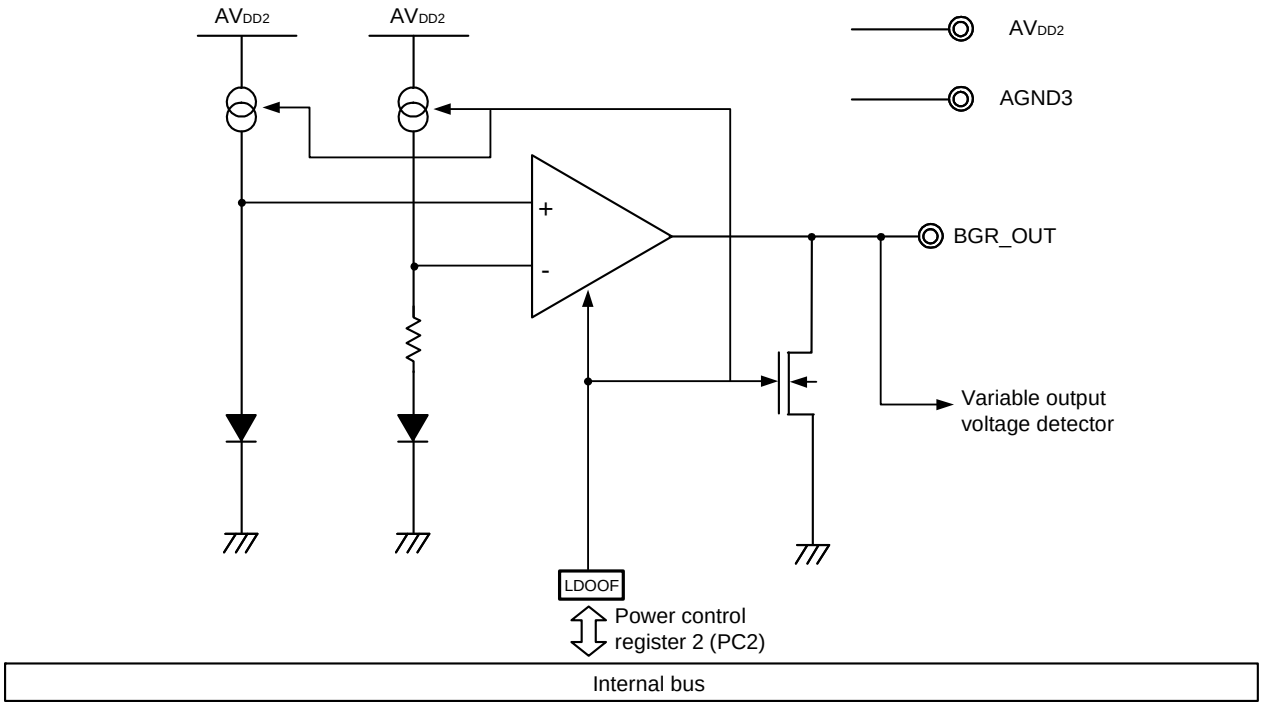
10. Reference Voltage Generator

The RAA730500 has one on-chip reference voltage generator channel.

10.1 Overview of Reference Voltage Generator Features

- Output reference voltage: 1.21 V (Typ.)
- Includes a power-off function.

10.2 Block Diagram



10.3 Registers Controlling the Reference Voltage Generator

The reference voltage generator is controlled by power control register 2 (PC2).
For details about the setting of power control register 2, see **9.3 (2) Power control register 2 (PC2)**.

10.4 Procedure for Operating the Reference Voltage Generator

For details about the procedures to start and stop the reference voltage generator, see **9.4 Procedure for Operating the Variable Output Voltage Regulator**.

10.5 Notes on Using the Reference Voltage Generator

Observe the following points when using the reference voltage generator:

(1) Only a very small current can flow from the BGR_OUT pin because the output impedance of the reference voltage generator is high. If the load input impedance is low, insert a follower amplifier between the load and the BGR_OUT pin. Also, make sure that the wiring between the pin and the follower amplifier or load is as short as possible (because of the high output impedance). If it is not possible to keep the wiring short, take measures such as surrounding the pin with a ground pattern.

11. SPI

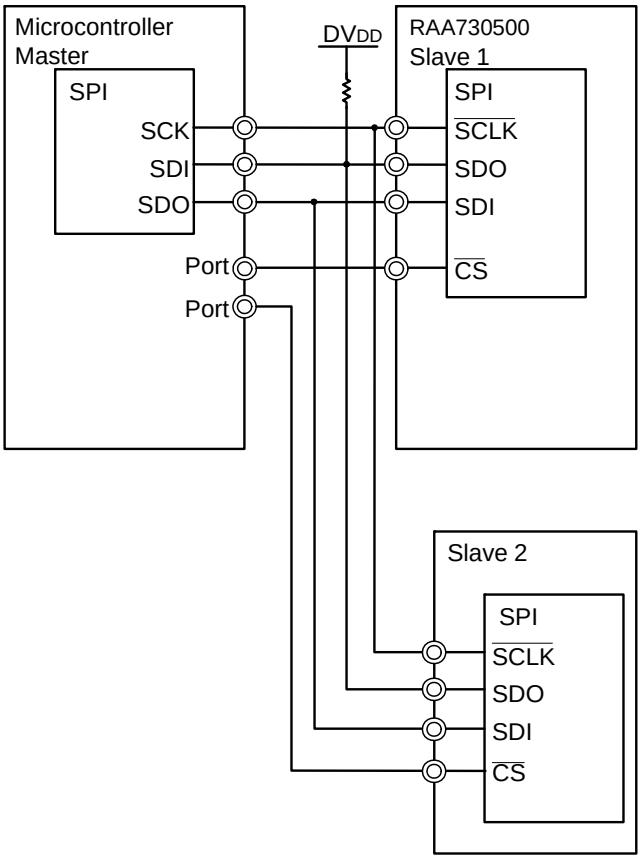
11.1 Overview of SPI Features

The SPI is used to allow control from external devices by using clocked communication via four lines: a serial clock line ($\overline{SCLK}$), two serial data lines (SDI and SDO), and a chip select input line ($\overline{CS}$).

Data transmission/reception:

- 16-bit data unit
- MSB first

Figure 11-1. SPI Configuration Example



<R> **Caution After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{RESET}$ pin before starting SPI communication. For details, see 12 Reset.**

11.2 SPI Communication

The SPI transmits and receives data in 16-bit units. Data can be transmitted and received when $\overline{CS}$ is low. Data is transmitted one bit at a time in synchronization with the falling edge of the serial clock, and is received one bit at a time in synchronization with the rising edge of the serial clock. When the R/W bit is 1, data is written to the SPI control register in accordance with the address/data setting after the 16th rising edge of $\overline{SCLK}$ has been detected following the fall of $\overline{CS}$. The operation specified by the data is then executed. When the R/W bit is 0, the data is output from the register in accordance with the address/data setting in synchronization with the 9th and later falling edges of $\overline{SCLK}$ following the fall of $\overline{CS}$.

Figure 11-2. SPI Communication Timing

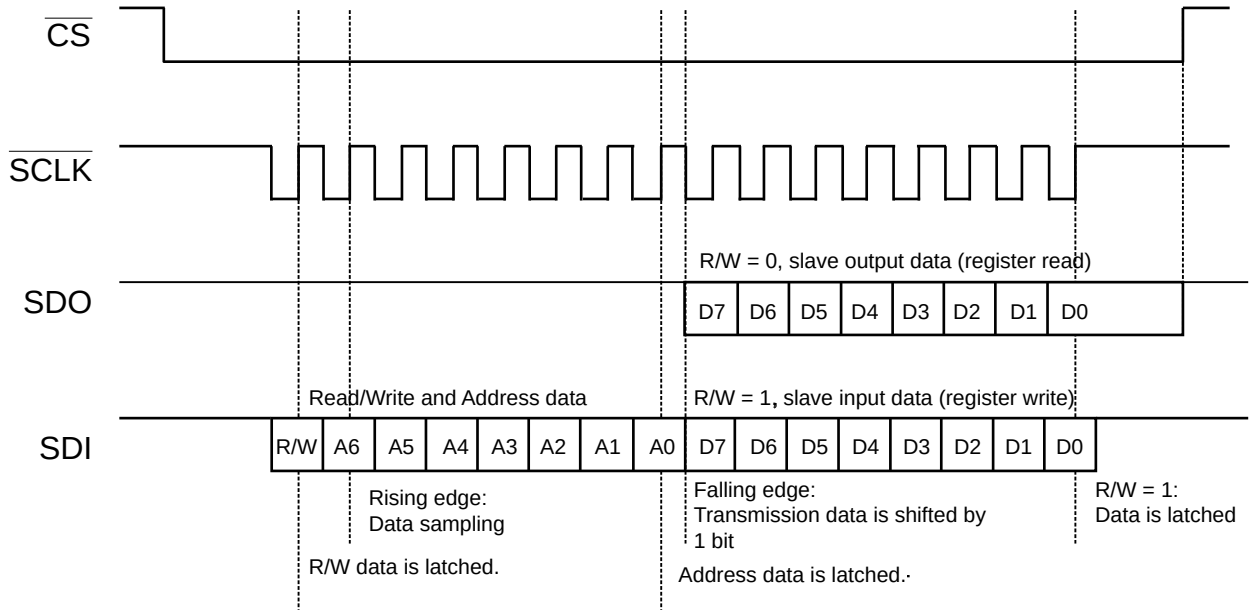


Table 11-1. SPI Control Registers

Address	SPI Control Register	R/W	After Reset
00H	Configuration register 1 (CONFIG1)	R/W	00H
01H	Configuration register 2 (CONFIG2)	R/W	00H
03H	MPX setting register 1 (MPX1)	R/W	00H
04H	MPX setting register 2 (MPX2)	R/W	00H
05H	MPX setting register 3 (MPX3)	R/W	00H
06H	Gain control register 1 (GC1)	R/W	00H
07H	Gain control register 2 (GC2)	R/W	00H
08H	Gain control register 3 (GC3)	R/W	00H
09H	AMP operation mode control register (AOMC)	R/W	00H
0AH	Gain control register 4 (GC4)	R/W	00H
0BH	LDO control register (LDOC)	R/W	0DH
0CH	DAC reference voltage control register (DACRC)	R/W	00H
0DH	DAC control register 1 (DAC1C)	R/W	80H
0EH	DAC control register 2 (DAC2C)	R/W	80H
0FH	DAC control register 3 (DAC3C)	R/W	80H
10H	DAC control register 4 (DAC4C)	R/W	80H
11H	Power control register 1 (PC1)	R/W	00H
12H	Power control register 2 (PC2)	R/W	00H
13H	Reset control register (RC)	R/W	00H[Note]

Note The reset control register (RC) is not initialized to 00H by generating internal reset of the reset control register (RC). For details, see **12. Reset**.

<R> 12. Reset

12.1 Overview of Reset Feature

The RAA730500 has an on-chip reset function. The SPI control registers are initialized by reset. A reset can be generated in the following two ways:

- External reset by inputting an external reset signal to the $\overline{\text{RESET}}$ pin
- Internal reset by writing 1 to the RESET bit of the reset control register (RC)

The functions of the external reset and the internal reset are described below.

- After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{\text{RESET}}$ pin before starting SPI communication.
- During reset, each function is shifted to the status shown in Table 12-1. The status of each SPI control register after reset has been acknowledged is shown in Table 12-2. After reset, the status of each pin is shown in Table 12-3.
- External reset is generated when a low-level signal is input to the $\overline{\text{RESET}}$ pin. On the other hand, internal reset is generated when 1 is written to the RESET bit of the reset control register (RC).
- External reset is subsequently cancelled by inputting a high-level signal to $\overline{\text{RESET}}$ pin after a low-level signal is input to this pin. On the other hand, internal reset is subsequently cancelled by writing 0 to the RESET bit of the reset control register (RC) after 1 is written to the same bit of this register.

Caution When generating an external reset, input a low-level signal to the $\overline{\text{RESET}}$ pin for at least 10 μs.

Table 12-1. Statuses During Reset

Function Block	External Reset from $\overline{\text{RESET}}$ Pin	Internal Reset by Reset Control Register (RC)
Configurable amplifier	Operation stops.	
General-purpose operational amplifier	Operation stops.	
Synchronous detection amplifier	Operation stops.	
D/A converter	Operation stops.	
Low-pass filter	Operation stops.	
High-pass filter	Operation stops.	
Temperature sensor	Operation stops.	
Variable output voltage regulator	Operation stops.	
Reference voltage generator	Operation stops.	
SPI	Operation stops.	Operation is enabled.

Table 12-2. Statuses of SPI Control Registers After a Reset Is Acknowledged

Address	SPI Control Register	Status After a Reset Is Acknowledged	
		External Reset	Internal Reset
00H	Configuration register 1 (CONFIG1)	00H	00H
01H	Configuration register 2 (CONFIG2)	00H	00H
03H	MPX setting register 1 (MPX1)	00H	00H
04H	MPX setting register 2 (MPX2)	00H	00H
05H	MPX setting register 3 (MPX3)	00H	00H
06H	Gain control register 1 (GC1)	00H	00H
07H	Gain control register 2 (GC2)	00H	00H
08H	Gain control register 3 (GC3)	00H	00H
09H	AMP operation mode control register (AOMC)	00H	00H
0AH	Gain control register 4 (GC4)	00H	00H
0BH	LDO control register (LDOC)	0DH	0DH
0CH	DAC reference voltage control register (DACRC)	00H	00H
0DH	DAC control register 1 (DAC1C)	80H	80H
0EH	DAC control register 2 (DAC2C)	80H	80H
0FH	DAC control register 3 (DAC3C)	80H	80H
10H	DAC control register 4 (DAC4C)	80H	80H
11H	Power control register 1 (PC1)	00H	00H
12H	Power control register 2 (PC2)	00H	00H
13H	Reset control register (RC)	00H[Note]	01H[Note]

Note The reset control register (RC) is not initialized by generating internal reset of the reset control register (RC), but it can be done to 00H by generating external reset from $\overline{\text{RESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Table 12-3. Pin Statuses After a Reset

Pin Name	External Reset from $\overline{\text{RESET}}$ Pin	Internal Reset by Reset Control Register (RC)
SC_IN	Hi-Z	Hi-Z
CLK_SYNCH	Pull-down input	Pull-down input
SYNCH_OUT	Hi-Z	Hi-Z
GAINAMP_OUT	Hi-Z	Hi-Z
GAINAMP_IN	Hi-Z	Hi-Z
MPXIN61	Hi-Z	Hi-Z
MPXIN51	Hi-Z	Hi-Z
MPXIN60	Hi-Z	Hi-Z
MPXIN50	Hi-Z	Hi-Z
AMP3_OUT	Hi-Z	Hi-Z
DAC3_OUT/VREFIN3	Pull-down input	Pull-down input
AMP2_OUT	Hi-Z	Hi-Z
AMP1_OUT	Hi-Z	Hi-Z
DAC2_OUT/VREFIN2	Pull-down input	Pull-down input
DAC1_OUT/VREFIN1	Pull-down input	Pull-down input
MPXIN41	Hi-Z	Hi-Z
MPXIN31	Hi-Z	Hi-Z
MPXIN40	Hi-Z	Hi-Z
MPXIN30	Hi-Z	Hi-Z
MPXIN21	Hi-Z	Hi-Z
MPXIN11	Hi-Z	Hi-Z
MPXIN20	Hi-Z	Hi-Z
MPXIN10	Hi-Z	Hi-Z
BGR_OUT	Pull-down	Pull-down
LDO_OUT	Pull-down	Pull-down
AMP4_OUT	Hi-Z	Hi-Z
AMP4_INN	Hi-Z	Hi-Z
AMP4_INP	Hi-Z	Hi-Z
TEMP_OUT	Pull down	Pull down
$\overline{\text{SCLK}}$	Hi-Z	Pull-up input
SDO	Hi-Z (open drain)	Hi-Z (open drain)
SDI	Hi-Z	Pull-up input
$\overline{\text{CS}}$	Hi-Z	Pull-up input
DAC4_OUT/VREFIN4	Pull-down input	Pull-down input
HPF_OUT	Hi-Z	Hi-Z
CLK_HPF	Pull-down input	Pull-down input
CLK_LPF	Pull-down input	Pull-down input
LPF_OUT	Hi-Z	Hi-Z

12.2 Registers Controlling the Reset Feature

(1) Reset control register (RC)

This register is used to control the reset feature.

An internal reset can be generated by writing 1 to the RESET bit. The reset control register (RC) is initialized to 00H by generating external reset from $\overline{\text{RESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Address: 13H After reset: 00H[Note] R/W

	7	6	5	4	3	2	1	0
RC	0	0	0	0	0	0	0	RESET

RESET	Reset request by internal reset signal
0	Do not make a reset request by using the internal reset signal, or cancel the reset.
1	Make a reset request by using the internal reset signal, or the reset signal is currently being input.

Note The reset control register (RC) is not initialized by generating internal reset of the reset control register (RC), but it can be done to 00H by generating external reset from $\overline{\text{RESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Caution When the RESET bit is 1, writing to any register other than the reset control register (RC) is ignored. Initializing the reset control register (RC) to 00H by external reset, or writing 0 to the RESET bit enable writing to all the registers.

Remark Bits 7 to 1 are fixed at 0 of read only.

13. Electrical Specifications

13.1 Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	AV_{DD}	AV_{DD1}, AV_{DD2}, AV_{DD3}	-0.3 to +6.0	V
	DV_{DD}	DV_{DD}	-0.3 to +6.0	V
	AGND	AGND1, AGND2, AGND3, AGND4	-0.3 to +0.3	V
	DGND	DGND	-0.3 to +0.3	V
Input voltage	V_{I1}	MPXIN10, MPXIN11, MPXIN20, MPXIN21, MPXIN30, MPXIN31, MPXIN40, MPXIN41, MPXIN50, MPXIN51, MPXIN60, MPXIN61, SC_IN, CLK_SYNCH, VREFIN1, VREFIN2, VREFIN3, VREFIN4, AMP4_INN, AMP4_INP, CLK_LPF, CLK_HPF, RESET	-0.3 to AV_{DD} + 0.3[Note]	V
	V_{I2}	$\overline{SCLK}$, SDI, $\overline{CS}$	-0.3 to DV_{DD} + 0.3[Note]	V
Output voltage	V_{O1}	LDO_OUT, BGR_OUT, AMP1_OUT, AMP2_OUT, AMP3_OUT, AMP4_OUT, GAINAMP_OUT, SYNCH_OUT, LPF_OUT, HPF_OUT, DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT, TEMP_OUT	-0.3 to AV_{DD} + 0.3[Note]	V
	V_{O2}	SDO	-0.3 to DV_{DD} + 0.3[Note]	V
Output current	I_{O1}	AMP1_OUT, AMP2_OUT, AMP3_OUT, AMP4_OUT, GAINAMP_OUT, SYNCH_OUT LPF_OUT, HPF_OUT DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT, TEMP_OUT	1	mA
	I_{O2}	SDO	-10	mA
	I_{LDOOUT}	LDO_OUT	15	mA
Operating ambient temperature	T_A		-40 to +105	°C
<R> Storage temperature	T_{stg}		-40 to +150	°C

Note Must be 6.0 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

<R> 13.2 Operating condition

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Power supply voltage range	V_{DDOP}	AV_{DD1}, AV_{DD2}, AV_{DD3}, DV_{DD}	3.0	–	5.5	V
Operating temperature range	T_{OP}		-40	–	105	°C

13.3 Supply Current Characteristics

($-40°C \le T_A \le 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0$ V)

Parameter	Symbol	Conditions		Ratings			Unit
				MIN	TYP	MAX	
<R> Supply current	I_{stby11} Note	PC1 = 00H, PC2 = 00H	T_A = -40°C	–	100	150	nA
			T_A = +25°C	–	140	210	nA
			T_A = +50°C	–	290	550	nA
			T_A = +85°C	–	850	1850	nA
			T_A = +105°C	–	1600	4000	nA
	I_{m111} Note	PC1 = 47H (configurable amplifiers Ch1 to Ch3 and D/A converters Ch3 are operating) PC2 = 00H, CC1, CC0 = 0, 0, DACRC = 00H		–	1.55	3.6	mA
	I_{m112} Note	PC1 = F7H, PC2 = 13H (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, synchronous detection amplifier, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 0, 0, DACRC = 00H		–	3.4	7.6	mA
	I_{m113} Note	PC1 = 7FH, PC2 = 0FH (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, low-pass filter, high-pass filter, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 0, 0, DACRC = 00H		–	4.5	11.0	mA
	I_{m114} Note	PC1 = FFH, PC2 = 1FH (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, general-purpose operational amplifier, low-pass filter, high-pass filter, synchronous detection amplifier, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 0, 0, DACRC = 00H		–	5.0	12.4	mA
	I_{m121} Note	PC1 = 47H (configurable amplifiers Ch1 to Ch3 and D/A converters Ch1 to Ch3 are operating), CC1, CC0 = 1, 1, DACRC = 00H		–	0.73	1.8	mA
	I_{m122} Note	PC1 = F7H, PC2 = 13H (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, synchronous detection amplifier, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 1, 1, DACRC = 00H		–	2.6	5.8	mA
	I_{m123} Note	PC1 = F7H, PC2 = 0FH (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, low-pass filter, high-pass filter, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 1, 1, DACRC = 00H		–	3.7	9.2	mA
	I_{m124} Note	PC1 = FFH, PC2 = 1FH (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, genenal-purpose operational amplifier, low-pass filter, high-pass filter, synchronous detection amplifier, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 1, 1, DACRC = 00H		–	4.4	10.6	mA

Note Total current flowing to internal power supply pins AV_{DD1}, AV_{DD2}, AV_{DD3}, and DV_{DD}. Current flowing through the pull-up resistor is not included. The input leakage current flowing when the level of the input pin is fixed to AV_{DD1}, AV_{DD2}, AV_{DD3} or DV_{DD}, or AGND1, AGND2, AGND3, AGND4, or DGND is included. See the table below to check the definition of those symbols of the current flowing.

Parameter	Symbol	Analog function with power on												
		Configurable amplifier			General-purpose operational amplifier	Gain amplifier and synchronous detector	D/A converter				Low-pass filter	High-pass filter	Temperature sensor	Variable output voltage regulator
		Ch 1	Ch 2	Ch 3			Ch 1	Ch 2	Ch 3	Ch 4				
Supply current	Im111 Note1	ON	ON	ON	–	–	–	–	ON	–	–	–	–	–
	Im112 Note1	ON	ON	ON	–	ON	ON	ON	ON	ON	–	–	ON	ON
	Im113 Note1	ON	ON	ON	–	–	ON	ON	ON	ON	ON	ON	ON	ON
	Im114 Note1	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
	Im121 Note2	ON	ON	ON	–	–	–	–	ON	–	–	–	–	–
	Im122 Note2	ON	ON	ON	–	ON	ON	ON	ON	ON	–	–	ON	ON
	Im123 Note2	ON	ON	ON	–	–	ON	ON	ON	ON	ON	ON	ON	ON
	Im124 Note2	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON

Note1. CC1, CC0 = 0, 0

2. CC1, CC0 = 1, 1

13.4 Electrical Specifications of Each Block

(1) Configurable amplifier block characteristics

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, non-inverting amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CC1, CC0 = 0, 0	–	330	720	µA
	Icc01	CC1, CC0 = 0, 1	–	175	390	µA
	Icc10	CC1, CC0 = 1, 0	–	125	275	µA
	Icc11	CC1, CC0 = 1, 1	–	55	120	µA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 µA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 µA	AV_{DD1} - 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (9.5 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	µs
	t_{SET_AMP01}	GCn = 00H (9.5 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	µs
	t_{SET_AMP10}	GCn = 00H (9.5 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	28	µs
	t_{SET_AMP11}	GCn = 00H (9.5 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	71	µs
Gain bandwidth	GBW00	CLMAX = 30 pF, CC1, CC0 = 0, 0 GCn = 11H (40.1 dB)	–	2.3		MHz
	GBW01	CLMAX = 30 pF,CC1, CC0 = 0, 1 GCn = 11H (40.1 dB)	–	1.1		MHz
	GBW10	CLMAX = 30 pF, CC1, CC0 = 1, 0 GCn = 11H (40.1 dB)	–	0.71		MHz
	GBW11	CLMAX = 30 pF, CC1, CC0 = 1, 1 GCn = 11H (40.1 dB)	–	0.22		MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 f = 1 kHz, GCn = 11H (40.1 dB)	–	64	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 f = 1 kHz, GCn = 11H (40.1 dB)	–	85	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 f = 1 kHz, GCn = 11H (40.1 dB)	–	107	–	nV/√ Hz
	En11	CC1, CC0 = 1, 1 f = 1 kHz, GCn = 11H (40.1 dB)	–	159	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C GCn = 07H (20.8 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C GCn = 07H (20.8 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C GCn = 07H (20.8 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C GCn = 07H (20.8 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	µV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.68	–	V/µs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.35	–	V/µs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.25	–	V/µs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.09	–	V/µs
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0, GCn = 00H (9.5 dB), f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1, GCn = 00H (9.5 dB), f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0, GCn = 00H (9.5 dB), f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1, GCn = 00H (9.5 dB), f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 105°C	-1.0	–	1.0	dB

Remark n = 1 to 3

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF, inverting amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CC1, CC0 = 0, 0	–	330	720	µA
	Icc01	CC1, CC0 = 0, 1	–	175	390	µA
	Icc10	CC1, CC0 = 1, 0	–	125	275	µA
	Icc11	CC1, CC0 = 1, 1	–	55	120	µA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 µA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 µA	AV_{DD1} - 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (6 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	µs
	t_{SET_AMP01}	GCn = 00H (6 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	µs
	t_{SET_AMP10}	GCn = 00H (6 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	28	µs
	t_{SET_AMP11}	GCn = 00H (6 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	71	µs
Gain bandwidth	GBW00	CLMAX = 30 pF,CC1, CC0 = 0, 0 GCn = 11H (40 dB)	–	1.5		MHz
	GBW01	CLMAX = 30 pF,CC1, CC0 = 0, 1 GCn = 11H (40 dB)	–	0.9		MHz
	GBW10	CLMAX = 30 pF,CC1, CC0 = 1, 0 GCn = 11H (40 dB)	–	0.67		MHz
	GBW11	CLMAX = 30 pF,CC1, CC0 = 1, 1 GCn = 11H (40 dB)	–	0.22		MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 f = 1 kHz, GCn = 11H (40 dB)	–	63	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 f = 1 kHz, GCn = 11H (40 dB)	–	85	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 f = 1 kHz, GCn = 11H (40 dB)	–	105	–	nV/√ Hz
	En11	CC1, CC0 = 1, 1 f = 1 kHz, GCn = 11H (40 dB)	–	150	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C GCn = 07H (20 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C GCn = 07H (20 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	µV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (6 dB)	–	0.68	–	V/µs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.35	–	V/µs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GCn = 00H (6 dB)	–	0.25	–	V/µs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.09	–	V/µs
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0 GCn = 00H (6 dB), f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1 GCn = 00H (6 dB), f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0 GCn = 00H (6 dB), f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1 GCn = 00H (6 dB), f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 105°C	-1.0	–	1.0	dB

Remark n = 1 to 3

($-40°C \le T_A \le 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0$ V, VREFIN = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, differential amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CC1, CC0 = 0, 0	–	330	720	µA
	Icc01	CC1, CC0 = 0, 1	–	175	390	µA
	Icc10	CC1, CC0 = 1, 0	–	125	275	µA
	Icc11	CC1, CC0 = 1, 1	–	55	120	µA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 µA	–	AGND1 + 0.02	AGND1+ 0.06	V
	VOUTH	IOH = 200 µA	AV_{DD1}- 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (6 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	µs
	t_{SET_AMP01}	GCn = 00H (6 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	µs
	t_{SET_AMP10}	GCn = 00H (6 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	28	µs
	t_{SET_AMP11}	GCn = 00H (6 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	71	µs
Gain bandwidth	GBW00	CLMAX = 30 pF, CC1, CC0 = 0, 0, GCn = 11H (40 dB)	–	1.5	–	MHz
	GBW01	CLMAX = 30 pF, CC1, CC0 = 0, 1, GCn = 11H (40 dB)	–	1.0	–	MHz
	GBW10	CLMAX = 30 pF, CC1, CC0 = 1, 0, GCn = 11H (40 dB)	–	0.67	–	MHz
	GBW11	CLMAX = 30 pF, CC1, CC0 = 1, 1, GCn = 11H (40 dB)	–	0.22	–	MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 f = 1 kHz, GCn = 11H (40 dB)	–	63	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 f = 1 kHz, GCn = 11H (40 dB)	–	85	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 f = 1 kHz, GCn = 11H (40 dB)	–	106	–	nV/√ Hz
	En11	CC1, CC0 = 1, 1 f = 1 kHz, GCn = 11H (40 dB)	–	160	–	nV/√ Hz
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C GCn = 07H (20 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C GCn = 07H (20 dB)	-12	–	12	mV

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	µV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 Pf, GCn = 00H (6 dB)	–	0.68	–	V/µs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.35	–	V/µs
	SR10	CC1, CC0 = 1, 0 CL = 30 pF, GCn = 00H (6 dB)	–	0.25	–	V/µs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.09	–	V/µs
Common mode rejection ratio	CMRR00	CC1, CC0 = 0, 0, GCn = 11H (40 dB), f = 1 kHz	–	84	–	dB
	CMRR01	CC1, CC0 = 0, 1, GCn = 11H (40 dB) f = 1 kHz	–	82	–	dB
	CMRR10	CC1, CC0 = 1, 0, GCn = 11H (40 dB) f = 1 kHz	–	80	–	dB
	CMRR11	CC1, CC0 = 1, 1, GCn = 11H (40 dB) f = 1 kHz	–	76	–	dB
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0, GCn = 00H (6 dB), f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1, GCn = 00H (6 dB) f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0, GCn = 00H (6 dB) f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1, GCn = 00H (6 dB) f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 105°C	-1.0	–	1.0	dB

Remark n = 1 to 3

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, transimpedance amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CC1, CC0 = 0, 0	–	330	720	µA
	Icc01	CC1, CC0 = 0, 1	–	175	390	µA
	Icc10	CC1, CC0 = 1, 0	–	125	275	µA
	Icc11	CC1, CC0 = 1, 1	–	55	120	µA
Input current	IINL	GCn = 0FH (Rfb = 640 kΩ)	(10)			nA
Output voltage	VOUTL	IOL= -200 µA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 µA	AV_{DD1}- 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (20 kΩ), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	µs
	t_{SET_AMP01}	GCn = 00H (20 kΩ), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	µs
	t_{SET_AMP10}	GCn = 00H (20 kΩ), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	28	µs
	t_{SET_AMP11}	GCn = 00H (20 kΩ), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	71	µs
Current-to-voltage conversion gain bandwidth	GBW00_0	CLMAX = 30 pF, CC1, CC0 = 0, 0, GCn = 00H (Rfb = 20 kΩ)	–	1.3	–	MHz
	GBW00_1	CLMAX = 30 pF, CC1, CC0 = 0, 0, GCn = 0FH (Rfb = 640 kΩ)	–	1.0	–	MHz
	GBW01_0	CLMAX = 30 pF, CC1, CC0 = 0, 1, GCn = 00H (Rfb = 20 kΩ)	–	0.79	–	MHz
	GBW01_1	CLMAX = 30 pF, CC1, CC0 = 0, 1, GCn = 0FH (Rfb = 640 kΩ)	–	0.51	–	MHz
	GBW10_0	CLMAX = 30 pF, CC1, CC0 = 1, 0, GCn = 00H (Rfb = 20 kΩ)	–	0.58	–	MHz
	GBW10_1	CLMAX = 30 pF, CC1, CC0 = 1, 0, GCn = 0FH (Rfb = 640 kΩ)	–	0.31	–	MHz
	GBW11_0	CLMAX = 30 pF, CC1, CC0 = 1, 1, GCn = 00H (Rfb = 20 kΩ)	–	0.25	–	MHz
	GBW11_1	CLMAX = 30 pF, CC1, CC0 = 1, 1, GCn = 0FH (Rfb = 640 kΩ)	–	0.09	–	MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	66	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	90	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	116	–	nV/√ Hz
	En11	CC1, CC0 = 1, 1 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	193	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark1. In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

2. n = 1 to 3

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	µV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.68	–	V/µs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.35	–	V/µs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.25	–	V/µs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.09	–	V/µs
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0, GCn = 00H (Rfb = 20 kΩ)	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1, GCn = 00H (Rfb = 20 kΩ)	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0, GCn = 00H (Rfb = 20 kΩ)	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1, GCn = 00H (Rfb = 20 kΩ)	–	50	–	dB
Rfb setting error	Rfb_Accu1	T_A = 25°C	-25	–	25	%
	Rfb_Accu2	T_A = –40 to 105°C	-35	–	35	%

Remark n = 1 to 3

($-40°C \le T_A \le 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0$ V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, GC1 = GC2 = 03H, instrumentation amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	Icc00	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 0, 0	–	970	2150	µA
	Icc01	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 0, 1	–	510	1150	µA
	Icc10	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 1, 0	–	350	780	µA
	Icc11	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 1, 1	–	140	330	µA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 µA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 µA	AV_{DD1}- 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GC3 = 00H (20 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	µs
	t_{SET_AMP01}	GC3 = 00H (20 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	µs
	t_{SET_AMP10}	GC3 = 00H (20 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	28	µs
	t_{SET_AMP11}	GC3 = 00H (20 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	71	µs
Gain bandwidth	GBW00	CLMAX = 30 pF, CC1, CC0 = 0, 0 GC3 = 11H (54 dB)	–	1.82	–	MHz
	GBW01	CLMAX = 30 pF, CC1, CC0 = 0, 1 GC3 = 11H (54 dB)	–	1.03	–	MHz
	GBW10	CLMAX = 30 pF, CC1, CC0 = 1, 0 GC3 = 11H (54 dB)	–	0.69	–	MHz
	GBW11	CLMAX = 30 pF, CC1, CC0 = 1, 1 GC3 = 11H (54 dB)	–	0.22	–	MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 GC3 = 11H (54 dB) f = 1 kHz	–	90	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 GC3 = 11H (54 dB) f = 1 kHz	–	119	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 GC3 = 11H (54 dB) f = 1 kHz	–	150	–	nV/√ Hz
	En11	CC1, CC0 = 1, 1 GC3 = 11H (54 dB) f = 1 kHz	–	260	–	nV/√ Hz

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C, GC3 = 00H (20 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C, GC3 = 00H (20 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C, GC3 = 00H (20 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C, GC3 = 00H (20 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6.0	–	µV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GC3 = 00H (20 dB)	–	0.68	–	V/µs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GC3 = 00H (20 dB)	–	0.35	–	V/µs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GC3 = 00H (20 dB)	–	0.25	–	V/µs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GC3 = 00H (20 dB)	–	0.09	–	V/µs
Common mode rejection ratio	CMRR00	CC1, CC0 = 0, 0 GC3 = 11H (54 dB) f = 1 kHz	–	86	–	dB
	CMRR01	CC1, CC0 = 0, 1 GC3 = 11H (54 dB) f = 1 kHz	–	84	–	dB
	CMRR10	CC1, CC0 = 1, 0 GC3 = 11H (54 dB) f = 1 kHz	–	82	–	dB
	CMRR11	CC1, CC0 = 1, 1 GC3 = 11H (54 dB) f = 1 kHz	–	76	–	dB
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0 GC3 = 00H (20 dB) f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1 GC3 = 00H (20 dB) f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0 GC3 = 00H (20 dB) f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1 GC3 = 00H (20 dB) f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 105°C	-1.0	–	1.0	dB

(2) General-purpose operational amplifier

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, AMP4OF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	500	1150	µA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 0.05	V
Output voltage	VOUTL	IOL = -100 µA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 100 µA	AV_{DD1} - 0.06	AV_{DD1} - 0.02	–	V
Gain bandwidth	GBW	Configured as an inverting amplifier with 20 dB gain, CLMAX = 30 pF	–	1.15	–	MHz
Input conversion offset voltage	VOFF	T_A = 25°C, AMP4_INP = 2.5 V	-15	–	15	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±4	–	µV/°C
Slew rate	SR	CL = 30 pF	–	1.2	–	V/µs
Equivalent input noise	En_Gain	Configured as an inverting amplifier with 20 dB gain, f = 1 kHz	–	650	–	nV/√ Hz
Common mode rejection ratio	CMRR	Configured as a differential amplifier with 20 dB gain, resistance error: ±1%, f = 1 kHz	–	80	–	dB
Power supply rejection ratio	PSRR	Configured as an inverting amplifier with 20 dB gain, f = 1 kHz	–	60	–	dB

(3) Synchronous detection amplifier

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN4 = 1.7 V, GAINOF = 1, DAC4OF = 0)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	530	1300	µA
Input voltage	VINL		AGND2 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 0.05	V
Output voltage	VOUTL1	IOL = -100 µA, GAINAMP_OUT pin	–	AGND2 + 0.02	AGND2 + 0.05	V
	VOUTH1	IOH = 100 µA, GAINAMP_OUT pin	AV_{DD1} - 0.05	AV_{DD1} - 0.02	–	V
	VOUTL2	IOL = -100 µA, SYNCH_OUT pin	–	AGND2 + 0.03	AGND2 + 0.06	V
	VOUTH2	IOH = 100 µA, SYNCH_OUT pin	AV_{DD1} - 0.06	AV_{DD1} - 0.03	–	V
Gain bandwidth	GBW1	CLK_SYNCH = H, SYNCH_OUT pin, C_{LMAX} = 30 pF, GC4 = 11H (40 dB)	–	1.38	–	MHz
	GBW2	CLK_SYNCH = L, SYNCH_OUT or GAINAMP_OUT pin C_{LMAX} = 30 pF, GC4 = 11H (40 dB)	–	0.86	–	MHz
Input conversion offset voltage	VOFF	GC4 = 00H (6 dB), T_A = 25°C, GAINAMP_IN = 2.5 V	-30	–	30	mV
Input conversion offset voltage temperature coefficient	VOTC1	CLK_SYNCH = H, SYNCH_OUT pin	–	±6	–	µV/°C
	VOTC2	CLK_SYNCH = L, GAINAMP_OUT pin	–	±18	–	µV/°C
Slew rate	SR	CL = 30 pF	–	0.9	–	V/µs
Equivalent input noise	En_Gain	f = 1 kHz, GC4 = 11H (40 dB) GAINAMP_OUT pin	–	700	–	nV/√ Hz
Power supply rejection ratio	PSRR1	CLK_SYNCH = H, SYNCH_OUT pin, f = 1 kHz, GC4 = 00H (6 dB)	–	60	–	dB
	PSRR2	CLK_SYNCH = L, SYNCH_OUT or GAINAMP_OUT pin, f = 1 kHz, GC4 = 00H (6 dB)	–	45	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 105°C	-1.0	–	1.0	dB
CLK_SYNCH low-level input voltage	V_{ILCLK_SYNCH}				0.3 × AV_{DD3}	V
CLK_ SYNCH high-level input voltage	V_{IHCLK_SYNCH}		0.7 × AV_{DD3}			V

(4) D/A converter

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
DAC ALL ON current consumption 1	$I_{\_DAC\_ON1}$	DAC1OF = DAC2OF = DAC3OF = DAC4OF = 1, VRB1, VRB0 = 0, 0	–	1400	2950	µA
DAC ALL ON current consumption 2	$I_{\_DAC\_ON2}$	DAC1OF = DAC2OF = DAC3OF = DAC4OF = 1, VRB1, VRB0 ≠ 0, 0	–	1620	3360	µA
Buffer AMP ON current consumption 1 Note1	$I_{\_DAC\_Buff1}$	DACxOF = 1, VRB1, VRB0 = 0, 0 (x = 1, 2, 3, 4)	–	390	820	µA
Buffer AMP ON current consumption 2 Note1	$I_{\_DAC\_Buff2}$	DACxOF = 1, VRB1, VRB0 ≠ 0, 0 (x = 1, 2, 3, 4)	–	610	1320	µA
DAC1 GAMP ON current consumption	$I_{\_DAC\_AMP1}$	DAC1OF = 1	–	140	320	µA
DAC2 GAMP ON current consumption	$I_{\_DAC\_AMP2}$	DAC2OF = 1	–	120	265	µA
DAC3 GAMP ON current consumption	$I_{\_DAC\_AMP3}$	DAC3OF = 1	–	120	265	µA
DAC4 GAMP ON current consumption	$I_{\_DAC\_AMP4}$	DAC4OF = 1	–	630	1370	µA
Resolution	RES		–	–	8	bit
Settling time	t_{SET}	output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 990 mV	–	–	100	µs
Differential non-linearity error Note2	DNL	VRT1 = VRT0 = 0, VRB1 = VRB0 = 0	-2	–	2	LSB
Integral non-linearity error	INL	VRT1 = VRT0 = 0, VRB1 = VRB0 = 0	-2	–	2	LSB

Notes1. Buffer amplifier is powered on when one of DACx (x = 1, 2, 3, 4) is powered on at least. For example, the current consumption ($I_{\_EXAMPLE}$) is shown as a following equation when “DAC1OF=DAC2OF=1”, and “VRB1, VRB0=0, 0”. $I_{\_EXAMPLE}$ = $I_{\_DAC\_Buff1}$ + $I_{\_DAC\_AMP1}$ + $I_{\_DAC\_AMP2}$

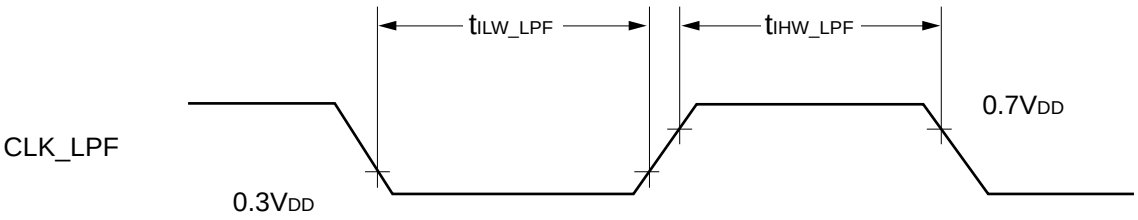
2. Guaranteed monotonic.

(5) Low-pass filter

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0 V, LPFOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	800	1800	µA
Input voltage	V_{ILLPF}		AGND4 +0.2	–	–	V
	V_{IHLPF}		–	–	AV_{DD3} - 1.5	V
Output voltage	V_{OLLPF}	IOL = -200 µA	–	AGND4 + 0.22	AGND4 +0.25	V
	V_{OHLPF}	IOH = 200 µA	AV_{DD3} – 1.55	AV_{DD3} – 1.52	–	V
Cutoff frequency	fc1	f_{CLK_LPF} = 2 kHz	–	9	–	Hz
	fc2	f_{CLK_LPF} = 1 MHz	–	4.5	–	kHz
CLK_LPF low-level input voltage	V_{ILCLK_LPF}				0.3 × AV_{DD3}	V
CLK_LPF high-level input voltage	V_{IHCLK_LPF}		0.7 × AV_{DD3}			V
CLK_LPF Input frequency	f_{CLK_LPF}		2	–	1000	kHz
CLK_LPF Input low-level-width Input high-level-width	t_{ILW_HPF} t_{IHW_HPF}		200	–	–	ns

Clock Timing

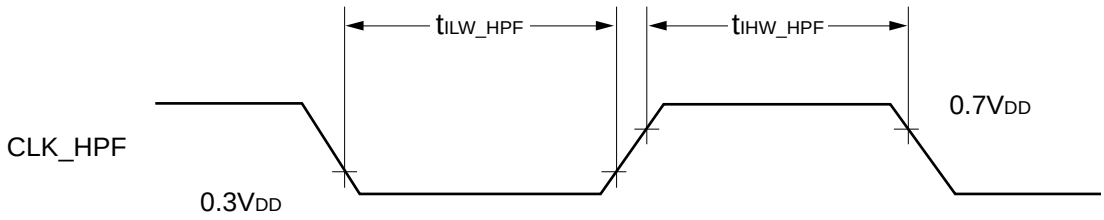


(6) High-pass filter

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0 V, HPFOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	800	1800	µA
Input voltage	V_{ILHPF}		AGND4 +0.2	–	–	V
	V_{IHHPF}		–	–	AV_{DD3} - 1.5	V
Output voltage	V_{OLHPF}	IOL = -200 µA	–	AGND4 + 0.22	AGND4 + 0.25	V
	V_{OHHPF}	IOH = 200 µA	AV_{DD3} - 1.55	AV_{DD3} - 1.52	–	V
Cutoff frequency	fc1	f_{CLK_HPF} = 2 kHz	–	8	–	Hz
	fc2	f_{CLK_HPF} = 200 kHz	–	800	–	Hz
CLK_HPF low-level input voltage	V_{ILCLK_HPF}				0.3 × AV_{DD3}	V
CLK_HPF high-level input voltage	V_{IHCLK_HPF}		0.7 × AV_{DD3}			V
CLK_HPF Input frequency	f_{CLK_HPF}		2	–	200	kHz
CLK_HPF Input low-level-width Input high-level-width	t_{ILW_HPF} t_{IHW_HPF}		200	–	–	ns

Clock Timing



(7) Temperature sensor

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0 V, TEMPOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	105	220	µA
Output voltage	V_O	T_A = 25°C	–	1.67	–	V
Temperature sensitivity	T_{SE}		–	-5.0	–	mV/°C

(8) Variable output voltage regulator

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0 V, LDOOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
<R> Current consumption	IccON	Iout = 0 mA	–	150	320	µA
Output voltage accuracy	V_Accu	Iout = 0 mA	-10	–	10	%
Load current characteristics	Vout_load	Iout = 0 to 5 mA	–	15	30	mV
Output current	Io		–	–	15	mA
Dropout voltage Note	Vd	Iout = 15 mA	–	–	0.4	V
Power supply rejection ratio	PSRR	f = 1 kHz, CL = 4.7 µF, Io = 5 mA, AV_{DD2} = 5.0 V, LDOC = 0DH (3.3 V)	–	60	–	dB
Discharge resistance	Rs	LDOOF = 0	540	715	1200	Ω
Settling time	Tset_rise	CL = 4.7 µF, C_{BGR_OUT} = 0.1 µF	–	–	5.0	ms
	Tset_fall	CL = 4.7 µF, C_{BGR_OUT} = 0.1 µF	–	–	45	ms

Note The output voltage range is determined not only by dropout voltage but also by output voltage accuracy.

(9) Reference voltage generator

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0 V, LDOOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Output voltage	V_{BGR}		–	1.21	–	V

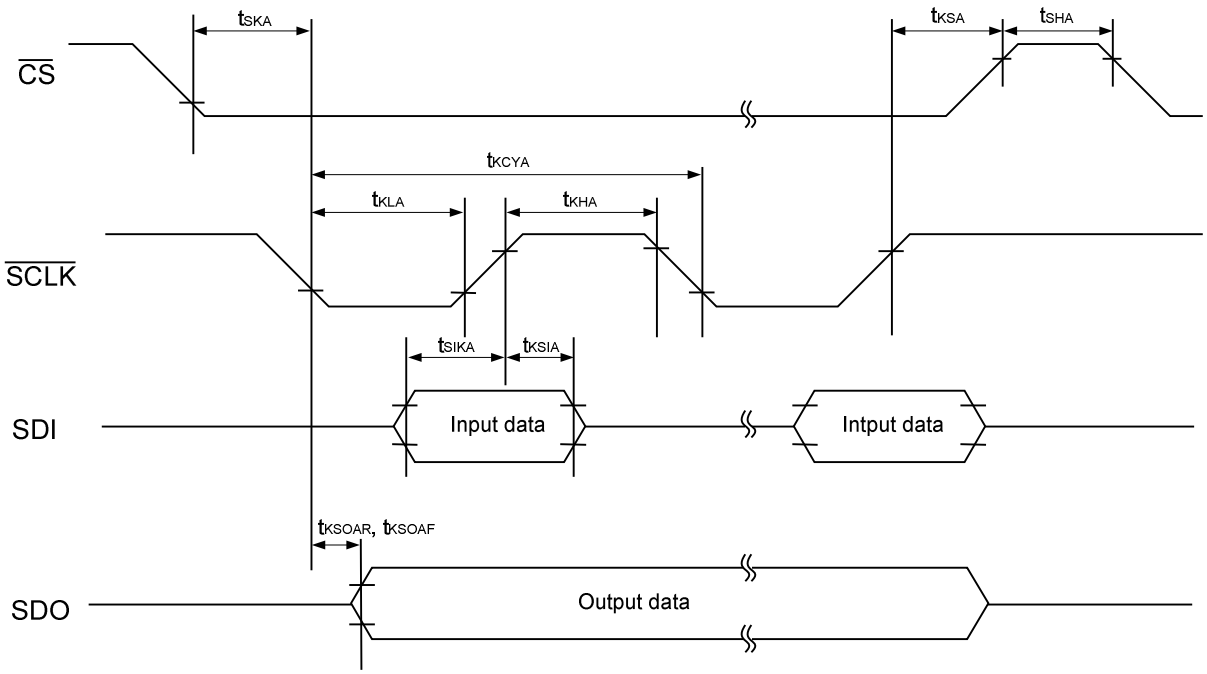
(10) SPI

($-40°C \le T_A \le 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V)

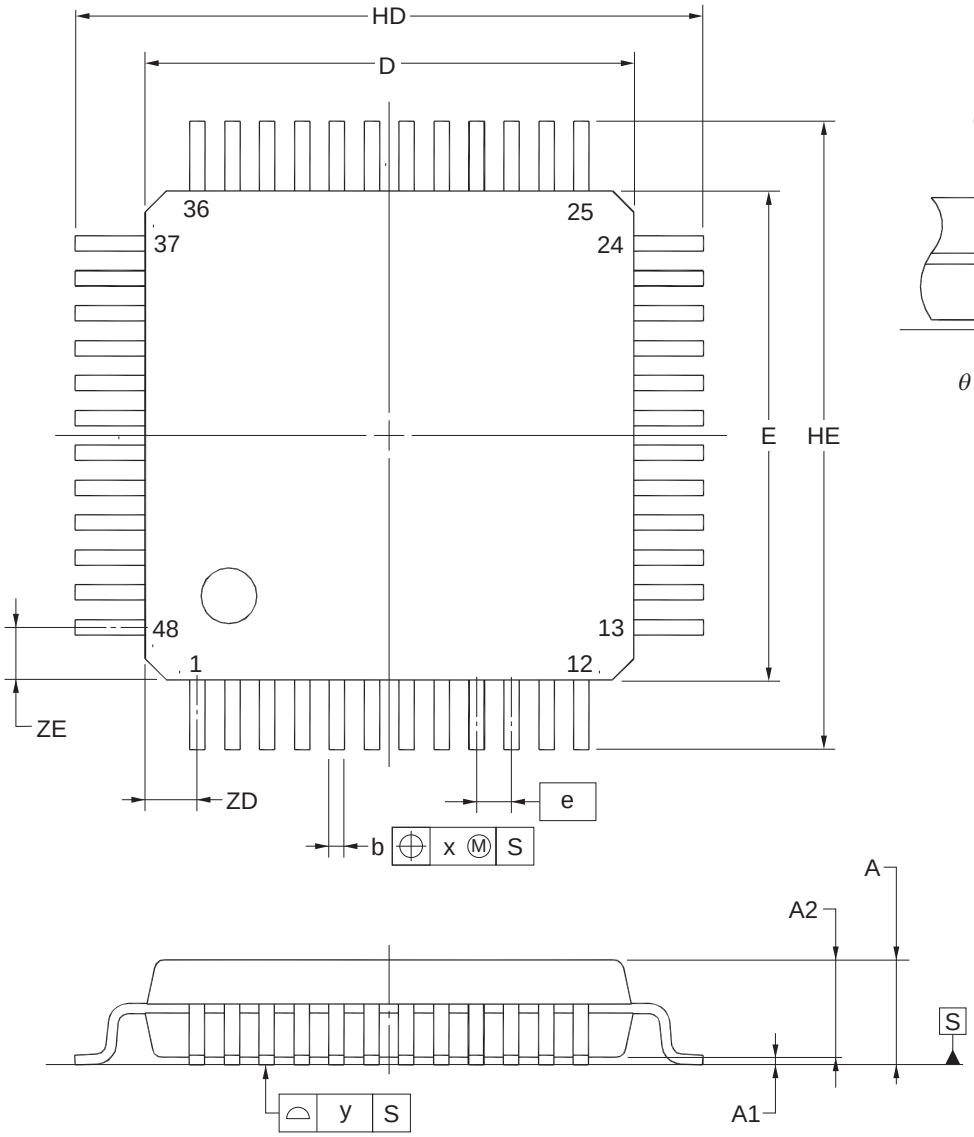
Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input voltage, high	V_{IH}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin, $\overline{RESET}$ pin	2.0	DV_{DD}	DV_{DD} + 0.1	V
Input voltage, low	V_{IL}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin, $\overline{RESET}$ pin	-0.1	DGND	0.7	V
Leakage current during high level input	I_{leak_Hi1}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin	-1	–	2	µA
	I_{leak_Hi2}	$\overline{RESET}$ pin	-1	–	2	µA
Leakage current during low level input[Note]	I_{leak_Lo1}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin	50	100	200	µA
	I_{leak_Lo2}	$\overline{RESET}$ pin	-1	–	2	µA
Low-level output voltage at SDO pin	V_{SDO_Lo}	Io = -5 mA	–	140	280	mV
Leakage current when SDO pin is off	I_{leak_SDO}		-1	–	2	µA
Pull-up resistance	R_{SPI}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin	32.5	50	67.5	kΩ
$\overline{SCLK}$ cycle time	t_{KCYA}		100	–	–	ns
$\overline{SCLK}$ high-level width low-level width	t_{KHA}, t_{KLA}		$0.9t_{KCYA}/2$	–	–	ns
SDI setup time (to $\overline{SCLK}$ ↑)	t_{SIKA}		40	–	–	ns
SDI hold time (from $\overline{SCLK}$ ↑)	t_{KSIA}		20	–	–	ns
Delay time from $\overline{SCLK}$ ↓ to SDO output	t_{KSOAR}	Pull-up resistance = 10 kΩ, CL = 5 pF, VSDO = 5.0 V	–	250	300	ns
	t_{KSOAF}	Pull-up resistance = 10 kΩ, CL = 5 pF, VSDO = 5.0 V	–	–	20	ns
<R> $\overline{CS}$ high-level width	t_{SHA}		200	–	–	ns
Delay time from $\overline{CS}$ ↓ to $\overline{SCLK}$ ↓	t_{SKA}		200	–	–	ns
Delay time from $\overline{SCLK}$ ↑ to $\overline{CS}$ ↑	t_{KSA}		200	–	–	ns

Note Including the current flowing into each pull-up resistor

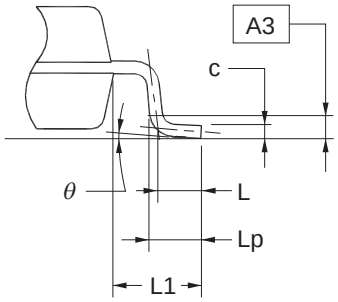
SPI transfer clock timing



14. Package Drawing



detail of lead end



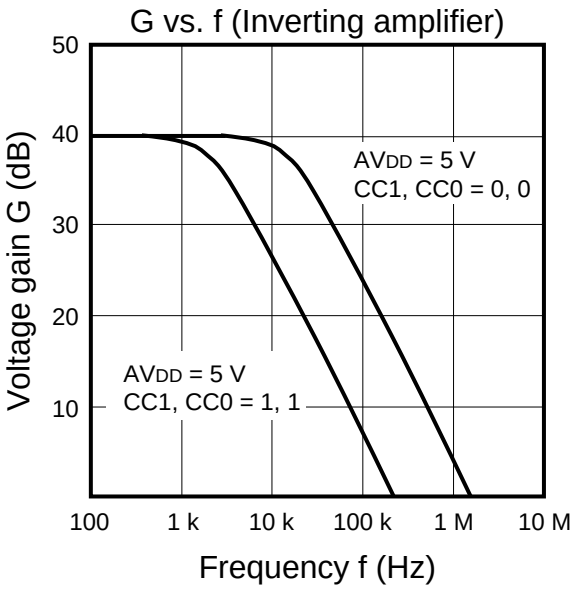
(UNIT:mm)

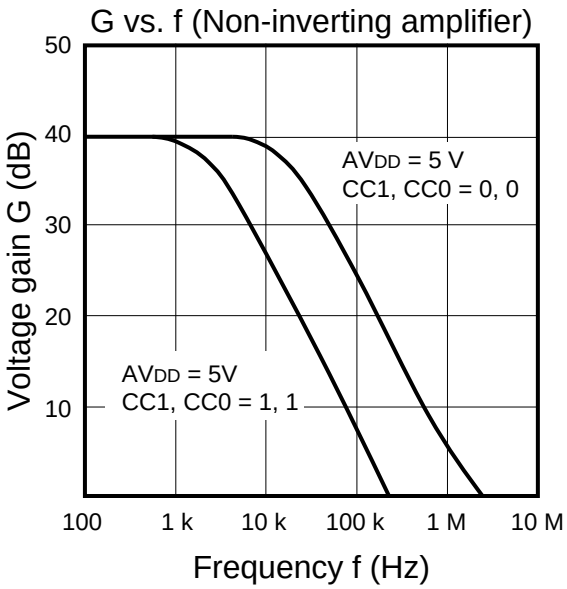
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

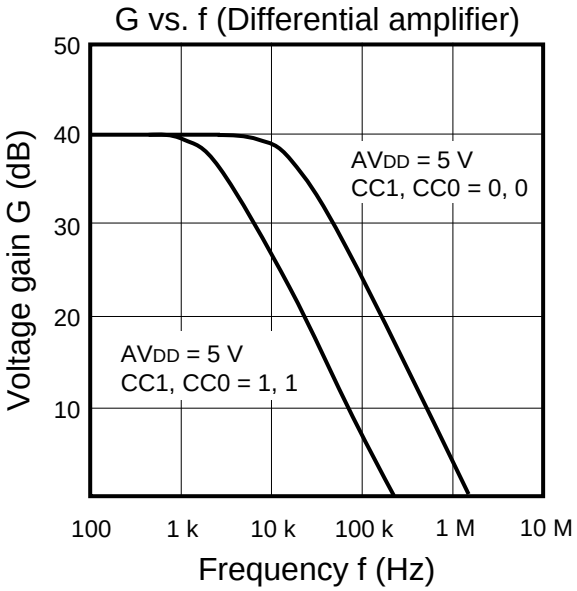
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

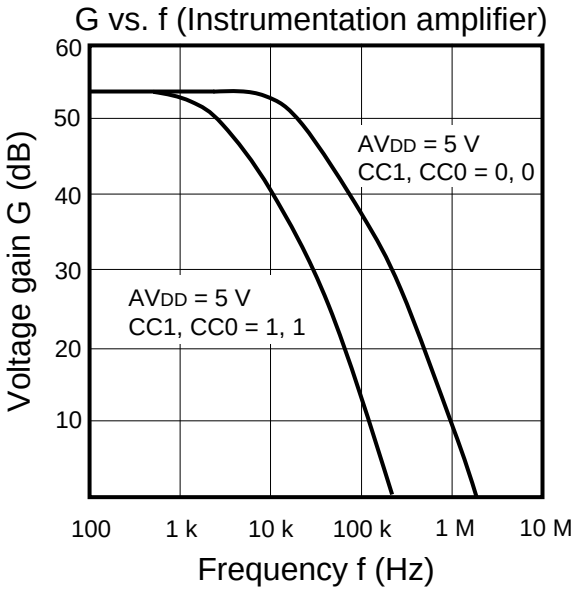
Characteristics Curve (T_A = 25°C, TYP.) (reference value)

- Configurable amplifier

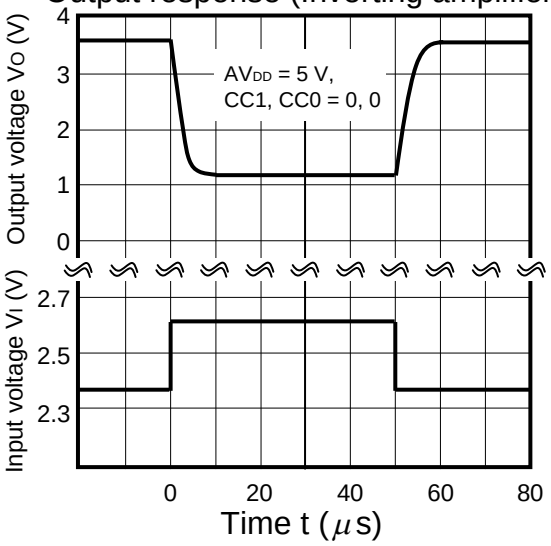




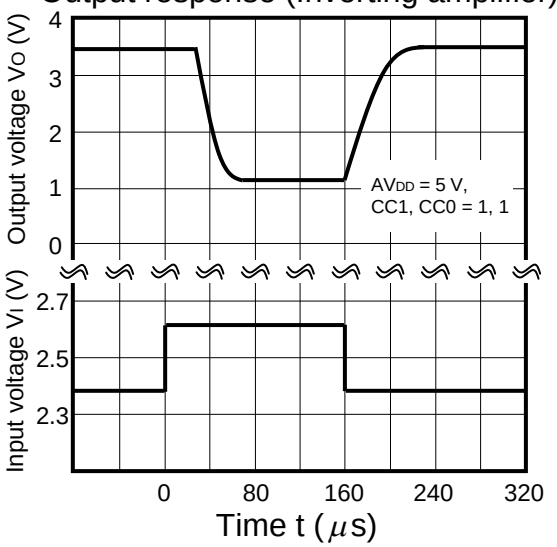




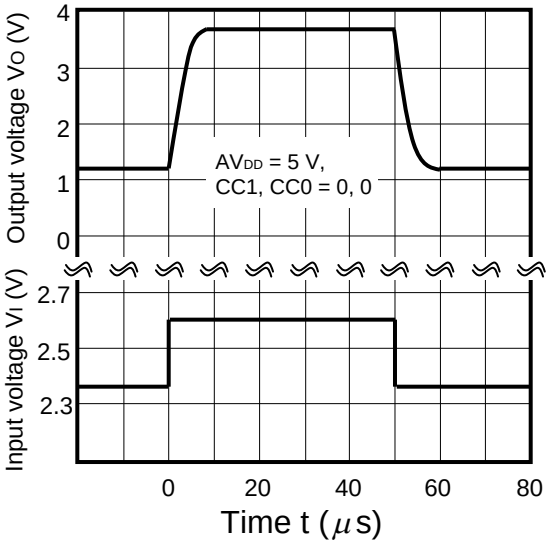
Output response (Inverting amplifier)



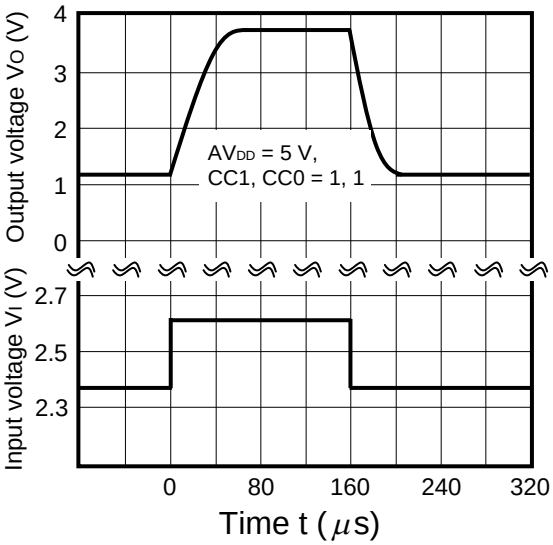
Output response (Inverting amplifier)



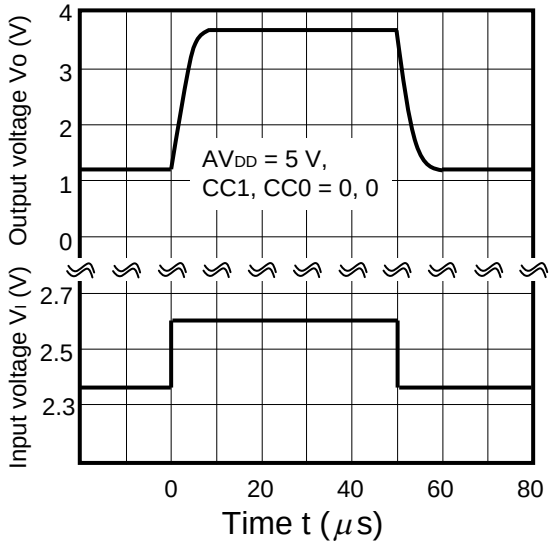
Output response (Non-inverting amplifier)



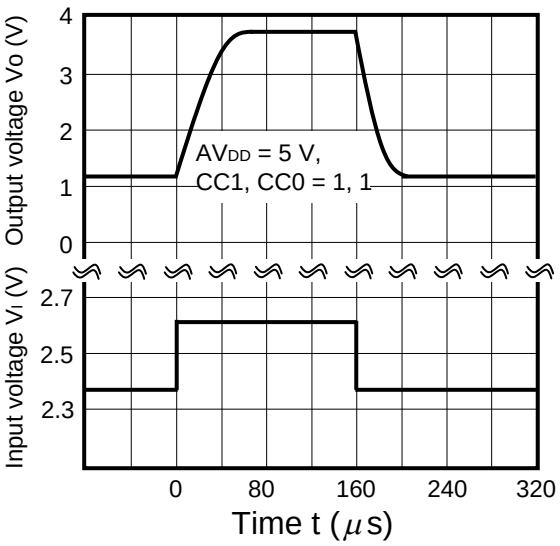
Output response (Non-inverting amplifier)



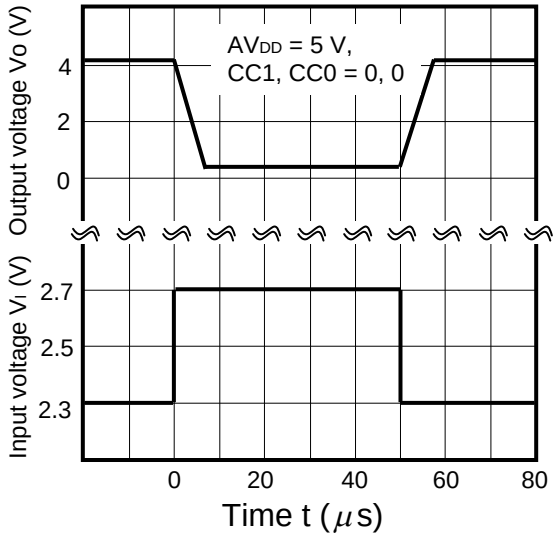
Output response (Differential amplifier)



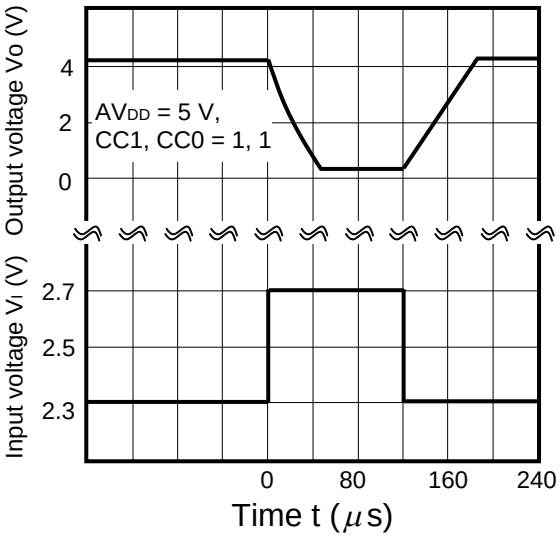
Output response (Differential amplifier)

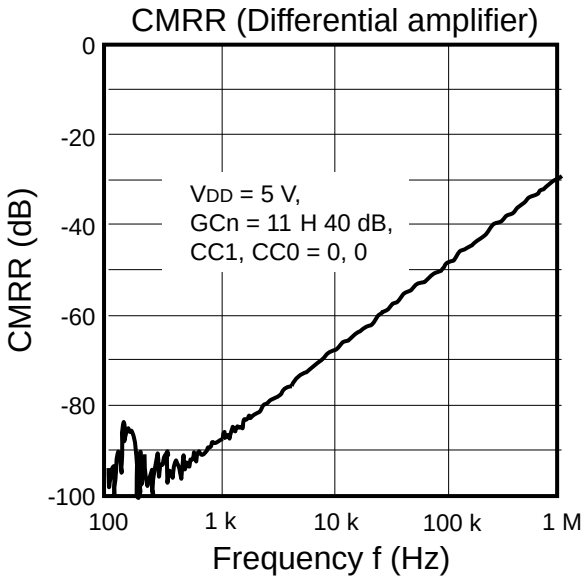


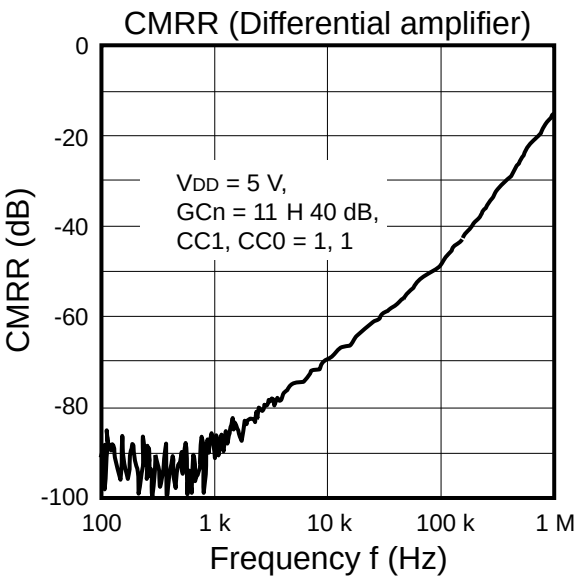
Output response (Instrumentation amplifier)

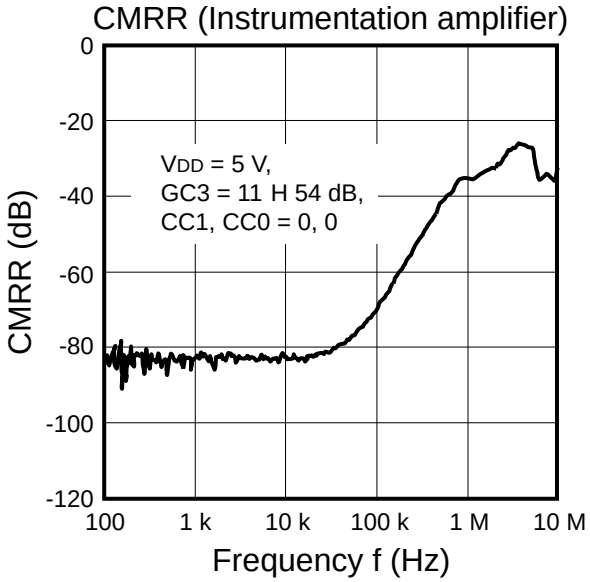


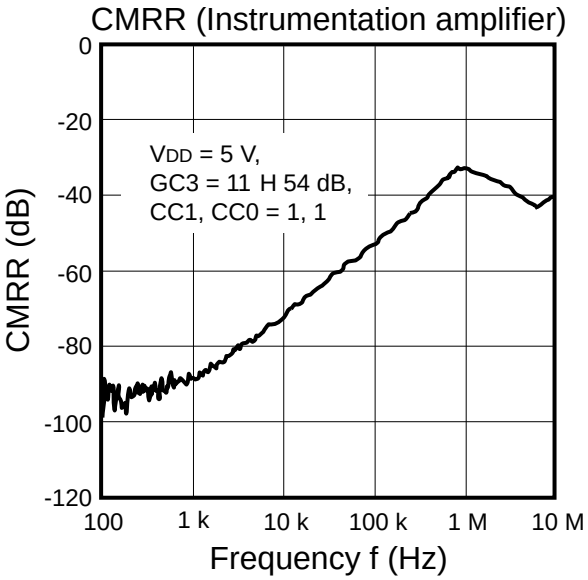
Output response (Instrumentation amplifier)

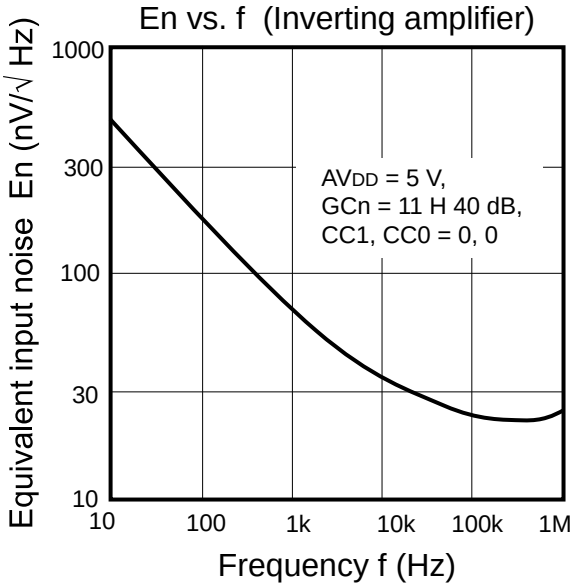


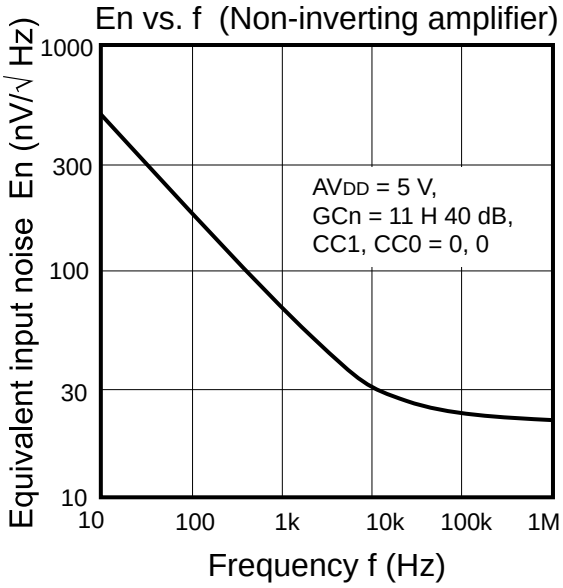

CMRR (Differential amplifier)
0
-20
-40
-60
-80
-100
CMRR (dB)
VDD = 5 V,
GCn = 11 H 40 dB,
CC1, CC0 = 0, 0
100
1 k
10 k
100 k
1 M
Frequency f (Hz)

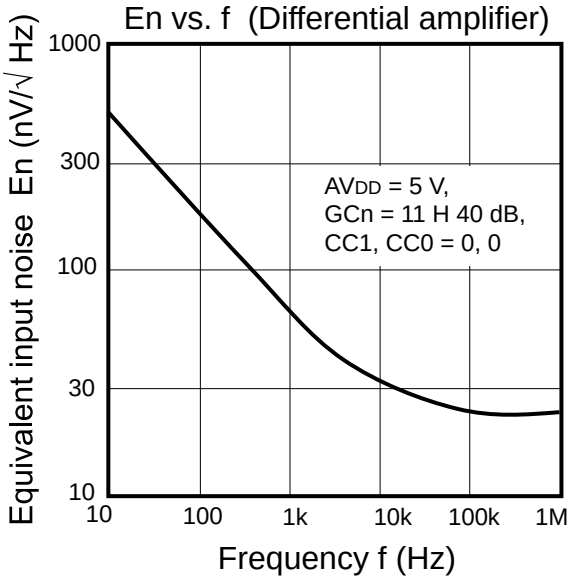

CMRR (Differential amplifier)
0
-20
-40
-60
-80
-100
CMRR (dB)
VDD = 5 V,
GCn = 11 H 40 dB,
CC1, CC0 = 1, 1
100
1 k
10 k
100 k
1 M
Frequency f (Hz)

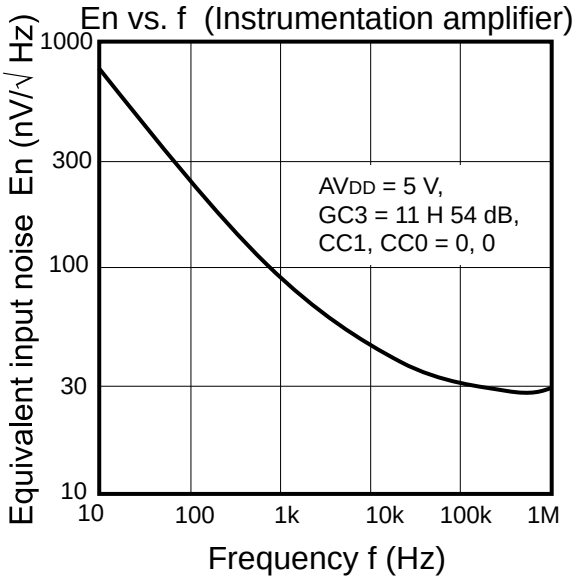

CMRR (Instrumentation amplifier)
0
-20
-40
-60
-80
-100
-120
CMRR (dB)
VDD = 5 V,
GC3 = 11 H 54 dB,
CC1, CC0 = 0, 0
100
1 k
10 k
100 k
1 M
10 M
Frequency f (Hz)


CMRR (Instrumentation amplifier)
0
-20
-40
-60
-80
-100
-120
CMRR (dB)
VDD = 5 V,
GC3 = 11 H 54 dB,
CC1, CC0 = 1, 1
100
1 k
10 k
100 k
1 M
10 M
Frequency f (Hz)

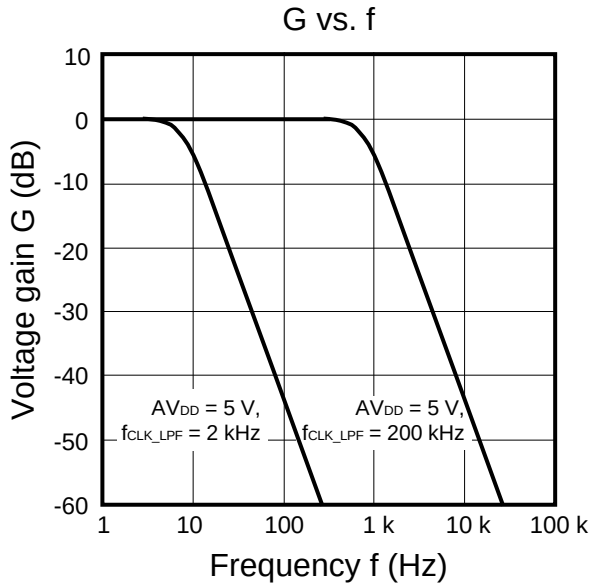

En vs. f (Inverting amplifier)
Equivalent input noise En (nV/√ Hz)
1000
300
100
30
10
AVDD = 5 V,
GCn = 11 H 40 dB,
CC1, CC0 = 0, 0
10
100
1k
10k
100k
1M
Frequency f (Hz)

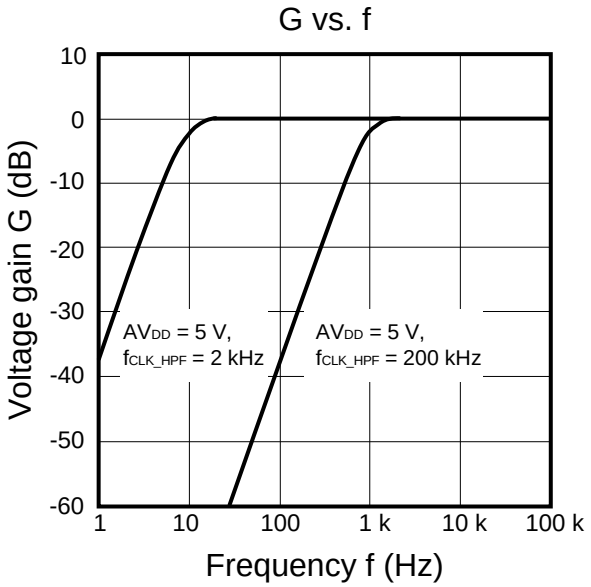

En vs. f (Non-inverting amplifier)
Equivalent input noise En (nV/√ Hz)
1000
300
100
30
10
AVDD = 5 V,
GCn = 11 H 40 dB,
CC1, CC0 = 0, 0
10
100
1k
10k
100k
1M
Frequency f (Hz)


En vs. f (Differential amplifier)
Equivalent input noise En (nV/√ Hz)
1000
300
100
30
10
AVDD = 5 V,
GCn = 11 H 40 dB,
CC1, CC0 = 0, 0
10
100
1k
10k
100k
1M
Frequency f (Hz)

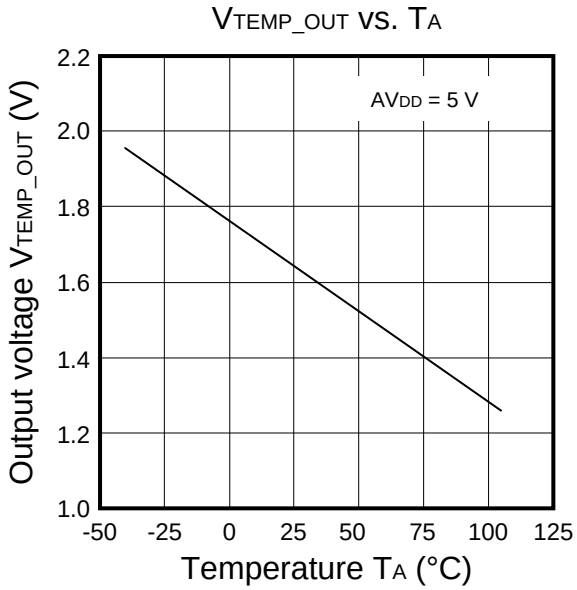

En vs. f (Instrumentation amplifier)
Equivalent input noise En (nV/√ Hz)
1000
300
100
30
10
AVDD = 5 V,
GC3 = 11 H 54 dB,
CC1, CC0 = 0, 0
10
100
1k
10k
100k
1M
Frequency f (Hz)

- Low-pass filter and high-pass filter

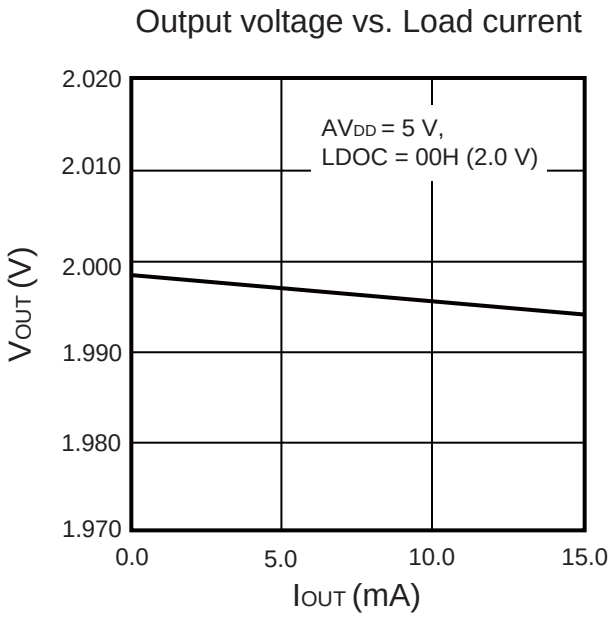


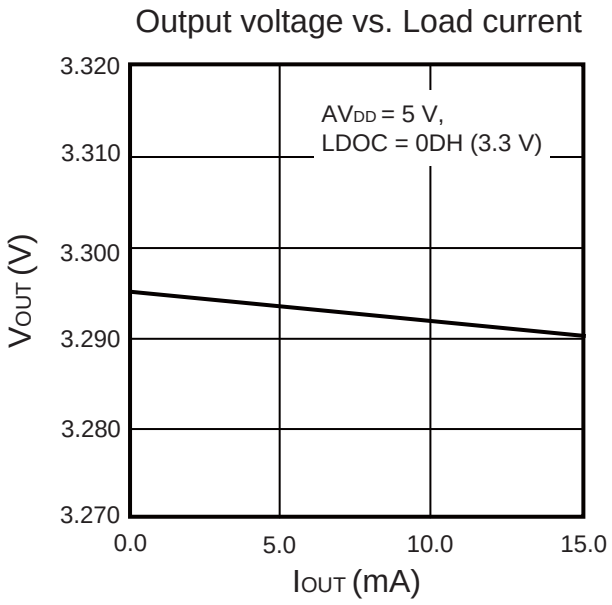


- Temperature sensor



- Variable output voltage regulator





Revision History	RAA730500 Monolithic Programmable Analog IC

Rev.	Date	Description	
		Page	Summary
0.01	Sep. 5, 2011	–	First edition issued.
0.02	Mar. 9, 2012	8	Addition of pins (LDO_OUT, BGR_OUT, and $\overline{\text{RESET}}$) to *Table 1-2 Connection of Unused Pins*
		10	Change of equivalent circuit diagrams in *Figure 1-1 Pin I/O Circuit Type (2/4)*
		11	Change of pin name OUT_SYNCH to SYNCH_OUT in *Figure 1-1 Pin I/O Circuit Type (3/4)*
		13	Change of amplification ratio of non-inverting amplifier, inverting amplifier, differential amplifier, and transimpedance amplifier
			Change of amplification ratio of instrumentation amplifier
		22	Prohibition of setting 42 to 46 dB in Table 2-1 Gain of Configurable Amplifier Ch1 (Non-Inverting Amplifier)
		23	Prohibition of setting 42 to 46 dB in *Table 2-2 Gain of Configurable Amplifier Ch1 (Inverting Amplifier and Differential Amplifier)*
		24	Change of selectable steps in *Table 2-3 Feedback Resistance of Configurable Amplifier Ch1 (Transimpedance Amplifier)*
		25	Prohibition of setting 42 to 46 dB in *Table 2-4 Gain of Configurable Amplifier Ch2 (Non-Inverting Amplifier)*
		26	Prohibition of setting 42 to 46 dB in *Table 2-5 Gain of Configurable Amplifier Ch2 (Inverting Amplifier and Differential Amplifier)*
		27	Change of selectable steps in *Table 2-6 Feedback Resistance of Configurable Amplifier Ch2 (Transimpedance Amplifier)*
		28	Prohibition of setting 42 to 46 dB in *Table 2-7 Gain of Configurable Amplifier Ch3 (Non-Inverting Amplifier)*
		29	Prohibition of setting 42 to 46 dB in *Table 2-8 Gain of Configurable Amplifier Ch3 (Inverting Amplifier and Differential Amplifier)*
		30	Change of selectable steps in *Table 2-9 Feedback Resistance of Configurable Amplifier Ch3 (Transimpedance Amplifier)*
		31	Prohibition of setting 42 to 46 dB in *Table 2-10 Gain of Configurable Amplifier Ch3 (Instrumentation Amplifier)*
		32	Change of CC in bit assignment table to AOMC in *2.3 (8) AMP operation mode control register (AOMC)*
		51	Change of output signal name OUT_SYNCH to SYNCH_OUT in *4.2 Block Diagram*
		52	Correction of source of synchronous detection amplifier input
		61	Addition of Remark 2 to *6.1 Overview of Low-Pass Filter Features*
		62	Correction of source of low-pass filter input
		65	Addition of Remark 2 to *7.1 Overview of High-Pass Filter Features*
		76	Change of output reference voltage in *10.1 Overview of Reference Voltage Generator Features*
		78	Addition of caution to *11.1 SPI Interface Features*
		79	Change of description in *11.2 SPI Communication* and change of *Figure 11-2 SPI Communication Timing*
		82	Change of *Table 12-1 Statuses During Reset*
		83	Addition of *Table 12-3 Pin Statuses After a Reset*
		85	Addition of output current I_{O2} to *13.1 Absolute Maximum Ratings*
		86	Addition of new conditions (AV_{DD1}, AV_{DD2}, AV_{DD3}, DV_{DD}) to *Power supply voltage* in *13.2 Recommended Operating Range*
		87	Change of conditions and ratings in *13.3 Supply Current Characteristics*

Rev.	Date	Description	
		Page	Summary
0.02	Mar. 9, 2012	88	Change of ratings of IccOF, VOUTH, and VOUTL in *13.4 (1) Configurable amplifier (non-inverting amplifier)*
			Change of conditions and ratings of gain bandwidth in *13.4 (1) Configurable amplifier (non-inverting amplifier)*
			Change of conditions of equivalent input noise and input conversion offset voltage VOFF2 in *13.4 (1) Configurable amplifier (non-inverting amplifier)*
			Addition of input conversion offset voltage temperature coefficient VOTC to *13.4 (1) Configurable amplifier (non-inverting amplifier)*
			Deletion of gain setting error GAIN_Accu2 from *13.4 (1) Configurable amplifier (non-inverting amplifier)*
		89	Change of ratings of current consumption, input voltage, and output voltage in *13.4 (1) Configurable amplifier (inverting amplifier)*
			Change of conditions and ratings of gain bandwidth and equivalent input noise and input conversion offset voltage in *13.4 (1) Configurable amplifier (inverting amplifier)*
			Addition of input conversion offset voltage temperature coefficient VOTC to *13.4 (1) Configurable amplifier (inverting amplifier)*
			Deletion of gain setting error GAIN_Accu12 from *13.4 (1) Configurable amplifier (inverting amplifier)*
		90	Change of ratings of current consumption and output voltage in *13.4 (1) Configurable amplifier (differential amplifier)*
			Change of conditions and ratings of equivalent input noise, input conversion offset voltage, and common mode rejection ratio in *13.4 (1) Configurable amplifier (differential amplifier)*
		91	Deletion of gain setting error GAIN_Accu2 from *13.4 (1) Configurable amplifier (differential amplifier)*
		92	Change of ratings of current consumption, output voltage, and offset voltage in *13.4 (1) Configurable amplifier (transimpedance amplifier)*
			Addition of input conversion offset voltage temperature coefficient VOTC to *13.4 (1) Configurable amplifier (transimpedance amplifier)*
		93	Change of ratings of current consumption, input voltage, and output voltage in *13.4 (1) Configurable amplifier (instrumentation amplifier)*
			Change of conditions and ratings of gain bandwidth and equivalent input noise and conditions and ratings of input conversion offset voltage in *13.4 (1) Configurable amplifier (instrumentation amplifier)*
			Addition of input conversion offset voltage temperature coefficient VOTC to *13.4 (1) Configurable amplifier (instrumentation amplifier)*
		94	Change of conditions and ratings of power supply rejection ratio in *13.4 (1) Configurable amplifier (instrumentation amplifier)*
			Deletion of gain setting error GAIN_Accu2 from *13.4 (1) Configurable amplifier (instrumentation amplifier)*
		95	Change of conditions and ratings in *13.4 (2) General amplifier*
		96	Change of conditions and ratings in *13.4 (3) Synchronous detection amplifier*
		96	Change of conditions and ratings of DACALL ON current consumption 1 and DACALL OFF current consumption in *13.4 (4) D/A converter*
			Addition of DACALL ON current consumption 2 to *13.4 (4) D/A converter*
		97	Change of conditions and ratings in *13.4 (5) Low-pass filter*
		97	Change of conditions and ratings in *13.4 (6) High-pass filter*
		98	Change of ratings of current consumption in *13.4 (7) Temperature sensor*
			Change of ratings of current consumption in *13.4 (8) Variable output voltage regulator*
			Change of ratings of output voltage in *13.4 (9) Reference voltage generator*
		99	Addition of Ieak_Hi2, Ieak_Lo2, and Remark to *13.4 (10) SPI interface*
			Change of ratings of t_{KSOAR} in *13.4 (10) SPI interface*
		102	Addition of *Characteristics Curve (T_A = 25°C, TYP.) (reference)*

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 31, 2012	87	Change of condition and ratings in *13.3 Supply Current characteristics*
		88	Change of conditions and ratings and addition of settling time in *13. 4 (1) Configurable amplifier block characteristics*
		95	Change of conditions and ratings in *13. 4 (2) General amplifier*
		96	Change of conditions and ratings in *13. 4 (3) Synchronous detection amplifier*
		96	Change of conditions and ratings in *13. 4 (4) D/A converter*
		97	Change of conditions and ratings in *13. 4 (5) Low-pass filter*
		97	Change of conditions and ratings in *13. 4 (7) Temperature sensor*
		102	Change of conditions and ratings in *13. 4 (8) Variable output voltage regulator*
		103	Change of conditions and ratings in *13. 4 (10) SPI interface*
1.01	Sep. 07, 2012	102	Change of conditions in *13. 4 (8) Variable output voltage regulator*
		103	Change of ratings in *13. 4 (10) SPI interface*
1.10	Jan. 31, 2013	53	Change of description to *4. 3 (1) MPX setting register3 (MPX3)*
		62	Deletion of Internal control clock frequency (fs) range from *6. 1 Overview of Low-pass Filter Features*
		66	Deletion of Internal control clock frequency (fs) range from *7. 1 Overview of High-pass Filter Features*
		74	Addition of NOTE to *9. 3 (1) LDO control register (LDOC)*
		88	Change of conditions and ratings (I_{m111}, I_{m112}, I_{m124}) in *13.3 Supply Current Characteristics*
		88	Change of Note to *13. 3 Supply Current Characteristics*
		89	Addition of table of Analog function with power on
		96	Addition of input conversion offset voltage in *13. 4 (1) configurable amplifier black characteristics (transimpedance amplifier)*
		98	Deletion of Input conversion offset voltage from *13. 4 (1) Configurable amplifier block characteristics (instrumentation)*
		102	Addition of parameters (Buffer AMPOM, DAC1AMPON, DAC2AMPON, DAC3AMPON, DAC4AMPON) to*13. 4 (4) D/A converter*
		102	Addition of Note to *13. 4 (4) D/A converter*
		103	Addition of Clock Timing Figure to *13. 4 (5) Low-pass filter*
		104	Addition of Clock Timing Figure to *13. 4 (6) High-pass filter*
		105	Addition of Note to *13. 4 (8) Variable output voltage regulator*
		106	Deletion of F_{SCLK} from *13. 4 (10) SPI*
		115	Addition of Variable output voltage regulator in charcferisfics curve
1.20	May. 31, 2014	14	Change of description about reference voltage in *2. 1 Configurable Amplifiers*
		34	Change of description in *2. 3 (9) Power control register 1 (PC1)*
		52	Change of description about reference voltage in *4. 1 Synchronous Detection Amplifier*
		57	Change of the calculating formula about output voltage in *5. 1 D/A Converters*
		58	Change of description in *5. 3 (1) DAC reference voltage control register (DACRC)*
		62	Change of description about reference voltage in *6. 1 Low-pass Filter*
		66	Change of description about reference voltage in *7. 1 High-Pass Filter*
		67	Change of description in *7. 3 (1) MPX setting register3 (MPX3)*
		79	Addition of Caution about external reset to *11. SPI*
		82	Change of description in *12. Reset*
		86	Deletion of Junction temperature from *13. 1 Absolute Maximum Ratings*
		87	Change of the title to *Operation condition* in *13. 2*
		88	Addition of the MAX value to I_{stby11} (T_A = -40°C) in *13. 3*
		105	Correction of the current consumption in *13. 4 (8)*
		106	Correction of the unit of $\overline{CS}$ high-level width in *13.4 (10)*

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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