

## Description

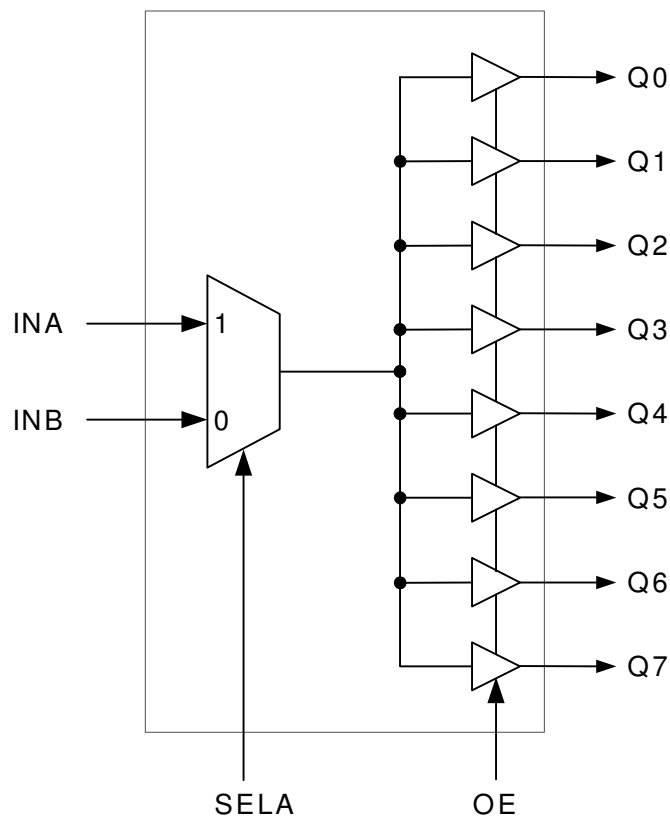
The ICS552-02 is a low skew, single-input to eight-output clock buffer. The device offers a dual input with pin select for switching between two clock sources. It is part of IDT's ClockBlocks™ family. See the ICS553 for a 1 to 4 low skew buffer. For more than 8 outputs see the MK74CBxxx Buffalo™ series of clock drivers.

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

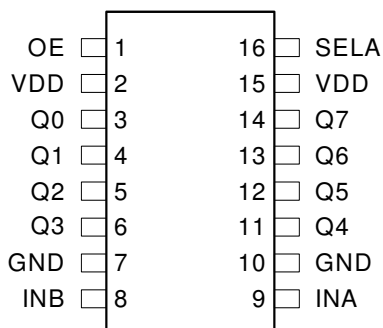
## Features

- Extremely low skew outputs (50ps maximum)
- Packaged in 16 pin TSSOP
- Pb (lead) free package
- Low power CMOS technology
- Operating Voltages of 2.5 V to 5 V
- Output Enable pin tri-states outputs
- 5 V tolerant input clocks
- Input/Output clock frequency up to 200 MHz
- Input clock multiplexer simplifies clock selection
- Industrial temperature

## Block Diagram



## Pin Assignment



16 Pin TSSOP

## Input Source Select

SELA	Input
0	INB
1	INA

## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	OE	Input	Output Enable. Tri-states outputs when low. Internal pull-up resistor.
2	VDD	Power	Connect to +2.5V, +3.3V or +5.0V. Must be the same as pin 15.
3	Q0	Output	Clock Output 0
4	Q1	Output	Clock Output 1
5	Q2	Output	Clock Output 2
6	Q3	Output	Clock Output 3
7	GND	Power	Connect to ground.
8	INB	Input	Clock Input B. 5V tolerant input.
9	INA	Input	Clock Input A. 5V tolerant input.
10	GND	Power	Connect to ground.
11	Q4	Output	Clock Output 4
12	Q5	Output	Clock Output 5
13	Q6	Output	Clock Output 6
14	Q7	Output	Clock Output 7
15	VDD	Power	Connect to +2.5V, +3.3V or +5.0V. Must be the same as pin 2.
16	SELA	Input	Selects either INA or INB. Internal pull-up resistor.

## External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01  $\mu$ F should be connected between VDD on pin 2 and GND on pin 7, and between VDD on pin 15 and GND on pin 10, as close to the device as possible. A 33  $\Omega$  series terminating resistor should be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skews that the ICS552-02 is capable of, careful attention must be paid to board layout. Essentially, all 8 outputs must have identical terminations, identical loads, and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30 $\Omega$  series termination on one output (with 33 $\Omega$  on the others) will cause at least 15ps of skew.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS552-02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
SELA, OE, and all Outputs	-0.5 V to VDD+0.5 V
INA and INB	-0.5V to 5.5V
Ambient Operating Temperature	-40 to +85 °C
Storage Temperature	-65 to +150 °C
Junction Temperature	175 °C
Soldering Temperature	260 °C

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40	–	+85	°C
Power Supply Voltage (measured in respect to GND)	+2.375		+5.25	V

## DC Electrical Characteristics

VDD=2.5 V ±5%, Ambient temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, INA, INB	V <sub>IH</sub>	Note 1	VDD/2+0.5		5.5	V
Input Low Voltage, INA, INB	V <sub>IL</sub>	Note 1			VDD/2-0.5	V
Input High Voltage, OE, SELA	V <sub>IH</sub>		1.8		VDD	V
Input Low Voltage, OE, SELA	V <sub>IL</sub>				0.7	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -16 mA	2			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 16 mA			0.4	V
Operating Supply Current	IDD	No load, 135 MHz		35		mA
Short Circuit Current	I <sub>OS</sub>	Each output		60		mA

## DC Electrical Characteristics (continued)

**VDD=3.3 V ±5%**, Ambient temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, INA, INB	V <sub>IH</sub>	Note 1	VDD/2+0.7		5.5	V
Input Low Voltage, INA, INB	V <sub>IL</sub>	Note 1			VDD/2-0.7	V
Input High Voltage, OE, SELA	V <sub>IH</sub>		2		VDD	V
Input Low Voltage, OE, SELA	V <sub>IL</sub>				0.8	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -25 mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OH</sub> = 25 mA			0.4	V
Output High Voltage (CMOS Level)	V <sub>OH</sub>	I <sub>OH</sub> = -12 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, 135 MHz		50		mA
Short Circuit Current	I <sub>OS</sub>	Each output		80		mA

**VDD=5 V ±5%**, Ambient temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		4.75		5.25	V
Input High Voltage, INA, INB	V <sub>IH</sub>	Note 1	VDD/2+1		5.5	V
Input Low Voltage, INA, INB	V <sub>IL</sub>	Note 1			VDD/2-1	V
Input High Voltage, OE, SELA	V <sub>IH</sub>		2		VDD	V
Input Low Voltage, OE, SELA	V <sub>IL</sub>				0.8	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -35 mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 35 mA			0.4	V
Output High Voltage (CMOS Level)	V <sub>OH</sub>	I <sub>OH</sub> = -12 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, 135 MHz		85		mA
Short Circuit Current	I <sub>OS</sub>	Each output		100		mA

Note: 1. Nominal switching threshold is VDD/2

## AC Electrical Characteristics

**VDD = 2.5V ±5%**, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t <sub>OR</sub>	0.8 to 2.0 V, C <sub>L</sub> =15 pF		1.0	1.5	ns
Output Fall Time	t <sub>OF</sub>	2.0 to 0.8 V, C <sub>L</sub> =15 pF		1.0	1.5	ns
Propagation Delay	Note 1			3.5		ns
Output to output skew	Note 2	Rising edges at VDD/2		0	50	ps
Input A to Input B skew	Note 3			0	50	ps

**VDD = 3.3V ±5%**, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t <sub>OR</sub>	0.8 to 2.0 V, C <sub>L</sub> =15 pF		0.6	1.0	ns
Output Fall Time	t <sub>OF</sub>	2.0 to 0.8 V, C <sub>L</sub> =15 pF		0.6	1.0	ns
Propagation Delay	Note 1		2.0	3.0	5.5	ns
Output to output skew	Note 2	Rising edges at VDD/2		0	50	ps
Input A to Input B skew	Note 3			0	50	ps
Part to Part Skew					3.5	ns

**VDD = 5.0V ±5%**, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t <sub>OR</sub>	0.8 to 2.0 V, C <sub>L</sub> =15 pF		0.3	0.7	ns
Output Fall Time	t <sub>OF</sub>	2.0 to 0.8 V, C <sub>L</sub> =15 pF		0.3	0.7	ns
Propagation Delay	Note 1			2.8		ns
Output to output skew	Note 2	Rising edges at VDD/2		0	50	ps
Input A to Input B skew	Note 3			0	50	ps

Notes: 1. With rail-to-rail input clock.

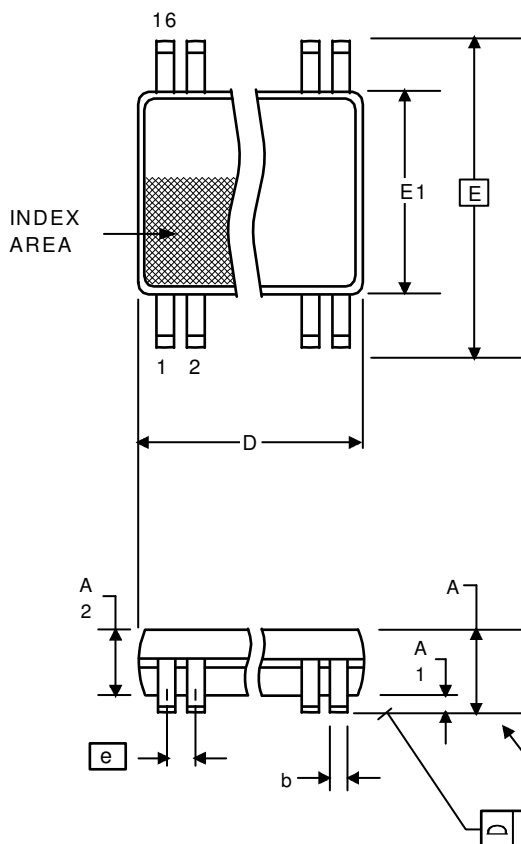
2. Between any two outputs with equal loading.

3. Propagation delay matching through the part.

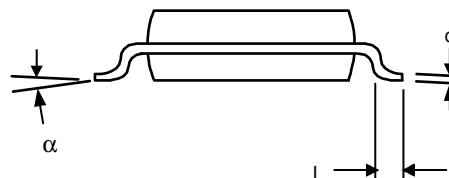
4. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

## Package Outline and Package Dimensions (16 pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
$\alpha$	0°	8°	0°	8°
aaa	--	0.10	--	0.004



## Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
552G-02ILN	552G02IN	Tubes	16-pin TSSOP	-40 to +85 °C
552G-02ILNT	552G02IN	Tape and Reel	16-pin TSSOP	-40 to +85 °C

**“LN” suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.