2N6387, 2N6388

Plastic Medium-Power Silicon Transistors

These devices are designed for general-purpose amplifier and low-speed switching applications.

Features

- High DC Current Gain $-h_{FE} = 2500$ (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage @ 100 mAdc $V_{CEO(sus)} = 60 \text{ Vdc} (Min) - 2N6387$
- = 80 Vdc (Min) 2N6388 • Low Collector-Emitter Saturation Voltage -
 - $V_{CE(sat)} = 2.0 \text{ Vdc} (Max) @ I_C$
 - = 5.0 Adc 2N6387, 2N6388
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS (Note 1)

Rating		Symbol	Value	Unit
Collector-Emitter Voltage	2N6387 2N6388	V _{CEO}	60 80	Vdc
Collector-Base Voltage	2N6387 2N6388	V _{CB}	60 80	Vdc
Emitter-Base Voltage		V _{EB}	5.0	Vdc
Collector Current – Continuous – Peak		Ι _C	10 15	Adc
Base Current		Ι _Β	250	mAdc
Total Power Dissipation @ $T_C = 2$ Derate above 25°C	25°C	PD	65 0.52	W W/°C
Total Power Dissipation @ $T_A = 2$ Derate above 25°C	25°C	PD	2.0 0.016	W W/°C
Operating and Storage Junction, Temperature Range		T _J , T _{stg}	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Indicates JEDEC Registered Data.

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

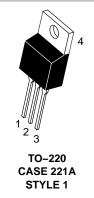
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



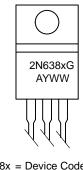
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DARLINGTON NPN SILICON POWER TRANSISTORS 8 AND 10 AMPERES 65 WATTS, 60 - 80 VOLTS



MARKING DIAGRAM



2N638x = Device Code

x = 7 or 8

- G = Pb-Free Package
- = Assembly Location Α
- = Year Υ
- ww = Work Week

ORDERING INFORMATION

Device	Package	Shipping
2N6387G	TO–220 (Pb–Free)	50 Units / Rail
2N6388G	TO–220 (Pb–Free)	50 Units / Rail

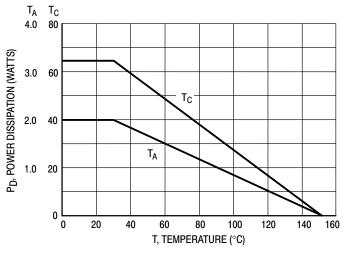


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted) (Note 2)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 3) $(I_C = 200 \text{ mAdc}, I_B = 0)$	2N6387 2N6388	V _{CEO(sus)}	60 80		Vdc
Collector Cutoff Current $(V_{CE} = 60 \text{ Vdc}, I_B = 0)$ $(V_{CE} = 80 \text{ Vdc}, I_B = 0)$	2N6387 2N6388	I _{CEO}		1.0 1.0	mAdc
	2N6387 2N6388 2N6387 2N6388	I _{CEX}	- - - -	300 300 3.0 3.0	μAdc mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I _{EBO}	-	5.0	mAdc
ON CHARACTERISTICS (Note 3)					
DC Current Gain $(I_C = 5.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc})$ $(I_C = 1.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc})$	2N6387, 2N6388 2N6387, 2N6388	h _{FE}	1000 100	20,000 -	-
Collector–Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}, I_B = 0.01 \text{ Adc}$) ($I_C = 10 \text{ Adc}, I_B = 0.1 \text{ Adc}$)	2N6387, 2N6388 2N6387, 2N6388	V _{CE(sat)}		2.0 3.0	Vdc
$\begin{array}{l} \text{Base-Emitter On Voltage} \\ (I_C = 5.0 \text{ Adc}, \text{ V}_{CE} = 3.0 \text{ Vdc}) \\ (I_C = 10 \text{ Adc}, \text{ V}_{CE} = 3.0 \text{ Vdc}) \end{array}$	2N6387, 2N6388 2N6387, 2N6388	V _{BE(on)}		2.8 4.5	Vdc
DYNAMIC CHARACTERISTICS			1	1	

Small–Signal Current Gain ($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc, $f_{test} = 1.0$ MHz)	h _{fe}	20	-	-
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C _{ob}	-	200	pF
Small–Signal Current Gain (I _C = 1.0 Adc, V _{CE} = 5.0 Vdc, f = 1.0 kHz)	h _{fe}	1000	-	-

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Indicates JEDEC Registered Data. 3. Pulse Test: Pulse Width \leq 300 µs, Duty Cycle \leq 2.0%.

2N6387, 2N6388

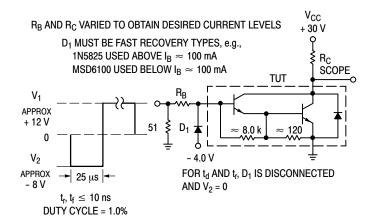
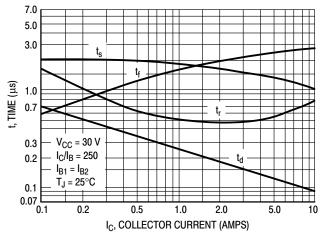
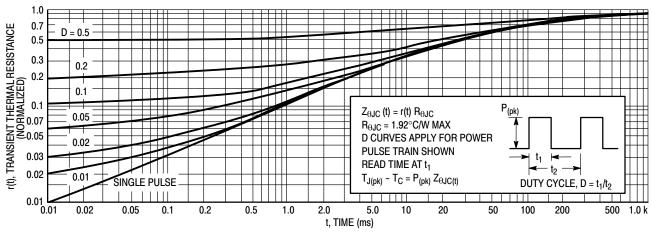


Figure 2. Switching Times Test Circuit









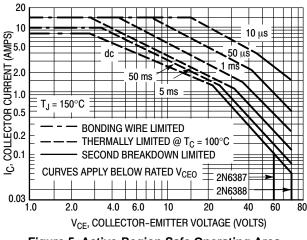
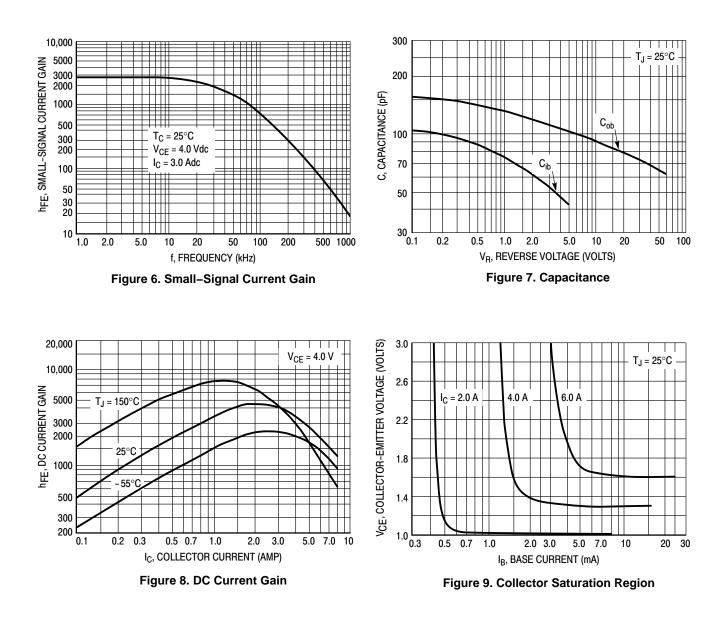
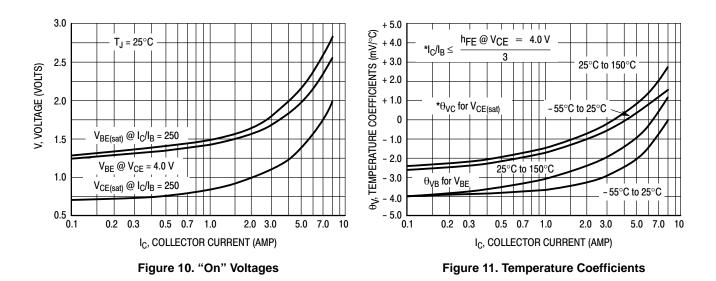


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}$ C; T_{C} is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}$ C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown





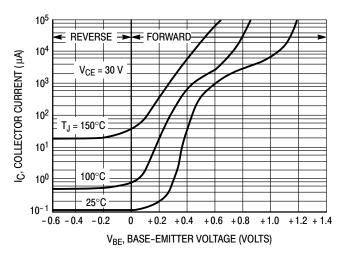


Figure 12. Collector Cut-Off Region

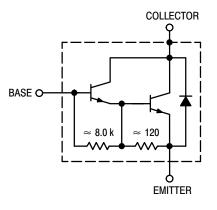


Figure 13. Darlington Schematic

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