

LS259

T-46-07-11



54LS259/DM74LS259 8-Bit Addressable Latches

General Description

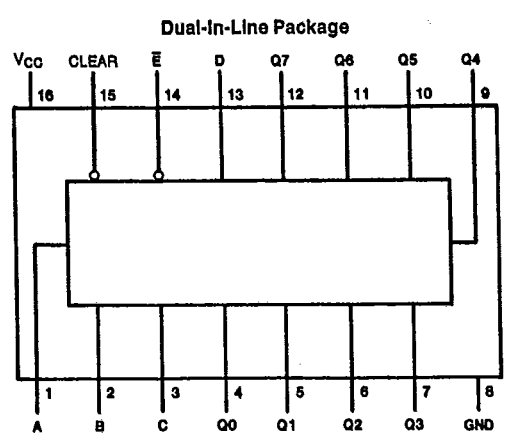
These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

Features

- 8-Bit parallel-out storage register performs serial-to-parallel conversion with storage
- Asynchronous parallel clear
- Active high decoder
- Enable/disable input simplifies expansion
- Direct replacement for Fairchild 9334
- Expandable for N-bit applications
- Four distinct functional modes
- Typical propagation delay times:
 - Enable-to-output 18 ns
 - Data-to-output 16 ns
 - Address-to-output 21 ns
 - Clear-to-output 17 ns
- Fan-out
 - I_{OL} (sink current)
 - 54LS259 4 mA
 - 74LS259 8 mA
 - I_{OH} (source current) -0.4 mA
- Typical I_{CC} 22 mA

Connection Diagram



Function Table

Inputs		Output of Addressed Latch	Each Other Output	Function
Clear	\bar{E}			
H	L	D	Q _{i0}	Addressable Latch
H	H	Q _{i0}	Q _{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = High Level, L = Low Level
 D = the Level of the Data Input
 Q_i = the Level of Q_i (i = 0, 1, ..., 7, as Appropriate) before the Indicated Steady-State Input Conditions Were Established.

Order Number 54LS259DMQB, 54LS259FMQB, 54LS259LMQB, DM74LS259WM or DM74LS259N
 See NS Package Number E20A, J16A, M16B, N16E or W16A



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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	-55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS259			DM74LS259			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
t _w	Pulse Width (Note 7)	Enable	17		15			ns
		Clear	17		15			
t _{SU}	Setup Time (Notes 1, 2, 3 & 7)	Data	20 ↑		15 ↑			ns
		Select	15 ↓		15 ↓			
t _H	Hold Time (Notes 1, 2 & 7)	Data	5 ↑		0 ↑			ns
		Select	0 ↑		0 ↑			
T _A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	54LS	2.5		V
			DM74	2.7	3.4	
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IL} = Max, V _{IH} = Min	54LS		0.4	V
			DM74		0.35	
			DM74		0.25	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V V _I = 10V			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.4	mA
	Enable	V _{CC} = 5.0, V _I = 0.4V			-0.8	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 5)	54LS	-20	-100	mA
			DM74	-20	-100	
I _{CC}	Supply Current	V _{CC} = Max (Note 6)		22	36	mA

Note 1: The symbols (↓, ↑) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Note 2: Setup and hold times are with reference to the enable input.

Note 3: The select-to-enable setup time is the time before the High-to-Low enable transition that the select must be stable so that the correct latch is selected and the others not affected.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all inputs at 4.5V, and all outputs open.

Note 7: T_A = 25°C and V_{CC} = 5V.

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Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS		DM74LS		Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$ $R_L = 2\text{ k}\Omega$		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		27		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		30		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		29		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		18		36	ns

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