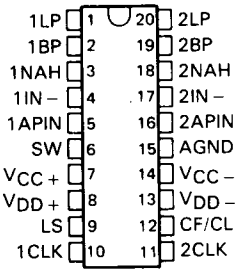
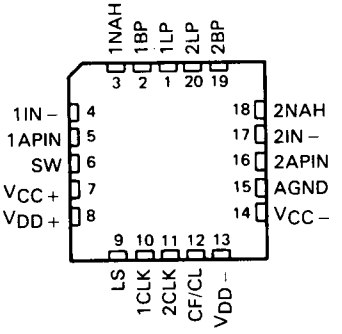
D2952, AUGUST 1986—REVISED NOVEMBER 1988

- **Maximum Clock to Center-Frequency Ratio Error**
  TLC10 . . . ±0.6%
  TLC20 . . . ±1.5%
- **Filter Cutoff Frequency Stability Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations over Time and Temperature**
- **Critical-Frequency Times Q Factor Range Up to 200 kHz**
- **Critical-Frequency Operation Up to 30 kHz**
- **Designed to be Interchangeable with:**
  National MF10
  Maxim MF10
  Linear Technology LTC1060

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC10/MF10A and TLC20/MF10C are monolithic general-purpose switched-capacitor CMOS filters each containing two independent active-filter sections. Each device facilitates configuration of Butterworth, Bessel, Cauer, or Chebyshev filter design.

Filter features include cutoff frequency stability that is dependent only on the external clock frequency stability and minimal response deviation over time and temperature. Features also include a critical-frequency times filter quality (Q) factor range of up to 200 kHz.

With external clock and resistors, each filter section can be used independently to produce various second-order functions or both sections can be cascaded to produce fourth-order functions. For functions greater than fourth-order, ICs can be cascaded.

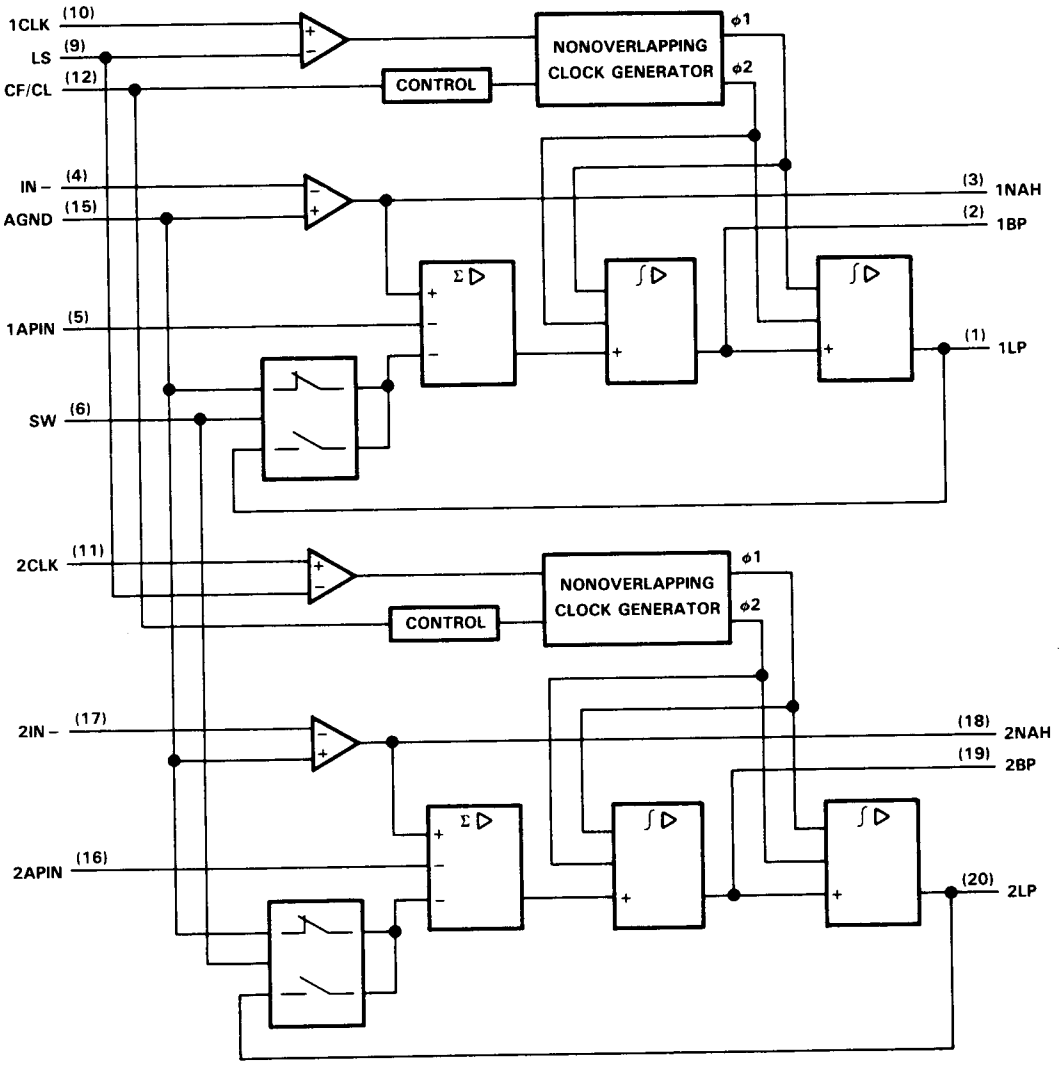
The TLC10/MF10A and TLC20/MF10C are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	MAX f_{clock}/fc ERROR	PACKAGE	
		CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	±0.6%	TLC10CFN or MF10ACFN	TLC10CN or MF10ACN
	±1.5%	TLC20CFN or MF10CCFN	TLC20CN or MF10CCN

PIN NAME	PIN NO.	I/O	DESCRIPTION
AGND	15	I	Analog Ground — The noninverting inputs to the input operational amplifiers of both filter sections. This terminal should be at ground for dual supplies or at mid-supply level for single-supply operation.
1APIN 2APIN	5 16	I	All-Pass Inputs — The all-pass input to the summing amplifier of each respective filter section used for all-pass filter applications in configuration modes 1a, 4, 5, and 6. This terminal should be driven from a source having an impedance of less than 1 kΩ. In all other modes, this terminal is grounded. See Typical Application Data.
1BP 2BP	2 19	O	Band-Pass Outputs — The band-pass output of each respective filter section provides the second-order band-pass filter functions.
CF/CL	12	I	Center Frequency/Current Limit — This input terminal provides the option to select the input-clock-to-center-frequency ratio of 50:1 or 100:1 or to limit the current of the IC. For a 50:1 ratio, the CF/CL terminal is set to V_{DD+}. For a 100:1 ratio, the CF/CL terminal is set to ground for dual supplies or to mid-supply level for single-supply operation. For current limiting, the CF/CL terminal is set to V_{DD-}. This aborts filtering and limits the IC current to 0.5 milliamperes.
1CLK 2CLK	10 11	I	Clock Inputs — The clock input to the two-phase nonoverlapping generator of each respective filter section is used to generate the center frequency of the complex pole pair second-order function. Both clocks should be of the same level (TTL or CMOS) and have duty cycles close to 50%, especially when clock frequencies (f_{clock}) greater than 200 kHz are used. At this duty cycle, the operational amplifiers have the maximum time to settle while processing analog samples.
1IN− 2IN−	4 17	I	Inverting Inputs — The inverting input side of the input operational amplifier whose output drives the summing amplifier of each respective filter section.
1LP 2LP	1 20	O	Low-Pass Outputs — The low-pass outputs of the second-order filters.
LS	9	I	Level Shift — This terminal accommodates various input clock levels of bipolar (CMOS) or unipolar (TTL or other clocks) to function with single or dual supplies. For CMOS (±5-volt) clocks, V_{DD-} or ground is applied to the LS terminal. For TTL and other clocks, ground is applied to the LS terminal.
1NAH 2NAH	3 18	O	Notch, All-Pass, or High-Pass Outputs — The output of each respective filter section can be used to provide either a second-order notch, all-pass, or high-pass output filter function, depending on circuit configuration.
SW	6	I	Switch Input — This input terminal is used to control internal switches to connect either the AGND input or the LP output to one of the inputs of the summing amplifier. The terminal controls both independent filter sections and places them in the same configuration simultaneously. If V_{CC-} is applied to the SW terminal, the AGND input terminal will be connected to one of the inputs of each summing amplifier. If V_{CC+} is applied to the SW terminal, the LP output will be connected to one of the inputs of the summing amplifier.
V_{CC+}	7		Analog positive supply voltage terminal
V_{CC-}	14		Analog negative supply voltage terminal
V_{DD+}	8		Digital positive supply voltage terminal
V_{DD-}	13		Digital negative supply voltage terminal

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Analog supply voltage, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Digital supply voltage, $V_{DD\pm}$ . . . . . ±7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, $V_{CC\pm}$, (see Note 2)	±4	±5	±6	V
Digital supply voltage, $V_{DD\pm}$, (see Note 2)	±4	±5	±6	V
Clock frequency, f_{clock}, (see Note 3)	0.008		1.0	MHz
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. A common supply voltage source should be used for the analog and digital supply voltages. Although each has separate terminals, they are connected together internally at the substrate. V_{CC+} and V_{DD+} can be connected together at the device terminals or at the supply voltage source. The same is true for V_{CC-} and V_{DD-}.
3. Both input clocks should be of the same level type (TTL or CMOS), and their duty cycles should be at 50% above 200 kHz to allow the operational amplifiers the maximum time to settle while processing analog samples.

electrical characteristics at $V_{CC\pm}$ = ±5 V, $V_{DD\pm}$ + = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TLC10/MF10A			TLC20/MF10C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OPP}	Maximum peak-to-peak output voltage swing		R_L = 3.5 kΩ at all outputs	±4	±4.1		±3.8	±3.9		V
I_{OS}	Short-circuit output current, Pins 3 and 18	Source	See Note 4		2			2		mA
		Sink			50			50		
I_{CC}	Supply current				8	10		8	10	mA

NOTE 4: The short-circuit output current for pins 1, 2, 19, and 20 will be typically the same as pins 3 and 18.

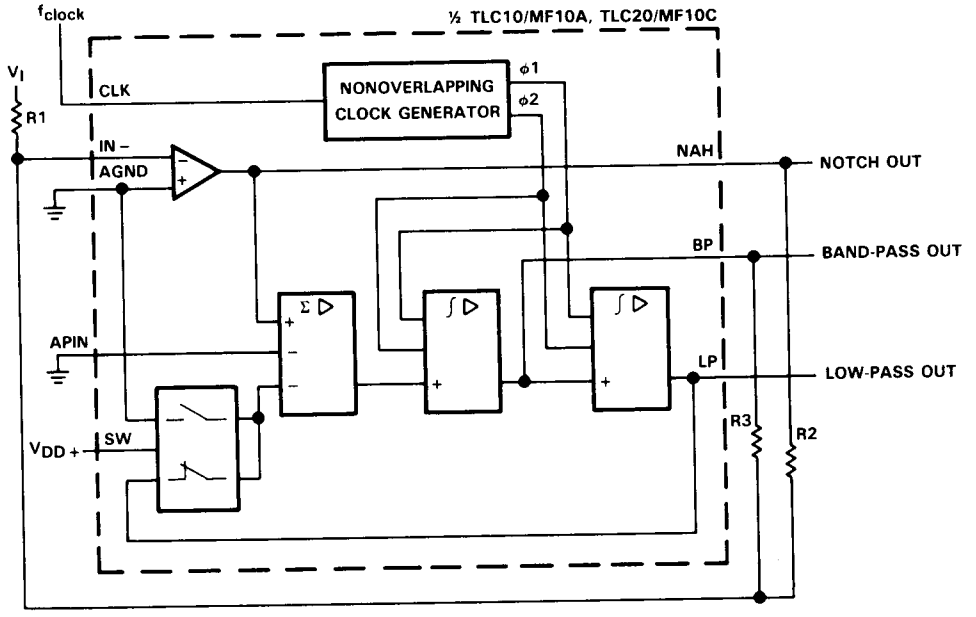
operating characteristics at $V_{CC\pm}$ = ±5 V, $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC10/MF10A			TLC20/MF10C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Critical-frequency range	$f_o \times Q \leq 200$ kHz		20	30		20	30		kHz
Maximum clock frequency, f_{clock}	See Note 3		1	1.5		1	1.5		MHz
Clock to center-frequency ratio	$f_o \leq 5$ kHz, R3/R2 = 10, Mode 1, See Figure 1	Pin 12 at 5 V	49.64	49.94	50.24	49.24	49.94	50.64	
		Pin 12 at 0 V	98.75	99.35	99.95	97.86	99.35	100.84	
Temperature coefficient of center frequency	$f_o \leq 5$ kHz, R3/R2 = 20, Mode 1, See Figure 1	Pin 12 at 5 V		±10			±10		ppm/°C
		Pin 12 at 0 V		±100			±100		
Filter Q (quality factor) deviation from 20	$f_o \leq 5$ kHz, R3/R2 = 20, Mode 1, See Figure 1	Pin 12 at 5 V		±2%	±4%		±2%	±6%	
		Pin 12 at 0 V		±2%	±3%		±2%	±6%	
Temperature coefficient of measured filter Q	$f_o \leq 5$ kHz, R3/R2 = 20, Mode 1			±500			±500		ppm/°C
Low-pass output deviation from unity gain	R1 = R2 = 10 kΩ, Mode 1, See Figure 1				±2%			±2%	
Crosstalk attenuation				60			60		dB
Clock feedthrough voltage				10			10		mV
Operational amplifier gain-bandwidth product				2.5			2.5		MHz
Operational amplifier slew rate				7			7		V/μs

TYPICAL APPLICATION DATA

modes of operation

The TLC10/MF10A and TLC20/MF10C are switched-capacitor (sampled-data) filters that closely approximate continuous filters. Each filter section is designed to approximate the response of a second-order variable filter. When the sampling frequency is much larger than the frequency band of interest, the sampled-data filter is a good approximation to its continuous time equivalent. In the case of the TLC10/MF10A and TLC20/MF10C, the ratio is about 50:1 or 100:1. To fully describe their transfer function, a time domain approach would be appropriate. Since this may appear cumbersome, the following application examples are based on the well known frequency domain. It should be noted that in order to obtain the actual filter response, the filter's response must be examined in the z-domain.

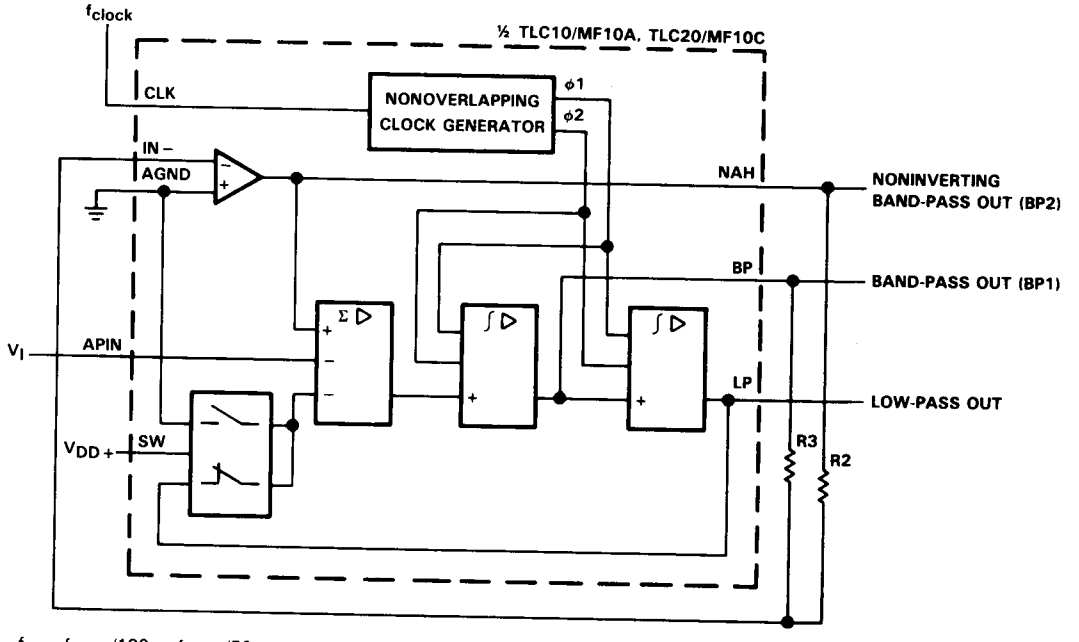


$f_o = f_{clock}/100$ or $f_{clock}/50$
$f_{notch} = f_o$
$H_{OLP} = -R2/R1$ (as $f \rightarrow 0$)
$H_{OBP} = -R3/R1$ (at $f = f_o$)
H_{ON} = notch gain { as f approaches 0 $-R2/R1$; as f approaches 0.5 f_{clock}
$Q = f_o/BW = R3/R2$

Circuit dynamics:
The following expressions determine the swing at each output as a function of the desired Q of the second-order function.
$H_{OLP} = H_{OBP}/Q$ or $H_{OLP} \times Q = H_{ON} \times Q$
H_{OLP} (peak) $= Q \times H_{OLP}$ (for high Qs)

FIGURE 1. MODE 1 FOR NOTCH, BAND-PASS, AND LOW-PASS OUTPUTS: $f_{notch} = f_o$

TYPICAL APPLICATION DATA



$f_o = f_{clock}/100$ or $f_{clock}/50$
$Q = R3/R2$
$H_{OLP} = -1$ H_{OLP} (peak) $= Q \times H_{OLP}$ (for high Qs)
$H_{OBP1} = -R3/R2$
$H_{OBP2} = 1$ (noninverting)

Circuit dynamics:
$H_{OBP1} = Q$

FIGURE 2. MODE 1a FOR NONINVERTING BAND-PASS AND LOW-PASS OUTPUTS

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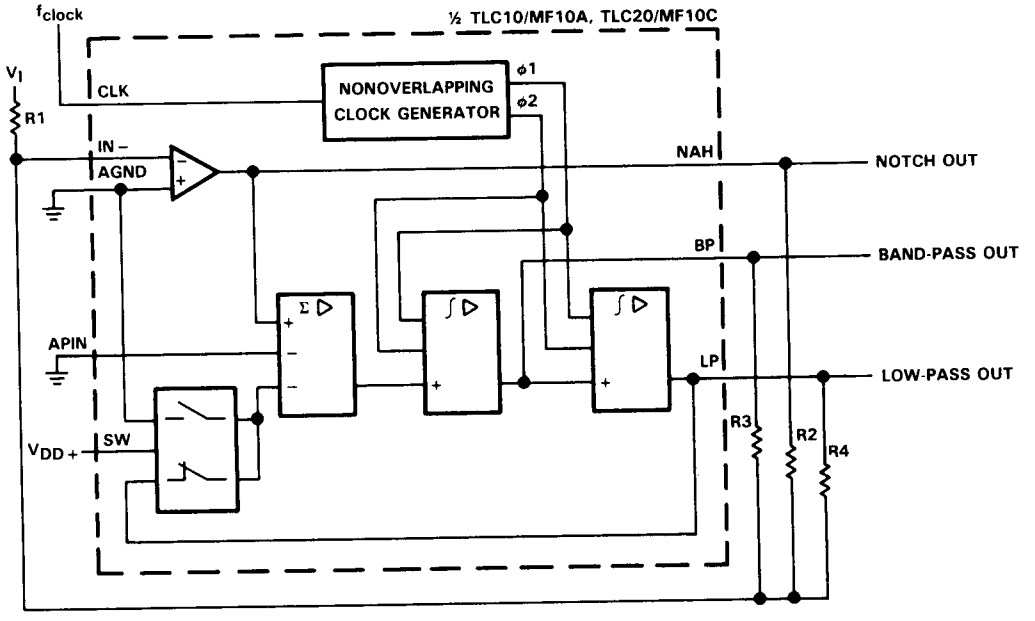
TYPICAL APPLICATION DATA



$f_o = f_{notch} \times \sqrt{R2/R4 + 1}$

$f_{notch} = f_{clock}/100$ or $f_{clock}/50$

$Q = \dfrac{\sqrt{R2/R4 + 1}}{R2/R3}$

H_{OLP} (as f approaches 0) $= \dfrac{-R2/R1}{R2/R4 + 1}$

H_{OBP} (at $f = f_o$) $= -R3/R1$

H_{ON1} (as f approaches 0) $= \dfrac{-R2/R1}{R2/R4 + 1}$

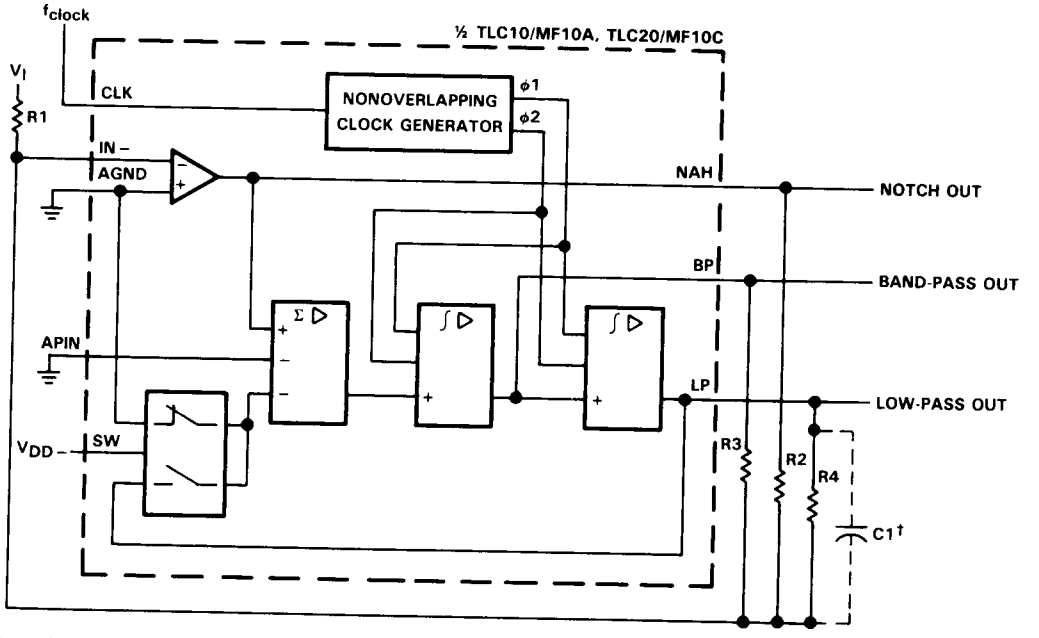
H_{ON2} (as f approaches 0.5 f_{clock}) $= -R2/R1$

Circuit dynamics:

$H_{OBP} = Q\sqrt{H_{OLP} \times H_{ON2}} = Q\sqrt{H_{ON1} \times H_{ON2}}$

FIGURE 3. MODE 2 FOR NOTCH 2, BAND-PASS, AND LOW-PASS OUTPUTS: $f_{notch} < f_o$

TYPICAL APPLICATION DATA



$f_o = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{R2/R4}$

$Q = \sqrt{R2/R4} \times R3/R2$

H_{OHP} (as f approaches 0.5 f_{clock}) = $-R2/R1$

H_{OLP} (as f approaches 0) = $-R4/R1$

H_{OBP} (at $f = f_o$) = $-R3/R1$

Circuit dynamics:

$R2/R4 = H_{OHP}/H_{OLP}$: $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q$

H_{OLP} (peak) = $Q \times H_{OLP}$ (for high Qs)

H_{OHP} (peak) = $Q \times H_{OHP}$ (for high Qs)

†In this mode, the feedback loop is closed around the input summing amplifier; the finite GBW product of this operational amplifier will cause a slight Q enhancement. If this is a problem, connect a low-value capacitor (10 pF to 100 pF) across R4 to provide some phase lead.

FIGURE 4. MODE 3 FOR HIGH-PASS, BAND-PASS, AND LOW-PASS OUTPUTS

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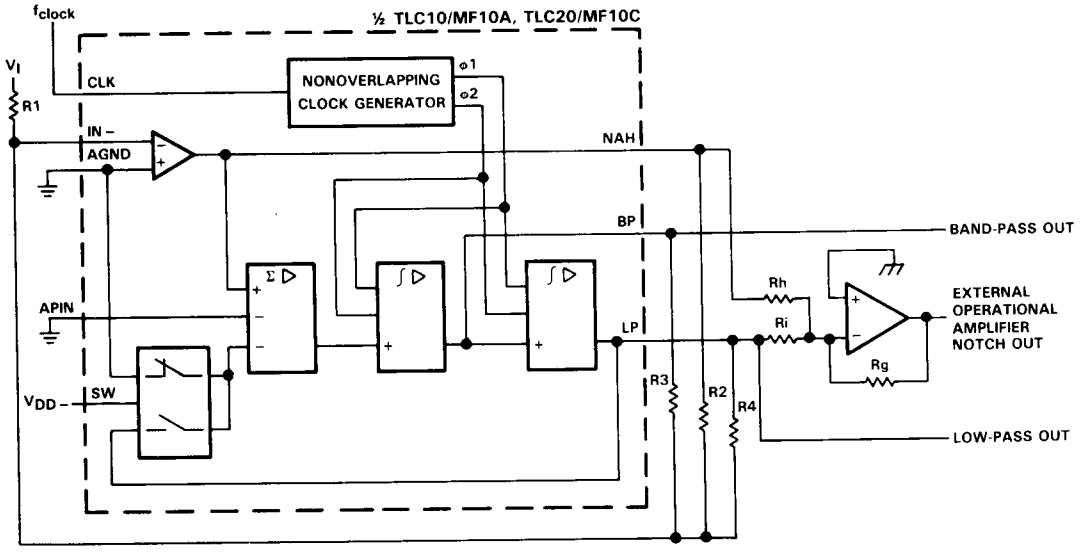
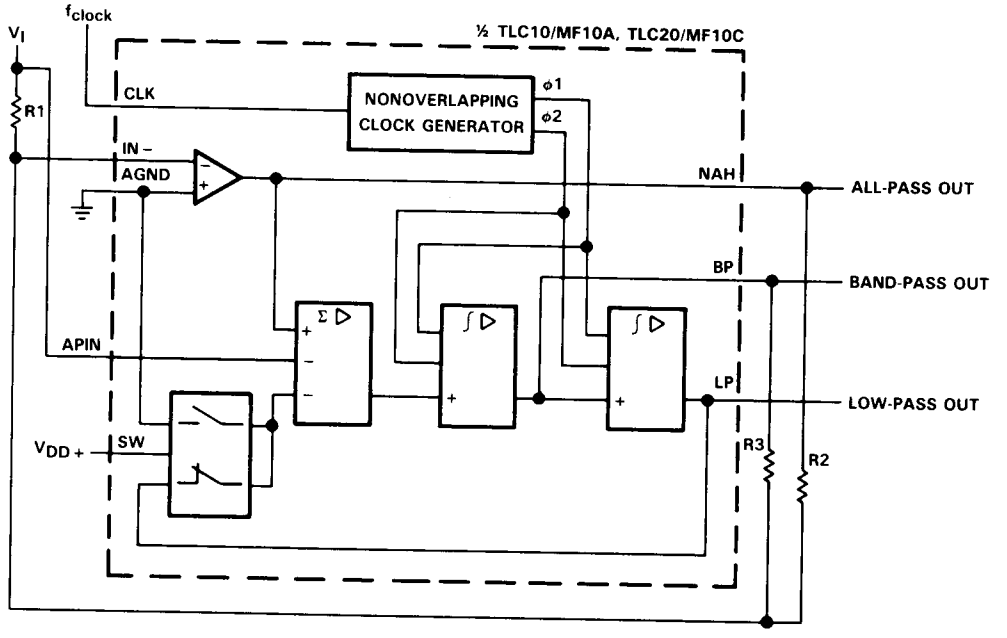
TYPICAL APPLICATION DATA



$f_o = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{R2/R4}$
$Q = \sqrt{R2/R4} \times R3/R2$
$H_{OHP} = -R2/R1$
$H_{OBP} = -R3/R1$
$H_{OLP} = -R4/R1$
$f_{notch} = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{Rh/Ri}$
H_{ON} (at $f = f_o$) $= |Q(Rg/Ri \times H_{OLP} - Rg/Rh \times HOHP)|$
H_{ON1} (as f approaches 0) $= Rg/Ri \times H_{OLP}$
H_{ON2} (as f approaches 0.5 f_{clock}) $= -Rg/Rh \times H_{OHP}$

FIGURE 5. MODE 3a FOR HIGH-PASS, BAND-PASS, LOW-PASS, AND NOTCH OUTPUTS WITH EXTERNAL OPERATIONAL AMPLIFIER

TYPICAL APPLICATION DATA



$f_o = f_{clock}/100$ or $f_{clock}/50$

$f_z = f_o$[†]

$Q = f_o/BW = R3/R2$

$Q_z = R3/R1$

H_{OAP} (at $0 \le f \le 0.5\ f_{clock}$) $= -R2/R1 = -1$
(for AP output R1 = R2)

H_{OLP} (as f approaches 0) $= -(R2/R1 + 1) = -2$

H_{OBP} (at $f = f_o$) $= -R3/R2\ (R2/R1 + 1) = -2\ (R3/R2)$

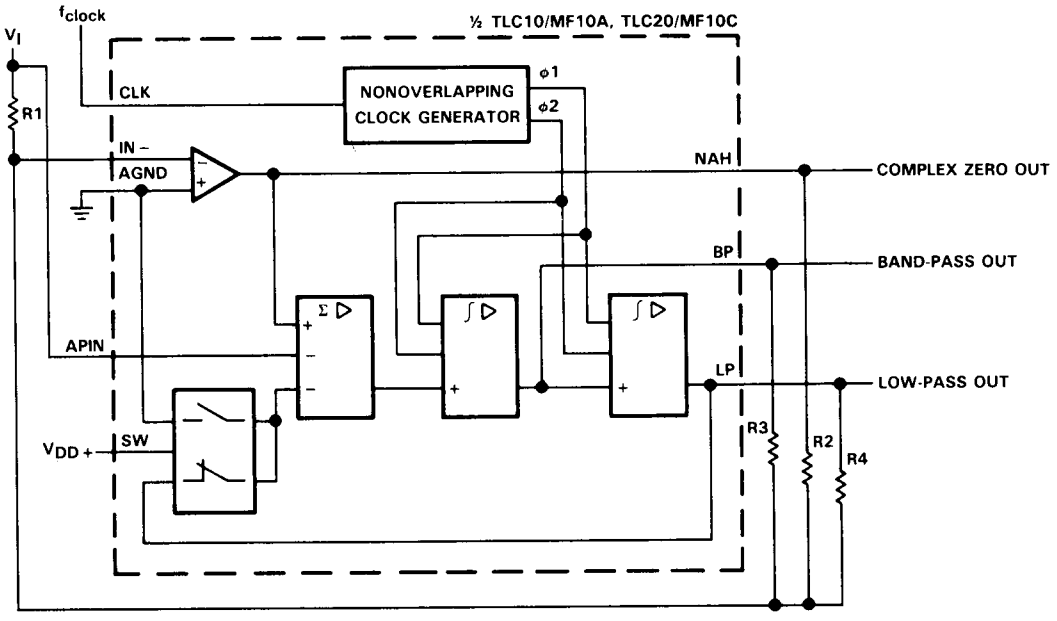
Circuit dynamics:

$$H_{OBP} = H_{OLP} \times Q = (H_{OAP} + 1)\ Q$$

[†]Due to the sampled-data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4-dB peaking around f_o of the all-pass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

FIGURE 6. MODE 4 FOR ALL-PASS, BAND-PASS, AND LOW-PASS OUTPUTS

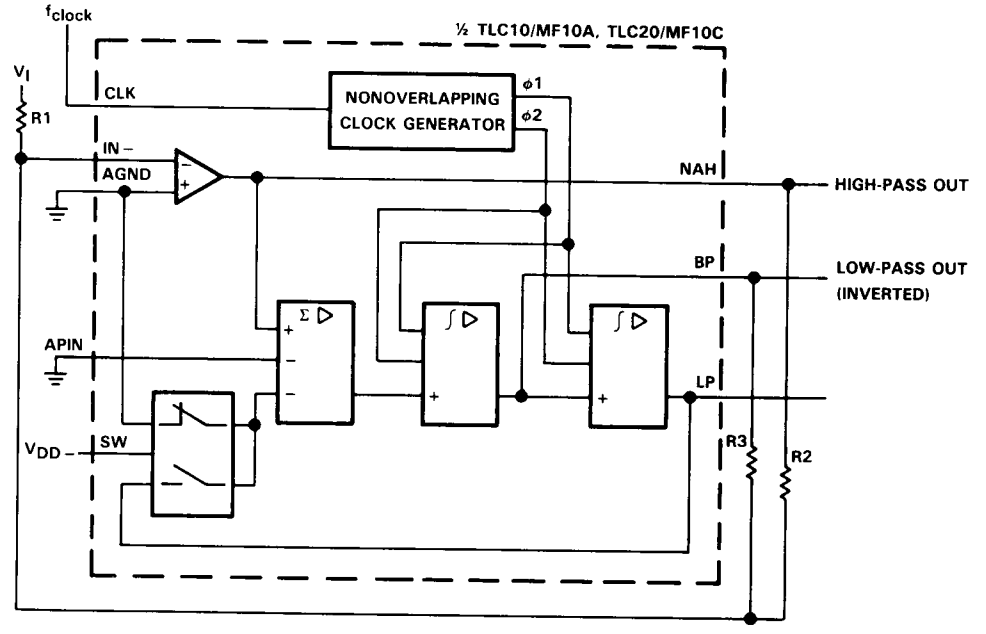
TYPICAL APPLICATION DATA



$f_o = \sqrt{R2/R4 + 1} \times (f_{clock}/100 \text{ or } f_{clock}/50)$
$f_z = \sqrt{1 - R1/R4} \times (f_{clock}/100 \text{ or } f_{clock}/50)$
$Q = \sqrt{R2/R4 + 1} \times R3/R2$
$Q_z = \sqrt{1 - R1/R4} \times R3/R1$
H_{OZ1} (as f approaches 0) = R2 (R4 – R1)/R1 (R2 + R4)
H_{OZ2} (as f approaches 0.5 f_{clock}) = R2/R1
$H_{OBP} = (R2/R1 + 1) \times R3/R2$
$H_{OLP} = (R2 + R1)/(R2 + R4) \times R4/R1$

FIGURE 7. MODE 5 FOR NUMERATOR COMPLEX ZEROS, BAND-PASS, AND LOW-PASS OUTPUTS

TYPICAL APPLICATION DATA



f_c = R2/R3 (f_{clock}/100 or f_{clock}/50)
H_{OLP} = –R3/R1
H_{OHP} = –R2/R1

FIGURE 8. MODE 6 FOR SINGLE-POLE HIGH-PASS AND LOW-PASS OUTPUT

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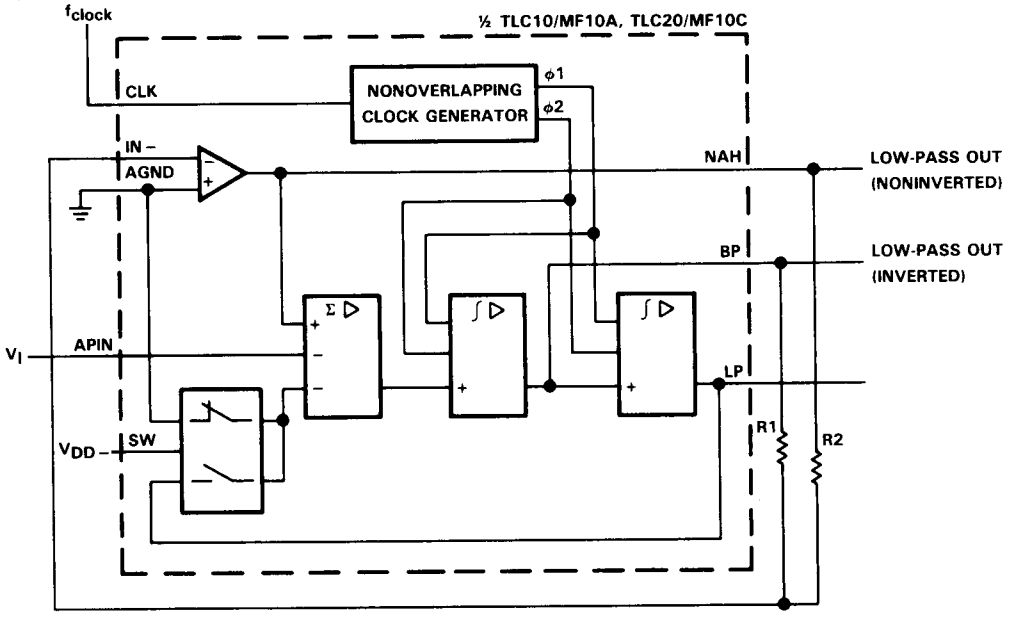
TYPICAL APPLICATION DATA



f_c = R2/R3 × (f_{clock}/100 or f_{clock}/50)
H_{OLP1} = 1 (noninverting)
H_{OLP2} = –R3/R2

FIGURE 9. MODE 6a FOR SINGLE-POLE LOW-PASS OUTPUT (INVERTED AND NONINVERTED)

TYPICAL APPLICATION DATA

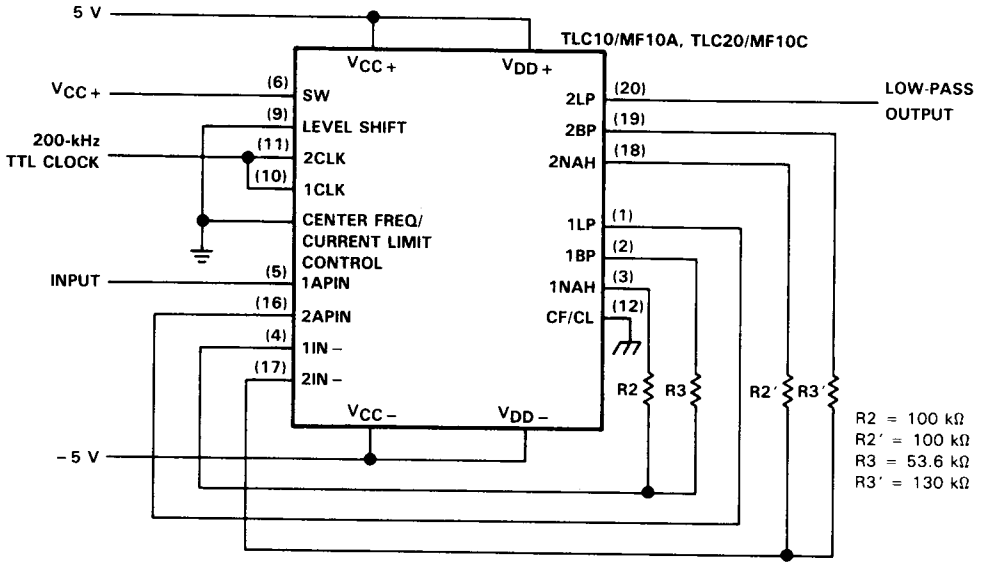
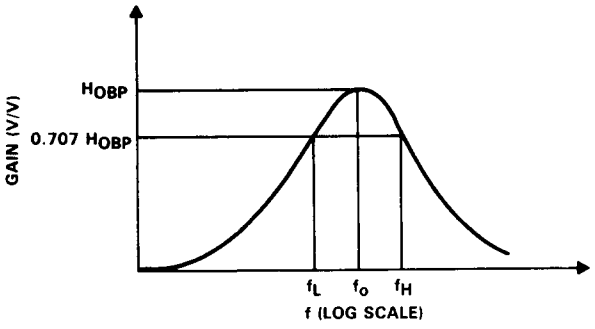


FIGURE 10. FOURTH-ORDER 2-kHz LOW-PASS BUTTERWORTH FILTER

filter terminology

f_c	The cutoff frequency of the low-pass or high-pass filter output
f_{clock}	The input clock frequency to the device
f_{notch}	The notch frequency of the notch output
f_o	The center frequency of the complex pole pair second-order function
f_z	The center frequency of the complex zero pair
H_{OBP}	The band-pass output voltage gain (V/V) at the band-pass center frequency
H_{OHP}	The high-pass output voltage gain (V/V) as the frequency approaches 0.5 f_{clock}
H_{OLP}	The low-pass output voltage gain (V/V) as the frequency approaches 0
H_{ON}	The notch output voltage gain (V/V) at the notch frequency
H_{ON1}	The low-side notch output voltage gain as the frequency approaches 0
H_{ON2}	The high-side notch output voltage gain as the frequency approaches 0.5 f_{clock}
H_{OZ1}	Gain at complex zero output (as $f \rightarrow 0$ Hz)
H_{OZ2}	Gain at complex zero output (as f approaches 0.5 f_{clock})
Q	The quality factor of the complex pole pair second-order function. Q is the ratio of f_o to the 3-dB bandwidth of the band-pass output. The value of Q also affects the possible peaking of the low-pass and high-pass outputs.
Q_z	The quality factor of the complex zero pair, if such a complex pair exists. This parameter is used when an all-pass filter output is desired.

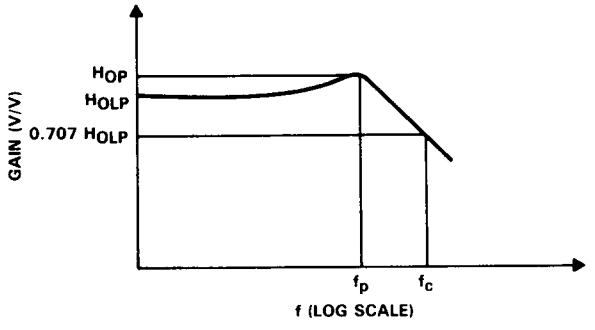


$$Q = \frac{f_o}{f_H - f_L} \; ; \; f_o = \sqrt{f_L f_H}$$

$$f_L = f_o \left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_o \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

FIGURE 11. BAND-PASS OUTPUT

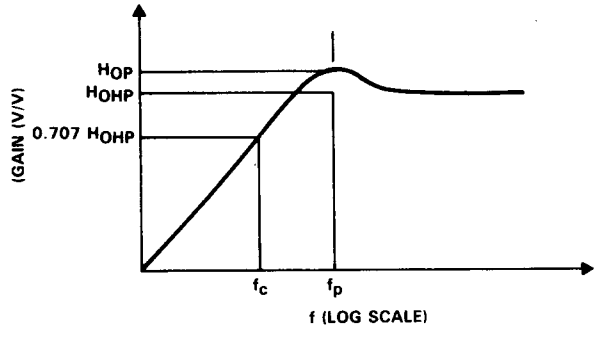


$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_o \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 12. LOW-PASS OUTPUT



$$f_c = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \right]^{-1}$$

$$f_p = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}} \right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 13. HIGH-PASS OUTPUT