

MM54HC373/MM74HC373



T-46-07-11

MM54HC373/MM74HC373 TRI-STATE® Octal D-Type Latch

General Description

These high speed octal D-type latches utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present

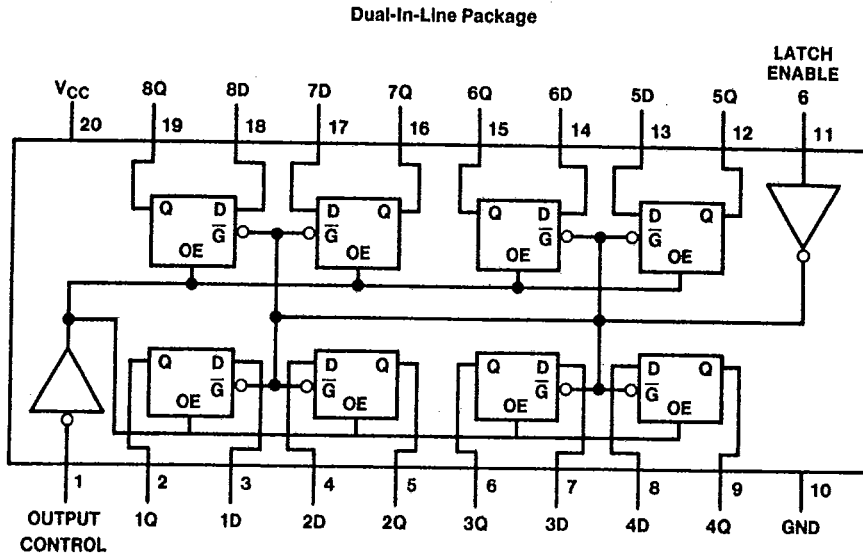
at the other inputs and the state of the storage elements.

The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum (74 Series)
- Output drive capability: 15 LS-TTL loads

Connection Diagram



Top View

TL/F/5335-1

Order Number MM54HC373* or MM74HC373*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Output Control	Latch Enable	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
 Q_0 = level of output before steady-state input conditions were established.
 Z = high impedance



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})	-0.5 to +7.0V
DC Input Voltage (V _{IN})	-1.5 to V _{CC} + 1.5V
DC Output Voltage (V _{OUT})	-0.5 to V _{CC} + 0.5V
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA
DC Output Current, per pin (I _{OUT})	±35 mA
DC V _{CC} or GND Current, per pin (I _{CC})	±70 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Power Dissipation (P _D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T _L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage (V _{IN} , V _{OUT})	0	V _{CC}	V
Operating Temp. Range (T _A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t _r , t _f)			
V _{CC} =2.0V		1000	ns
V _{CC} =4.5V		500	ns
V _{CC} =6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		74HC T _A = -40 to 85°C		54HC T _A = -55 to 125°C		Units
				Typ	Guaranteed Limits					
V _{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	1.5	V	
			4.5V		3.15	3.15	3.15	V		
			6.0V		4.2	4.2	4.2	V		
V _{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	0.5	V	
			4.5V		1.35	1.35	1.35	V		
			6.0V		1.8	1.8	1.8	V		
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	4.4	V		
			6.0V	6.0	5.9	5.9	5.9	V		
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	4.5V	4.2	3.98	3.84	3.7	V		
			6.0V	5.7	5.48	5.34	5.2	V		
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	0.1	0.1	V	
			4.5V	0	0.1	0.1	0.1	V		
			6.0V	0	0.1	0.1	0.1	V		
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	4.5V	0.2	0.26	0.33	0.4	V		
			6.0V	0.2	0.26	0.33	0.4	V		
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA		
I _{OZ}	Maximum TRI-STATE Output Leakage Current	V _{IN} = V _{IH} or V _{IL} , OC = V _{IH} V _{OUT} = V _{CC} or GND	6.0V		±0.5	±5	±10	μA		
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0V		8.0	80	160	μA		

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.
 Note 2: Unless otherwise specified all voltages are referenced to ground.
 Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.
 Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.
 **V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

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AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, t_r=t_f=6ns$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L = 45 pF$	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to Q	$C_L = 45 pF$	21	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$ $C_L = 45 pF$	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$ $C_L = 5 pF$	18	25	ns
t_S	Minimum Set Up Time			5	ns
t_H	Minimum Hold Time			10	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0-6.0V, C_L=50 pF, t_r=t_f=6ns$ (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^{\circ}C$		74HC $T_A = -40$ to $85^{\circ}C$		54HC $T_A = -55$ to $125^{\circ}C$		Units
				Typ	Guaranteed Limits	Typ	Guaranteed Limits	Typ	Guaranteed Limits	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L = 50 pF$ $C_L = 150 pF$	2.0V	50	150	188	225	ns		
			2.0V	80	200	250	300	ns		
		4.5V	22	30	37	45	ns			
			30	40	50	60	ns			
		6.0V	19	26	31	39	ns			
26	35		44	53	ns					
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to Q	$C_L = 50 pF$ $C_L = 150 pF$	2.0V	63	175	220	263	ns		
			2.0V	110	225	280	338	ns		
		4.5V	25	35	44	52	ns			
			35	45	56	68	ns			
		6.0V	21	30	37	45	ns			
28	39		49	59	ns					
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$ $C_L = 50 pF$ $C_L = 150 pF$	2.0V	50	150	188	225	ns		
			2.0V	80	200	250	300	ns		
		4.5V	21	30	37	45	ns			
			30	40	50	60	ns			
		6.0V	19	26	31	39	ns			
26	35		44	53	ns					
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$ $C_L = 50 pF$	2.0V	50	150	188	225	ns		
			4.5V	21	30	37	45	ns		
			6.0V	19	26	31	39	ns		
t_S	Minimum Set Up Time		2.0V		50	60	75	ns		
			4.5V		9	13	15	ns		
			6.0V		9	11	13	ns		
t_H	Minimum Hold Time		2.0V		5	5	5	ns		
			4.5V		5	5	5	ns		
			6.0V		5	5	5	ns		
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns		
			4.5V	10	16	20	24	ns		
			6.0V	9	14	18	20	ns		
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50 pF$	2.0V	25	60	75	90	ns		
			4.5V	7	12	15	18	ns		
			6.0V	6	10	13	15	ns		
C_{PD}	Power Dissipation Capacitance (Note 5)	(per latch) $OC = V_{CC}$ $OC = GND$		30				pF		
C_{IN}	Maximum Input Capacitance			5	10		10	pF		
C_{OUT}	Maximum Output Capacitance			15	20		20	pF		

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

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