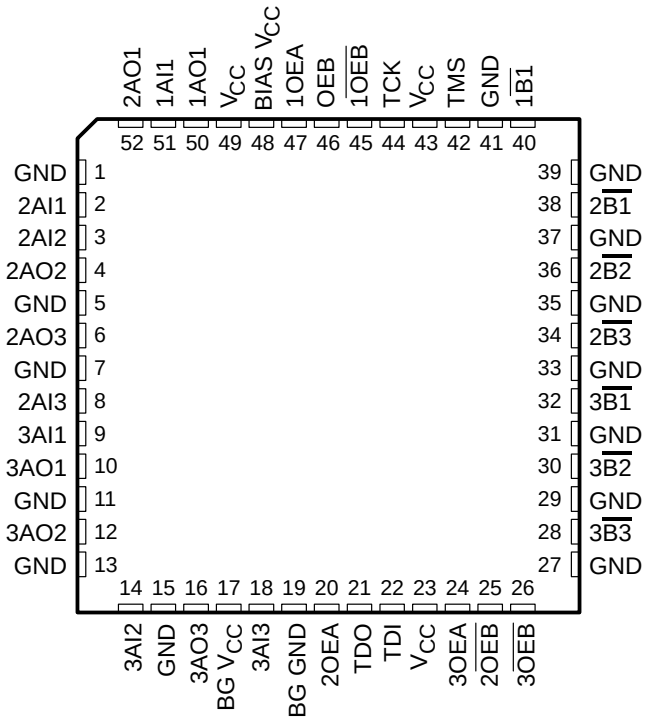
- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination**

RC PACKAGE
(TOP VIEW)



description

The SN74FB2041A is a 7-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. The device is specifically designed to be compatible with IEEE Std 1194.1-1991.

The $\overline{B}$ port operates at BTL signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.1 V, the $\overline{B}$ port is turned off. The enable/disable logic partitions the device as two 3-bit sections and one 1-bit section.

The A port operates at TTL signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

description (continued)

The pins TMS, TCK, TDI, and TDO are nonfunctional, i.e., not intended for use with the IEEE Std 1149.1 (JTAG) test bus. TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

ORDERING INFORMATION

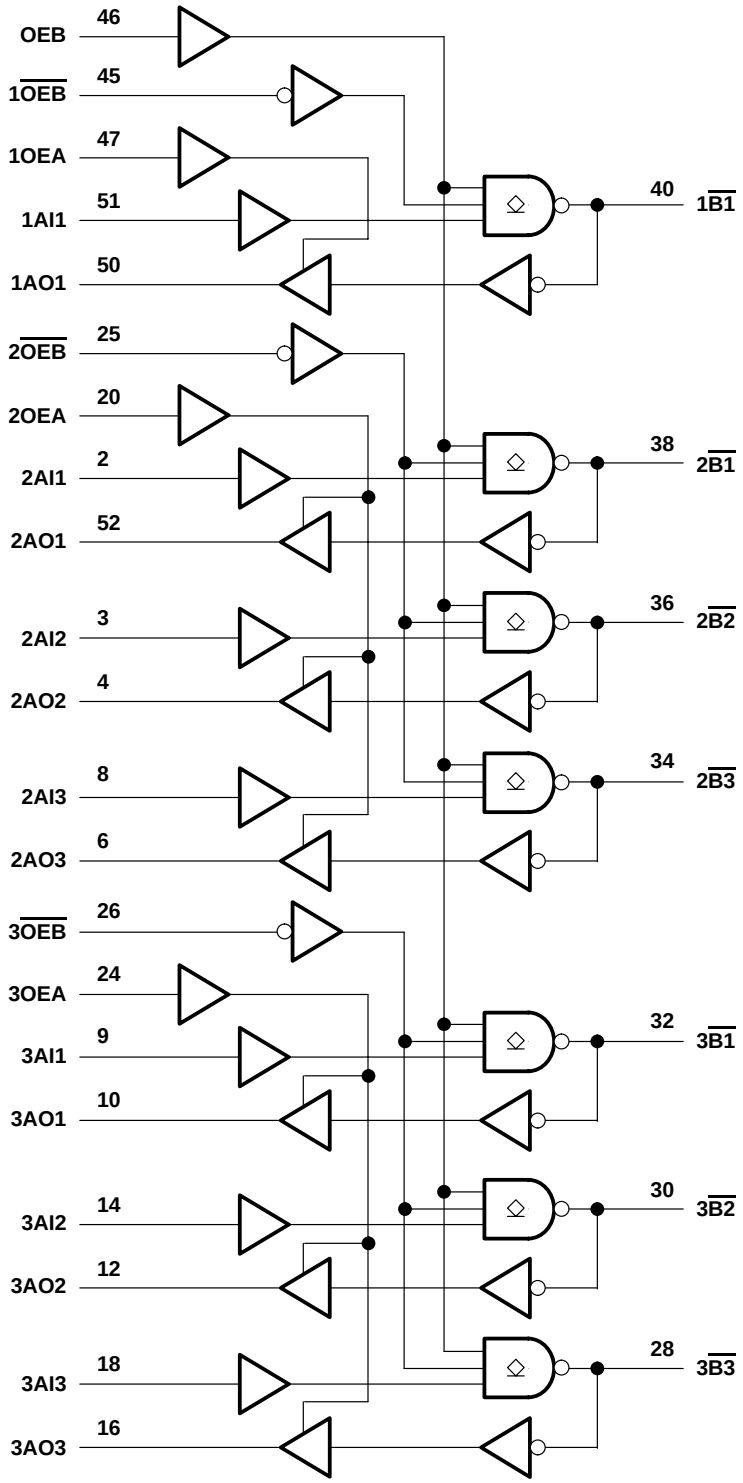
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFP – RC	Tube	SN74FB2041ARC	FB2041A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	$\overline{B}$ data to AO bus
X	H	H	
H	L	L	$\overline{AI}$ data to B bus
H	L	H	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O: A port . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 44°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO port			–3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
	Except $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –40 mA			–0.5	
V_{OH}	AO port	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5	3.3		V
V_{OL}	AO port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	V
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50	µA
	$\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100	µA
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_{OZPU}	AO port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50	µA
I_{OZPD}	AO port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OS}§	AO port	V_{CC} = 5.5 V,	V_O = 0	–30		–180	mA
I_{CC}	AI port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0			45	mA
	$\overline{B}$ port to AO port					65	
C_i	AI port	V_I = 0.5 V or 2.5 V			3		pF
	Control inputs				3		
C_o	AO port	V_O = 0.5 V or 2.5 V			5.5		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 to 4.5 V				5	pF
		V_{CC} = 4.5 V to 5.5 V				5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

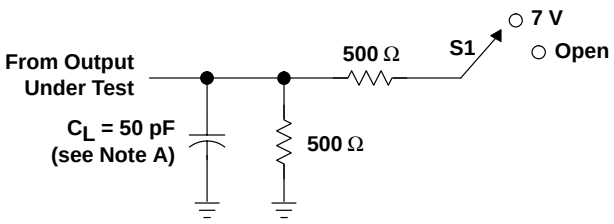
PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450	µA
		V_{CC} = 4.5 V to 5.5 V				10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 5 V		1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

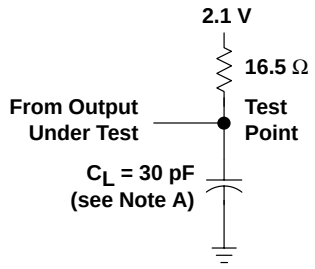
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	AI	$\overline{B}$	2.3	3.9	5.1	2	5.6	ns
t_{PHL}			2.6	4.1	5	2.5	5.3	
t_{PLH}	$\overline{B}$	AO	2	3.6	4.8	1.7	5.3	ns
t_{PHL}			2.3	3.8	4.9	2	6.4	
t_{PLH}	OEB	$\overline{B}$	3	4.6	5.8	2.6	6.3	ns
t_{PHL}			3.1	4.7	6	3.1	6.2	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	2.7	4.3	5.6	2.6	5.8	ns
t_{PHL}			2.7	4.2	5.3	2.5	6.4	
t_{PZH}	OEA	AO	1.5	3.2	5.2	1.5	5.2	ns
t_{PZL}			1.1	2.8	5	1	5	
t_{PHZ}	OEA	AO	1	2.4	3.9	1	4.2	ns
t_{PLZ}			2.2	3.8	5.6	1.7	5.8	
$t_{sk(p)}$†	Pulse skew, AI to $\overline{B}$ or $\overline{B}$ to AO			0.5				ns
$t_{sk(o)}$†	Output skew, AI to $\overline{B}$ or $\overline{B}$ to AO			0.4				ns
t_t	Rise time, 1.3 V to 1.8 V, $\overline{B}$ outputs		1	1.6	2.4	1	2.5	ns
	Fall time, 1.8 V to 1.3 V, $\overline{B}$ outputs		1	1.4	2.3	1	2.4	
$t_{(pr)}$	$\overline{B}$-port input pulse rejection		1			1		ns

† Skew values are applicable for through mode only.

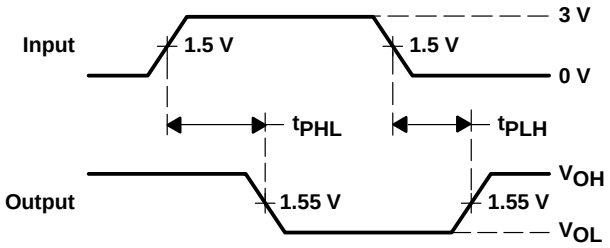
PARAMETER MEASUREMENT INFORMATION



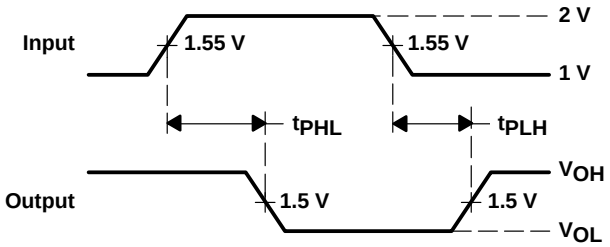
LOAD CIRCUIT FOR A OUTPUTS



LOAD CIRCUIT FOR B OUTPUTS

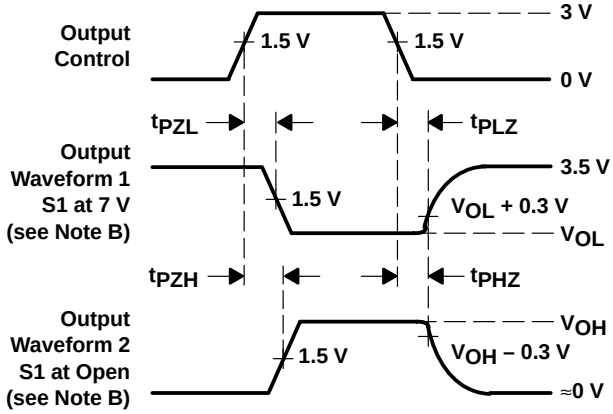


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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