

SN54HC257, SN54HC258, SN74HC257, SN74HC258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SCLS224B – DECEMBER 1982 – REVISED SEPTEMBER 2003

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Inverting Outputs Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- 'HC257 . . . Typical $t_{pd} = 9$ ns
- 'HC258 . . . Typical $t_{pd} = 12$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Provides Bus Interface from Multiple Sources in High-Performance Systems

SN54HC257, SN54HC258 . . . J PACKAGE
SN74HC257, SN74HC258 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC257, SN54HC258 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC257N	SN74HC257N	
			SN74HC258N	SN74HC258N	
	SOIC – D	Tube of 40	SN74HC257D	HC257	
			Reel of 2500		SN74HC257DR
			Reel of 250		SN74HC257DT
			Reel of 2500	SN74HC258D	HC258
				SN74HC258DR	
				SN74HC258DR	
	SOP – NS	Reel of 2000	SN74HC257NSR	HC257	
			SN74HC258NSR	HC258	
TSSOP – PW	Tube of 90	SN74HC257PW	HC257		
		Reel of 2000		SN74HC257PWR	
		Reel of 250		SN74HC257PWT	
	Reel of 250	SN74HC258PW	HC258		
		Reel of 2000		SN74HC258PWR	
		Reel of 250		SN74HC258PWT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC257J	SNJ54HC257J	
			SNJ54HC258J	SNJ54HC258J	
	LCCC – FK	Tube of 55	SNJ54HC257FK	SNJ54HC257FK	
			SNJ54HC258FK	SNJ54HC258FK	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

These devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable (\overline{G}) input is at a high logic level.

To ensure the high-impedance state during power up or power down, \overline{G} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

\overline{G}	INPUTS			OUTPUT Y	
	$\overline{A/B}$	A	B	'HC257	'HC258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

'HC257 logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, and PW packages.

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recommended operating conditions (see Note 2)

		SN54HC257, SN54HC258			SN74HC257, SN74HC258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 6 V		4.2	4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V			0.3		0.5	V
		V _{CC} = 4.5 V			0.9		1.35	
		V _{CC} = 6 V			1.2		1.8	
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise/fall time	V _{CC} = 2 V			1000		1000	ns
		V _{CC} = 4.5 V			500		500	
		V _{CC} = 6 V			400		400	
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC257, SN54HC258		SN74HC257, SN74HC258		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V
			4.5 V	4.4	4.499		4.4		4.4	
		6 V	5.9	5.999		5.9		5.9		
		I _{OH} = -6 mA	4.5 V	3.98	4.3		3.7		3.84	
6 V	5.48		5.8		5.2		5.34			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1	0.1	V
			4.5 V		0.001	0.1		0.1	0.1	
		6 V		0.001	0.1		0.1	0.1		
		I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4	0.33	
6 V			0.15	0.26		0.4	0.33			
I _I	V _I = V _{CC} or 0	6 V		±0.1	±100		±1000	±1000	nA	
I _{OZ}	V _O = V _{CC} or 0	6 V		±0.01	±0.5		±10	±5	μA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V			8		160	80	μA	
C _i		2 V to 6 V		3	10		10	10	pF	



SN54HC257, SN54HC258, SN74HC257, SN74HC258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC257		SN74HC257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		9	17		25		21	
	\bar{A}/\bar{B}	Any Y	2 V		50	100		150		125	
			4.5 V		10	20		30		25	
			6 V		9	17		25		21	
t_{en}	\bar{G}	Any Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	\bar{G}	Any Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC257		SN74HC257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		75	150		245		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
	\bar{A}/\bar{B}	Any Y	2 V		75	150		245		190	
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{en}	\bar{G}	Any Y	2 V		100	200		300		250	ns
			4.5 V		24	40		60		50	
			6 V		18	34		51		43	
t_t		Any Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	



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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC258		SN74HC258		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		60	100		150		125	ns
			4.5 V		13	20		30		25	
			6 V		12	17		25		21	
	\bar{A}/B	Any Y	2 V		60	115		175		145	
			4.5 V		13	23		35		29	
			6 V		12	20		30		25	
t_{en}	\bar{G}	Any Y	2 V		70	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	\bar{G}	Any Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC258		SN74HC258		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		95	150		245		190	ns
			4.5 V		23	30		45		38	
			6 V		21	26		38		32	
	\bar{A}/B	Any Y	2 V		95	165		240		210	
			4.5 V		23	33		48		42	
			6 V		21	28		41		36	
t_{en}	\bar{G}	Any Y	2 V		100	200		300		250	ns
			4.5 V		24	40		60		50	
			6 V		18	34		51		43	
t_t		Any Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, $T_A = 25^\circ\text{C}$

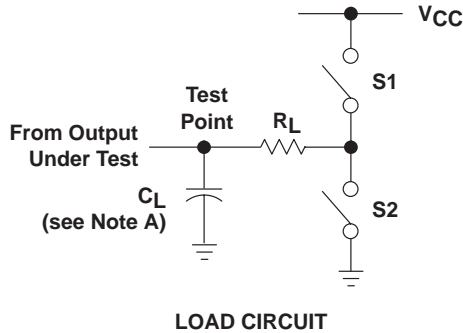
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per multiplexer	No load	40	pF



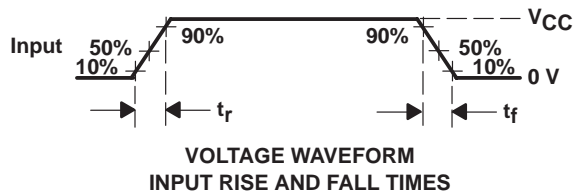
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PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2	
t_{en}	t_{PZH}	1 k Ω	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 k Ω	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t	--	50 pF or 150 pF	Open	Open	



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
85124012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85124012A SNJ54HC 257FK	Samples
8512401EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8512401EA SNJ54HC257J	Samples
SN54HC257J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC257J	Samples
SN74HC257DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC257	Samples
SN74HC257N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC257N	Samples
SN74HC257NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC257	Samples
SN74HC257PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC257	Samples
SN74HC258D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258	Samples
SN74HC258DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258	Samples
SN74HC258N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC258N	Samples
SN74HC258NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258	Samples
SN74HC258PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258	Samples
SN74HC258PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258	Samples
SNJ54HC257FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85124012A SNJ54HC 257FK	Samples
SNJ54HC257J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8512401EA SNJ54HC257J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC257, SN74HC257 :

● Catalog : [SN74HC257](#)

● Military : [SN54HC257](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC257DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC257DR	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HC257NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC257NSR	SO	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC257PWR	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74HC258DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC258NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC258PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC257DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC257DR	SOIC	D	16	2500	366.0	364.0	50.0
SN74HC257NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC257NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC257PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC257PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC257PWR	TSSOP	PW	16	2000	366.0	364.0	50.0
SN74HC258DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC258NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC258PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
85124012A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74HC257N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC257N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC258D	D	SOIC	16	40	507	8	3940	4.32
SN74HC258N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC258N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC258PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SNJ54HC257FK	FK	LCCC	20	1	506.98	12.06	2030	NA



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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