

# CDx4HC(T)166 High-Speed CMOS Logic 8-Bit Parallel-In/Serial-Out Shift Register

## 1 Features

- Buffered inputs
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL Loads
  - Bus driver outputs: 15 LSTTL Loads
- Wide operating temperature range: -55°C to 125°C
- Balanced propagation delay and transition time
- Significant power reduction compared to LSTTL Logic ICs
- HC Types
  - 2 V to 6 V operation
  - High noise immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5 V$
- HCT Types
  - 4.5 V to 5.5 V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2 V$  (Min)

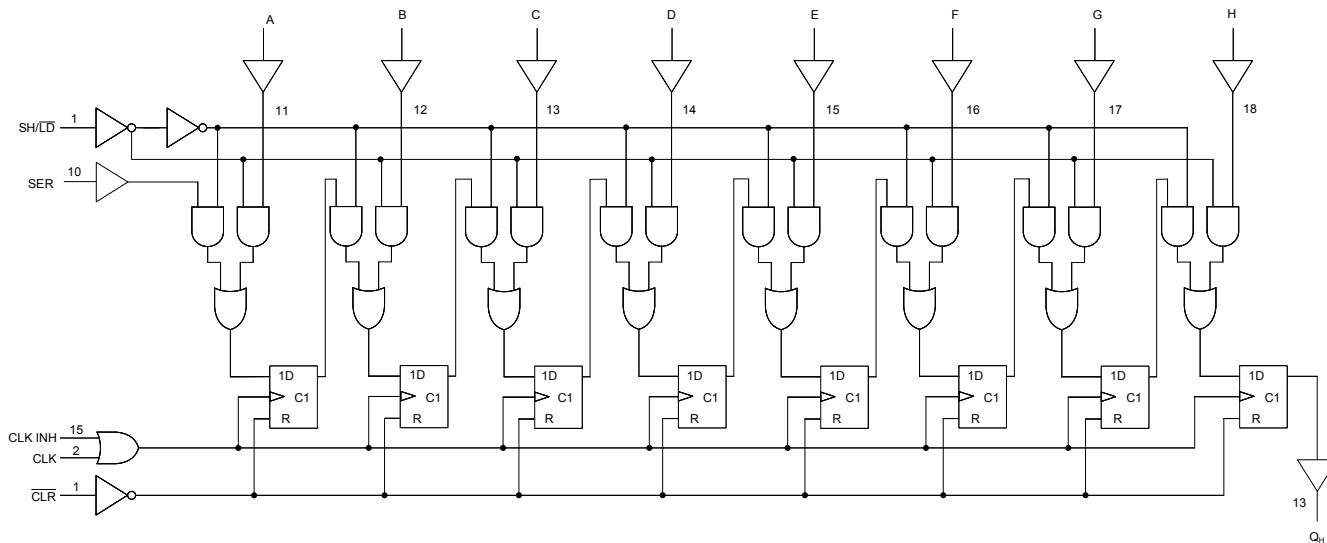
## 2 Description

The 'HC166 and 'HCT166 8-bit shift register is fabricated with silicon gate CMOS technology. It possesses the low power consumption of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device.

### Device Information

| PART NUMBER   | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)    |
|---------------|------------------------|--------------------|
| CD54HC166F3A  | CDIP (16)              | 24.38 mm × 6.92 mm |
| CD54HCT166F3A | CDIP (16)              | 24.38 mm × 6.92 mm |
| CD74HC166M    | SOIC (16)              | 9.90 mm × 3.90 mm  |
| CD74HCT166M   | SOIC (16)              | 9.90 mm × 3.90 mm  |
| CD74HC166E    | PDIP (16)              | 19.31 mm × 6.35 mm |
| CD74HCT166E   | PDIP (16)              | 19.31 mm × 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Functional Diagram**



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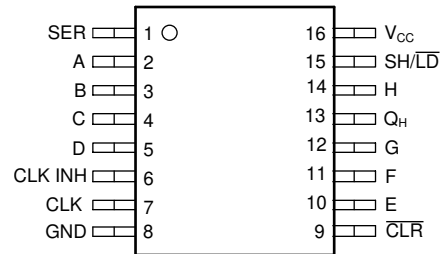
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### 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (October 2003) to Revision D (February 2022)  | Page |
|---|------|
| • Updated the numbering, formatting, tables, figures and cross-references throughout the document to reflect modern data sheet standards..... | 1    |

## 4 Pin Configuration and Functions



**J, N, or D package**  
**16-Pin CDIP, PDIP, or SOIC**  
**Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

|   |  | MIN   | MAX | UNIT      |
|---|--|---|-----|-----------|
| V <sub>CC</sub>   | Supply voltage                               | -0.5  | 7   | V         |
| I <sub>IK</sub>   | Input diode current                          | For V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V |     | ±20<br>mA |
| I <sub>OK</sub>   | Output diode current                         | For V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V |     | ±20<br>mA |
| I <sub>O</sub>  | Drain current, per output                    | For -0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V                   |     | ±25<br>mA |
| I <sub>O</sub>  | Output source or sink current per output pin | For V <sub>O</sub> > -0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V |     | ±25<br>mA |
| Continuous current through V <sub>CC</sub> or GND       |  |   |     | ±50<br>mA |
| T <sub>J</sub>  | Junction temperature                         |   |     | 150<br>°C |
| T <sub>stg</sub>  | Storage temperature range                    | -65   | 150 | °C        |
| Lead temperature (Soldering 10s)(SOIC - lead tips only) |  |   |     | 300<br>°C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Recommended Operating Conditions

|                                 |                          | MIN       | MAX             | UNIT |    |
|---------------------------------|--------------------------|-----------|-----------------|------|----|
| V <sub>CC</sub>                 | Supply voltage range     | HC Types  | 2               | 6    | V  |
|                                 |                          | HCT Types | 4.5             | 5.5  | V  |
| V <sub>I</sub> , V <sub>O</sub> | Input or output voltage  | 0         | V <sub>CC</sub> | V    |    |
| t <sub>t</sub>                  | Input rise and fall time | 2V        | 1000            |      | ns |
|                                 |                          | 4.5V      | 500             |      |    |
|                                 |                          | 6V        | 400             |      |    |
| T <sub>A</sub>                  | Temperature range        | -55       | 125             | °C   |    |

### 5.3 Thermal Information

| THERMAL METRIC   |   | D (SOIC) | N (PDIP) | UNIT |
|------------------|---|----------|----------|------|
|                  |   | 16 PINS  | 16 PINS  |      |
| R <sub>θJA</sub> | Junction-to-ambient thermal resistance <sup>(1)</sup> | 73       | 67       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

| PARAMETER                       |   | TEST CONDITIONS <sup>(2)</sup>                   | V <sub>CC</sub> (V) | 25°C    |     |     | -40°C to 85°C |     | -55°C to 125°C |     | UNIT |
|---------------------------------|---|--|---------------------|---------|-----|-----|---------------|-----|----------------|-----|------|
|                                 |   |  |                     | MIN     | TYP | MAX | MIN           | MAX | MIN            | MAX |      |
| <b>HC TYPES</b>                 |   |  |                     |         |     |     |               |     |                |     |      |
| V <sub>IH</sub>                 | High level input voltage                |  | 2                   | 1.5     |     |     | 1.5           |     | 1.5            |     | V    |
|                                 |   |  | 4.5                 | 3.15    |     |     | 3.15          |     | 3.15           |     | V    |
|                                 |   |  | 6                   | 4.2     |     |     | 4.2           |     | 4.2            |     | V    |
| V <sub>IL</sub>                 | Low level input voltage                 |  | 2                   | 0.5     |     |     | 0.5           |     | 0.5            |     | V    |
|                                 |   |  | 4.5                 | 1.35    |     |     | 1.35          |     | 1.35           |     | V    |
|                                 |   |  | 6                   | 1.8     |     |     | 1.8           |     | 1.8            |     | V    |
| V <sub>OH</sub>                 | High level output voltage               | I <sub>OH</sub> = -20 μA                         | 2                   | 1.9     |     |     | 1.9           |     | 1.9            |     | V    |
|                                 |   | I <sub>OH</sub> = -20 μA                         | 4.5                 | 4.4     |     |     | 4.4           |     | 4.4            |     | V    |
|                                 |   | I <sub>OH</sub> = -20 μA                         | 6                   | 5.9     |     |     | 5.9           |     | 5.9            |     | V    |
|                                 | High level output voltage               | I <sub>OH</sub> = -4 mA                          | 4.5                 | 3.98    |     |     | 3.84          |     | 3.7            |     | V    |
|                                 |   | I <sub>OH</sub> = -5.2 mA                        | 6                   | 5.48    |     |     | 5.34          |     | 5.2            |     | V    |
| V <sub>OL</sub>                 | Low level output voltage                | I <sub>OL</sub> = 20 μA                          | 2                   | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                                 |   | I <sub>OL</sub> = 20 μA                          | 4.5                 | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                                 |   | I <sub>OL</sub> = 20 μA                          | 6                   | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                                 | Low level output voltage                | I <sub>OL</sub> = 4 mA                           | 4.5                 | 0.26    |     |     | 0.33          |     | 0.4            |     | V    |
|                                 |   | I <sub>OL</sub> = 5.2 mA                         | 6                   | 0.26    |     |     | 0.33          |     | 0.4            |     | V    |
| I <sub>I</sub>                  | Input leakage current                   | V <sub>I</sub> = V <sub>CC</sub> or GND          | 6                   | ±0.1    |     |     | ±1            |     | ±1             |     | μA   |
| I <sub>CC</sub>                 | Supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND          | 6                   | 8       |     |     | 80            |     | 160            |     | μA   |
| <b>HCT TYPES</b>                |   |  |                     |         |     |     |               |     |                |     |      |
| V <sub>IH</sub>                 | High level input voltage                |  | 4.5 to 5.5          | 2       |     |     | 2             |     | 2              |     | V    |
| V <sub>IL</sub>                 | Low level input voltage                 |  | 4.5 to 5.5          | 0.8     |     |     | 0.8           |     | 0.8            |     | V    |
| V <sub>OH</sub>                 | High level output voltage               | I <sub>OH</sub> = -20 μA                         | 4.5                 | 4.4     |     |     | 4.4           |     | 4.4            |     | V    |
|                                 | High level output voltage               | I <sub>OH</sub> = -4 mA                          | 4.5                 | 3.98    |     |     | 3.84          |     | 3.7            |     | V    |
| V <sub>OL</sub>                 | Low level output voltage                | I <sub>OL</sub> = 20 μA                          | 4.5                 | 0.1     |     |     | 0.1           |     | 0.1            |     | V    |
|                                 | Low level output voltage                | I <sub>OL</sub> = 4 mA                           | 4.5                 | 0.26    |     |     | 0.33          |     | 0.4            |     | V    |
| I <sub>I</sub>                  | Input leakage current                   | V <sub>I</sub> = V <sub>CC</sub> or GND          | 5.5                 | ±0.1    |     |     | ±1            |     | ±1             |     | μA   |
| I <sub>CC</sub>                 | Supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND          | 5.5                 | 8       |     |     | 80            |     | 160            |     | μA   |
| ΔI <sub>CC</sub> <sup>(1)</sup> | Additional supply current per input pin | DS, D0-D7 inputs held at V <sub>CC</sub> - 2.1 V | 4.5 to 5.5          | 100 72  |     |     | 90            |     | 98             |     | μA   |
|                                 |   | PE input held at V <sub>CC</sub> - 2.1 V         | 4.5 to 5.5          | 100 126 |     |     | 157.5         |     | 171.5          |     |      |
|                                 |   | CP, CE inputs held at V <sub>CC</sub> - 2.1 V    | 4.5 to 5.5          | 100 180 |     |     | 225           |     | 245            |     |      |
|                                 |   | MR inputs held at V <sub>CC</sub> - 2.1 V        | 4.5 to 5.5          | 100 72  |     |     | 90            |     | 98             |     |      |

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(2)  $V_I = V_{IH}$  or  $V_{IL}$ , unless otherwise noted.

## 5.5 Prerequisite for Switching Characteristics

See (Parameter Measurement Information)

| PARAMETER        |   | $V_{CC}$ (V) | 25°C |     | -40°C to 85°C |     | -55°C to 125°C |     | UNIT |
|------------------|---|--------------|------|-----|---------------|-----|----------------|-----|------|
|                  |   |              | MIN  | MAX | MIN           | MAX | MIN            | MAX |      |
| <b>HC TYPES</b>  |   |              |      |     |               |     |                |     |      |
| $f_{MAX}$        | Clock frequency                                       | 2            | 6    |     | 5             |     | 4              |     | MHz  |
|                  |   | 4.5          | 30   |     | 25            |     | 20             |     | MHz  |
|                  |   | 6            | 35   |     | 29            |     | 23             |     | MHz  |
| $t_w$            | $\overline{MR}$ pulse width                           | 2            | 100  |     | 125           |     | 150            |     | ns   |
|                  |   | 4.5          | 20   |     | 25            |     | 30             |     | ns   |
|                  |   | 6            | 17   |     | 21            |     | 26             |     | ns   |
| $t_w$            | Clock pulse width                                     | 2            | 80   |     | 100           |     | 120            |     | ns   |
|                  |   | 4.5          | 16   |     | 20            |     | 24             |     | ns   |
|                  |   | 6            | 14   |     | 17            |     | 20             |     | ns   |
| $t_{SU}$         | Set-up time<br>Data and $\overline{CE}$ to clock      | 2            | 80   |     | 100           |     | 120            |     | ns   |
|                  |   | 4.5          | 16   |     | 20            |     | 24             |     | ns   |
|                  |   | 6            | 14   |     | 17            |     | 20             |     | ns   |
| $t_H$            | Hold time data to clock                               | 2            | 1    |     | 1             |     | 1              |     | ns   |
|                  |   | 4.5          | 1    |     | 1             |     | 1              |     | ns   |
|                  |   | 6            | 1    |     | 1             |     | 1              |     | ns   |
| $t_{REM}$        | Removal time $\overline{MR}$ to clock                 | 2            | 0    |     | 0             |     | 0              |     | ns   |
|                  |   | 4.5          | 0    |     | 0             |     | 0              |     | ns   |
|                  |   | 6            | 0    |     | 0             |     | 0              |     | ns   |
| $t_{SU}$         | Set-up time $\overline{PE}$ to CP                     | 2            | 145  |     | 180           |     | 220            |     | ns   |
|                  |   | 4.5          | 29   |     | 36            |     | 44             |     | ns   |
|                  |   | 6            | 25   |     | 31            |     | 38             |     | ns   |
| $t_H$            | Hold time<br>$\overline{PE}$ to CP or $\overline{CE}$ | 2            | 0    |     | 0             |     | 0              |     | ns   |
|                  |   | 4.5          | 0    |     | 0             |     | 0              |     | ns   |
|                  |   | 6            | 0    |     | 0             |     | 0              |     | ns   |
| <b>HCT TYPES</b> |   |              |      |     |               |     |                |     |      |
| $f_{MAX}$        | Clock frequency                                       | 4.5          | 25   |     | 20            |     | 16             |     | MHz  |
| $t_w$            | $\overline{MR}$ pulse width                           | 4.5          | 35   |     | 44            |     | 53             |     | ns   |
| $t_w$            | Clock pulse width                                     | 4.5          | 20   |     | 25            |     | 30             |     | ns   |
| $t_{SU}$         | Set-up time data and $\overline{CE}$ to clock         | 4.5          | 16   |     | 20            |     | 24             |     | ns   |
| $t_H$            | Hold time data to clock                               | 4.5          | 0    |     | 0             |     | 0              |     | ns   |
| $t_{REM}$        | Removal time $\overline{MR}$ to clock                 | 4.5          | 0    |     | 0             |     | 0              |     | ns   |
| $t_{SU}$         | Set-up time $\overline{PE}$ to CP                     | 4.5          | 30   |     | 38            |     | 45             |     | ns   |
| $t_H$            | Hold time $\overline{PE}$ to CP or $\overline{CE}$    | 4.5          | 0    |     | 0             |     | 0              |     | ns   |

## 5.6 Switching Characteristics

Input  $t_r$ ,  $t_f$  = 6 ns. Unless otherwise specified,  $C_L$  = 50pF. See (Parameter Measurement Information)

| PARAMETER        |  | $V_{CC}$ (V) | 25°C              |     | -40°C to 85°C | -55°C to 125°C | UNIT |
|------------------|--|--------------|-------------------|-----|---------------|----------------|------|
|                  |  |              | TYP               | MAX | MAX           | MAX            |      |
| <b>HC TYPES</b>  |  |              |                   |     |               |                |      |
| $t_{pd}$         | Clock to output  | 2            |                   | 160 | 200           | 240            | ns   |
|                  |  | 4.5          | 13 <sup>(3)</sup> | 32  | 40            | 48             | ns   |
|                  |  | 6            |                   | 27  | 34            | 41             | ns   |
| $t_t$            | Output transition time   | 2            |                   | 75  | 95            | 110            | ns   |
|                  |  | 4.5          |                   | 15  | 19            | 22             | ns   |
|                  |  | 6            |                   | 13  | 16            | 19             | ns   |
| $t_{PHL}$        | Propagation delay MR to output                                 | 2            |                   | 160 | 200           | 240            | ns   |
|                  |  | 4.5          |                   | 32  | 40            | 48             | ns   |
|                  |  | 6            |                   | 27  | 34            | 41             | ns   |
| $C_i$            | Input capacitance  |              |                   | 10  | 10            | 10             | pF   |
| $C_{PD}$         | Power dissipation capacitance <sup>(1)</sup><br><sup>(2)</sup> | 5            | 41                |     |               |                | pF   |
| <b>HCT TYPES</b> |  |              |                   |     |               |                |      |
| $t_{pd}$         | Clock to output  | 4.5          |                   | 40  | 50            | 60             | ns   |
| $t_t$            | Output transition time   | 4.5          |                   | 15  | 19            | 22             | ns   |
| $t_{PHL}$        | Propagation delay<br>MR to output                              | 4.5          |                   | 40  | 50            | 60             | ns   |
| $C_i$            | Input capacitance  |              |                   | 10  | 10            | 10             | pF   |

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per gate.

(2)  $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_o)$  where  $f_i$  = Input Frequency,  $f_o$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

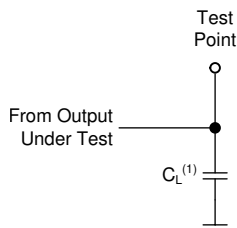
(3)  $C_L = 15$  and  $V_{CC} = 5$  V.

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .

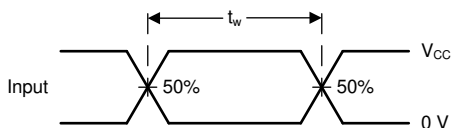
For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

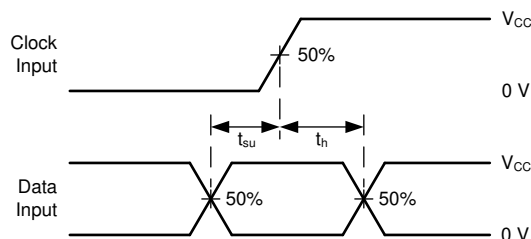


(1)  $C_L$  includes probe and test-fixture capacitance.

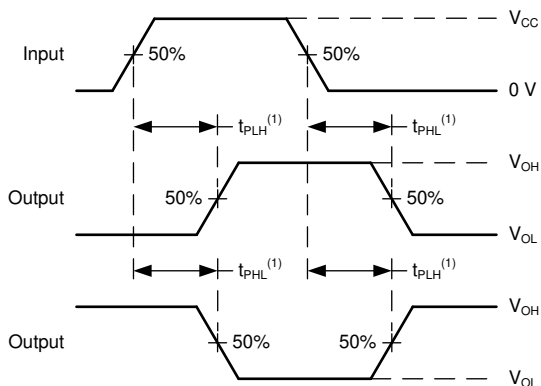
**Figure 6-1. Load Circuit for Push-Pull Outputs**



**Figure 6-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration**

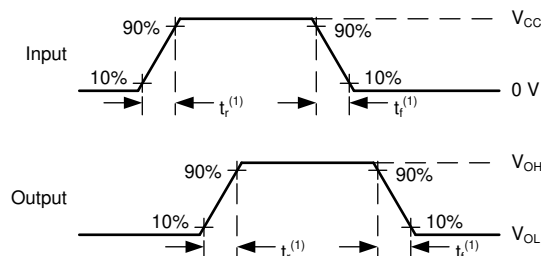


**Figure 6-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**Figure 6-4. Voltage Waveforms, Standard CMOS Inputs Setup Propagation Delays**



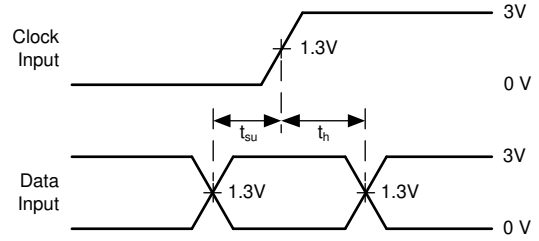
(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

**Figure 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Input Devices**

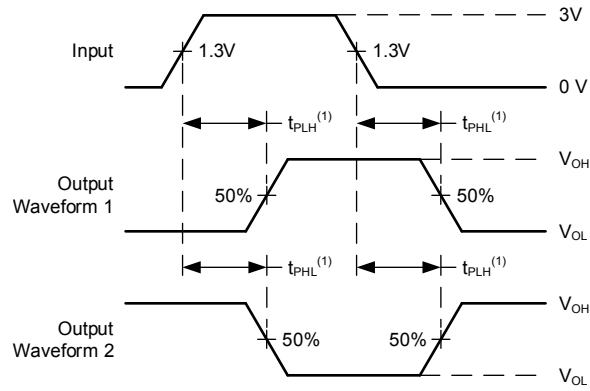




**Figure 6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration**



**Figure 6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**Figure 6-8. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays**

## 7 Detailed Description

### 7.1 Overview

The 'HC166 and 'HCT166 8-bit shift register is fabricated with silicon gate CMOS technology. It possesses the low power consumption of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device.

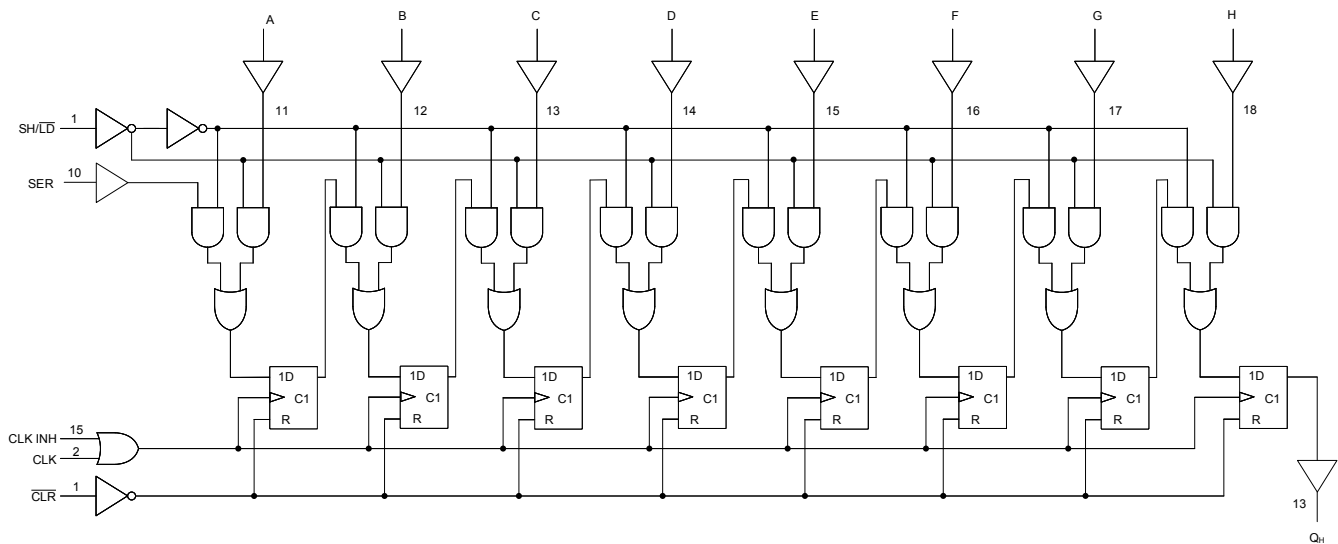
The 'HCT166 is functionally and pin compatible with the standard 'LS166.

The 166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable ( $\overline{PE}$ ) input. When the  $\overline{PE}$  is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When  $\overline{PE}$  is HIGH, data is entered into the internal bit position Q0 from Serial Data Input (DS), and the remaining bits are shifted one place to the right (Q0 → Q1 → Q2, etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q7 output is connected to the DS input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable ( $\overline{CE}$ ) input. The pin assignment for the CP and  $\overline{CE}$  inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of  $\overline{CE}$  input should only take place while the CP is HIGH for predictable operation.

A LOW on the Controller Reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

### 7.2 Functional Block Diagram



### 7.3 Device Functional Modes

**Table 7-1. Truth Table<sup>(1)</sup>**

| INPUTS       |                 |              |       |        |          | INTERNAL Q STATES |     | OUTPUT Q7 |
|--------------|-----------------|--------------|-------|--------|----------|-------------------|-----|-----------|
| MASTER RESET | PARALLEL ENABLE | CLOCK ENABLE | CLOCK | SERIAL | PARALLEL | Q0                | Q1  |           |
|              |                 |              |       |        | D0 D7    |                   |     |           |
| L            | X               | X            | X     | X      | X        | L                 | L   | L         |
| H            | X               | L            | L     | X      | X        | Q00               | Q10 | Q0        |
| H            | L               | L            | ↑     | X      | a...h    | a                 | b   | h         |
| H            | H               | L            | ↑     | H      | X        | H                 | Q0n | Q6n       |
| H            | H               | L            | ↑     | L      | X        | L                 | Q0n | Q6n       |
| H            | X               | H            | ↑     | X      | X        | Q00               | Q10 | Q70       |

- (1) H = High Voltage Level,  
L = Low Voltage Level,  
X = Don't Care,  
↑ = Transition from Low to High Level,  
a...h = The level of steady-state input at inputs D0 thru D7, respectively,  
Q00, Q10, Q70 = The level of Q0, Q1, or Q7, respectively, before the indicated steady-state input conditions were established  
Q0n, Q6n = The level of Q0 or Q6, respectively, before the most recent ↑ transition of the clock.

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)  | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD54HC166F3A     | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | CD54HC166F3A            | <a href="#">Samples</a> |
| CD54HCT166F3A    | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | CD54HCT166F3A           | <a href="#">Samples</a> |
| CD74HC166E       | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD74HC166E              | <a href="#">Samples</a> |
| CD74HC166M96     | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green     | NIPDAU   SN                          | Level-1-260C-UNLIM   | -55 to 125   | HC166M                  | <a href="#">Samples</a> |
| CD74HCT166E      | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD74HCT166E             | <a href="#">Samples</a> |
| CD74HCT166EE4    | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD74HCT166E             | <a href="#">Samples</a> |
| CD74HCT166M96    | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green     | NIPDAU   SN                          | Level-1-260C-UNLIM   | -55 to 125   | HCT166M                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC166, CD54HCT166, CD74HC166, CD74HCT166 :**

- Catalog : [CD74HC166](#), [CD74HCT166](#)
- Military : [CD54HC166](#), [CD54HCT166](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC166M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC166M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.6     | 9.3     | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HCT166M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HCT166M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.6     | 9.3     | 2.1     | 8.0     | 16.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC166M96  | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| CD74HC166M96  | SOIC         | D               | 16   | 2500 | 366.0       | 364.0      | 50.0        |
| CD74HCT166M96 | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| CD74HCT166M96 | SOIC         | D               | 16   | 2500 | 366.0       | 364.0      | 50.0        |

**TUBE**


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC166E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC166E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT166E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT166E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT166EE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT166EE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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