LMC6042 CMOS Dual Micropower Operational Amplifier

Check for Samples: **LMC6042**

FEATURES

- **Low Supply Current: 10 µA/Amp (typ)**
- **Operates from 4.5V to 15V Single Supply**
- **Ultra Low Input Current: 2 fA (typ)**
- **Rail-to-Rail Output Swing**
- **Input Common-Mode Range Includes Ground**

APPLICATIONS

- **Battery Monitoring and Power Conditioning**
- **Photodiode and Infrared Detector Preamplifier**
- **Silicon Based Transducer Systems**
- **Hand-Held Analytic Instruments**
- **pH Probe Buffer Amplifier**
- **Fire and Smoke Detection Systems**
- **Charge Amplifier for Piezoelectric Transducers**

DESCRIPTION

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6042. Providing input currents of only 2 fA typical, the LMC6042 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.
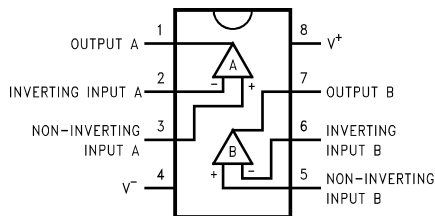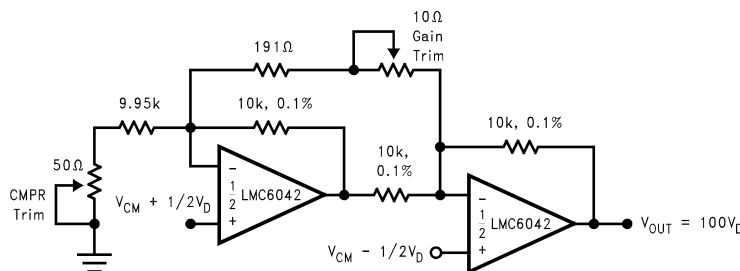
The LMC6042 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6042 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with TI's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6041 for a single, and the LMC6044 for a quad amplifier with these features.

Connection Diagram

Figure 1. 8-Pin PDIP/SOIC

Figure 2. Low-Power Two-Op-Amp Instrumental Amplifier

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Absolute Maximum Ratings [(1)](2)

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	See [(3)]
Output Short Circuit to V^-	See [(4)]
Lead Temperature (Soldering, 10 seconds)	260°C
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	See [(5)]
Storage Temperature Range	−65°C to +150°C
Junction Temperature [(5)]	110°C
ESD Tolerance [(6)]	500V
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.
(4) Applies to both single-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.
(6) Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings

Temperature Range	LMC6042AI, LMC6042I	−40°C ≤ T_J ≤ +85°C
Supply Voltage		4.5V ≤ V^+ ≤ 15.5V
Power Dissipation		See [(1)]
Thermal Resistance (θ_{JA}), [(2)]	8-Pin PDIP	101°C/W
	8-Pin SOIC	165°C/W
	8-Pin CDIP	115°C/W

(1) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.
(2) All numbers apply for packages soldered directly into a PC board.

Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical[(1)]	LMC6042AI Limit[(2)]	LMC6042I Limit[(2)]	Units (Limit)
V_{OS}	Input Offset Voltage		1	3 **3.3**	6 **6.3**	mV Max
TCV_{OS}	Input Offset Voltage Average Drift		1.3			µV/°C
I_B	Input Bias Current		0.002	**4**	**4**	pA (Max)
I_{OS}	Input Offset Current		0.001	**2**	**2**	pA (Max)
R_{IN}	Input Resistance		>10			TeraΩ

(1) Typical values represent the most likely parametric norm.
(2) All limits are specified at room temperature (standard type face) or at operating temperature extremes (bold face type).

Product Folder Links: *LMC6042*

Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typical[1]	LMC6042AI Limit[2]	LMC6042I Limit[2]	Units (Limit)
CMRR	Common Mode	$0V ≤ V_{CM} ≤ 12.0V$		75	68	62	dB
	Rejection Ratio	$V^+ = 15V$			**66**	**60**	Min
+PSRR	Positive Power Supply	$5V ≤ V^+ ≤ 15V$		75	68	62	dB
	Rejection Ratio	$V_O = 2.5V$			**66**	**60**	Min
−PSRR	Negative Power Supply	$0V ≤ V^- ≤ −10V$		94	84	74	dB
	Rejection Ratio	$V_O = 2.5V$			**83**	**73**	Min
CMR	Input Common-Mode	$V^+ = 5V$ and $15V$		−0.4	−0.1	−0.1	V
	Voltage Range	For CMRR ≥ 50 dB			**0**	**0**	Max
				$V^+ - 1.9V$	$V^+ - 2.3V$	$V^+ - 2.3V$	V
					$V^+ - 2.5V$	**$V^+ - 2.4V$**	Min
A_V	Large Signal	$R_L = 100 kΩ$ [3]	Sourcing	1000	400	300	V/mV
	Voltage Gain				**300**	**200**	Min
			Sinking	500	180	90	V/mV
					120	**70**	Min
		$R_L = 25 kΩ$ [3]	Sourcing	1000	200	100	V/mV
					160	**80**	Min
			Sinking	250	100	50	V/mV
					60	**40**	Min
V_O	Output Swing	$V^+ = 5V$		4.987	4.970	4.940	V
		$R_L = 100 kΩ$ to $V^+/2$			**4.950**	**4.910**	Min
				0.004	0.030	0.060	V
					0.050	**0.090**	Max
		$V^+ = 5V$		4.980	4.920	4.870	V
		$R_L = 25 kΩ$ to $V^+/2$			**4.870**	**4.820**	Min
				0.010	0.080	0.130	V
					0.130	**0.180**	Max
		$V^+ = 15V$		14.970	14.920	14.880	V
		$R_L = 100 kΩ$ to $V^+/2$			**14.880**	**14.820**	Min
				0.007	0.030	0.060	V
					0.050	**0.090**	Max
		$V^+ = 15V$		14.950	14.900	14.850	V
		$R_L = 25 kΩ$ to $V^+/2$			**14.850**	**14.800**	Min
				0.022	0.100	0.150	V
					0.150	**0.200**	Max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$		22	16	13	mA
					10	**8**	Min
		Sinking, $V_O = 5V$		21	16	13	mA
					8	**8**	Min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$		40	15	15	mA
					10	**10**	Min
		Sinking, $V_O = 13V$[4]		39	24	21	mA
					8	**8**	Min

(3) $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V ≤ V_O ≤ 11.5V$. For Sinking tests, $2.5V ≤ V_O ≤ 7.5V$.
(4) Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical[1]	LMC6042AI Limit[2]	LMC6042I Limit[2]	Units (Limit)
I_S	Supply Current	Both Amplifiers	20	34	45	µA
		$V_O = 1.5V$		**39**	**50**	Max
		Both Amplifiers	26	44	56	µA
		$V^+ = 15V$		**51**	**65**	Max

AC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ[1]	LMC6042AI Limit[2]	LMC6042I Limit[2]	Units (Limit)
SR	Slew Rate	See [3]	0.02	0.015	0.010	V/µs
				0.010	**0.007**	Min
GBW	Gain-Bandwidth Product		100			kHz
φ_m	Phase Margin		60			Deg
	Amp-to-Amp Isolation	See [4]	115			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	83			nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.0002			pA/$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	f = 1 kHz, $A_V = -5$ $R_L = 100$ kΩ, $V_O = 2$ V_{PP} ±5V Supply	0.01			%

(1) Typical values represent the most likely parametric norm.
(2) All limits are ensured at room temperature (standard type face) or at operating temperature extremes (bold face type).
(3) $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred $V^+ = 15V$ and $R_L = 100$ kΩ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12$ V_{PP}.

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Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified
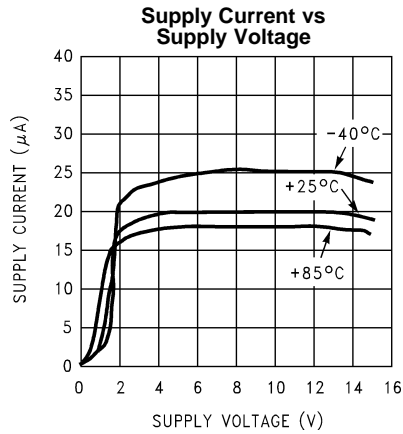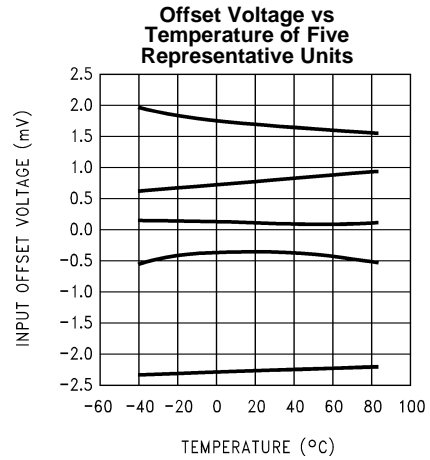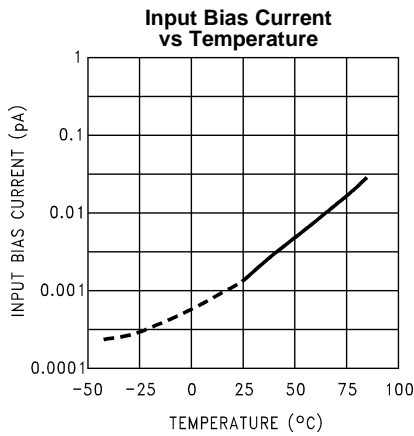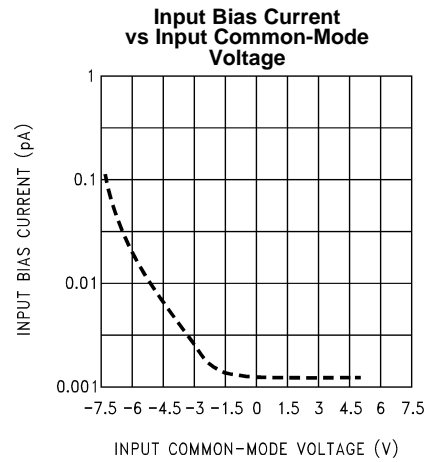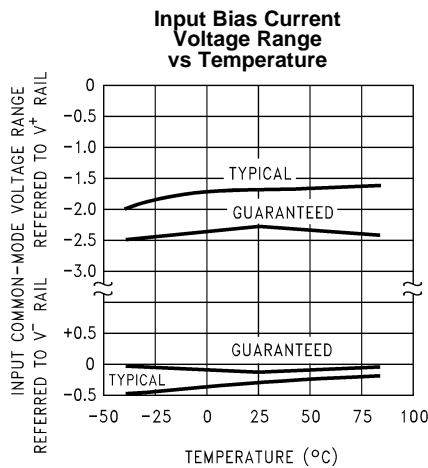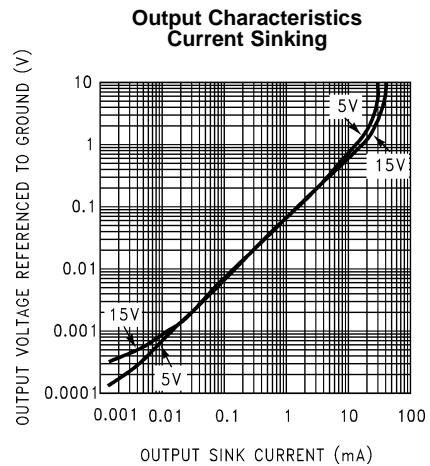
Supply Current vs Supply Voltage

Figure 3.

Offset Voltage vs Temperature of Five Representative Units

Figure 4.

Input Bias Current vs Temperature

Figure 5.

Input Bias Current vs Input Common-Mode Voltage

Figure 6.

Input Bias Current Voltage Range vs Temperature

Figure 7.

Output Characteristics Current Sinking

Figure 8.

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Typical Performance Characteristics (continued)

$V_S = \pm7.5V$, $T_A = 25°C$ unless otherwise specified

**Output Characteristics
Current Sourcing**

Figure 9.

**Input Voltage Noise
vs Frequency**

Figure 10.

**Crosstalk Rejection
vs Frequency**

Figure 11.

**CMRR
vs
Frequency**

Figure 12.

**CMRR
vs
Temperature**

Figure 13.

**Power Supply Rejection
Ratio
vs
Frequency**

Figure 14.

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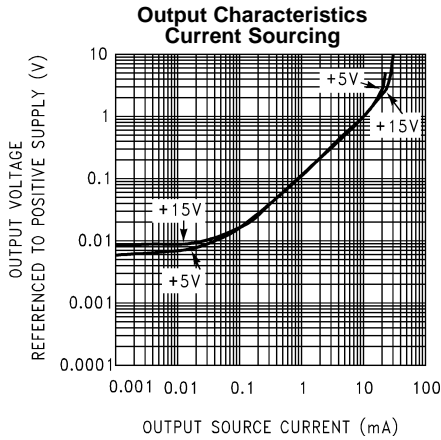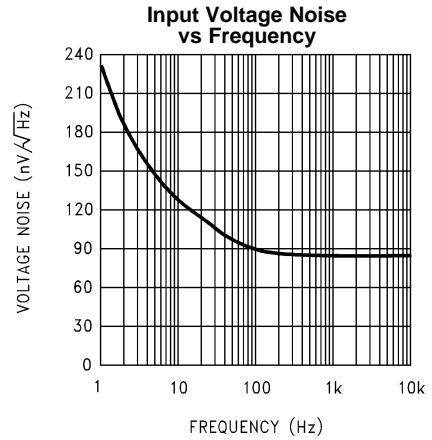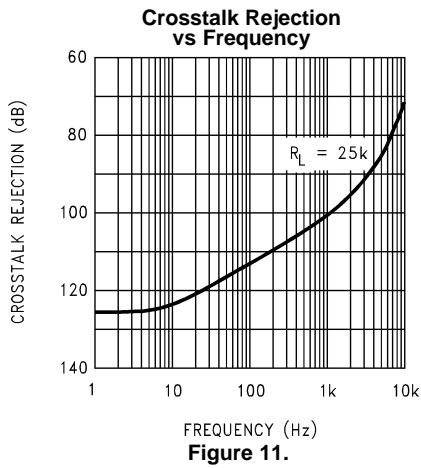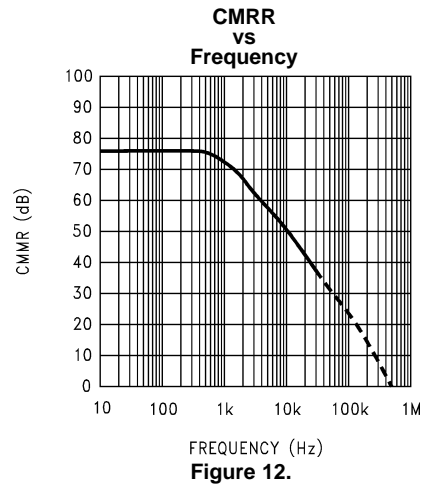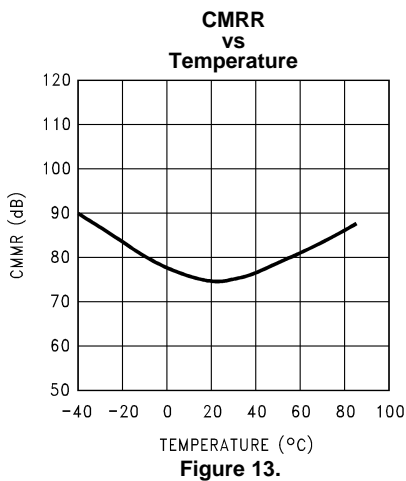
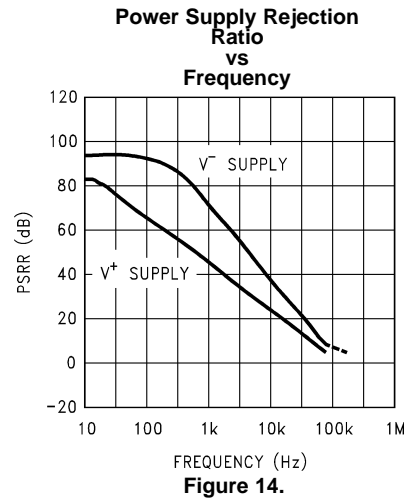## Typical Performance Characteristics (continued)

$V_S = \pm7.5V$, $T_A = 25°C$ unless otherwise specified

Open-Loop Voltage Gain vs Temperature

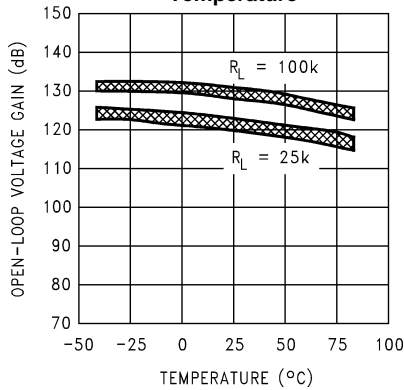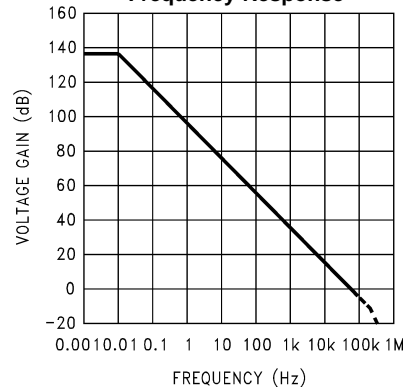

Figure 15.

Open-Loop Frequency Response

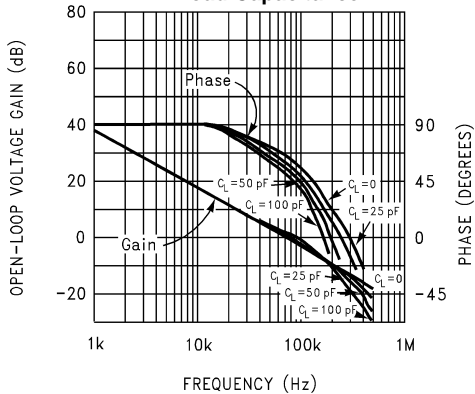**Figure 16.**

Gain and Phase Responses vs Load Capacitance

Figure 17.

Gain and Phase Response vs Temperature
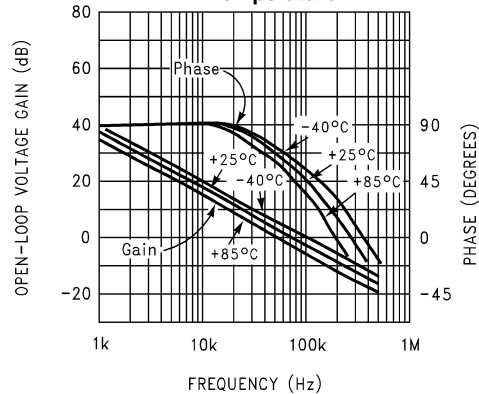

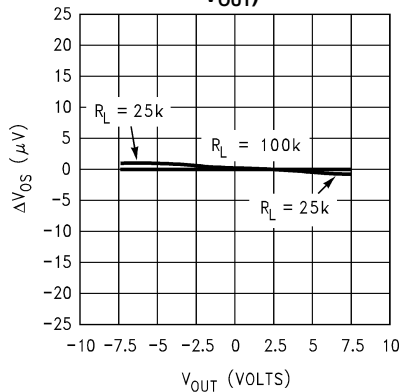**Figure 18.**

Gain Error (V_{OS} vs V_{OUT})

Figure 19.
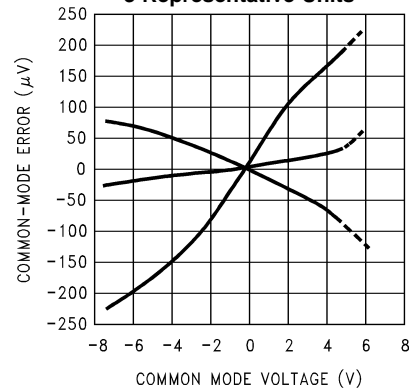
Common-Mode Error vs Common-Mode Voltage of 3 Representative Units

Figure 20.

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Typical Performance Characteristics (continued)

$V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

Non-Inverting Slew Rate vs Temperature

Figure 21.

Inverting Slew Rate vs Temperature

Figure 22.

Non-Inverting Large Signal Pulse Response ($A_V = +1$)

Figure 23.

Non-Inverting Small Signal Pulse Response

Figure 24.

Inverting Large-Signal Pulse Response

Figure 25.

Inverting Small Signal Pulse Response

Figure 26.

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Typical Performance Characteristics (continued)

$V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

**Stability
vs
Capacitive Load**

Figure 27.

**Stability
vs
Capacitive Load**

Figure 28.

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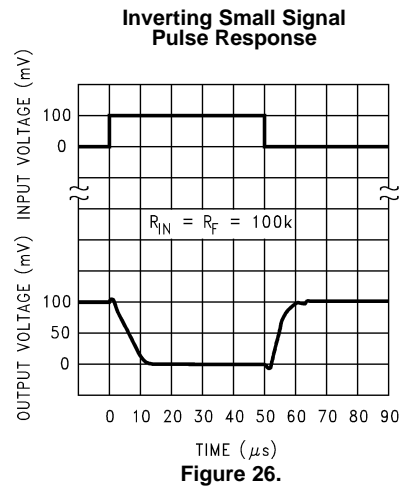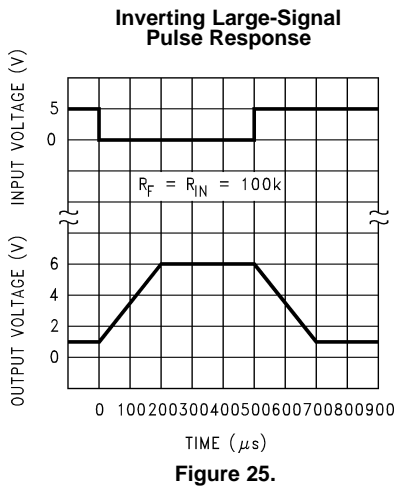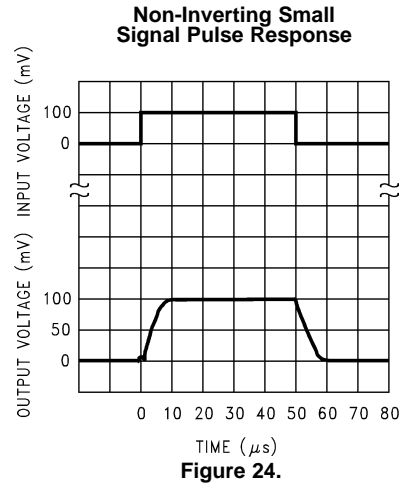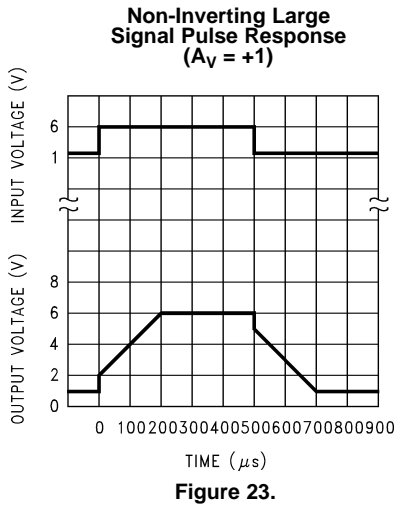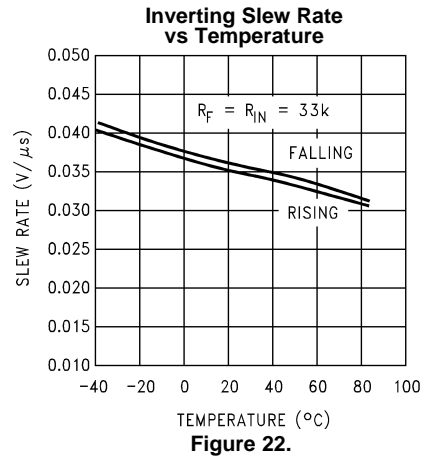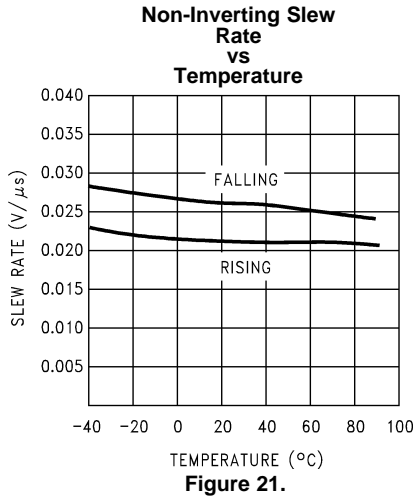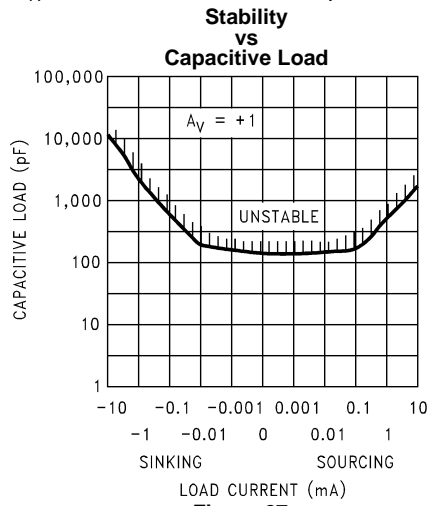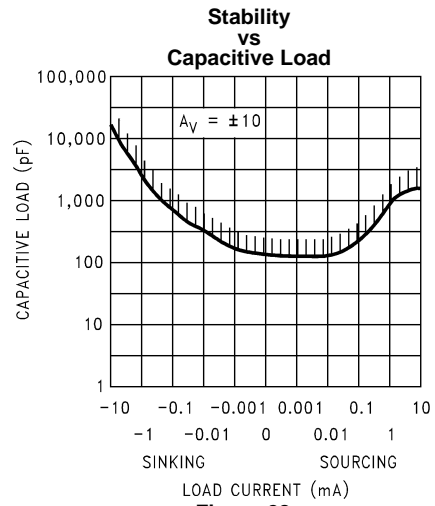
APPLICATIONS HINTS

AMPLIFIER TOPOLOGY

The LMC6042 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6042 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input curent, like the LMC6042.

Although the LMC6042 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6042 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See Printed-Circuit-Board Layout for High Impedance Work).
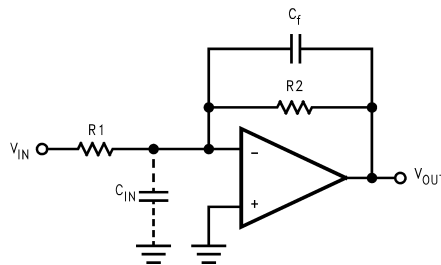
Figure 29. Cancelling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in Figure 29) such that:

$$\frac{1}{2\pi R1\ C_{IN}} \geq \frac{1}{2\pi R2\ C_f}$$

(1)

or

$$R1\ C_{IN} \leq R2\ C_f$$

(2)

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 30.

Product Folder Links: *LMC6042*

Figure 30. LMC6042 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

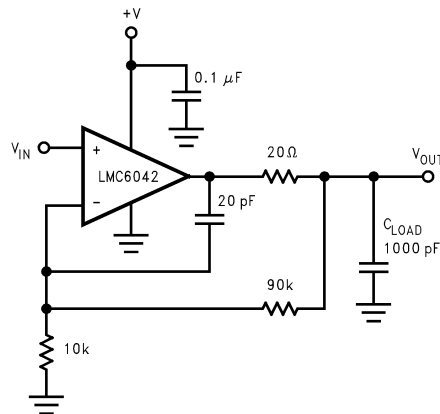In the circuit of Figure 30, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 31). Typically a pull up resistor conducting 10 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).
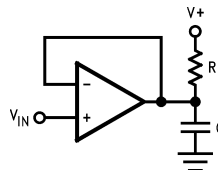

**Figure 31. Compensating for Large
Capacitive Loads with a Pull Up Resistor**

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6042, typically less than 2 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6042's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in Figure 32. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6042's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 36 for typical connections of guard rings for standard op-amp configurations.
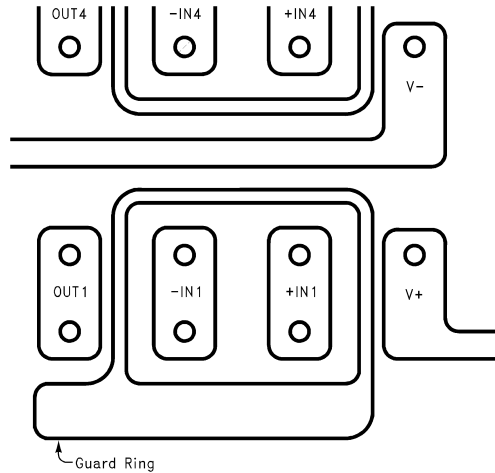
Figure 32. Example of Guard Ring in P.C. Board Layout

Figure 33. Inverting Amplifier
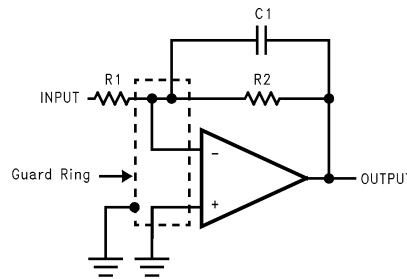
Figure 34. Non-Inverting Amplifier
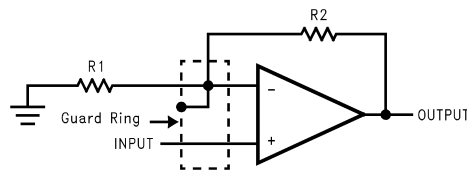
Figure 35. Follower
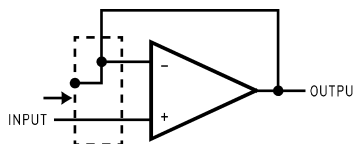
Figure 36. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 37.
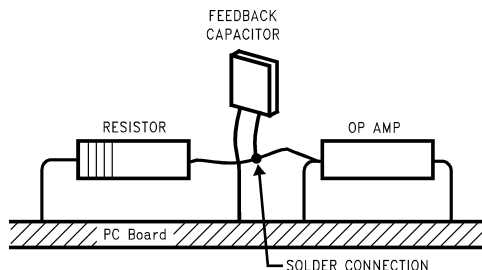
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 37. Air Wiring

Typical Single-Supply Applications

$(V^+ = 5.0\ V_{DC})$

The extremely high input impedance, and low power consumption, of the LMC6042 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

The circuit in Figure 38 is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 20 µA. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to Figure 38, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D.

Rejection of the common-mode component of the input is accomplished by making the ratio of R1/R2 equal to R3/R4. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R0}\right)V_D$$

(3)

A suggested design guideline is to minimize the difference of value between R1 through R4. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If RN = R1 = R2 = R3 = R4 then the gain equation can be simplified:

$$V_{OUT} = 2\left(1 + \frac{RN}{R0}\right)V_D$$

(4)

Due to the "zero-in, zero-out" performance of the LMC6042, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to V_S − 2.3V, worst case at room temperature. This feature of the LMC6042 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 39. Provisions have been made for low sensitivity trimming of CMRR and gain.
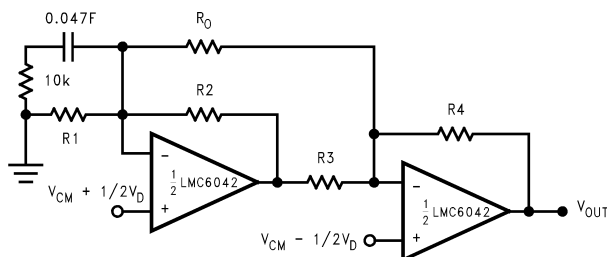

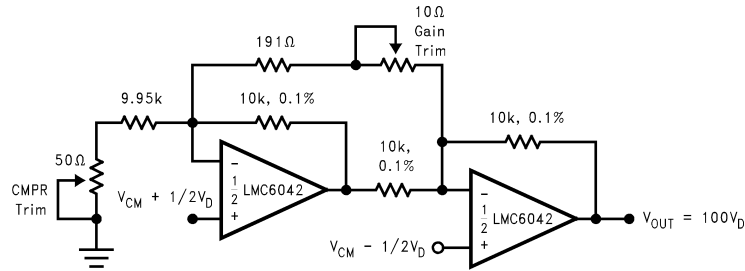**Figure 38. Two Op-Amp Instrumentation Amplifier**

Figure 39. Low-Power Two-Op-Amp Instrumentation Amplifier
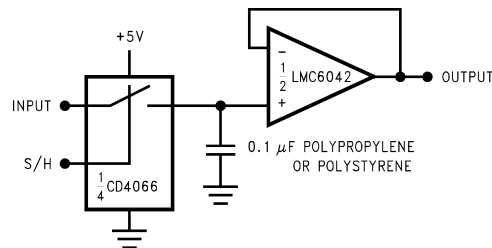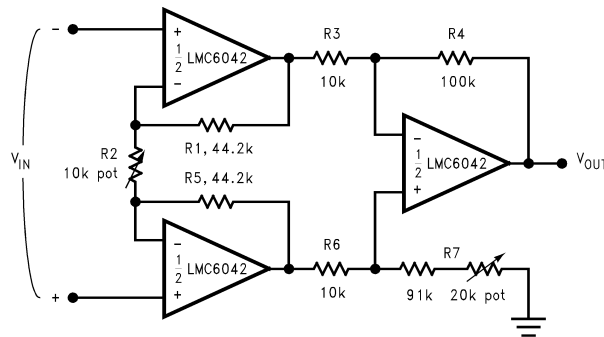

Figure 40. Low-Leakage Sample and Hold
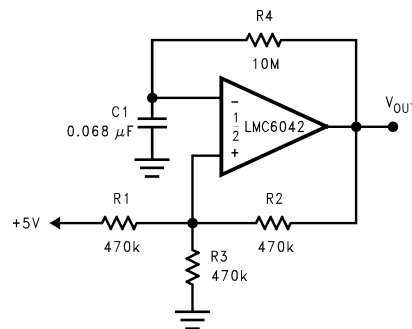

Figure 41. Instrumentation Amplifier

Figure 42. 1 Hz Square Wave Oscillator

Product Folder Links: *LMC6042*
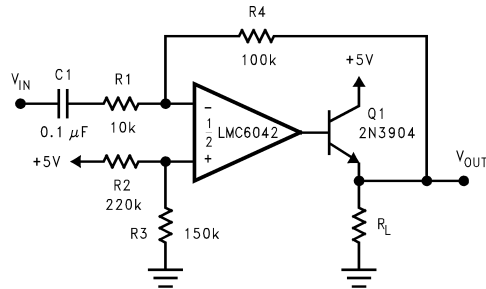
Figure 43. AC Coupled Power Amplifier

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6042AIJ	ACTIVE	CDIP	NAB	8	40	TBD	Call TI	Call TI		LMC6042AIJ	Samples
LMC6042AIM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC60 42AIM	
LMC6042AIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 42AIM	Samples
LMC6042AIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 42AIM	Samples
LMC6042AIN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LMC60 42AIN	Samples
LMC6042IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 42IM	Samples
LMC6042IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 42IM	Samples
LMC6042IN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LMC60 42IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

![Texas Instruments logo]

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6042AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6042IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6042AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6042IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

NAB0008A

.400 MAX
[10.16]

8   5

.310 MAX
[7.87]

R.025
[0.64]

R.010 TYP
[0.25]

1   4

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

8X .055±.010
[1.4±0.25]

.290-.320
[7.37-8.13]

GLASS SEALANT

.200 MAX TYP
[5.08]

.180 MAX
[4.57]

8X .125-.200
[3.18-5.08]

90° ±4°
TYP

.020-.060
[0.51-1.52]
TYP

95° ±5°
TYP

8X .010±.002
[0.25±0.05]

8X .018±.003
[0.46±0.07]

.055 MAX TYP
[1.40]

6X .100±.010
[2.54±0.25]

.310-.410
[7.87-10.41]

J08A (Rev M)

.228-.244   TYP
[5.80-6.19]

A

PIN 1 ID AREA

1

8

6X .050
[1.27]

2X

.150
[3.81]

.189-.197
[4.81-5.00]
NOTE 3

4

5

8X .012-.020
[0.31-0.51]

B

.150-.157
[3.81-3.98]
NOTE 4

⊕ .010 [0.25]Ⓜ C A B

C

SEATING PLANE

⌒ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010   TYP
[0.13-0.25]

.010
[0.25]

0° - 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C   02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

1

8X (.024)
[0.6]

SYMM
℄

SEE
DETAILS

8

SYMM
℄

6X (.050)
[1.27]

4

(R.002) TYP
[0.05]

5

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

.0028 MIN
[0.07]
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

1

8X (.024)
[0.6]

SYMM
℄

SYMM
℄

8

(R.002) TYP
[0.05]

5

6X (.050)
[1.27]

4

(.213)
[5.4]

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R−PDIP−T8)   PLASTIC DUAL−IN−LINE PACKAGE

0.400 (10,16)
―――――――――
0.355 (9,02)

8   5

0.260 (6,60)
―――――――――
0.240 (6,10)

1   4

0.070 (1,78)
―――――――――
0.045 (1,14)

0.045 (1,14)
―――――――――
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
―――――――――
0.015 (0,38)

⊕ | 0.010 (0,25) Ⓜ

0.325 (8,26)
―――――――――
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92)
MAX

4040082/E   04/2010

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001 variation BA.

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