CLOCK DISTRIBUTION CIRCUIT

IDT6T39007A

Description

The IDT6T39007A is a low-power, four output clock distribution circuit. The device takes a TCXO or 1.8 V to 2.5 V LVCMOS input and generates four high-quality LVDS outputs, and two programmable divided outputs.

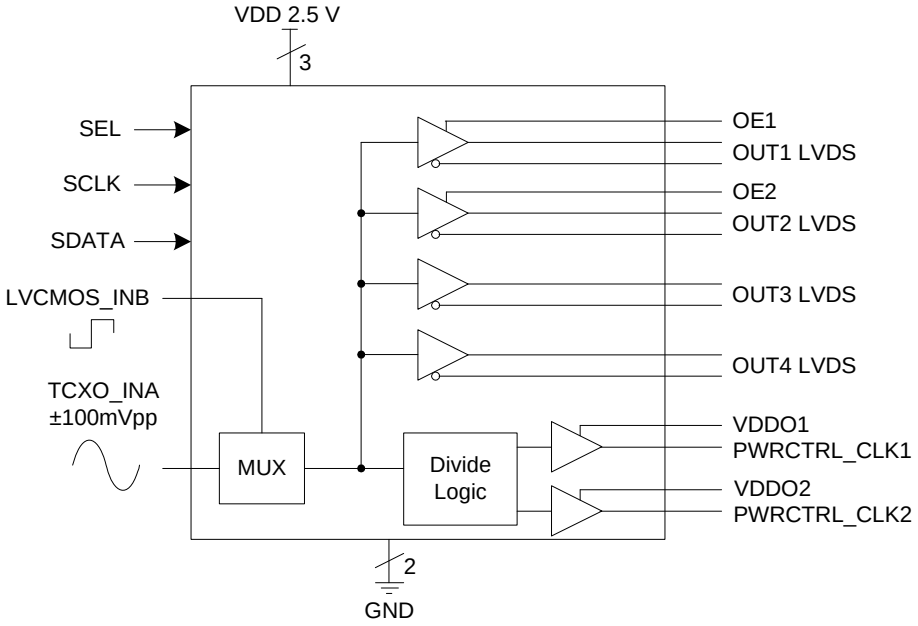
It includes a redundant input with automatic glitch-free switching when the primary reference is removed. The primary input may be selected by the user by pulling the SEL pin low or high. If the primary input is removed and brought back, it will not be re-selected until 1024 cycles have passed.

The IDT6T39007A specifically addresses the needs of handheld applications in both performance and package size. The device is packaged in a small 4mm x 4mm 24-pin QFN, allowing optimal use for limited board space.

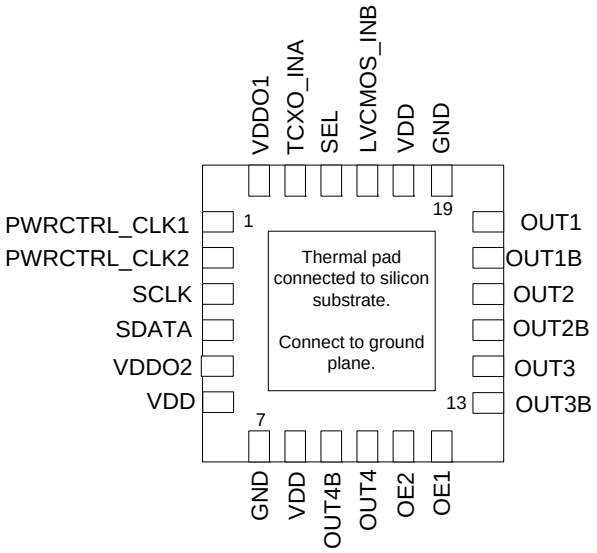
Features

- Packaged in 24-pin QFN
- TCXO sine wave input
- +2.5 V operating voltage
- Four buffered LVDS outputs
- Two programmable outputs for power control up to 3.0 V LVCMOS levels based on VDDO1/VDDO2
- Individual output enables controlled via I^2C or OEx
- Pb-free, RoHS compliant package
- Industrial temperature range (-40°C to +85°C)

Block Diagram



Pin Assignment



24- pin QFN

SEL Pin Configuration Table

SEL	Primary Input
0	LVCMOS_INB
1	TCXO_INA

OE Pin Configuration Table

OEx	OUTx LVDS
0	Disabled
1	Enabled

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	PWRCTRL_CLK1	Output	Programmable power control output 1. See I^2C table.
2	PWRCTRL_CLK2	Output	Programmable power control output 2. See I^2C table.
3	SCLK	Input	I^2C clock input.
4	SDATA	Input	I^2C data input.
5	VDDO2	Power	Connect to +3.0 V.
6	VDD	Power	Connect to +2.5 V.
7	GND	Power	Connect to ground.
8	VDD	Power	Connect to +2.5 V.
9	OUT4B	Output	Buffered LVDS output. Outputs tri-state when disabled.
10	OUT4	Output	Buffered LVDS output. Outputs tri-state when disabled.
11	OE2	Input	Output enable control for OUT2 LVDSpins. Internal pull-up resistor. See table above.
12	OE1	Input	Output enable control for OUT1 LVDSpins. Internal pull-up resistor. See table above.
13	OUT3B	Output	Buffered LVDS output. Outputs tri-state when disabled.
14	OUT3	Output	Buffered LVDS output. Outputs tri-state when disabled.
15	OUT2B	Output	Buffered LVDS output. Outputs tri-state when disabled.

Pin Number	Pin Name	Pin Type	Pin Description
16	OUT2	Output	Buffered LVDS output. Outputs tri-state when disabled.
17	OUT1B	Output	Buffered LVDS output. Outputs tri-state when disabled.
18	OUT1	Output	Buffered LVDS output. Outputs tri-state when disabled.
19	GND	Power	Connect to ground.
20	VDD	Power	Connect to +2.5 V.
21	LVCMOS_INB	Input	Connect to primary LVCMOS input INB. See table above.
22	SEL	Input	Select pin for primary inputs. See table above. Internal pull-up resistor.
23	TCXO_INA	Input	Connect to TCXO input.
24	VDDO1	Power	Connect to +3.0 V.

General I²C Serial Interface

How to Write:

- Controller (host) sends a start bit
- Controller (host) sends the write address $D4_{(H)}$
- IDT clock will *acknowledge*
- Controller (host) sends the beginning byte location =N
- IDT clock will *acknowledge*
- Controller (host) sends the data byte count = X
- IDT clock will *acknowledge*
- Controller (host) starts sending *Byte N through Byte N + X - 1* (see Note 2)
- IDT clock will *acknowledge* each byte *one at a time*
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) sends a start bit
- Controller (host) sends the write address $D4_{(H)}$
- IDT clock will *acknowledge*
- Controller (host) sends the beginning byte location =N
- IDT clock will *acknowledge*
- Controller (host) will send a separate start bit
- Controller (host) sends the read address $D5_{(H)}$
- IDT clock will *acknowledge*
- Controller (host) sends the data byte count = X
- IDT clock sends *Byte N + X - 1*
- IDT clock sends *Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)*
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			IDT (Slave/Receiver)
T	starTbit		
Slave Address $D4_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte = N		.	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			IDT (Slave/Receiver)
T	starTbit		
Slave Address $D4_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D5_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		.	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

I²C Address

The IDT6T39007A is a slave-only device that supports block read and block write protocol using a single 7 bit address and read/write bit. A block write ($D4_{(H)}$) or block read ($D5_{(H)}$) is made up of seven (7) bits and one (1) read/write bit.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	1	0	X

In applications where the indexed block write and block read are used, the dummy byte (bit 11-18) functions as a register-offset (8 bits) pointer.

Byte 0: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Reserved	R	Undefined	Not applicable	
6	Reserved	R	Undefined	Not applicable	
5	OE for OUT3	RW	1	LVDS clock output	1=enabled 0=disabled
4	OE for OUT4	RW	1	LVDS clock output	1=enabled 0=disabled
3	Reserved	R	Undefined	Not applicable	
2	Reserved	R	Undefined	Not applicable	
1	Reserved	R	Undefined	Not applicable	
0	Reserved	R	Undefined	Not applicable	

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	PWRCTRL_CLK1 Divider SEL bit 7	RW	0	PWRCTRL_CLK1	Default is /15 to get 866.666 kHz from 13 MHz
6	PWRCTRL_CLK1 Divider SEL bit 6	RW	0	PWRCTRL_CLK1	Default is /15 to get 866.666 kHz from 13 MHz
5	PWRCTRL_CLK1 Divider SEL bit 5	RW	0	PWRCTRL_CLK1	Default is /15 to get 866.666 kHz from 13 MHz
4	PWRCTRL_CLK1 Divider SEL bit 4	RW	0	PWRCTRL_CLK1	Default is /15 to get 866.666 kHz from 13 MHz
3	PWRCTRL_CLK1 Divider SEL bit 3	RW	1	PWRCTRL_CLK1	Default is /15 to get 866.666 kHz from 13 MHz
2	PWRCTRL_CLK1 Divider SEL bit 2	RW	1	PWRCTRL_CLK1	Default is /15 to get 866.666 kHz from 13 MHz
1	PWRCTRL_CLK1 Divider SEL bit 1	RW	1	PWRCTRL_CLK1	Default is /15 to get 866.666 kHz from 13 MHz
0	PWRCTRL_CLK1 Divider SEL bit 0	RW	1	PWRCTRL_CLK1	Default is /15 to get 866.666 kHz from 13 MHz

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	PWRCTRL_CLK2 Divider SEL bit 7	RW	0	PWRCTRL_CLK2	Default is /46 to get 282.6kHz from 13 MHz
6	PWRCTRL_CLK2 Divider SEL bit 6	RW	0	PWRCTRL_CLK2	Default is /46 to get 282.6kHz from 13 MHz
5	PWRCTRL_CLK2 Divider SEL bit 5	RW	1	PWRCTRL_CLK2	Default is /46 to get 282.6kHz from 13 MHz
4	PWRCTRL_CLK2 Divider SEL bit 4	RW	0	PWRCTRL_CLK1	Default is /46 to get 282.6kHz from 13 MHz
3	PWRCTRL_CLK2 Divider SEL bit 3	RW	1	PWRCTRL_CLK1	Default is /46 to get 282.6kHz from 13 MHz

2	PWRCTRL_CLK2 Divider SEL bit 2	RW	1	PWRCTRL_CLK1	Default is /46 to get 282.6kHz from 13 MHz
1	PWRCTRL_CLK2 Divider SEL bit 1	RW	1	PWRCTRL_CLK1	Default is /46 to get 282.6kHz from 13 MHz
0	PWRCTRL_CLK2 Divider SEL bit 0	RW	0	PWRCTRL_CLK1	Default is /46 to get 282.6kHz from 13 MHz

Byte 3: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not applicable	

Byte 4 through 5: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not applicable	

Byte 6: Control Register

Bit	Description	Type	Power Up	Output(s) Affected	Notes
7	Revision ID bit 3	R	0	Not applicable	
6	Revision ID bit 2	R	0	Not applicable	
5	Revision ID bit 1	R	0	Not applicable	
4	Revision ID bit 0	R	0	Not applicable	
3	Vendor ID bit 3	R	0	Not applicable	
2	Vendor ID bit 2	R	0	Not applicable	
1	Vendor ID bit 1	R	0	Not applicable	
0	Vendor ID bit 0	R	1	Not applicable	

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 μF should be connected between VDD and GND as close to the device as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into IDT pin.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.

2. No vias should be used between decoupling capacitor and VDD pin.

3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the IDT6T39007A.This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT6T39007A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Max Supply Voltage, VDD	5 V
LVCMOS_INB, SCLK and SDATA Inputs	-0.5 V to +3.3 V
All Other Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Peak Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+2.25	+2.5	+2.75	V
Output Supply Voltage (VDDO1, VDDO2)	VDD	+3.0	+3.15	V

DC Electrical Characteristics

Unless otherwise specified, **VDD =2.5 V ±10%**, **VDDO1 = VDDO2 = 3.0 V ±5%**, Ambient Temp. -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Voltage	VDD		+2.25	+2.5	+2.75	V
Output Supply Voltage	VDDO	VDDO1, VDDO2	VDD	3.0	3.15	V
Input High Voltage	V_{IH}	SEL, OEx, LVCMOS_INB	0.75xVDD			V
		SCLK and SDATA	0.7xVDD			
Input Low Voltage	V_{IL}	SEL, OEx, LVCMOS_INB			0.35xVDD	V
		SCLK and SDATA			0.3xVDD	
High-Level Output Voltage	V_{OH}	I_{OH} = -4 mA	1.7			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4 mA			0.7	V
Operating Supply Current	IDD	No load, all outputs switching at 13 MHz		15	18	mA
		All outputs disabled		TBD		mA
Short Circuit Current	I_{OS}	Single-ended clocks		±70		mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Impedance	Z_O	All clock outputs, OEx=1		15		Ω
Internal Pull-Up Resistance	R_{pu}	SEL, OEx		500		kΩ
Input Capacitance	C_{IN}	All input pins		6		pF

AC Electrical Characteristics - Single-Ended Outputs

Unless otherwise stated, **VDD =2.5 V ±10%**, **VDDO1 = VDDO2 = 3.0 V ±5%**, Ambient Temp. -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}		12.6	13	13.4	MHz
Variance Input Frequencies		LVCMOS_INB, TCXO_INA, Note 2			0.4	MHz
Time Switch Clock Inputs		LVCMOS_INB, TCXO_INA, Note 3		80		µs
TCXO Input Swing		TCXO_INA	±100		±900	mV
Output Frequency Error				0		ppm
Output Rise Time	t_{OR}	20% to 80%, Note 1		1	1.5	ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		1	1.5	ns
Output Clock Duty Cycle		Measured at VDDO/2, Note 1	45	50	55	%
Output Enable time		OE goes high, output within 1% of final frequency			1	ms
Clock Stabilization Time from Power Up		Power up, output within 1% of final frequency		3	10	ms

Note 1: CL = 8 pF.

Note 2: Delta from 13 MHz.

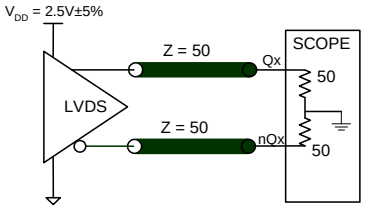
Note 3: By removing primary input and then bringing back primary input.

AC Electrical Characteristics - LVDS Outputs

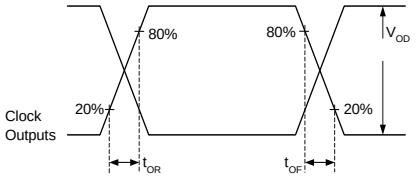
Unless otherwise stated, **VDD = 2.5 V ±10%**, Ambient Temperature -40 to +85° C

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential Output Voltages | V_{OD} |	R_L = 100Ω	250	350	450	mV
Δ V_{OD}	V_{OD} Magnitude Change	-40	0	40	mV
Offset Voltage (V_{OS})		1.125	1.25	1.375	V
Output CLock Duty Cycle	Measured at V_{OS}	45	50	55	%
Δ V_{OS}	V_{OS} Magnitude Change		3	25	mV
Output Short Circuit Current (I_{OS})			-10		mA
Output Rise Time	20% to 80%, R_L = 100Ω		0.5	1.0	ns
Output Fall Time	20% to 80%, R_L = 100Ω		0.5	1.0	ns

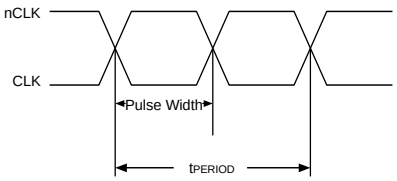
Parameter Measurement Information



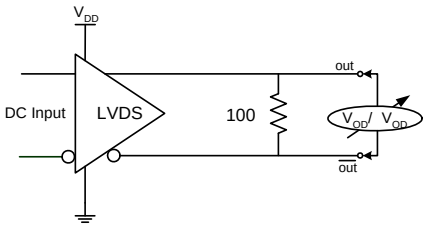
2.5V OUTPUT LOAD AC TEST CIRCUIT



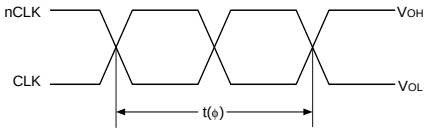
OUTPUT RISE/FALL TIME



t_{PW} & t_{PERIOD}

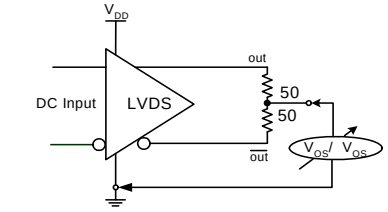


V_{OD} SETUP

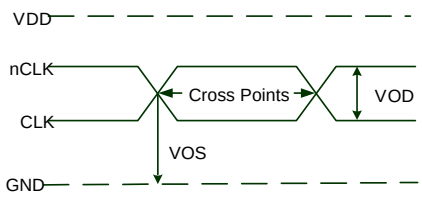


$t_{jit(\phi)} = |t_{(\phi)} - t_{(\phi)mean}|$ = Phase Jitter

PHASE JITTER



V_{OS} SETUP



DIFFERENTIAL INPUT LEVEL

Marking Diagram

Notes:

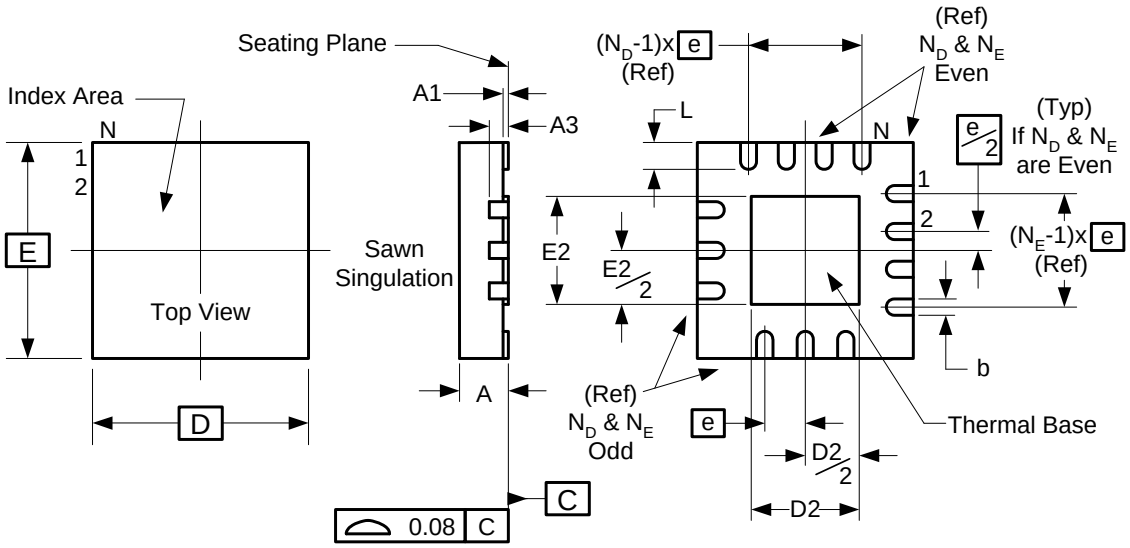
1. YYWW is the last two digits of the year and week that the part was assembled.
2. “$” is the assembly mark code.
3. “G” after the two-letter package code designates RoHS compliant package.
4. “I” at the end of part number indicates industrial temperature range.
5. Bottom marking: country of origin if not USA.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		29.1		°C/W
	θ_{JA}	1 m/s air flow		22.8		°C/W
	θ_{JA}	2.5 m/s air flow		21.0		°C/W
Thermal Resistance Junction to Case	θ_{JC}			41.8		°C/W

Package Outline and Package Dimensions (24-pin QFN)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N	24	
N_D	6	
N_E	6	
D x E BASIC	4.00 x 4.00	
D2	2.3	2.55
E2	2.3	2.55
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
6T39007ANLGI	see page 13	Tray	24-pin QFN	-40 to +85° C
6T39007ANLGI8		Tape and Reel	24-pin QFN	-40 to +85° C

"G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
H	RDW	02/22/12	1. Added device top-side marking.

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