

DEM-ADS7864
ADC Evaluation Board

User's Guide

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Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the DEM-ADS7864 parallel analog to digital converter evaluation board. A complete circuit description as well as schematic diagram and bill of materials are included.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Evaluation Board Overview
- Chapter 2—Analog and Digital Interface
- Chapter 3—Power Supply Requirements
- Chapter 4—Initial Board Setup and Operation
- Appendix A—Board Layer Artwork and Schematic for the DEM-ADS7864

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This is an example of a caution statement.
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The information in a caution is provided for your protection. Please read each caution carefully.

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Data Sheets	Literature Number:
ADS7864	SBAS141
OPA340	SBOS073
OPA343	SBOS090A
OPA350	SBOS099
OPA353	SBOS103
OPA132	SBOS054

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Evaluation Board Overview

This chapter gives a brief description of the operation and features of the DEM-ADS7864 ADC evaluation board.

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1.1 Introduction

The ADS7864 is a high speed, low power, dual 12-bit A/D converter that operates from a single 5-V supply. The input channels are fully differential with a typical common-mode rejection of 80 dB. The part contains dual 2- μ s successive approximation ADCs, six differential sample-and-hold amplifiers, an internal 2.5-V reference with REF_{IN} and REF_{OUT} pins and a high-speed parallel interface.

There are six analog inputs that are grouped into three channels (A, B and C). Each A/D converter has three inputs (A0, B0, C0 or A1, B1, C1) that can be sampled and converted simultaneously. This preserves the relative phase information of the signals on the analog inputs. Each pair of channels has a hold signal (HOLDA, HOLDB, and HOLDC) that when strobed together, allows simultaneous sampling on all 6 channels. The part accepts an analog input voltage in the range of $-V_{REF}$ to $+V_{REF}$, centered on the internal 2.5-V reference. The part will also accept bipolar input ranges when a level shift circuit is used in the analog front-end circuitry (see Figure 1-1).

Conversion time for the ADS7864 is 1.75 μ s when an 8-MHz external clock is used. The corresponding acquisition time is 0.25 μ s. To achieve maximum output rate (500 kHz), the read function can be performed during the start of the next conversion.

The evaluation board provides analog input flexibility, permitting evaluation of the user's own application. The digital interface of the DEM-ADS7864 provides direct connection to the computer interface board (CIB), allowing the user to evaluate device performance with the BBEval™ software.

In the factory default configuration, a 5-V analog and 5-V digital supply are required for proper operation of the DEM-ADS7864 board. The analog buffer amplifiers are socketed, allowing the user to easily change input configurations. The input power circuit can be modified to allow up to ± 15 -V analog supply operation.

1.2 Features

- Full-featured evaluation board for the ADS7864 500 kHz, 12-Bit, 6-channel simultaneous sampling analog to digital converter
- Operates with a single 5-V power supply—can be configured for ± 15 V operation
- Accepts wide range of operational amplifiers in different configurations
- Direct interface to CIB board
- High-speed parallel interface to the PC

Analog and Digital Interface

This chapter describes the analog and digital interface circuits of the ADS7864.

Operating the DEM-ADS7864 with the CIB controller is preferred. The evaluation board may be connected to the user's own control board using proper interconnect cabling. The series resistors on the digital I/O lines will reduce noise injected by long cables or improper layout of the control board.

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2.1 Analog Interface

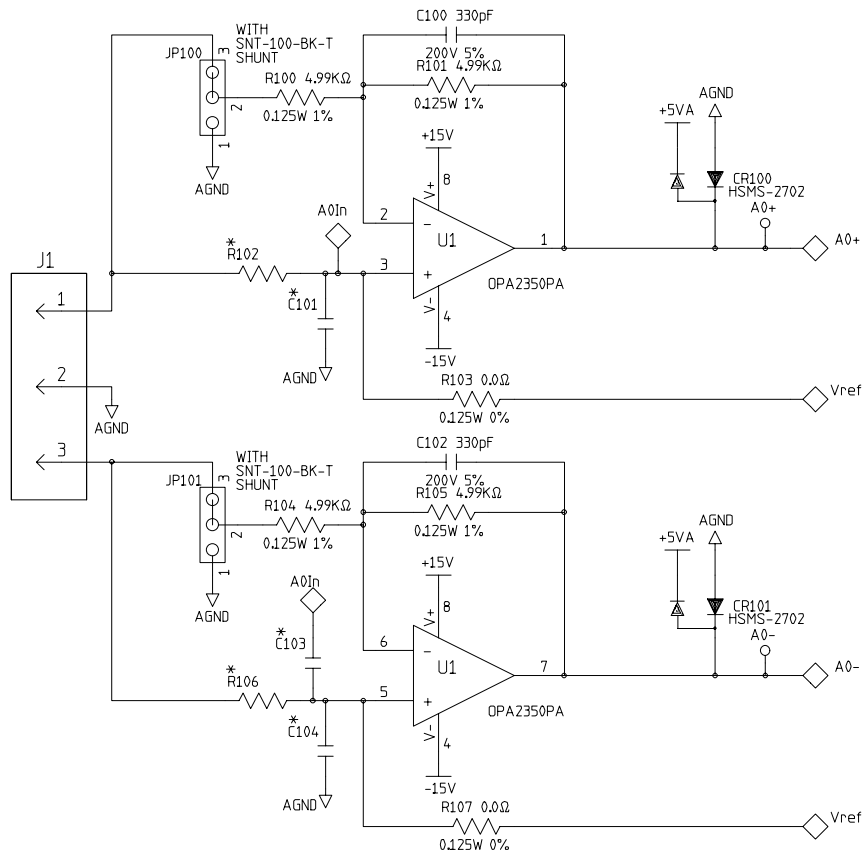
The analog circuit of the board is divided in two parts. The input buffer represents the front-end circuit of the A/D converter. Its function is to provide level and impedance adaptation of the input signal. The second part is a voltage reference circuit. In addition to being the conversion reference, the ADS7864 reference output is used for level shifting the analog input.

2.1.1 Single Supply—Input Buffer

The analog input to the DEM-ADS7864 board is comprised of six independent OPA2350 operational amplifiers. The OPA2350 devices are powered from the 5-V analog supply, and arranged as inverting amplifiers with a gain of 1. The internal 2.5-V reference voltage is applied to the noninverting input of the OPA2350 devices. Figure 2–1 shows the analog input circuit of channel A0.

This configuration allows single ended signals of ± 2.5 V (5 Vpp) to be applied to either input of channels A, B or C (JX pin 1 or 3 referenced to pin 2). Differential signal inputs of ± 1.25 V (2.5 Vpp) can be applied to the channel input pairs (JX pins 1 and 3).

Figure 2–1. DEM–ADS7864 Schematic—Analog Input Section



Note: Figure 1 depicts the actual board layout. The factory configuration of the DEM-ADS7864 evaluation board does not use ± 15 V. See section 2.1.3 for ± 15 V operation. Components marked with an asterisk (*) are not installed.

2.1.2 Bipolar Inputs

Table 1–1 lists various combinations of resistors, capacitors and jumpers (refer to Figure 1–1). By changing components and setting the appropriate jumper, it is possible to adapt the input buffer to accept bipolar input voltages. Table 1–1 is related to the schematic presented in Figure 1–1 and represents channel A0 of the ADC. Channels B0, C0, A1, B1 and C1 follow a similar pattern, with only the most significant digit of the reference designator changing.

The capacitors C103 through C603 are used only in differential signal configurations. For single-ended signals, the second operational amplifier can be used to buffer the reference voltage to the input of A/D converter.

Table 2–1. Combinations of Resistors, Capacitors and Jumpers

Input Voltage	R102 R106	R100 R104	R103 R107	R101 R105	C101 C104	C100 C102	JP100 JP101
0 – 5	5 k Ω	open	open	short	330 pF	open	open
0 – 2.5	5 k Ω	5 k Ω	open	5 k Ω	open	330 pF	1–2
(–2.5) – 2.5	20 k Ω	4 k Ω	20 k Ω	4 k Ω	open	330 pF	1–2
(–5) – 5	20 k Ω	4 k Ω	10 k Ω	2 k Ω	open	330 pF	1–2
(–10) – 10	20 k Ω	4 k Ω	5 k Ω	1 k Ω	open	330 pF	1–2
(–5) – 0	open	5 k Ω	open	5 k Ω	short	330 pF	2–3
0 – 5	open	5 k Ω	open	5 k Ω	short	330 pF	2–3

2.1.3 Dual Supply—Input Buffer

The DEM-ADS7864 board is configured at the factory for 5-V analog operation. It is possible however, for the user to modify the input power circuit to allow up to ± 15 -V analog supplies. Care must be taken to ensure a proper input buffer op-amp is used.

Caution

The OPA2350 is a single supply device; it *must* be removed prior to changing the input voltage.

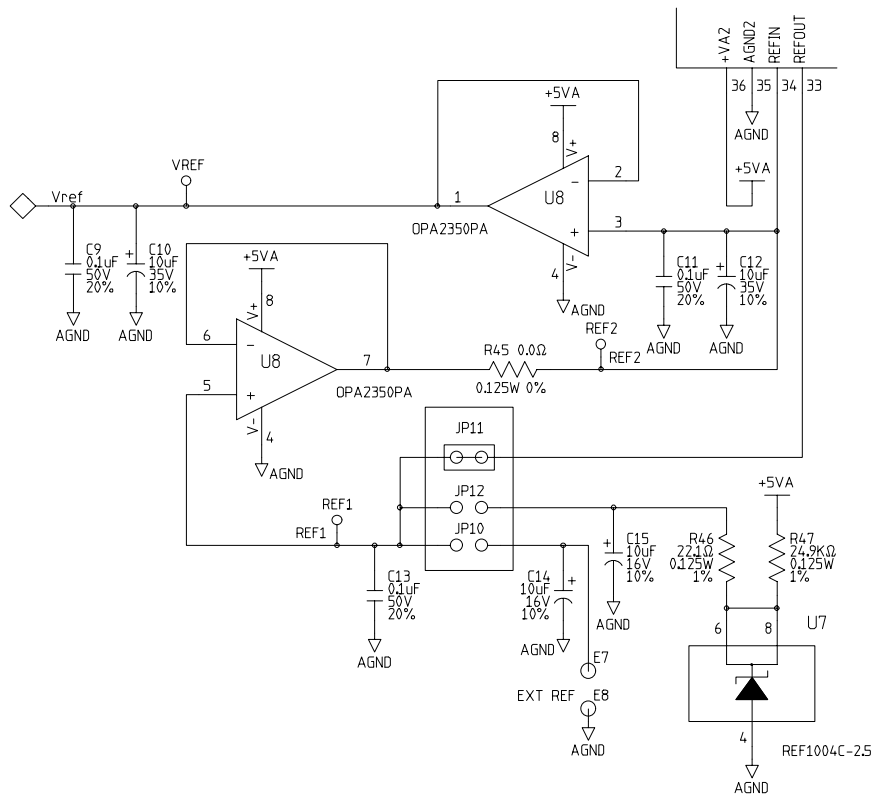
Modifying the evaluation board for dual analog supplies requires the user to cut the wire links at JP7 and JP8. These are located near the input power connector (J7). The user must also install a 5-V linear regulator (Texas Instruments part number μ A7805CKC) at U15. This voltage is required by the ADC as well as the internal reference circuit U7.

2.1.4 Reference Voltage

The ADS7864 has an internal 2.5-V reference source, accessed by closing JP11. If an external reference source is desired, the DEM-ADS7864 provides the user two options. Closing JP12 provides an onboard reference source, via U7 (REF1004C–2.5). If a different voltage is required, the jumper at JP10 will connect the buffers to an off-board source applied at E7, referenced to E8.

The resistor R45 on the output of the buffer will provide a low pass filter for further noise reduction. If maximum speed is required, the 0-Ω resistor can be left in as a short circuit.

Figure 2–2. DEM-ADS7864 Reference Circuit



2.2 Digital Interface

The biggest problem in mixed signal circuits is the noise injected from the digital devices to the analog. To reduce noise injection, the digital I/O to the DEM-ADS7864 is buffered. Placing the buffers near the ADS7864 and keeping the lines as short as possible minimizes the digital noise.

2.2.1 Control Signals

The $\overline{\text{RESET}}$ and chip select ($\overline{\text{CS}}$) signals are connected through U12, an SN74HC244. In this way, the system reset will take immediate action on the ADS7864. The gating signal of the latch is permanently connected to ground. The $\overline{\text{CS}}$ and $\overline{\text{BYTE}}$ inputs have pull-up resistors, to prevent the ADS7864 from operating without control signals.

2.2.2 Bus Width

The DEM-ADS7864 board defaults the ADC output data to 8-bit mode. The lower 8-bits [DB7 – DB0] are accessed via U12 on the first $\overline{\text{RD}}$ signal, while the upper 8-bits are accessed on the second $\overline{\text{RD}}$ signal. U12 is defaulted to the active state through pull-down resistor R20.

Full 16-bit access requires the user to pull both the gate of 8-bit buffer U10 and the $\overline{\text{BYTE}}$ signal low. The gate control for U10 is provided through hex inverter U14, defaulting the buffer to its high-impedance state through pulldown resistor R10. This requires the user to assert a logic high on P1 pin 20, and logic low on P1 pin 7.

The CIB board connects to the user's host computer through a 25-pin connector on the parallel port. Communication with the CIB board is through an 8-bit bus.

2.2.3 External Clock and Trigger

Operating at 56MHz, the CIB board provides a clock frequency of 7 MHz to the DEM-ADS7864 board. To test the device at some other frequency, provision is made to supply an external clock. *NOTE – The maximum frequency of the ADS7864 is 8MHz.* The external clock is applied to inverting Schmitt trigger 74HC14 through P2. The clock is then routed into the DEM-CIB, which uses a multiplexer to send the signal back to the DEM-ADS7864. A state machine on the CIB controls $\overline{\text{CS}}$, $\overline{\text{HOLDx}}$, $\overline{\text{RD}}$, A0, A1 and A2 based on either the internal or external clock source. The user must configure the BBEval software to facilitate the use of the external clock. Review the software documentation for details on using an external clock source.

If the evaluation requires a specific instant to be captured, an external trigger input applied to the BNC connector at location P3 can start the A/D converter capturing an event. This feature is also controlled by the BBEval software. Please review the software documentation for details of the external trigger operation.



Power Supply

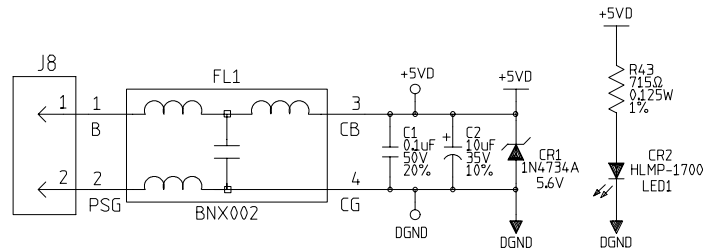
This chapter describes the digital and analog power supply requirements of the DEM-ADS7864 evaluation board. While the digital supply is always maintained at a 5-V level, the analog supply can be either 5 V (default settings) or up to ± 15 V.

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3.1 Digital Supply

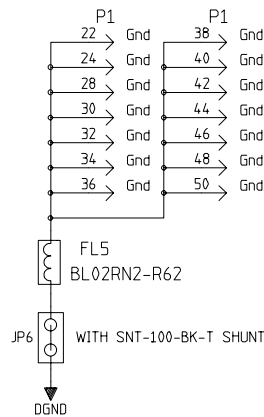
The evaluation board digital 5-V power supply can be the same power supply for the CIB or user's control board. To prevent ground loops of the digital power supply, a BNX filter (FL1) is placed on the digital power input (see Figure 3-1). The zener diode (CR1) protects against over-voltage as well as reverse voltage on the digital input.

Figure 3–1. Digital Power Input



If the user furnishes different power supplies for the CIB board and for the digital portion of the evaluation board, the high frequency inductor at FL5 will help to reduce ground noise (see Figure 3-2).

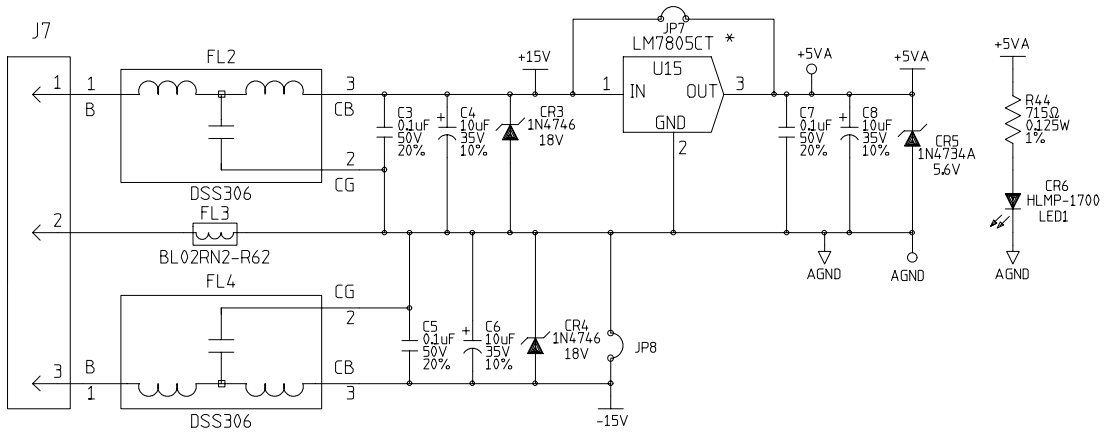
Figure 3–2. Secondary Digital Filter



3.2 Analog Supply

The analog power supply is more critical than the digital. The input DSS306 filters are placed on both analog power input supply lines. The zener diodes on the input lines protect against overvoltage or reverse voltage. Another inductor is placed on the input line to the analog ground. If the same power supply is used for the digital and analog circuits, the BL02 inductor (FL3) combined with the BNX filter (FL1) on the digital input, will break and separate the analog and digital grounds (see Figure 3-3).

Figure 3-3. Analog Power Input





Initial Board Setup

Factory setup of the board is for a 5-V analog and digital power supply. The socketed OP2350A is a rail-to-rail operational amplifier. The maximum analog input signals are 0-V to 5-V differential. The reference circuit is connected to the internal reference of the ADC (JP11 Closed) (refer to Table 4–1).

Table 4–1. Factory Defaults—Analog Input Buffers

Input Voltage	R102 R106	R100 R104	R103 R107	R101 R105	C101 C104	C100 C102	JP100 JP101
0 – 5	open	4.99 kΩ	open	4.99 kΩ	short	330 pF	2–3

The analog inputs to the DEM-ADS7864 board can be applied to any one or all of the input channels. Single-ended inputs are to be applied between analog ground (center terminal of J1 – J6) and either the positive or negative terminals. Differential signals are to be applied between the positive and negative terminals.

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4.1 Computer Interface Board—BBEval Software Update

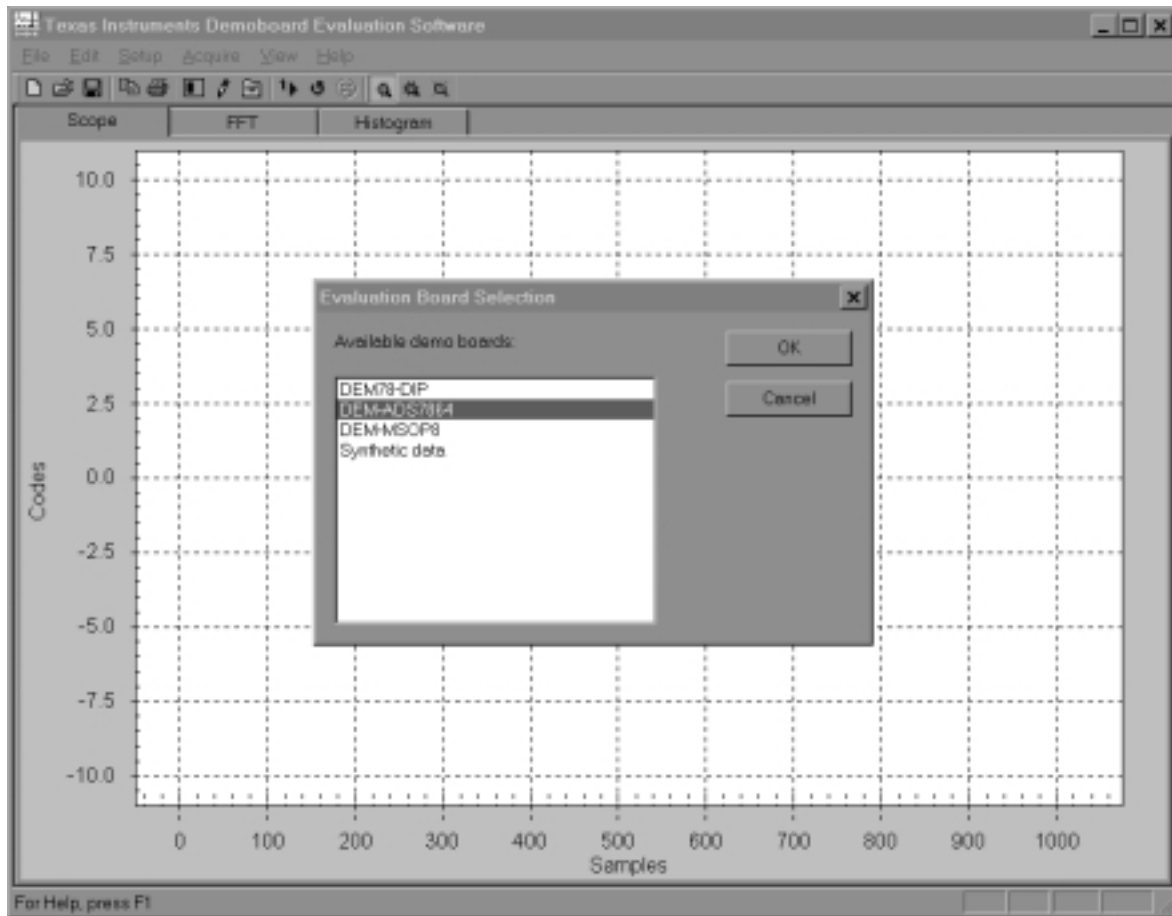
The DEM-ADS7864 board can be connected directly to the computer interface board through the P1 connector with the cable provided in the CIB kit. The DEM-CIB board controls all functions of the DEM-ADS7864.

A revised version of the BBEval software can be found in the DEM-CIB product folder at [:http://focus.ti.com/docs/tool/toolfolder.jhtml?PartNumber=DEM-CIB](http://focus.ti.com/docs/tool/toolfolder.jhtml?PartNumber=DEM-CIB). This site can also be accessed from the development tools link in the ADS7864 product folder.

4.2 Getting Started With the DEM-ADS7864 and the CIB Board

The first step after installing BBEval is to select the appropriate demo board. From the Setup menu item in the main menu, select the *select demo board* item. The following dialog box will appear:

Figure 4–1. Board Selection Screen

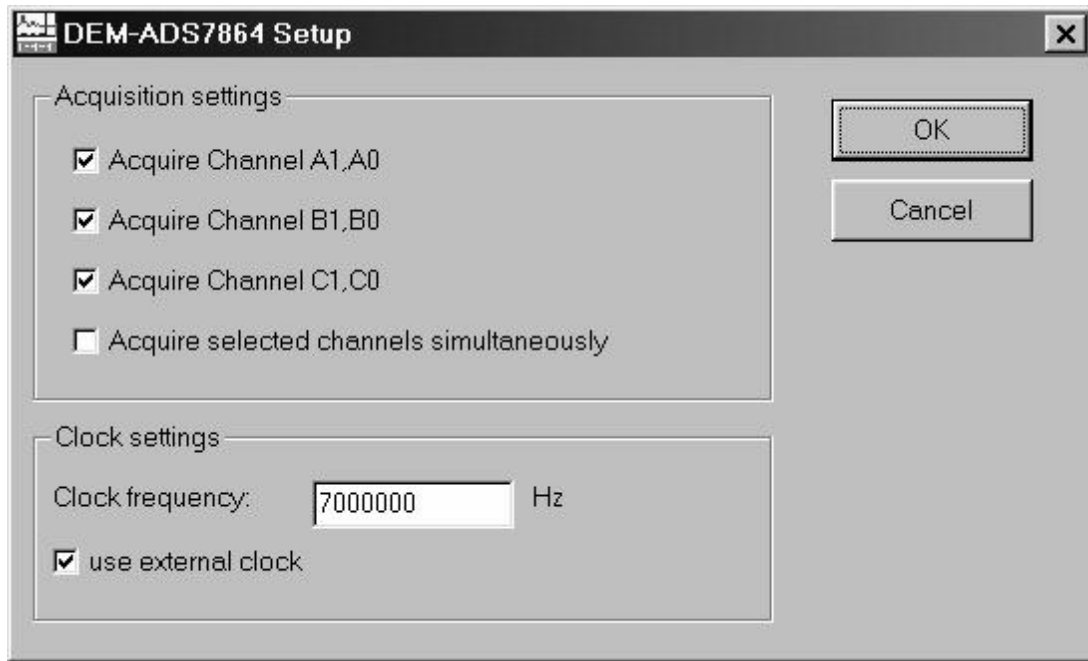


Select the DEM-ADS7864 and press OK. Note that this step has to be performed only once. This setting is stored and the same demo board is automatically selected again on subsequent invocations of BBEval.

4.2.1 Verify the Settings of the DEM-ADS7864

From the setup menu item in the main menu, select the Setup Demo Board menu item. The following dialog box will appear:

Figure 4-2. Setup Demo Board Dialog Box



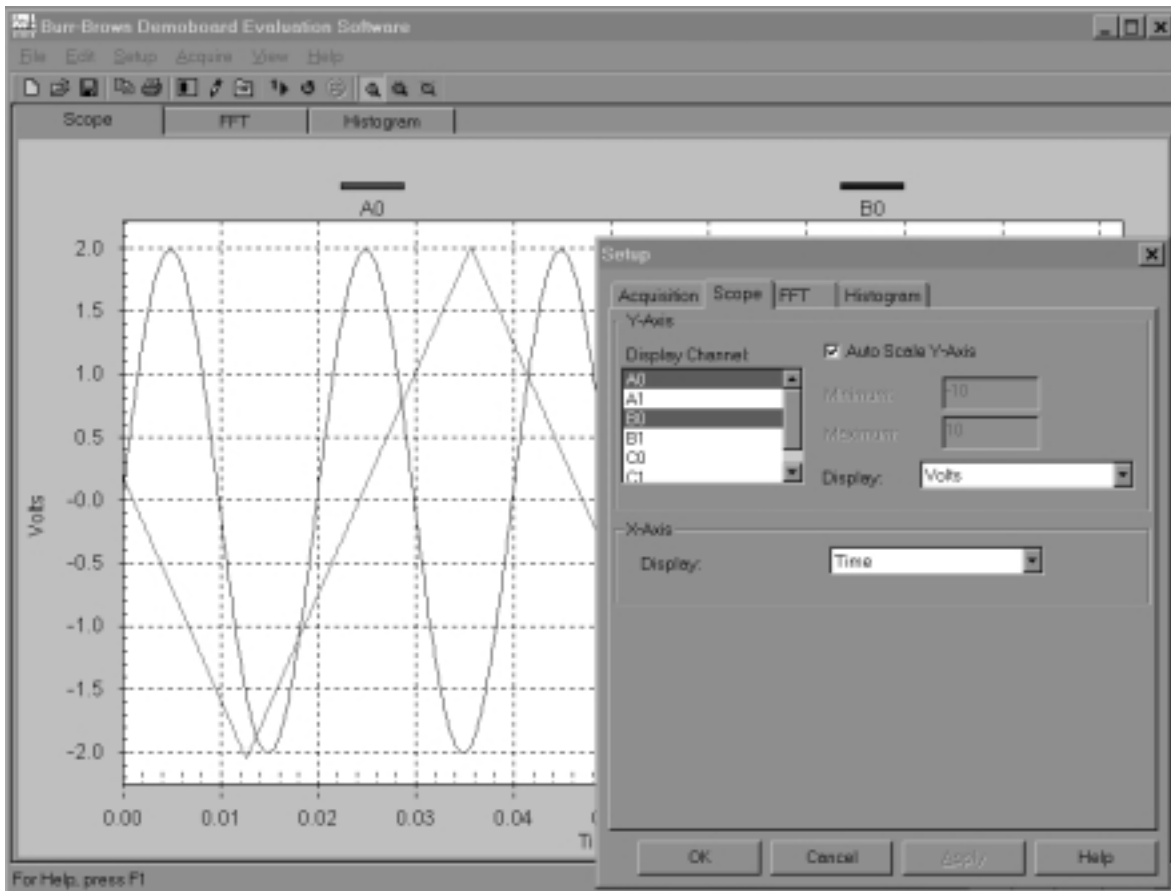
This dialog box allows the user to select the desired input channels of the DEM-ADS7864 board for signal acquisition. The *Acquire selected channels simultaneously* checkbox determines the timing of the $\overline{\text{HOLDn}}$ signals sent to the DEM-ADS7864. If the box is unchecked, as shown above, the selected channels are acquired and converted sequentially. If the box is checked, the selected channels are acquired simultaneously and converted sequentially.

The *use external clock* option, if checked, disables the DEM-CIB clock source and allows the user to set up a clock source from the DEM-ADS7864 via BNC P2.

4.3 Displaying Data

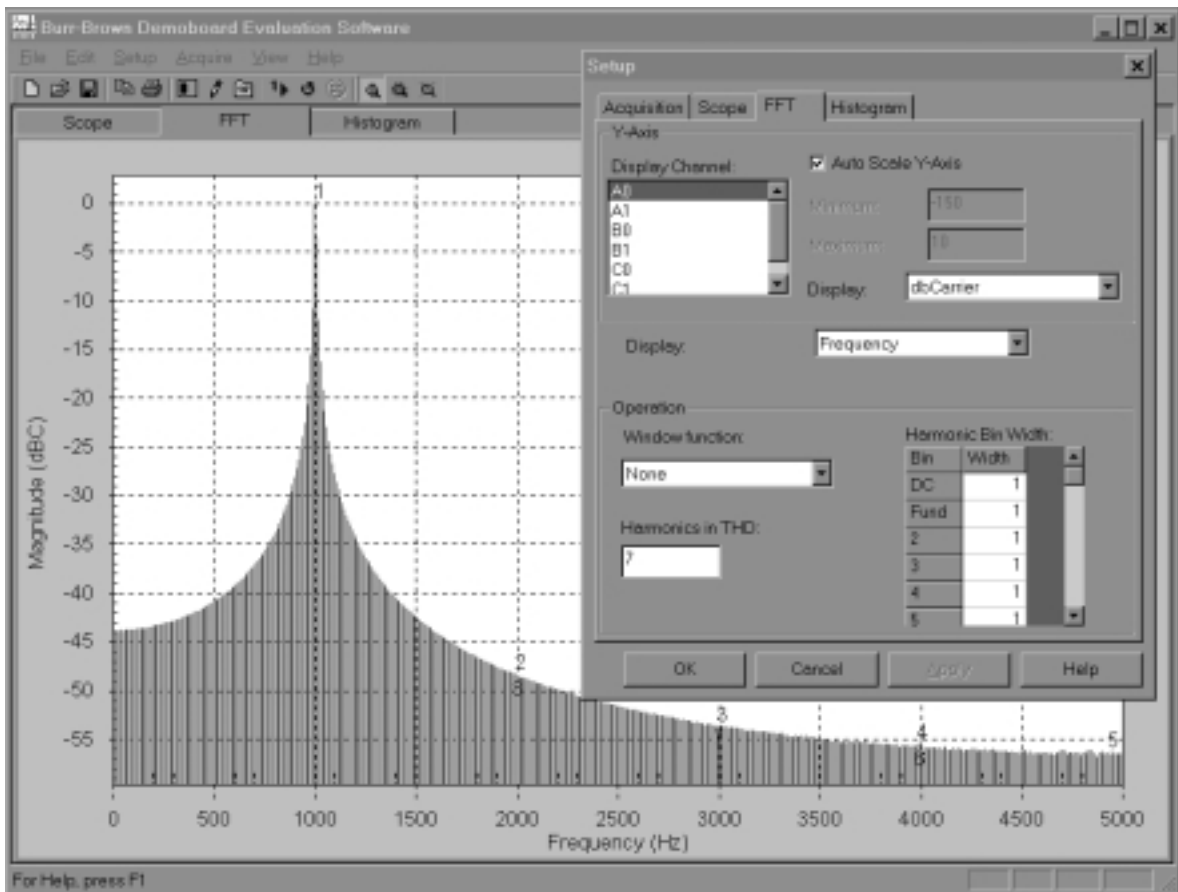
Sampling rate and the number of samples taken are independently controllable under the acquisition menu. Through the BBEval scope menu, the user can select the ADC channel to monitor on the scope interface. Multiple channels can be selected for display by pressing the CTRL key and clicking the appropriate channels with the mouse.

Figure 4–3. Setup Menu Channel Selection Screen



The FFT interface allows the user to view the spectral response of the acquired signal. Window function, number of harmonics, X and Y scale parameters, and channel selection are all user selectable.

Figure 4–4. Setup Menu FFT Interface Screen



The histogram feature allows the user to view the output codes and hits-per-code that were received from the ADC. All display functions can be used in either single-shot or continuous acquisition modes. Specific details of the operation of these features can be found in the on-line help section of the software.



Board Layer Artwork and Schematic

The following pages contain the artwork for the individual board layers and the circuit diagram of the DEM-ADS7864 demo board.

Figure A-1. Board Silkscreen Layer

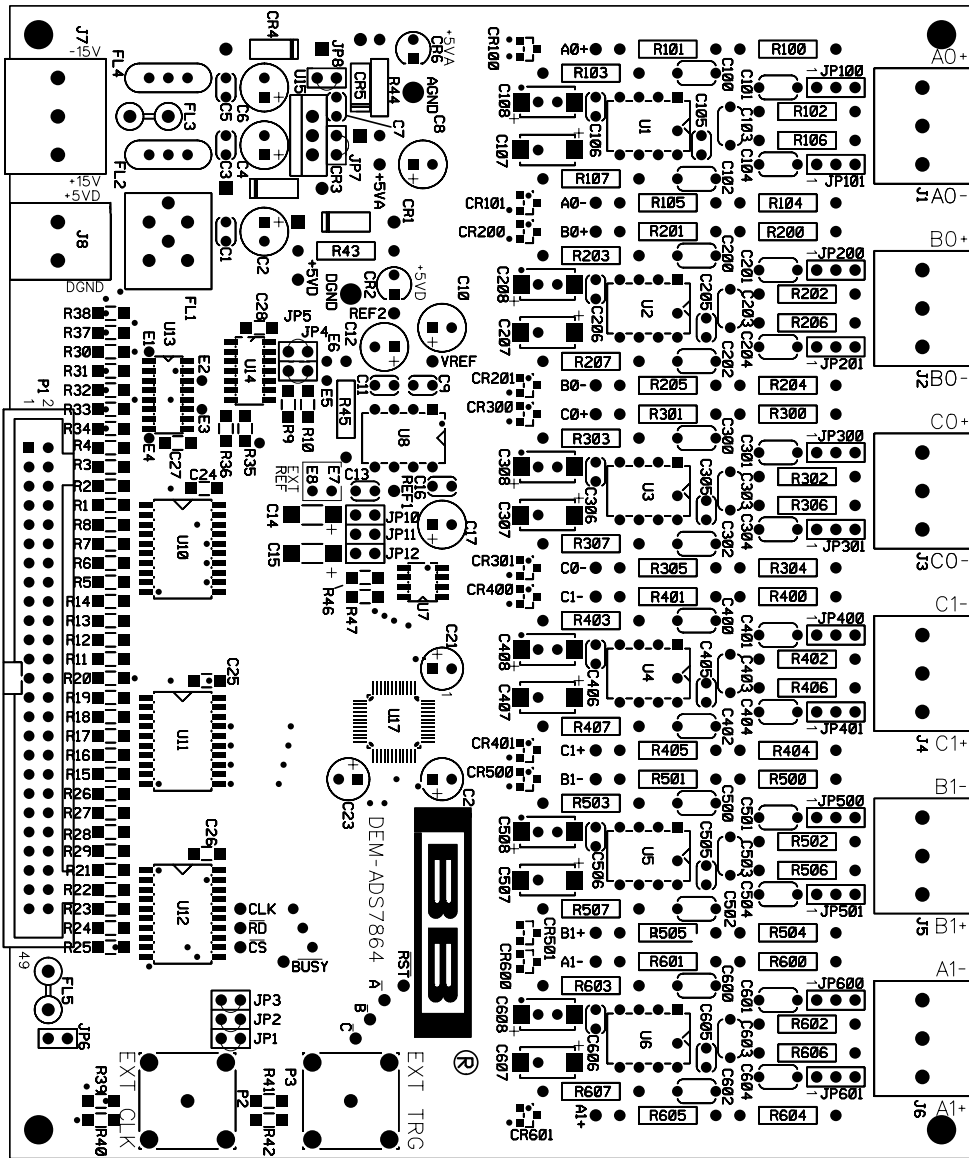


Figure A-2. Board Layer 1—Component Side

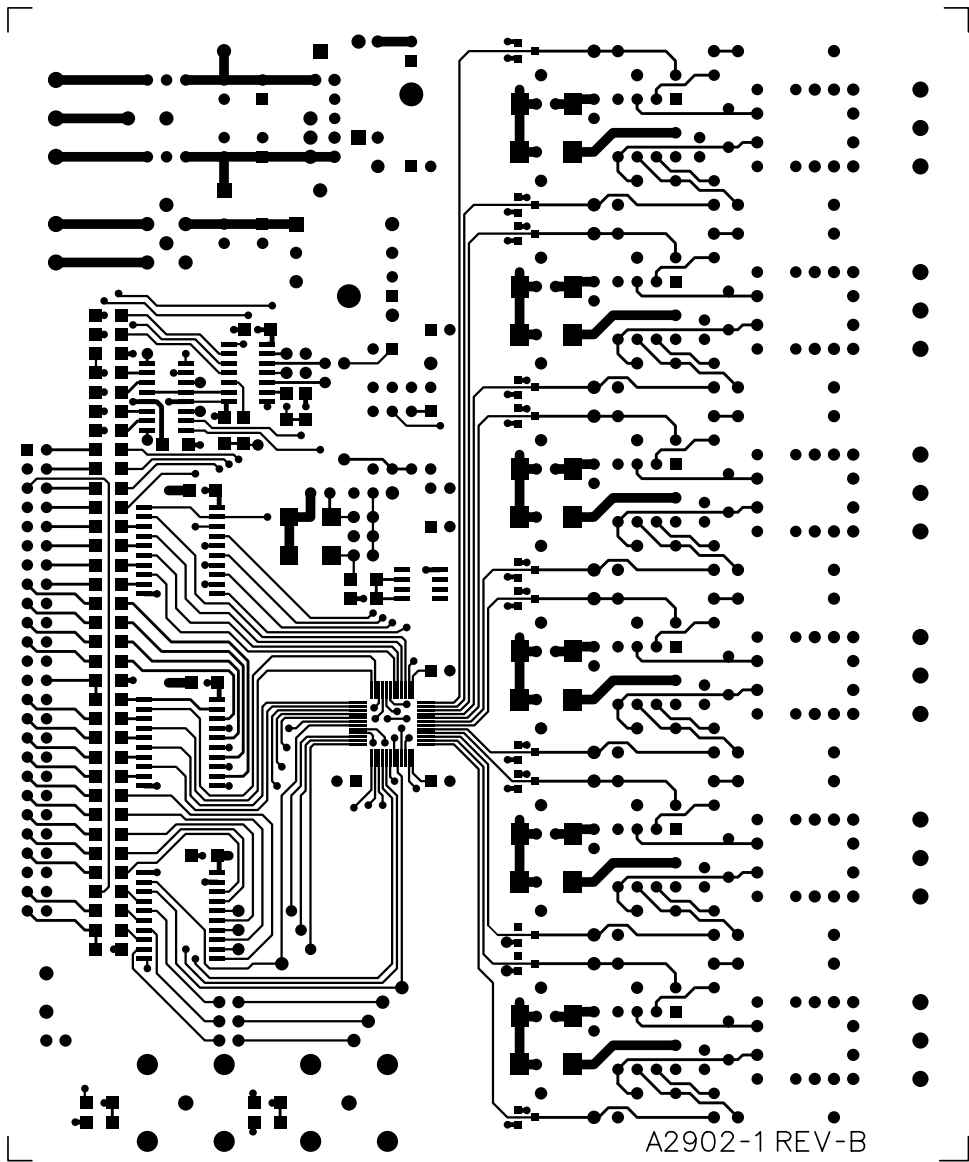


Figure A-3. Board Layer 2—Ground Plane

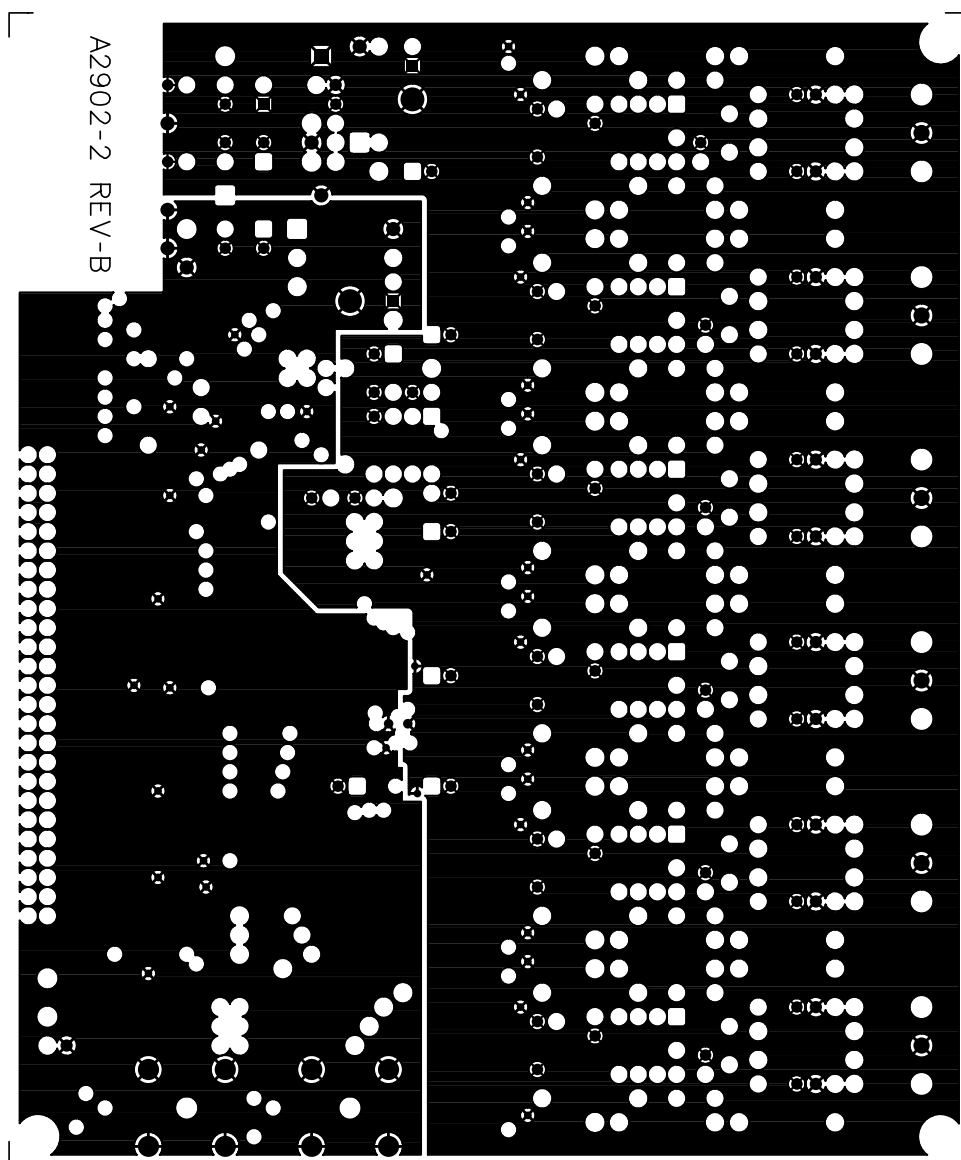


Figure A-4. Board Layer 3—Power Plane

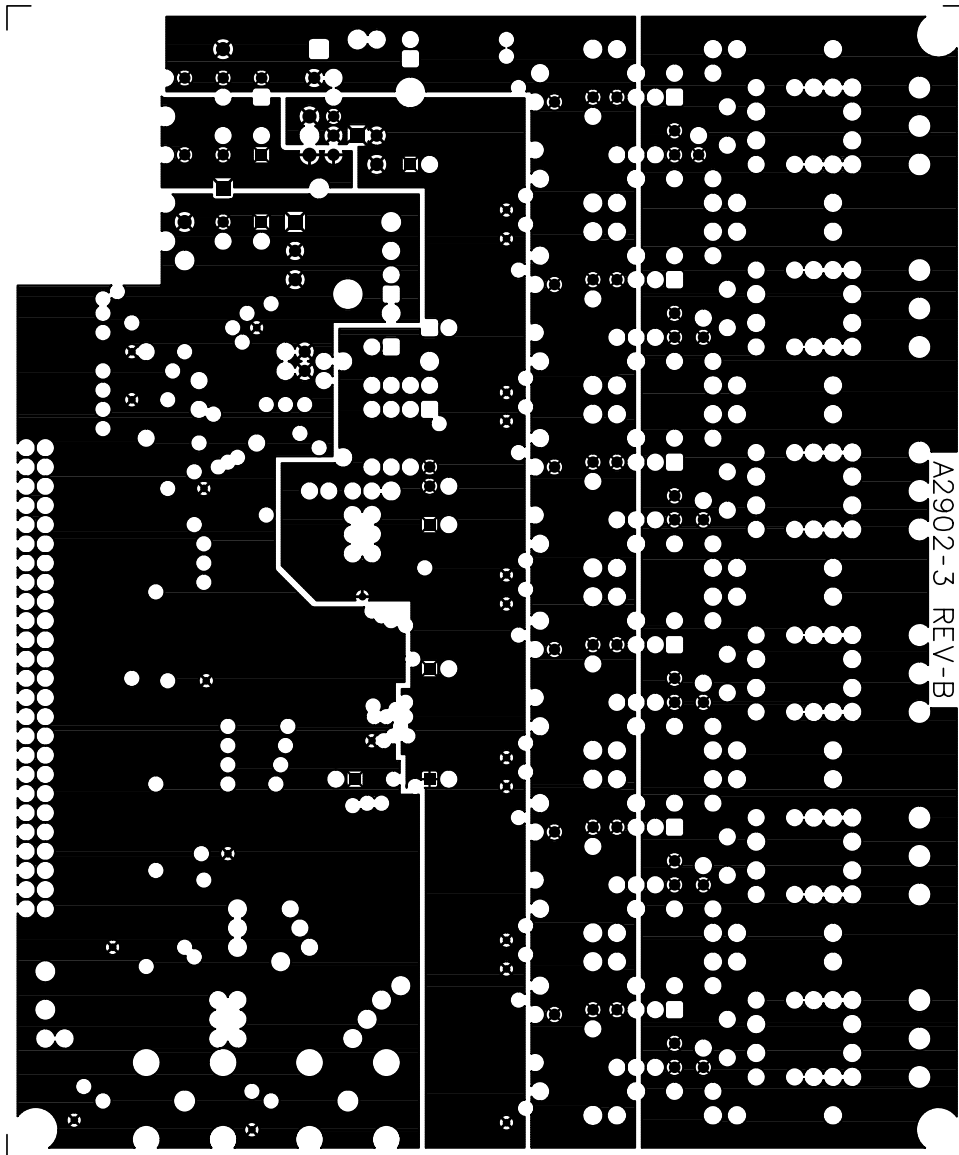


Figure A-5. Board Layer 4—Solder Side

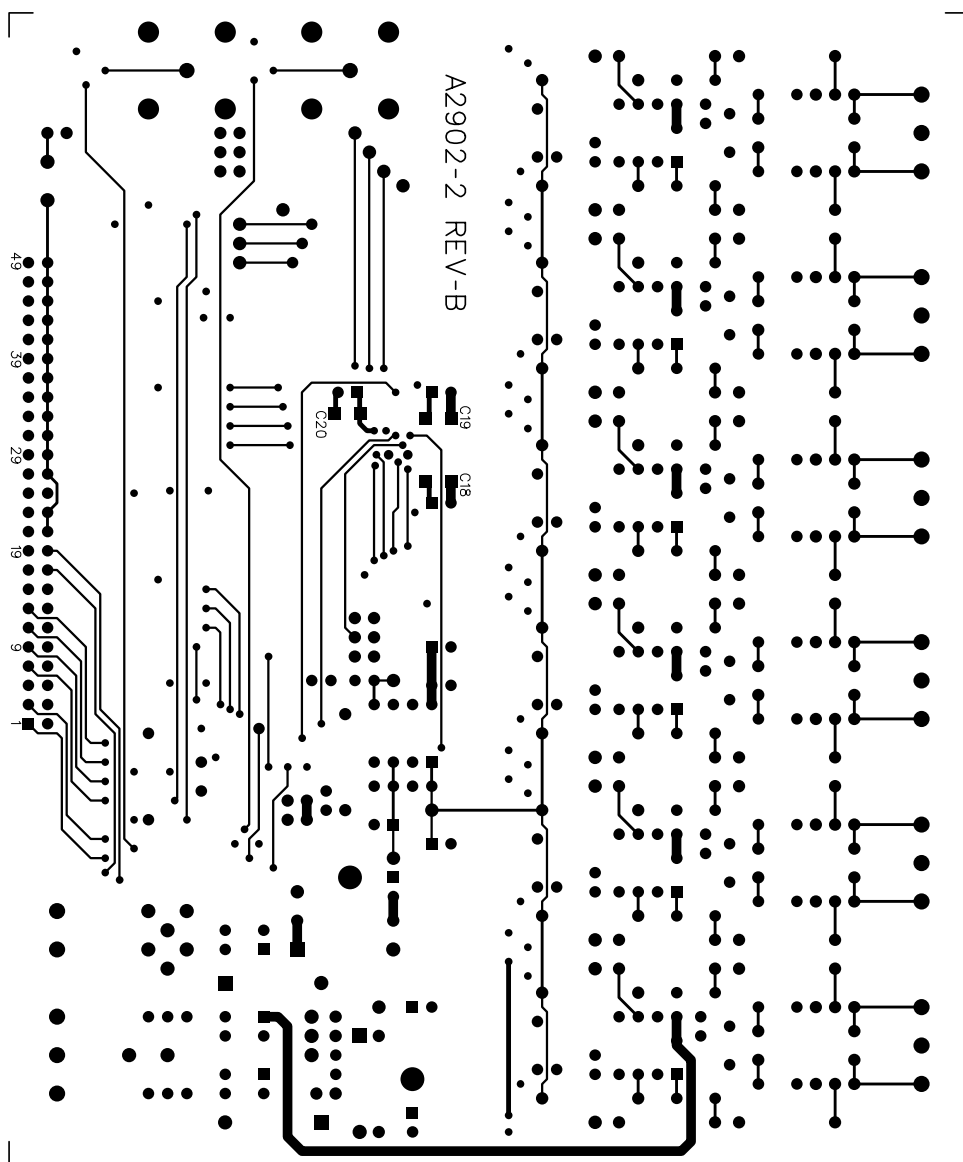
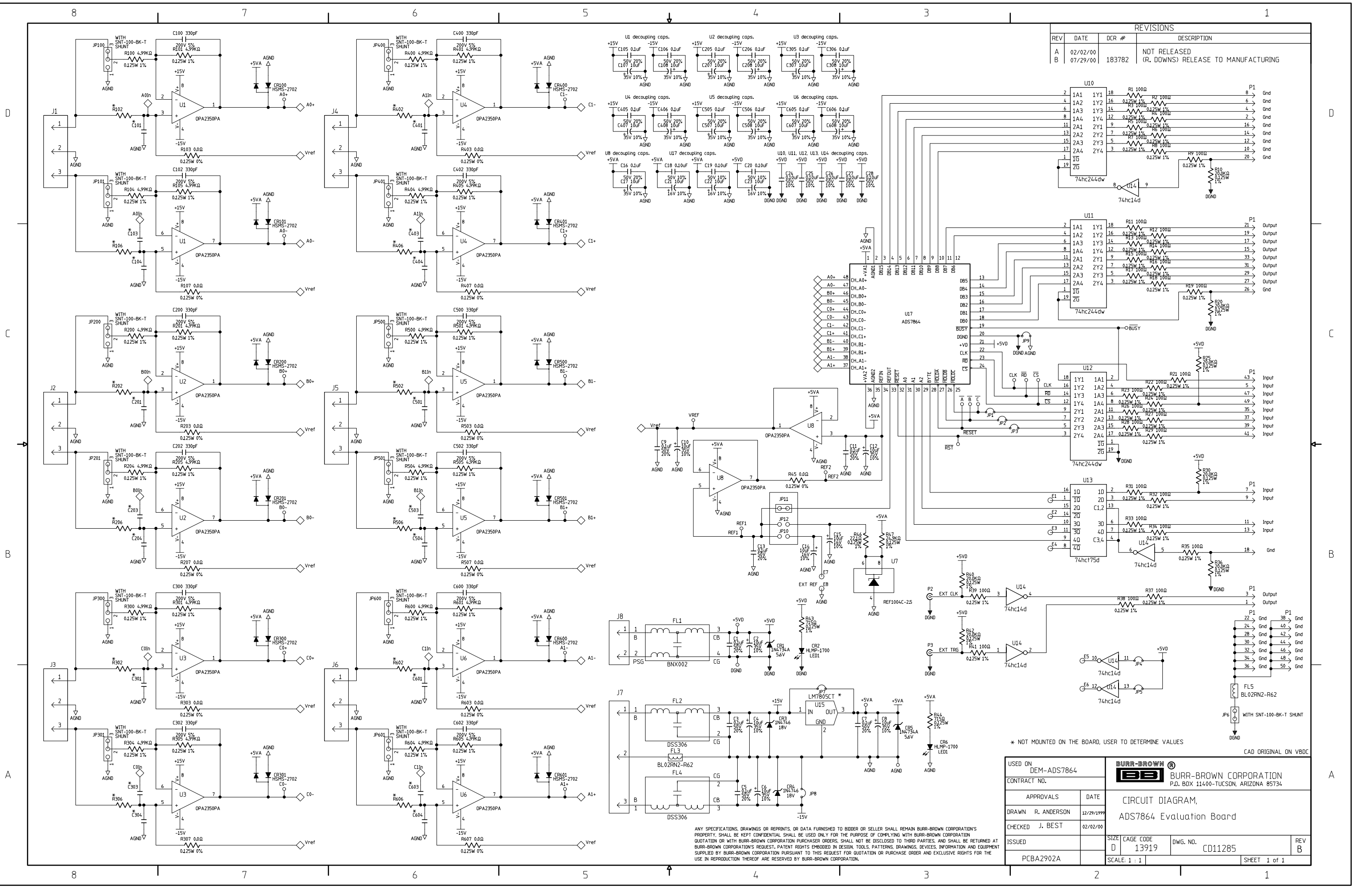


Figure A–6. DEM-ADS7864 Schematic

The following pages contain the foldout schematic for the DEM-ADS7864 demo board.

REVISIONS			
REV	DATE	DCR #	DESCRIPTION
A	02/02/00		NOT RELEASED
B	07/29/00	183782	(R. DOWNS) RELEASE TO MANUFACTURING



* NOT MOUNTED ON THE BOARD, USER TO DETERMINE VALUES

USED ON	DEM-ADS7864	Burr-Brown Corporation P.O. BOX 11400-TUCSON, ARIZONA 85734	
CONTRACT NO.		CIRCUIT DIAGRAM, ADS7864 Evaluation Board	
APPROVALS	DATE	SIZE	CAGE CODE
DRAWN R. ANDERSON	12/29/1999	D	13919
CHECKED J. BEST	02/02/00	DWG. NO.	CD11285
ISSUED		SCALE: 1 : 1	SHEET 1 of 1
PCBA2902A			

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