Data Sheet

ADIS16550

Autonomous Grade, Six Degrees of Freedom Inertial Sensor

FEATURES

- Triaxial, digital gyroscope, ±300°/sec
  - ±0.05° (typical) axis to axis misalignment
  - ±0.25° (maximum) axis to package misalignment
  - 1°/hr in-run bias stability
  - 0.13 °/√hr angular random walk
- Triaxial, digital accelerometer, ±14 *g*
  - 9 µ*g* in run bias stability
- Triaxial, delta angle and delta velocity outputs
- Factory calibrated sensitivity, bias, and axial alignment
  - Calibration temperature range: −40°C to +85°C
- SPI compatible
- Programmable operation and control
  - Manual bias correction controls
  - Digital I/O: data ready, external clock option
  - Sample clock options: internal, external, or scaled
  - On demand self test of inertial sensors
- Single-supply operation: 4.75 V to 5.25 V
- 1500 *g* mechanical shock survivability
- Operating temperature range: −40°C to +105°C

APPLICATIONS

- Precision instrumentation, stabilization
- Guidance, navigation, and control
- Precision autonomous machines and robotics
- Dead reckoning in global positioning system (GPS) denied environments

GENERAL DESCRIPTION

The ADIS16550 is a complete inertial system that includes a triaxis gyroscope and a triaxis accelerometer. Each inertial sensor in the ADIS16550 combines industry leading MEMS only technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, and alignment. As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The ADIS16550 provides a simple, cost-effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The serial peripheral interface (SPI) and register structure provide a simple interface for data collection and configuration control.

The footprint and connector system of the ADIS16550 enable a simple upgrade from the ADIS16485, ADIS16488A, ADIS16490, ADIS16495, and ADIS16497. The ADIS16550 is available in an aluminum package that is approximately 47 mm × 44 mm × 15 mm and includes a standard connector interface.

FUNCTIONAL BLOCK DIAGRAM

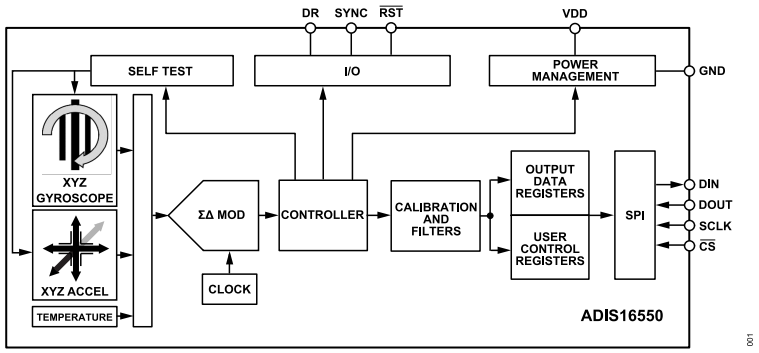

Figure 1. Functional Block Diagram

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

TABLE OF CONTENTS

REVISION HISTORY

4/2023—Revision 0: Initial Version

SPECIFICATIONS

T_C = 25°C, VDD = 5.0 V ± 5%, acceleration = 0 *g*, and angular rate = 0°/sec, unless otherwise noted. 1 *g* is the acceleration due to gravity and defined as 9.797464 m/sec^2. For complete definitions and conditions of all specifications, refer to the Terminology section.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±300			°/sec
Sensitivity	32 bit		5,242,880		LSB/°/sec
	16 bit		80		LSB/°/sec
Initial Sensitivity Error	µ + 1 σ		±0.045		%
Error Over Temperature	−40°C ≤ T_C ≤ +85°C, ±300°/sec, 1 σ		±0.08		%
	85°C ≤ T_C ≤ 105°C[1], ±300°/sec, 1 σ		±0.15		%
Repeatability[2]	µ + 1 σ		±0.35		%
Misalignment					
Axis to Axis	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.05		Degrees
Axis to Package[3]	−40°C ≤ T_C ≤ +85°C			±0.25	Degrees
Nonlinearity					
−125°/sec to +125°/sec	1 σ		0.25		% FSR
-300°/sec to +300°/sec	1 σ		0.25		% FSR
Microlinearity					
−125°/sec to +125°/sec	1 σ, ±5°/sec step size		0.05		%
−300°/sec to +300°/sec	1 σ, ±10°/sec step size		0.05		%
Bias					
Initial Bias Error	µ + 1 σ		±0.01		°/sec
Error over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.015		°/sec
	85°C ≤ T_C ≤ 105°C[1], 1 σ		±0.04		°/sec
Repeatability[2]	µ + 1 σ		±0.07		°/sec
In-Run Bias Stability	1 σ		1		°/hr
Angular Random Walk	1 σ		0.13		°/√hr
Linear Acceleration Effect	Any axis, 1 σ		5		°/hr/*g*
Vibration Rectification Error	1 σ		2.4		°/hr/*g*^{2}
Noise					
Output Noise	No filtering, 1 σ typical		0.065		°/sec RMS
Rate Noise Density[3, 4]	1 σ typical		0.0029	0.0033	°/sec/√Hz RMS
−3 dB Bandwidth[3]			400		Hz
Sensor Resonant Frequency			79		kHz
ACCELEROMETERS	Each axis				
Dynamic Range		±14			*g*
Sensitivity	32 bit		102400000		LSB/*g*
	16 bit		1562.5		LSB/*g*
Initial Sensitivity Error	µ + 1 σ		0.03		%
Error Over Temperature	−40°C ≤ T_C ≤ +85°C, ±1 *g*, 1 σ		±0.035		%
	85°C ≤ T_C ≤ 105°C[1], ±1 *g*, 1 σ		±0.05		%
Repeatability[2]	µ + 1 σ		±0.025		%
Misalignment					
Axis to Axis	−40°C ≤ T_C ≤+85°C, 1 σ		±0.05		Degrees
Axis to Package[3]	−40°C ≤ T_C ≤+85°C			±0.25	Degrees
Nonlinearity					
−2 *g* to +2 *g*	1 σ		0.001		% FSR
−14 *g* to +14 *g*	1 σ		0.3		% FSR

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Microlinearity					
−2 *g* to +2 *g*	1 σ, 1 *g* step size		0.55		%
−14 *g* to +14 *g*	1 σ, 1 *g* step size		2.0		%
Bias					
Initial Bias Error	μ + 1 σ		0.85		mg
Error over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.5		mg
	85°C ≤ T_C ≤ 105°C[1], 1 σ		±0.75		mg
Repeatability[2]	μ + 1 σ		±1.7		mg
In-Run Bias Stability	1 σ		9		μg
Velocity Random Walk	1 σ		0.03		m/sec/√hr
Noise					
Output Noise[3]	No filtering, 1 σ typical		1.8		mg RMS
Noise Density[3]	10 Hz to 40 Hz, no filtering, 1 σ typical		64	73	μg/√Hz RMS
−3 dB Bandwidth[3, 4]			700		Hz
Sensor Resonant Frequency			5.3		kHz
TEMPERATURE SENSOR					
Scale Factor	Output = 0x00000000 at 25°C (±5°C)		0.004		°C/LSB
LOGIC INPUTS[5]					
Input Voltage					
High, V_{IH}		2.0			V
Low, V_{IL}				0.8	V
$\overline{RST}$ Pulse Width		1			μs
Input Current					
Logic 1, I_{IH}	V_{IH} = 3.3 V			10	μA
Logic 0, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$, $\overline{CS}$				10	μA
$\overline{RST}$[6]			44	100	μA
$\overline{CS}$ Pin[6]			0.33		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[5]					
Output Voltage					
High, V_{OH}	Source current, I_{SOURCE} = 0.5 mA	2.4			V
Low, V_{OL}	Sink current, I_{SINK} = 2.0 mA			0.4	V
FLASH MEMORY	Endurance[7]	100,000			Cycles
Data Retention[8]	T_J = 105°C	20			Years
FUNCTIONAL TIMES[9]	Time until data is available				
Power-On Start-Up Time			350		ms
Reset Recovery Time[10]	$\overline{RST}$ pulled low, then restored to high		350		ms
Software Reset Time			330		ms
Clear User Calibration			100		μs
Flash Memory					
Update Time[11]			110		ms
On Demand, Self Test Time[12]			21		ms
CONVERSION RATE			4000		SPS
Initial Clock Accuracy			0.02		%
Temperature Coefficient			40		ppm/°C
Synchronization Input Clock		3.0		4.5	kHz
Scaled Synchronization Input Clock		1		128	Hz

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY, VDD	Operating voltage range	4.75		5.25	V
Power Supply Current[13]	Normal mode, VDD = 5.0 V, μ + 1 σ		135	170	mA

[1] The ADIS16550 performance is characterized from 85°C to 105°C. It is not 100% tested in production in this temperature range.

[2] Repeatability provides an estimate for long-term drift in the bias, as observed during 500 hours of high-temperature operating life (HTOL) at 105°C and 1000 cycles of temperature cycle testing (TCT). Repeatability represents the root sum square (RSS) of the bias drift associated with HTOL and TCT.

[3] Minimum and maximum limit is guaranteed by design and characterization. It is not 100% tested in production.

[4] Magnitude between 10 Hz and 40 Hz, sample rate is 4000 SPS (nominal), no digital filtering.

[5] The digital input and output signals use a 3.3 V system.

[6] The $\overline{RST}$ and $\overline{CS}$ pins are connected to an internal 3.3 V regulated voltage through 75 kΩ and 10 kΩ pull-up resistors, respectively.

[7] Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.

[8] The data retention specification assumes a T_J of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.

[9] These times do not include thermal settling and internal filter response times, which can affect overall accuracy.

[10] The $\overline{RST}$ line must be in a low state for at least the duration specified in the $\overline{RST}$ pulse width specification to ensure a proper reset initiation and recovery.

[11] The flash memory update time increases over the life of the device up to 250 ms (typical).

[12] The self test time can extend when using the external clock rates that are lower than 4000 Hz.

[13] The supply current transients can reach 830 mA during initial startup or reset recovery (ignoring glitches <50 μs).

TIMING SPECIFICATIONS

T_C = 25°C and VDD = 5.0 V, unless otherwise noted.

Table 2. Timing Specifications for Normal Mode

Parameter	Description	Min[1]	Typ	Max[1]	Unit
f_{SCLK}	SCLK frequency	0.01		15	MHz
t_{STALL}[2]	Stall period between data	5			μs
	Stall period between data in burst mode	8			μs
t_{CLS}	SCLK low period	33			ns
t_{CHS}	SCLK high period	33			ns
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	32			ns
t_{DAV}	DOUT valid after SCLK edge			10	ns
t_{DSU}	DIN setup time before SCLK rising edge	2			ns
t_{DHD}	DIN hold time after SCLK rising edge	2			ns
t_{DR}, t_{DF}	DOUT rise and fall times, ≤100 pF loading		3	8	ns
t_{DSOE}	$\overline{CS}$ assertion to DOUT active	0		11	ns
t_{HD}	SCLK edge to DOUT invalid	0			ns
t_{SFS}	Last SCLK edge to $\overline{CS}$ deassertion	32			ns
t_{DSHI}	$\overline{CS}$ deassertion to DOUT high impedance	0		9	ns
t_{NV}	Data invalid time		20		μs
t_1	Input sync pulse width	5			μs
t_2	Input sync period[3]	222.2			μs
t_3	Input sync to invalid data		280		μs

[1] Guaranteed by design and characterization, but not tested in production.

[2] Monitoring the data ready signal for the return of regular pulsing can help minimize system wait times.

[3] This measurement represents the inverse of the maximum frequency for the input sample clock: 4500 Hz.

SPECIFICATIONS

TIMING DIAGRAMS

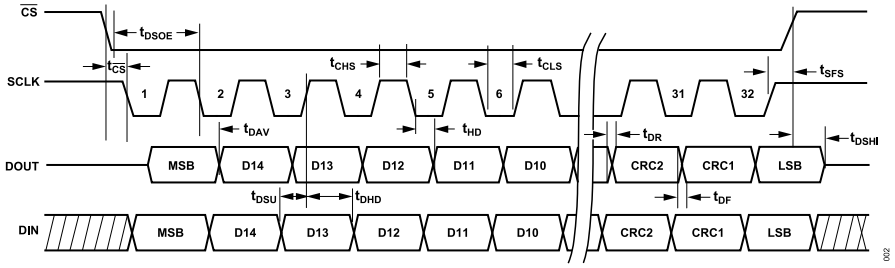

Figure 2. SPI Timing and Sequence

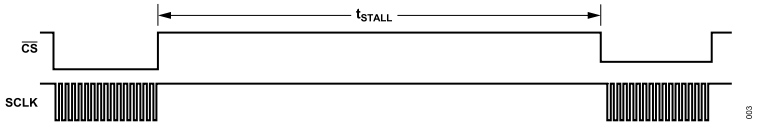

Figure 3. Stall Time and Data Rate

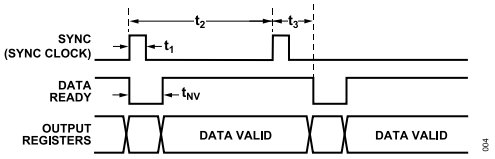

Figure 4. Input Clock Timing Diagram

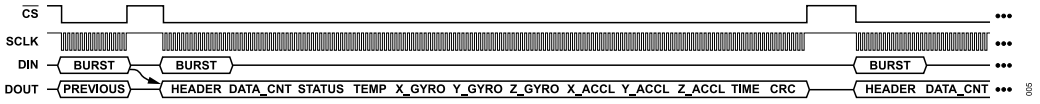

Figure 5. Burst Read Function Sequence Diagram, 12 Segments (32 Bits Each)

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
Mechanical Shock Survivability	
Any Axis, Unpowered	1500 *g*, 0.5 ms
Any Axis, Powered	1500 *g*, 0.5 ms
VDD to GND	−0.3 V to +5.25 V
Digital Input Voltage to GND	−0.3 V to +3.5 V
Digital Output Voltage to GND	−0.33 V to +3.8 V
Storage Temperature Range	−40°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Pay careful attention to PCB thermal design.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

The ADIS16550 is a multichip module, which includes many active components. The values in Table 4 identify the thermal response of the hottest component inside of the ADIS16550, with respect to the overall power dissipation of the module. This approach enables a simple method for predicting the temperature of the hottest junction, based on either ambient or case temperature.

For example, when the T_A = 70°C, the hottest junction inside of the ADIS16550 is 117.7°C.

$$T_J = \theta_{JA} \times V_{DD} \times I_{DD} + T_A$$

$$T_J = 70.6\ °C/W \times 5.0\ V \times 135\ mA + 70°C$$

$$T_J = 117.7°C$$

Table 4. Package Characteristics

Package Type[1]	θ_{JA}	θ_{JC}	Device Weight
ML-24-12	70.6°C/W	47.2°C/W	41.5 g

[1] Thermal impedance simulated values come from a case when 4 M2 × 0.4 mm machine screws (torque = 20 inch ounces) secure the ADIS16550 to the PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

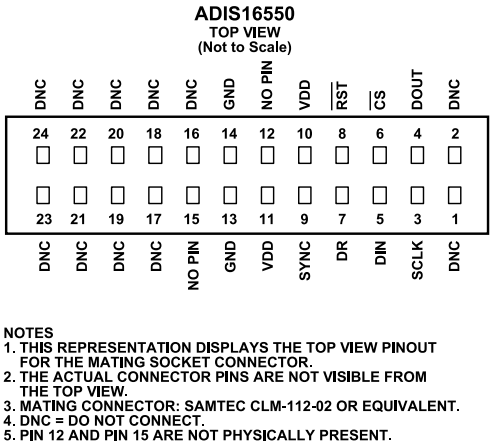

Figure 6. Pin Configuration

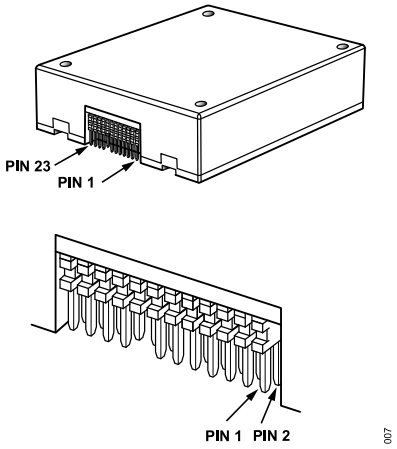

Figure 7. Axial Orientation (Top Side Facing Up)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 2, 16 to 24	DNC	Not applicable	Do Not Connect. Do not connect to these pins.
3	SCLK	Input	SPI Serial Clock.
4	DOUT	Output	SPI Data Output. Clocks output on the SCLK falling edge.
5	DIN	Input	SPI Data Input. Clocks input on the SCLK rising edge.
6	$\overline{CS}$	Input	SPI Chip Select.
7	DR	Output	Data Ready.
8	$\overline{RST}$	Input	Reset.
9	SYNC	Input	Input Synchronization Clock.
10, 11	VDD	Supply	5 V Power Supply.
12, 15	NO PIN	Not applicable	No Pin. These pins are not physically present.
13, 14	GND	Supply	Power Ground.
23			Do Not Connect. This pin is DNC, but for backwards compatibility with older ADIS1648x inertial measurement units (IMUs), it is acceptable to supply 3.3 V to this pin without incurring any additional power consumption.

TYPICAL PERFORMANCE CHARACTERISTICS

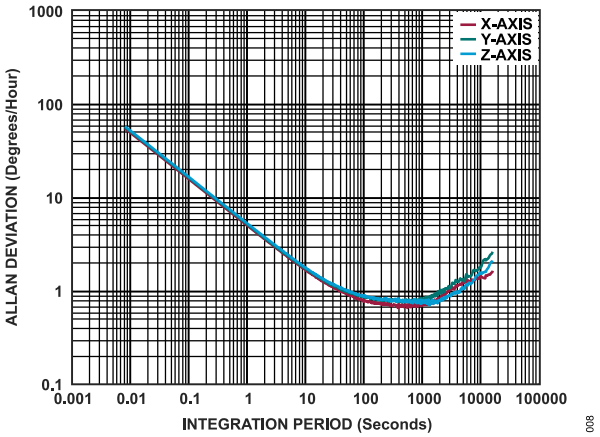

Figure 8. Gyroscope Allan Deviation

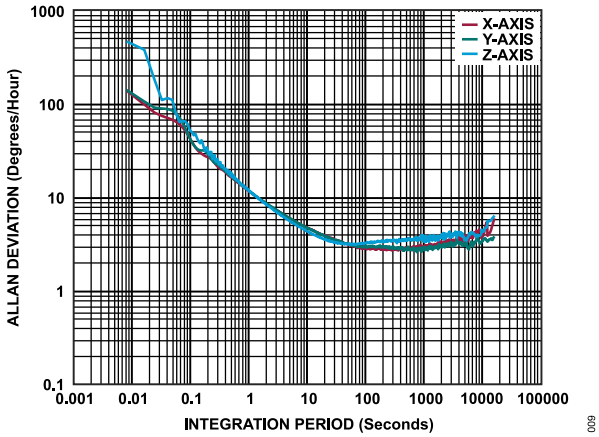

Figure 9. Accelerometer Allan Deviation

TERMINOLOGY

Gravity, 1 *g*

The gravity of Earth causes acceleration that is measurable by accelerometers. In this data sheet, gravitational acceleration is defined as

$$1\ \text{g} \quad = \quad 9.797464\ \text{m/sec}^2 \tag{1}$$

This value can be used to convert specifications from *g* to m/sec^2 throughout this data sheet.

It is important to keep in mind that the gravitational acceleration varies slightly across the surface of the earth. Consider the following factors when calculating the precise acceleration due to gravity at a specific location on Earth:

- Elevation (gravity decreases as elevation increases).
- Latitude. Earth is an oblate spheroid (gravity is weaker on the equator and stronger at the poles).
- The rotation of Earth (gravity is weaker on the equator due to rotational velocity/conservation of momentum).

In certain cases, small variations in gravitational acceleration are important. It is important for the user to account for this and realize that the output of an accelerometer varies slightly as a result of this.

Table 6. Gravitational Acceleration Examples

Location	Latitude (°)	Elevation (m)	Effective Gravitational Acceleration[1]
Equator	0	0	9.780325
North Pole	+90 or −90	0	9.832185
Analog Devices Factory	14.263	190.5	9.782872

[1] Accounts for elevation, the rotation of Earth, and the oblateness of Earth.

Use the following formula to determine the effective gravitational acceleration at a specific location on Earth (at sea level):

$$g_0 = \frac{R_{EQ} \times g_{EQ} \times \cos^2 LAT + R_{POL} \times g_{POL} \sin^2 LAT}{\sqrt{{R_{EQ}}^2 \times \cos^2 LAT + {R_{POL}}^2 \times \sin^2 LAT}} \tag{2}$$

where:
g_0 is the effective gravitation acceleration.
R_{EQ} is the radius of the Earth at the equator (6,378,127 m).
g_{EQ} is the effective acceleration at the equator (9.832185 m/sec^2).
R_{POL} is the radius of the Earth at the poles (6,356,752 m).
g_{POL} is the effective acceleration at the poles (9.780325 m/sec^2).
LAT is the latitude in degrees.

The previous equation accounts for the latitude and the rotation of the Earth but not the elevation. To correct for the elevation, use the following approximation:

$$\Delta g = g_H - g_0 \cong GM\left(\frac{1}{{R_H}^2} - \frac{1}{{R_0}^2}\right) \tag{3}$$

$$R_0 = \sqrt{\frac{\left({R_{EQ}}^2 \times \cos LAT\right)^2 + \left({R_{POL}}^2 \times \sin LAT\right)^2}{\left(R_{EQ} \times \cos LAT\right)^2 + \left(R_{POL} \times \sin LAT\right)^2}} \tag{4}$$

where:
g is the gravitational constant (6.67430 × 10^{-11} Nm^2/kg^2).
g_H is the effective gravitational acceleration at elevation R_H (in meters).
M is the mass of the Earth (5.972365 x 1024 kg).
R_H equals R_0 plus the elevation in meters.
R_0 is the radius of the Earth at a specific latitude.

The effective gravitational acceleration at the location including elevation is the sum of the effective gravitational acceleration = g_0 + Δg.

Output Full-Scale Range (FSR)

The output full-scale range is the guaranteed angular rate and acceleration measurement range at the output of the signal chain. The output full-scale range is specified as a minimum value and is guaranteed across all conditions. Angular rate and acceleration measurement is possible beyond this value; however, performance characteristics are not guaranteed.

Bias

Bias is any static (DC) error term on the output of the ADIS16550. It is measured as the deviation from 0°/sec or 0 *g* without externally applied angular rate or acceleration (including gravity). Bias is measured after the device is soldered to the application PCB.

To reduce the influence of external physical stimuli that can exist in the measurement system, average bias over a sufficiently long time window. Additionally, a data rate of >1 kHz is recommended.

$$Gyroscope = \Omega_{MEAS}(\Omega_{IN} = 0°/sec) \tag{5}$$

To calculate accelerometer bias, take measurements at orientations of +1 *g* and −1 *g* and calculate the average value of the two measurements.

$$XL = \frac{ACC_{MEAS}(g_{IN} = +1g) + ACC_{MEAS}(g_{IN} = -1g)}{2} \tag{6}$$

TERMINOLOGY

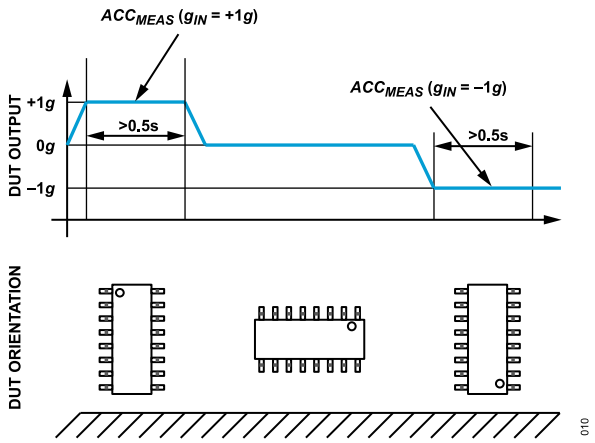

Figure 10. Acceleration Sensitivity Measurement Process

Bias Error over Temperature

Bias error over temperature is the change in bias directly attributed to changes in temperature. Bias error over temperature is measured relative to the bias at 25°C. Figure 11 shows the bias error over temperature expected for a device with a bias at 25°C equivalent to the initial (start of life) bias.

Bias drift over life can cause the offset measured at 25°C to diverge from the initial (start of life) bias measured during module manufacture. Figure 12 shows how the bias error over temperature limits are adjusted to accommodate divergence of the bias at 25°C and the initial bias.

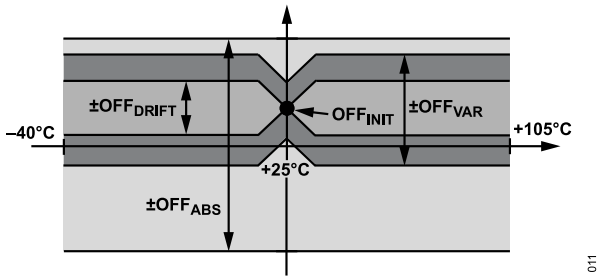

Figure 11. Bias Error over Temperature, $OFF_{INIT} = OFF_{AT\_25°C}$

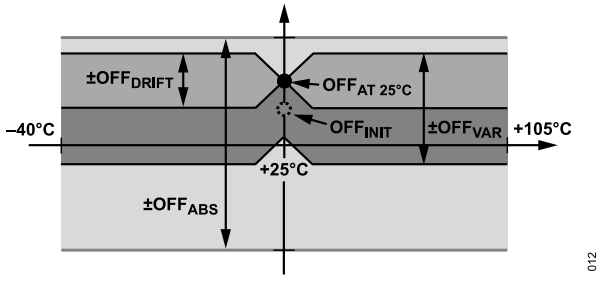

Figure 12. Bias Error over Temperature, $OFF_{INIT} \neq OFF_{AT\_25°C}$ (Change $OFF_{AT\_25°C}$ to $OFF_{AT\_25°C}$)

Bias Repeatability

Bias repeatability describes the long-term offset behavior over a variety of conditions. This repeatability represents a projection for long-term aging, which is derived from the drift behaviors that a sample of units exhibit throughout a 500 hours, 105°C HTOL stress and 1000 cycle TCT stress. Bias repeatability represents the RSS of the bias drift associated with HTOL and TCT.

In-Run Bias Stability

In-run bias (offset) stability is a measure of how quickly gyroscope (or accelerometer) outputs drift over time. It is derived from the minimum of the Allan variance curve as shown in Figure 13.

$$Accelerometer\ \ Allan\ \ Variance\left(\tau\right) = \sqrt{\frac{1}{2(n-1)}\sum_1\left(ACC_{MEAS(\tau)_{i+1}} - ACC_{MEAS(\tau)i}\right)^2} \quad (7)$$

$$Gyroscope\ \ Allan\ \ Variance\left(\tau\right) = \sqrt{\frac{1}{2(n-1)}\sum_1\left(\Omega_{MEAS(\tau)_{i+1}} - \Omega_{MEAS(\tau)i}\right)^2} \quad (8)$$

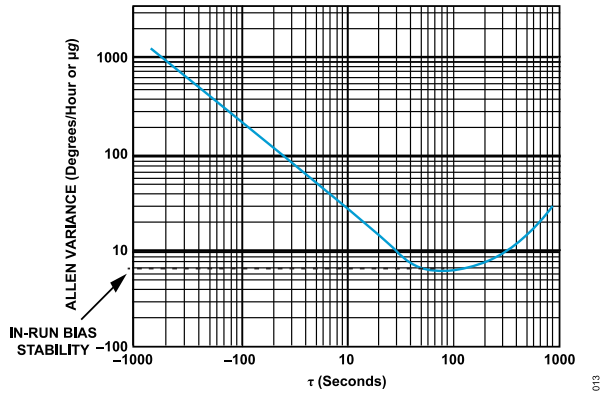

Figure 13. Example Allan Variance Plot

Inertial Data Format

The inertial data format is the digital representation of the angular rate or acceleration information output by the ADIS16550. Both the angular rate and acceleration information is transmitted as 16-bit (or 32-bit), twos complement values. Nominal sensitivity and nominal scale factor define the relationship for converting from the digital 16-bit (or 32-bit) value to either acceleration or angular rate.

Nominal Sensitivity

Nominal sensitivity is the slope of the line of the best fit for the angular rate and acceleration transfer functions, as measured across the output FSR of the ADIS16550. The sensitivity defines the change in output (LSB) per unit change of input (*g* or °/sec).

TERMINOLOGY

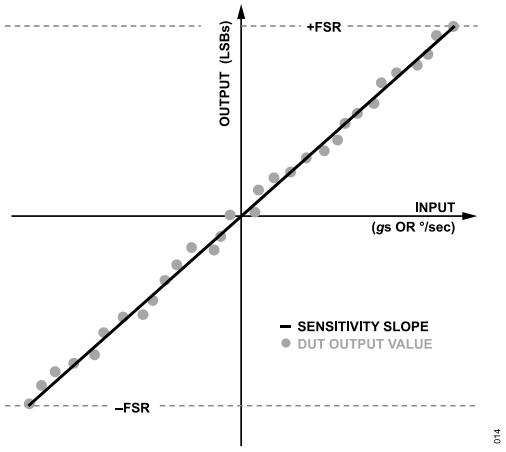

Figure 14. Nominal Sensitivity Slope

Nominal Scale Factor

The nominal scale factor is the inverse of the nominal sensitivity. It is the slope of the line of best fit for the angular rate and acceleration transfer functions, as measured across the output FSR of the ADIS16550. The nominal scale factor describes the change in input (*g* or °/sec) per change in the device output (LSB).

Sensitivity and Scale Factor Tolerance

The sensitivity and scale factor tolerance is the allowable variation between the applied angular rate or acceleration and the digital output (LSB). The acceleration sensitivity can be validated at inputs of ±1 *g*, and the angular rate sensitivity can be validated at any input greater than ±50°/sec.

$$Acceleration = \frac{ACC_{MEAS}(g_{IN} = +1g) - ACC_{MEAS}(g_{IN} = -1g)}{2g} \quad (9)$$

$$Gyroscope = \frac{\Omega_{MEAS}(\Omega_{IN} = +50°/sec) - \Omega_{MEAS}(\Omega_{IN} = -50°/sec)}{100°/sec} \quad (10)$$

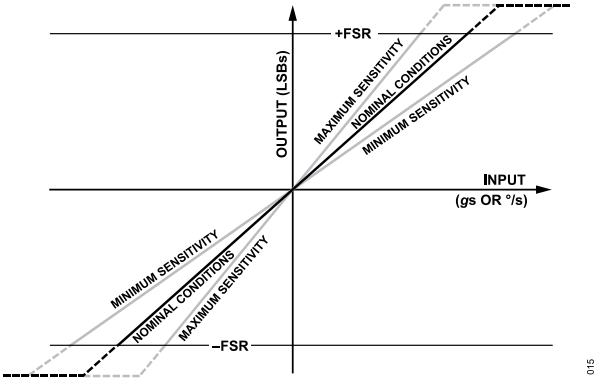

Figure 15. Sensitivity and Scale Factor Transfer Function

Cross Axis Sensitivity

Cross axis sensitivity is the measured output of the ADIS16550 in response to the input stimuli orthogonal to the measurement axis. It is measured as a percentage of the applied orthogonal acceleration or rotation rate. All stimulus axes are defined relative to the package body, as shown in Figure 38 and Figure 39.

$$Gyroscope = \left(\frac{\Omega_{MEAS}(\Omega_Z)}{\Omega_X(\Omega_Y)}\right) \times 100\,\% \quad (11)$$

$$Acceleration = \left(\frac{ACC_{MEAS}(g_X)}{g_Y(or\ \ g_Z)}\right) \times 100\,\% \quad (12)$$

where:
Ω_{MEAS} (Ω_Z) is the measured angular rate.
Ω_X (or Ω_Y) is the applied pitch or roll rate.
ACC_{MEAS} (g_X) is the measured x-axis acceleration.
g_Y (or g_Z) is the applied y-axis or z-axis acceleration.

Nonlinearity

Nonlinearity is the maximum deviation of any sensor data point ($\Omega_{MEAS}(\Omega_n)$ or $ACC_{MEAS}(g_n)$) from the least squares linear fit of the sensor data at an equivalent applied angular rate or acceleration. Nonlinearity is mathematically expressed as follows:

$$Gyroscope = \Omega_{MEAS}(\Omega_n) - \Omega_{CALC}(\Omega_n) \quad (13)$$

$$Acceleration = ACC_{MEAS}(g_n) - ACC_{CALC}(g_n) \quad (14)$$

where:
Ω_{MEAS} is the measured angular rate at Ω_N.
Ω_{CALC} is the linear fit calculation of the angular rate at Ω_n.
ACC_{MEAS} is the measured acceleration at g_n.
ACC_{CALC} is the linear fit calculation of acceleration at g_n.

For testing across a range of ±125°/sec (gyroscope) or ±2.5 *g* (accelerometer), apply the following input stimulus profile:

$\Omega_n = -125°/sec + (n \times 2.5)$

where n = 0, 1, ..., 100.

$g_n = -2.5\ g + (n \times 0.05)$

where n = 0, 1, ..., 100.

For testing across a range of ±300°/sec (gyroscope) or ±14 *g* (accelerometer), apply the following input stimulus profile:

$\Omega_n = -300°/sec + (n \times 5)$

where n = 0, 1, ..., 120.

$g_n = -14\ g + (n \times 0.2)$

where n = 0, 1, ..., 100.

TERMINOLOGY

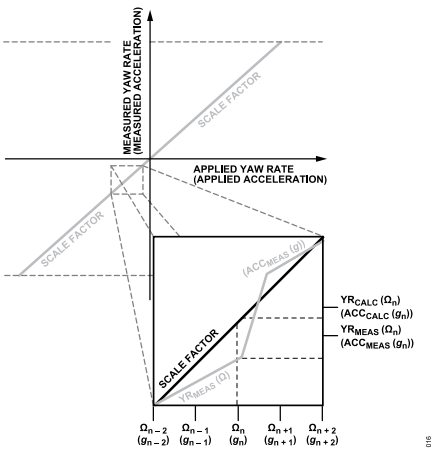

Figure 16. Nonlinearity Characteristic

Microlinearity

Microlinearity is the maximum deviation of the gradient between two neighboring sensor data points as compared to the scale factor calculated from the least squares linear fit of the sensor data. Microlinearity is mathematically expressed as follows:

$$Gyroscope = \left(\frac{\Omega_{MEAS}(\Omega_n - 1) - \Omega_{MEAS}(\Omega_n)}{\Omega_{STEP} \times Sensitivity} - 1\right) \times 100\,\% \quad (15)$$

$$Acceleration = \left(\frac{ACC_{MEAS}(g_n + 1) - ACC_{MEAS}(g_n)}{g_{STEP} \times Sensitivity} - 1\right) \times 100\,\% \quad (16)$$

where:
Ω_{MEAS} is the measured angular rate at a defined Ω_n.
ACC_{MEAS} is the measured acceleration at a defined g_n.

For testing across a range of ±125°/sec (gyroscope) or ±2.5 *g* (accelerometer), apply the following input stimulus profile:

Ω_{STEP} = 5°/sec

g_{STEP} = 100 mg

Ω_n = −125°/sec + (*n* x Ω_{STEP})

where *n* = 0, 1, …, 50.

g_n = −2.5 *g* + (*n* x g_{STEP})

where *n* = 0, 1, …, 50.

For testing across a range of ±300°/sec (gyroscope) or ±14 g (accelerometer), apply the following input stimulus profile:

Ω_{STEP} = 10°/sec

g_{STEP} = 250 mg

Ω_n = −300°/sec + (*n* x Ω_{STEP})

where *n* = 0, 1, …, 59.

g_n = −14 *g* + (*n* x g_{STEP})

where *n* = 0, 1, …, 95.

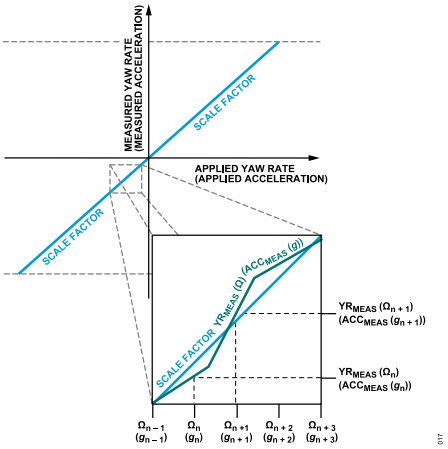

Figure 17. Microlinearity Characteristic

Cutoff (−3 dB) Frequency

For applied ac acceleration and angular rates, the cutoff (−3 dB) frequency is the frequency at which the input stimulus is attenuated in amplitude by 29.3% (1 − √2 ÷ 2) at the output of the signal chain. The −3 dB corner is set according to the electrical signal chain filter selected by the user. All other signal chain elements have an appreciably high bandwidth and are not significant contributors to the cutoff frequency.

Cutoff (−3 dB) Frequency Tolerance

Cutoff (−3 dB) frequency tolerance is the allowable variation to the frequency at which a −3 dB (29.3%) signal attenuation is achieved. The device clock directly correlates to the cutoff frequency achieved by the ADIS16550. For each percent that the device clock frequency varies from its nominal value, so too does the cutoff frequency.

Low-Pass Filter Group Delay

The low-pass filter group delay is the time required for the signal chain output to transition from 10% to 90% of its final value. The low-pass filter group delay is measured in response to an applied step change in acceleration or angular rate. The low-pass filter group delay tolerance is equivalent to the cutoff (−3 dB) frequency tolerance.

RMS Noise

The RMS noise is the standard deviation of the acceleration or angular rate output without an applied inertial stimulus. The RMS noise can be specified at either room temperature (25°C ± 5°C) or over the entire operating temperature range (−40°C to +105°C). The calculation method to assess the RMS noise is the same, regardless of the temperature range. Make this measurement with a sufficiently high sample rate and sufficiently long duration to ensure

TERMINOLOGY

that adequate accuracy and repeatability are achieved according to the requirements of the measurement system.

$$RMS\ Noise = \sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(x_i - \bar{x})^2} \quad (17)$$

where:
n is the number of sample values.
x_i is the individual sample value.
$\bar{x}$ is the mean value of the population.

Resonant Frequency

The resonant frequency is also known as the natural frequency (f_0). Input acceleration at the resonant frequency of a MEMS element causes the sensor to displace by an amount equivalent to the applied acceleration multiplied by the quality factor. For either underdamped or overdamped systems, acceleration applied at the resonant frequency is not inherently destructive to the MEMS element.

Quality Factor

The quality factor is a scalar factor that governs the increase or decrease in amplitude of an acceleration signal applied at the resonant frequency of a MEMS element.

Sensitivity to Linear Acceleration (Limited Condition, Gyroscope Only)

Sensitivity to linear acceleration is the change in the angular rate output of the ADIS16550 in response to an applied linear acceleration. It is measured in °/sec/*g*. Reduced sensitivity to linear acceleration improves the angular rate signal accuracy in harsh environments where shock and vibration are present. Analog Devices validates the gyroscope sensitivity to linear acceleration through the application of both DC acceleration and Haversine shock testing (<90 *g* peak and ≤10 ms duration).

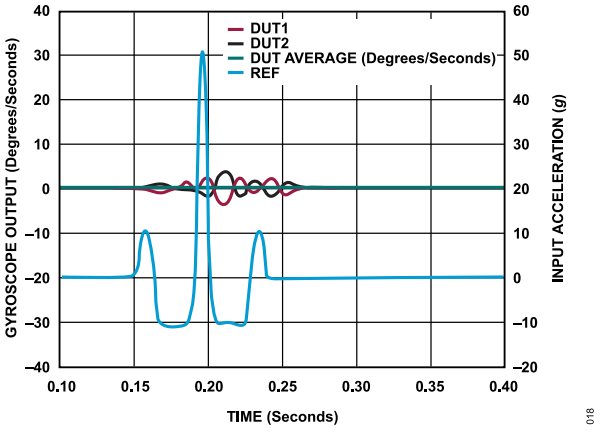

Figure 18. Sensitivity to Linear Acceleration

THEORY OF OPERATION

The ADIS16550 is an autonomous sensor system that starts up on its own when it has a valid power supply. After running through its initialization process, it begins sampling, processing, and loading calibrated sensor data into the output registers, which are accessible using the SPI port.

INERTIAL SENSOR SIGNAL CHAIN

Figure 19 shows the basic signal chain for the inertial sensors in the ADIS16550 that processes data at a rate of 4000 SPS when using the internal sample clock. Using one of the external clock options can provide some flexibility in selecting this rate.

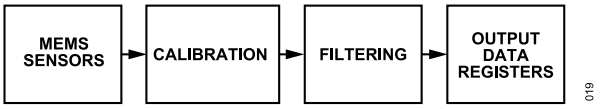

Figure 19. Signal Processing Diagram, Inertial Sensors

GYROSCOPE DATA SAMPLING

The ADIS16550 produces angular rate measurements around three orthogonal axes (x, y, and z). Figure 20 shows the basic signal flow for the production of x-axis gyroscope data (same as the y-axis and z-axis). This signal chain contains two digital MEMS gyroscopes (X_{G1} and X_{G2}) that have their own ADC and sample clocks that produce data independently from each other. Processing this data starts with calibrating and then combining the most recent sample from each gyroscope, which drives the rest of the digital signal processing (alignment and filtering) for the gyroscopes and accelerometers.

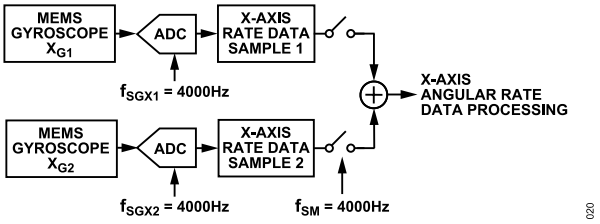

Figure 20. Gyroscope Data Sampling

ACCELEROMETER DATA SAMPLING

The ADIS16550 produces acceleration measurements around three orthogonal axes (x, y, and z). Figure 21 shows the basic signal flow for the production of x-axis acceleration data (same as y-axis and z-axis). This signal chain contains two digital MEMS accelerometers (X_{A1} and X_{A2}), which have their own ADC and sample clocks that produce data independently from each other. Although each accelerometer has its own clock (f_{SAX1} and f_{SAX2}), they use interpolation so that both are synchronous with the sample clock, f_{SM}. Processing this data starts with calibrating and then combining the most recent sample from each accelerometer, which drives the rest of the digital signal processing (alignment and filtering) for the gyroscopes and accelerometers.

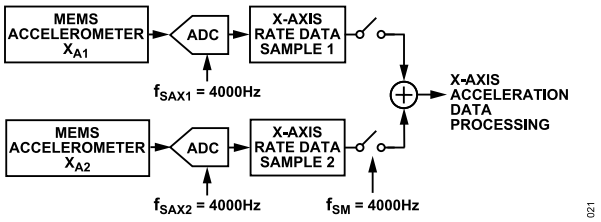

Figure 21. Accelerometer Data Sampling

EXTERNAL CLOCK OPTIONS

The ADIS16550 offers two modes of operation to control data production with an external clock: sync mode and scaled sync mode. In sync mode, the external clock directly controls the data sampling and production clock (f_{SM} in Figure 20 and Figure 21). The SYNC pin is configured to trigger on the rising edge of the external clock source. In scaled sync mode, the user can provide a lower input clock rate (1 Hz to 128 Hz) and use a scale factor (SYNC_SCALE register, see Table 94) to establish a data collection and processing rate that is between 3000 Hz and 4500 Hz for best performance.

INERTIAL SENSOR CALIBRATION

The calibration function for the gyroscopes and the accelerometers has two components: factory calibration and user calibration (see Figure 22).

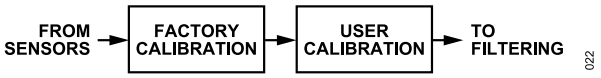

Figure 22. Gyroscope Calibration Processing

GYROSCOPE FACTORY CALIBRATION

Gyroscope factory calibration applies the following correction formula to the data of each gyroscope:

$$\begin{pmatrix}\omega_{XC}\\ \omega_{YC}\\ \omega_{ZC}\end{pmatrix}=\begin{pmatrix}m_{11}m_{12}m_{13}\\ m_{21}m_{22}m_{23}\\ m_{31}m_{32}m_{33}\end{pmatrix}\times\left(\begin{pmatrix}\omega_X\\ \omega_Y\\ \omega_Z\end{pmatrix}+\begin{pmatrix}b_x\\ b_y\\ b_z\end{pmatrix}\right) \quad (18)$$

where:
ω_{XC}, ω_{YC}, and ω_{ZC} are the postcalibration gyroscope data.
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} are the scale and alignment correction factors.
ω_X, ω_Y, and ω_Z are the precalibration gyroscope data.
b_X, b_Y, and b_Z are the bias correction factors.

All the correction factors in each matrix and array are derived from direct observation of the response of each gyroscope to a variety of rotation rates at multiple temperatures across the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but they are not available for observation. See Figure 42 for more details on the user calibration options that are available for the gyroscopes.

THEORY OF OPERATION

ACCELEROMETER FACTORY CALIBRATION

The accelerometer factory calibration applies the following correction formulas to the data of each accelerometer:

$$\begin{pmatrix} a'_X \\ a'_Y \\ a'_Z \end{pmatrix} = \begin{pmatrix} m_{11}m_{12}m_{13} \\ m_{21}m_{22}m_{23} \\ m_{31}m_{32}m_{33} \end{pmatrix} \times \left(\begin{pmatrix} a_X \\ a_Y \\ a_Z \end{pmatrix} + \begin{pmatrix} b_x \\ b_y \\ b_z \end{pmatrix} \right) + \begin{pmatrix} 0 & p_{12}p_{13} \\ p_{21} & 0 & p_{23} \\ p_{31}p_{32} & 0 \end{pmatrix} \times \begin{pmatrix} {\omega_{XC}}^2 \\ {\omega_{YC}}^2 \\ {\omega_{ZC}}^2 \end{pmatrix} \quad (19)$$

where:
a'_X, a'_Y, and a'_Z are the postcalibration accelerometer data.
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} are the scale and alignment correction factors.
a_X, a_Y, and a_Z are the precalibration accelerometer data.
b_X, b_Y, and b_Z are the bias correction factors.
0, p_{12}, p_{13}, p_{21}, p_{23}, p_{31}, and p_{32} are the point of percussion correction factors.
${\omega_{XC}}^2$, ${\omega_{YC}}^2$, and ${\omega_{ZC}}^2$ are the postcalibration gyroscope data (squared).

All the correction factors in each matrix and array are derived from direct observation of the response of each accelerometer to a variety of inertial test conditions at multiple temperatures across the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but they are not available for observation. Bit 6 in the CONFIG register provides an on and off control for the point of percussion alignment (see Table 90). See Figure 43 for more details on the user calibration options that are available for the accelerometers.

FILTERING

After calibration, the gyroscope and accelerometer data passes through a finite impulse response (FIR) filter that can either be enabled or disabled by the user. Next, the data is passed through a user-configurable decimation and averaging filter before being forwarded to the data registers (see Figure 23).

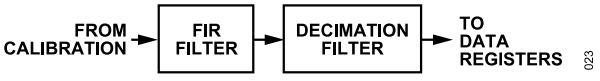

Figure 23. Inertial Sensor Filtering

The FIR filter is comprised a bank of coefficients that have of 120 taps each and has a default bandwidth of 100 Hz. Register CONFIG, Bit 2 and Bit 3, allow for the enabling or disabling of the accelerometer and gyroscope signals, respectively.

The FIR filter bank includes a preconfigured filter, but the user can design their own filters and write over these values using the register of each coefficient. For example, Table 118 provides the details for the COEFF_C70 register, which contains Coefficient 71. Refer to Figure 46 for the frequency response of the factory default filters. These filters do not represent any specific application environment; they are only examples.

The decimation filter averages multiple samples together to produce each register update. In this type of filter structure, the number of samples in the average is equal to the reduction in the update rate for the output data registers. See the DECIMATE register for the user controls for this filter (see Table 92).

REGISTER STRUCTURE

All communication with the ADIS16550 involves accessing its user registers. The register structure contains both output data and control registers. The output data registers include the latest sensor data, error flags, and identification data. The control registers include sample rate, filtering, calibration, and diagnostic configuration options. All communication between the ADIS16550 and an external processor involves either reading or writing to one of the user registers.

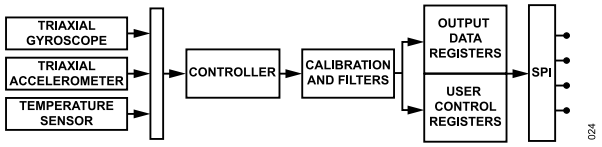

Figure 24. Basic Operation

The register structure uses a paged addressing scheme that contains 2 user-accessible pages, with each page containing 64 register locations. Each register is 32 bits wide, with each 16-bit register word having its own unique address within the memory map of that page. The SPI port has access to one page at a time, using the bit sequence in Figure 25. Select the page to activate for SPI access by writing its code to the PAGE_ID register. Read the PAGE_ID register to determine which page is currently active. Table 7 displays the PAGE_ID contents for each page and their basic functions. The PAGE_ID register is located at Address 0x00 on every page.

Table 7. User Register Page Assignments

Page	PAGE_ID	Function
0	0x00	Output data, clock, identification
1	0x01	FIR Filter Bank, Coefficient C0 to Coefficient C119

THEORY OF OPERATION

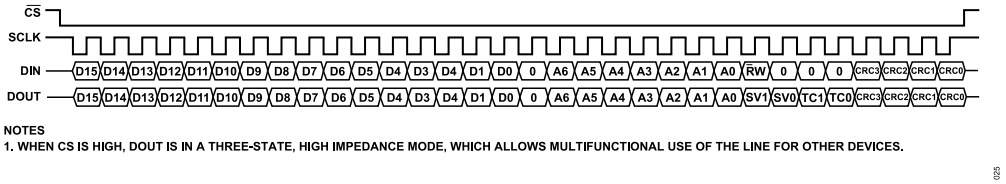

Figure 25. SPI Communication Bit Sequence

SERIAL PERIPHERAL INTERFACE

The SPI provides access to all of the user accessible registers (see Table 8) and typically connects to a compatible port on an embedded processor platform. See Figure 26 for a diagram that provides the most common connections between the ADIS16550 and an embedded processor.

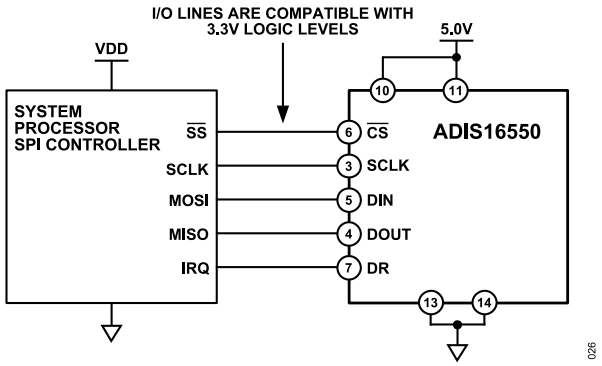

Figure 26. Electrical Connection Diagram

Table 8. Generic Controller Processor Pin Names and Functions

Mnemonic	Function
$\overline{SS}$	Subordinate select
IRQ	Interrupt request
MOSI	Controller output, subordinate input
MISO	Controller input, subordinate output
SCLK	Serial clock

Embedded processors typically use control registers to configure their serial ports for communicating with SPI subordinate devices such as the ADIS16550. Table 9 provides a list of settings that describe the SPI protocol of the ADIS16550. The initialization routine of the controller processor typically establishes these settings using firmware commands to write them into its serial control registers.

Table 9. Generic Controller Processor SPI Settings

Processor Setting	Description
Controller	ADIS16550 operates as subordinate
SCLK ≤ 15 MHz	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence, see Figure 25 for coding
32-Bit Mode	Shift register and data length

DATA READY

The ADIS16550 provides users with a data ready (DR) signal that pulses low when the output data registers are updating (see Figure 27). In this configuration, connect DR to an interrupt service pin on the embedded processor, which triggers data collection, when this signal pulses high.

Figure 27. Data Ready

During the start-up and reset recovery processes, the DR signal can exhibit some transient behavior before data production begins. Figure 28 provides an example of the DR behavior during startup, and Figure 29 and Figure 30 provide examples of the DR behavior during recovery from reset commands. Note that DR may toggle during the reset recover time after holding the $\overline{RST}$ pin low (Figure 30).

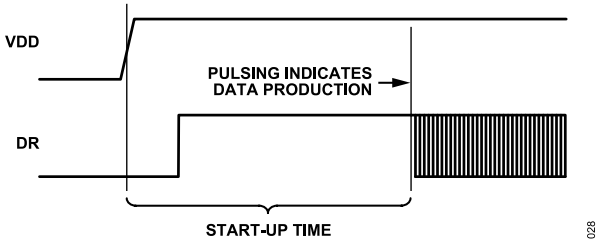

Figure 28. Data Ready Response During Startup

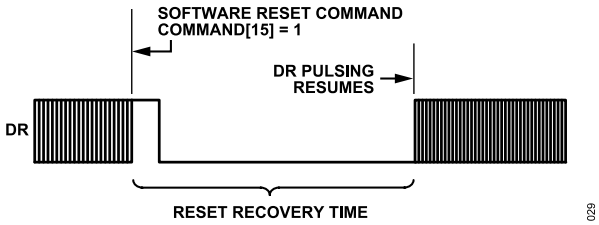

Figure 29. Data Ready Response During Reset (Register COMMAND, Bit 15 = 1) Recovery

THEORY OF OPERATION

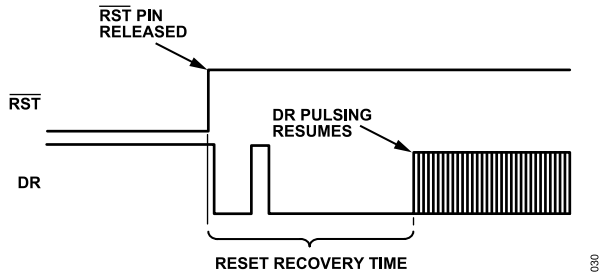

Figure 30. Data Ready Response During Reset (RST = 0) Recovery

READING SENSOR DATA

Reading a single register requires two 32-bit cycles on the SPI: one to request the contents of a register and another to receive those contents. The 32-bit command code (see Figure 25) for a read request on the SPI has five parts: the 16-bit data field is all zeros (because this is a read command), the 7-bit address code of the register to be read, the read bit ($\overline{R}/W$ = 0), four must be zero bits, and four cyclic redundancy check (CRC) bits. Figure 32 provides a generic example that includes two register reads in succession. This example shows that Response N is transmitted on DOUT one frame after Command N is issued on DIN. The sequence in Figure 32 also shows the full duplex mode of operation, which means that the ADIS16550 can receive requests on DIN while also transmitting data out on DOUT. Data bits are read on the rising SCLK edge, and the data bits are transitioned on the falling SCLK edge (see Figure 31). Clock phase and polarity are both equal to 1, meaning that data on the DOUT and DIN lines must be stable while the clock is high and can be changed when the clock is low.

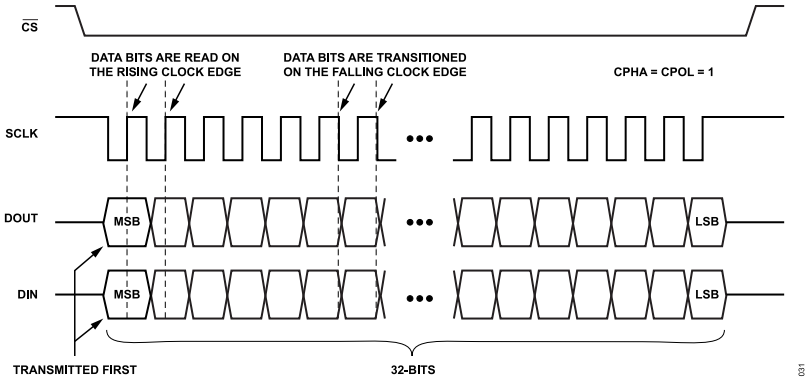

Figure 31. SPI Communication Structure

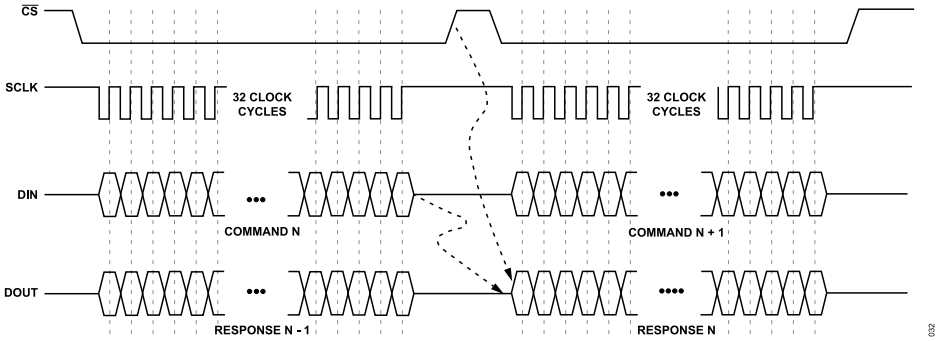

Figure 32. SPI Command and Response Format

SPI COMMUNICATION PROTOCOL

Table 10. SPI Signals

Signal	Symbol	Description
Serial Clock	SCLK	Exactly 32 clock cycles when $\overline{CS}$ is active
Chip Select	$\overline{CS}$	Active low
Controller Out/Subordinate In	MOSI/DIN	Data sent to the ADIS16550 from the main controller
Controller In/Subordinate Out	MISO/DOUT	Data sent to the main controller from the ADIS16550

Table 11. SPI Command Bits for Bits[31:16]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 12. SPI Command Bits for Bits[15:0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	A6	A5	A4	A3	A2	A1	A0	$\overline{R}$/W	0	0	0	CRC3	CRC2	CRC1	CRC0

Table 13. SPI Response Bits for Bits[31:16]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 14. SPI Response Bits for Bits[15:0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	A6	A5	A4	A3	A2	A1	A0	SV1	SV0	TC1	TC0	CRC3	CRC2	CRC1	CRC0

SPI COMMUNICATION PROTOCOL

SPI PROTOCOL IMPLEMENTATION

The ADIS16550 implements a generic read and write interface with only one command frame and one response frame. The SPI protocol uses a write 16 and read 16 format.

Write 16

For SPI writes, 16 bits of data are passed to the ADIS16550. The address field, A[6:0], specifies the exact register in which to write data. After writing the data, D[15:0], to the specified register, the ADIS16550 performs a readback of the register address, returning the data as the LSB of the 16-bit response data field, D[15:0]. By performing a readback of the written data, the ADIS16550 validates that the information is properly written to the register map and that no stuck at faults are present in the specified register.

The ADIS16550 uses 64, 32-bit registers with 128 addressable locations. Note that, partial register updates implemented by writing to a single address during the initialization mode can result in errant data within the output data registers. The output data does not recover until the full register update is completed by the writing of the second address associated with the register.

Read 16

For SPI reads issued by the controller device, the data field is ignored. The address field, A[6:0], specifies the exact register to be read. After sending the read command, the ADIS16550 sends a SPI response frame containing the data from the requested register address.

SPI PROTOCOL BIT FIELD DEFINITIONS

Table 15. DIN Command Bit Definitions

Bit Name	Position	Description	Definition
D[15:0]	31 … 16	Data field	Write command: contains the data to be written to the register specified in A[6:0].
0	15	Must be zero	Bit positions marked as 0 must contain a logical zero in the SPI command frame.
A[6:0]	14 … 8	Address field	Defines the address of the register from which data is read, or to which data is written.
$\overline{R}$/W	7	Read and/or write	Differentiates the DIN command as either read or write. 0: read. 1: write.
0	6 … 4	Must be zero	Bit positions marked as 0 must contain a logical zero in the SPI command frame. Any nonzero value placed in these positions results in an SPI error response.
CRC[3:0]	3 … 0	Cyclic redundancy check	4-bit CRC check. Polynomial: $x^4 + 1$. Seed value: 1010. Calculation order: MSB to LSB. The CRC calculation includes Bits[31:4] of the DIN command.

Table 16. DOUT Response Bit Definitions

Bit Name	Position	Description	Definition
D[15:0]	31 … 16	Data field	The 16-bit data field contains the data from the register addressed in Bits A[6:0] of the DIN command.
0	15	Zero	Must always be zero
A[6:0]	14 … 8	Address field	Contains the address associated with the data in D[15:0]. The system can compare this value to the address issued in the previous DIN command to ensure data integrity.
SV[1:0]	7, 6	State vector	Indicates the condition of the ADIS16550 at the time data is issued. 00: initialization phase. 01: run phase—device OK. 10: run phase—device NOK. 11: SPI error.
TC[1:0]	5, 4	Transaction counter	A 2-bit rollover counter that is incremented when the transmitted data is fresher than the previously transmitted data. See the Transaction Counter section for more information.
CRC[3:0]	3 … 0	Cyclic redundancy check	4-bit CRC check. Polynomial: $x^4 + 1$. Seed value: 1010. Calculation order: MSB to LSB. The CRC calculation includes Bits[31:4] of the DOUT response.

STATE VECTOR

The state vector is implemented as a method for communicating the state of the ADIS16550 as it relates to the data stored in D[15:0] of the DOUT response (see Table 16).

Precedence is assigned to the state vector values, in order, as follows:

1. SPI error.
2. Initialization.
3. Device NOK.
4. Device OK.

The initialization phase is the default state of the ADIS16550 at the conclusion of its POR routine. During the initialization phase, the controller device is capable of configuring the ADIS16550, as well as performing various ODST routines. Because these operations have the capability to affect the inertial data output, the ADIS16550 flags all transactions conducted during this phase with SV[1:0] = 00, unless a SPI error occurs, then SV[1:0] = 11. Inertial data acquired during the initialization phase must not be applied to any safety critical applications.

The ADIS16550 transitions to its run phase after the WRITE_LOCK bit is set in the Command register (Address 0x50 and Address 0x51); this represents the steady state operational phase of the ADIS16550. Data obtained during this phase can be fully applied to any system algorithms.

If a fault is present and detected in the ADIS16550, the state vector transitions to SV[1:0] = 10.

TRANSACTION COUNTER

A 2-bit transaction counter increments according to the following two criteria:

SPI PROTOCOL BIT FIELD DEFINITIONS

- The transmitted inertial data is fresh, meaning it occurs later than the previous DOUT response.
- A previous SPI transaction has been executed.

By linking these two events, the transaction counter provides coverage for two unique scenarios. First, linkage to the ADIS16550 internal clock oscillator is achieved through this implementation. Faults that can result in the output data registers becoming frozen are immediately identified by the system because TC[1:0] (the transaction counter (TC) value) ceases to increment. Second, inadvertent SPI commands cause unexpected increments to the TC[1:0] value that is also immediately detected at the system level.

Figure 33 shows the behavior of the transaction counter when the $\overline{CS}$ rate is appreciably fast relative to the data update rate. It is important to note that inertial data is latched on the rising edge of the $\overline{CS}$ pin. Figure 33 shows that the transaction counter does not increment until the rising edge of $\overline{CS}$ occurs after a new data update event occurs so that the next sequential response contains the fresh sample of data.

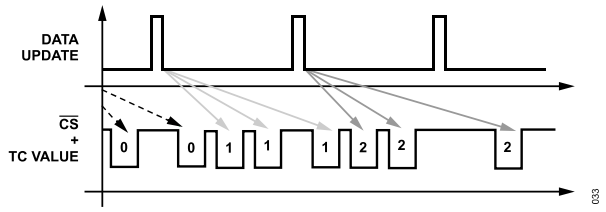

Figure 33. TC—Fast $\overline{CS}$ Rate

The behavior presented in Figure 34 is expected for systems where the $\overline{CS}$ rate is much slower than the data update rate. As each rising edge of the $\overline{CS}$ signal occurs after an internal data update event, the transaction counter updates sequentially with every new SPI exchange.

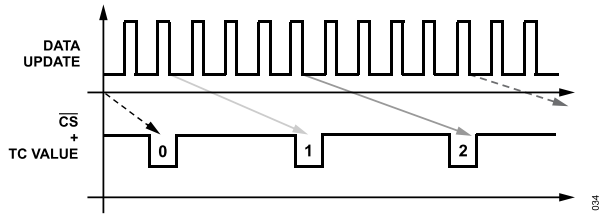

Figure 34. TC—Slow $\overline{CS}$ Rate

SPI errors do not affect the behaviors shown in Figure 33 and Figure 34. Although the SPI command payload is not valid, the rising edge of $\overline{CS}$ is still used to latch new data into the SPI output registers. If fresh data is latched during this event, the transaction counter updates accordingly. Inadvertent blips on the $\overline{CS}$ line are detected because these blips may induce an increment to the transaction counter.

SPI CRC

A 4-bit CRC must be calculated for all DIN commands sent to the ADIS16550. If the CRC is not properly calculated in the DIN command, the resulting DOUT response indicates an SPI error (SV[1:0] = 11), and the write command is blocked. The CRC is necessary to ensure the integrity of the command received by the ADIS16550.

The DOUT response also contains a 4-bit CRC calculated with the same polynomial and seed value used for the DIN command. For safety critical applications, it is strongly recommended that the controller device validate the DOUT CRC before applying the inertial data to any system level algorithms.

CRC IMPLEMENTATION IN LABVIEW

Use the following virtual interface (VI) to calculate the SPI CRC in the LabVIEW® programming environment. The VI provides a visual representation of the CRC calculation and is architected as follows, with the numbering of the steps correlating to the numerical labels in Figure 35:

1. The input to the VI is a 32-bit unsigned integer that represents the SPI word intended for transmission.
   a. Bits[31:4] contain the intended payload.
   b. Bits[3:0] contain zeroes in the CRC positions.
2. The 32-bit integer is converted to a Boolean array. A Boolean array is a binary representation of an integer value.
3. The 4 LSB from the Boolean array are stripped off, leaving just the SPI message payload, Bits[31:4].
4. The array is reversed such that the calculation is performed MSB to LSB.
5. The CRC calculation is iterated through the 28-bit array.
   a. The initialization value of 1010 is achieved by passing true and false constants into the for loop.
   b. Shift registers iterate the calculation, passing the result from one calculation to the input of the next.
   c. The for loop ends when the 28^{TH} bit of the SPI Boolean array is iterated through the for loop.
6. The four individual bits of the CRC are grouped into an array.
7. The array order is reversed such that proper order is achieved.
   a. CRC0 must be at Position 0 of the array.
8. The CRC Boolean array is converted to an integer value.
9. The CRC is output by the VI and can then be appended to the DIN/DOUT SPI frame.

SPI PROTOCOL BIT FIELD DEFINITIONS

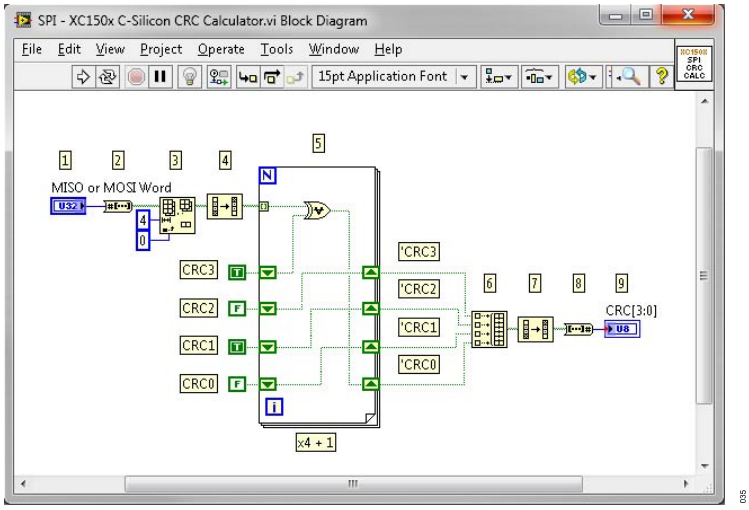

Figure 35. LabVIEW CRC Calculation (Block Diagram)

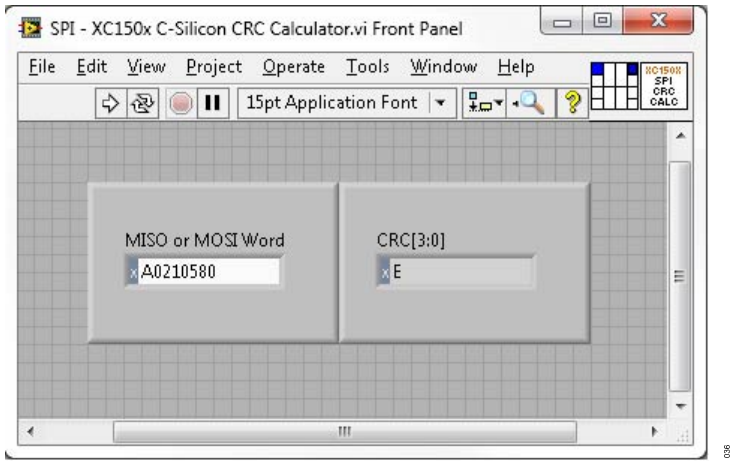

Figure 36. LabVIEW CRC Calculation Example (Front Panel)

SPI PROTOCOL BIT FIELD DEFINITIONS

CRC IMPLEMENTATION IN C CODE

Use the following C code to calculate the SPI CRC. The *MakeCRC function passes a char value representing the 28 MSBs of the DOUT or DIN command. This value passes such that BitString[0] represents the LSB of the SPI frame (Bit 4). The function performs a bitwise calculation of the SPI CRC and returns this value to the main function.

```
// ========================================================================
// CRC Generation Unit - Linear Feedback Shift Register implementation
// (c) Kay Gorontzi, GHSi.de, distributed under the terms of LGPL
// ========================================================================
char *MakeCRC(char *BitString)
   {
   static char Res[5];                                 // CRC Result array
   char CRC[4];                                        // CRC array
   int  i;                                             // generic counting variable
   char DoInvert;

   CRC[0] = 0;                                          // Init before calculation
   CRC[1] = 1;                                          // Init before calculation
   CRC[2] = 0;                                          // Init before calculation
   CRC[3] = 1;                                          // Init before calculation

   for (i=0; i<strlen(BitString); ++i)
      {
      DoInvert = ('1'==BitString[i]) ^ CRC[3];           // XOR required
      CRC[3] = CRC[2];                                  // shift CRC[2] to CRC[3]
      CRC[2] = CRC[1];                                  // shift CRC[1] to CRC[2]
      CRC[1] = CRC[0];                                  // shift CRC[0] to CRC[1]
      CRC[0] = DoInvert;                                // CRC[0] set to the result of DoInvert
operation
      }

   for (i=0; i<4; ++i)  Res[3-i] = CRC[i] ? '1': '0';   // Convert binary to ASCII
   Res[4] = 0;                                          // Set string terminator

   return(Res);
   }
```

SPI FEATURES

BURST READ FUNCTION

The burst read function (BRF) provides a method for reading a batch of data (data counter, status, temperature, gyroscopes and accelerometers or delta angle and delta velocity, timestamp, and CRC code), which does not require a stall time between each 32-bit segment and only requires a single SPI transaction to initiate. This mode ensures that all data is from the same sampling time. A burst read can be completed at any time by sending a burst command on DIN. The ADIS16550 provides a burst response in the next DOUT frame (see Figure 5). The burst response contains 12 segments as shown in Table 17. The burst command for inertial data is a read command of Address 0x0A (0x00000A00).

System processors can execute burst mode by taking the following steps (see Figure 5):

1. Send a burst read command (0x00000A00)
2. Bring $\overline{CS}$ high for at least t_{STALL}.
3. Send a valid SPI command (for example, burst read command) and continue to clock the device while holding the $\overline{CS}$ line in a low state until all 12, 32-bit data-words are received (see Table 17). If the $\overline{CS}$ line goes high before the completion of all data acquisitions, the data from that read request is lost.

The BRF can also allow for the reading of delta angle and delta velocity data instead of the gyroscope and accelerometer data, respectively. The burst command for integrated data is a read command of Address 0x0B (0x00000B01). The system processor executes this mode by reading each segment of data in the burst response (see Table 18), with all remaining controls remaining the same as previously noted.

Table 17. BRF Data Format—Inertial Data

Segment	DIN	DOUT
0	BURST	HEADER
1	Not applicable	DATA_CNT
2	Not applicable	STATUS
3	Not applicable	TEMP
4	Not applicable	X_GYRO
5	Not applicable	Y_GYRO
6	Not applicable	Z_GYRO
7	Not applicable	X_ACCL
8	Not applicable	Y_ACCL
9	Not applicable	Z_ACCL
10	Not applicable	TIMESTAMP
11	Not applicable	CRC

Table 18. BRF Data Format—Integrated Data

Segment	DIN	DOUT
0	BURST	HEADER
1	Not applicable	DATA_CNT
2	Not applicable	STATUS
3	Not applicable	TEMP
4	Not applicable	X_DELTANG
5	Not applicable	Y_DELTANG
6	Not applicable	Z_DELTANG
7	Not applicable	X_DELTVEL
8	Not applicable	Y_DELTVEL
9	Not applicable	Z_DELTVEL
10	Not applicable	TIMESTAMP
11	Not applicable	CRC

DEVICE CONFIGURATION

Each register contains 32 bits (four bytes). Bits[31:16] contain the upper two bytes, and Bits[15:0] contain the lower two bytes. The upper word and the lower word have their own unique address in the user register map (see Table 21). There are four parts to coding a SPI command (see Figure 25), which writes a new two bytes of data to a register: The new 16-bit data for that location, the 7-bit address code for register this command is updating, the write bit ($\overline{R}/W$ = 1), and the CRC value.

DUAL MEMORY STRUCTURE

The ADIS16550 uses a dual memory structure (see Figure 37), with static random access memory (SRAM) supporting high speed, real-time operation and flash memory providing nonvolatile storage of operational code, calibration coefficients, and user-configurable register settings. Two copies of this data reside in flash memory for redundancy and error recovery. The boot and initialization processes copy data from flash memory into the SRAM.

The manual flash update command provides a single-command method for storing user configuration settings into flash memory for automatic recall during the next power-on or reset recovery process. The flash memory has two independent blocks that act as copies of the stored data. During initialization, the ADIS16550 transfers the more recent copy of the configuration data from flash memory into SRAM if the CRC matches; otherwise, it transfers the alternate copy. Table 21 provides a memory map for the user registers in the ADIS16550, which includes a flash backup support (indicated by yes or no in the flash column).

During power-on or reset recovery, the ADIS16550 performs a CRC on both copies of the operational code stored in flash memory. The boot memory failure bit of the status register is set if either copy contains a CRC mismatch. If the first copy contains an error, the ADIS16550 reboots from the second copy.

SPI FEATURES

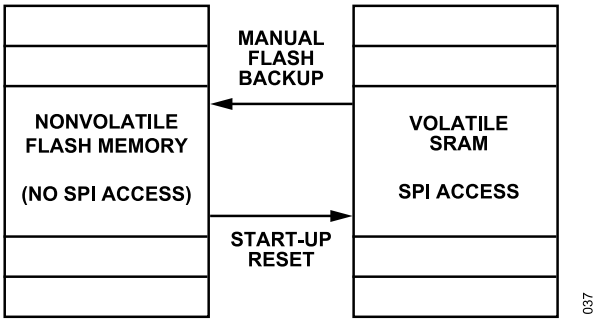

Figure 37. SRAM and Flash Memory Diagram

CRC32 CODING EXAMPLE

This section contains sample code and values for computing the CRC for the ADIS16550 register readback values.

In this coding example, the 32-bit CRC is first initialized with 0xFFFFFFFF. Next, each 16-bit word passes through the CRC computation in ascending order. Finally, the CRC is Xor'ed with 0xFFFFFFFF.

The ADIS16550 updates the CRC value for each data ready cycle. The registers listed in Table 19 are used as inputs for computing the CRC32 checksum. The registers can either be read individually in normal SPI mode or in burst mode, provided that all registers are all read during the same data ready cycle. The information in Table 19 is contained in the array data in the coding example.

Table 19. Sample Input Data for CRC Computation

Burst Word Number	Register	Input Value
0	Header	0x00000A55
1	DATA_CNT	0x00009361
2	Status	0x00000000
3	TEMP	0x0000F944
4	X_GYRO	0x00033272
5	Y_GYRO	0x0003BA86
6	Z_GYRO	0x000203AB
7	X_ACCL	0x00062482
8	Y_ACCL	0x001167C4
9	Z_ACCL	0x06196468
10	TIMESTAMP	0x00000000
11	BURST_CRC	0x6C0F3DE3

The BURST_CRC value is calculated on Burst Word 1 through Burst Word 10. The burst header response is treated as a regular SPI response. The header includes the address, state vector, transaction counter, and 4-bit CRC just like a single SPI response.

The subsequent 10 words contain the full 32-bit data from the corresponding register. The transaction counter does not increment during the burst read because the data reads come from the same point in time.

Based on the input shown in Table 19, the calculated 32-bit CRC is 0x6C0F3DE3.

The crc32_block function accepts an array of 32-bit numbers and computes the CRC byte-by-byte:

```
#include <stdio.h>
#include <stdlib.h>

unsigned long crc32_block(unsigned long crc, unsigned long data[], unsigned long crc_tab32[], int n)
{
  unsigned long long_c;
  int i;

  // cycle through memory
  for (i=0; i<n; i++)
    {
      // Get lowest byte
      long_c = 0x000000FF & (unsigned long)data[i];
      // Process with CRC
      crc = ((crc>>8) & 0x00FFFFFF) ^ crc_tab32[(crc^long_c) & 0xFF];
      // Get lower byte
      long_c = (0x000000FF & ((unsigned long)data[i]>>8));
      // Process with CRC
      crc = ((crc>>8) & 0x00FFFFFF) ^ crc_tab32[(crc^long_c)&0xFF];
      // Get upper byte
      long_c = (0x000000FF & ((unsigned long)data[i]>>16));
      // Process with CRC
      crc = ((crc>>8) & 0x00FFFFFF) ^ crc_tab32[(crc^long_c)&0xFF];
      // Get highest byte
      long_c = (0x000000FF & ((unsigned long)data[i]>>24));
      // Process with CRC
      crc = ((crc>>8) & 0x00FFFFFF) ^ crc_tab32[(crc^long_c)&0xFF];
    }
    return crc;
}
```

CRC32 CODING EXAMPLE

The main CRC function calculates the CRC table and uses this to find the 32-bit CRC value for the burst read data:

```
int main(void) {

  int arraysize = 10;
  int i, j;
  // example data from ADIS16550 burst read
  unsigned long data[10] =
     {0x00009361, 0x00000000, 0x0000F944, 0x00033272, 0x0003BA86,
      0x000203AB, 0x00062482, 0x001167C4, 0x06196468, 0x00000000};

  // Initialize CRC32 table
  int n = 256;
  unsigned long crc_i;
  unsigned long P_32;
  unsigned long crc_tab32[n];

  // CRC32 polynomial defined by IEEE-802.3
  P_32 = 0xEDB88320;

  // 8 bits require 256 entries in Table
  for (i=0; i<n; i++)
    {
    // start with table entry number
    crc_i = (unsigned long)i;

    // cycle through all bits in entry number
    for (j=0; j<8; j++)
    {
      // LSBit set?
      if ((crc_i & (unsigned long)0x00000001) != (unsigned long)0)
        {
         // process for bit set
         crc_i = (crc_i>>1) ^ P_32;
        }
      else
        {
          // process for bit clear
          crc_i = (crc_i>>1);
        }
    }
      // Store calculated value into table
      crc_tab32[i] = crc_i;
      }

  // Initialize CRC with seed value
  unsigned long crc = 0xFFFFFFFF;

  // Compute CRC in the order of bytes low-high
  // starting at 1-10, DATA_CNT, STATUS, ..., TIMESTAMP
  crc = crc32_block(crc, data, crc_tab32, arraysize);

  // Final operation per IEEE-802.3
  crc ^= 0xFFFFFFFF;
  printf("\nThe value of BURST_CRC is:
         0x%lx\n",crc);
```

CRC32 CODING EXAMPLE

```
  printf("Press any key to exit...");
  getchar();

  return EXIT_SUCCESS;
}
```

SPI INITIALIZATION SEQUENCE

The ADIS16550 performs self test diagnostics automatically as part of the boot process. Table 20 provides the recommended initialization sequence of commands to be provided by the user. A 500 ms wait time must be observed by the user after VDD reaches 5 V. Following this, a series of reads must be performed to determine device health and part identification information and to perform any configuration writes. Once the configuration is complete, the user must send the write lock command (0x00015086), which transitions the device from initialization mode into run mode. No further configuration writes can be made once the ADIS16550 is in run mode.

Table 20. Recommended Initialization Sequence

Sequence Step	Command (N)	Response (N + 1)	Time (ms)	Description
Reset	Not applicable	Not applicable	0	Apply 5 V to VDD to start the boot process.
Wait 500 ms	Not applicable	Not applicable	500	Wait for the firmware boot and initial the self test process to complete.
Read Status Lower 16 Bits	0x00000E04	0x00000E15	500	Lower half of the STATUS diagnostic flags register and is 0x0000 following an IMU reset.
Read Status Upper 16 Bits	0x00000F05	0x00000F27	500	Upper half of the STATUS diagnostic flags register and is 0x0000 following an IMU reset.
Read LOT_NUM Lower 16 Bits	0x00007409	Varies	501	Lower half of the lot number register. Value varies from lot to lot.
Read LOT_NUM Upper 16 Bits	0x00007508	Varies	501	Upper half of the lot number register. Value varies from lot to lot.
Read SER_NUM Lower 16 Bits	0x0000760B	Varies	502	Lower half of the serial number register. Value varies from device to device.
Read SER_NUM Upper 16 Bits	0x0000770A	Varies	502	Upper half of the serial number register. Value varies from device to device.
Read PROC_REV Lower 16 Bits	0x00007805	Varies	503	Lower half of the processor revision register. Upper 16 bits are unused.
Read FW_REV Lower 16 Bits	0x00007A07	Varies	503	Lower half of the firmware revision register. Upper 16 bits are unused.
Read FW_DATE Lower 16 Bits	0x00007C01	Varies	504	Lower half of the firmware date register.
Read FW_DATE Upper 16 Bits	0x00007D00	Varies	504	Upper half of the firmware date register.
Read PROD_ID Lower 16 Bits	0x00007E03	0x40A67E38	505	Lower half of the product ID register and is 0x40A6 (16,550). Upper 16 bits are unused.
Perform Any IMU Configuration	Not applicable	Not applicable	505	Perform any additional desired configuration (enable filtering, adjust scale/bias, external sync, etc.) here.
Run Write Lock Command	0x00015086	0x0000500F	506	Locks the IMU configuration registers and moves to run mode. Requires reset to return to initialization mode.
Read IMU Data	Not applicable	Not applicable	507	IMU data can be read using a burst read or via the sensor output registers.

USER REGISTER MEMORY MAP

In Table 21, N/A means not applicable.

Table 21. User Register Memory Map

Register Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
PAGE_ID	R/W	No	0x00	0x00, 0x01	0x00000000	Page identifier
Reserved	N/A	N/A	0x00	0x02 to 0x09	N/A	Reserved
BURST_RD	R	No	0x00	0x0A, 0x0B	N/A	Burst read configuration
DATA_CNT	R	No	0x00	0x0C, 0x0D	N/A	Data counter
STATUS	R	No	0x00	0x0E, 0x0F	N/A	Status flags indicating device health
TEMP	R	No	0x00	0x10, 0x11	N/A	Output, temperature
X_GYRO	R	No	0x00	0x12, 0x13	N/A	Output, x-axis gyroscope
Y_GYRO	R	No	0x00	0x14, 0x15	N/A	Output, y-axis gyroscope
Z_GYRO	R	No	0x00	0x16, 0x17	N/A	Output, z-axis gyroscope
X_ACCL	R	No	0x00	0x18, 0x19	N/A	Output, x-axis accelerometer
Y_ACCL	R	No	0x00	0x1A, 0x1B	N/A	Output, y-axis accelerometer
Z_ACCL	R	No	0x00	0x1C, 0x1D	N/A	Output, z-axis accelerometer
X_DELTANG	R	No	0x00	0x1E, 0x1F	N/A	Output, x-axis delta angle
Y_DELTANG	R	No	0x00	0x20, 0x21	N/A	Output, y-axis delta angle
Z_DELTANG	R	No	0x00	0x22, 0x23	N/A	Output, z-axis delta angle
X_DELTVEL	R	No	0x00	0x24, 0x25	N/A	Output, x-axis delta velocity
Y_DELTVEL	R	No	0x00	0x26, 0x27	N/A	Output, y-axis delta velocity
Z_DELTVEL	R	No	0x00	0x28, 0x29	N/A	Output, z-axis delta velocity
TIMESTAMP	R	No	0x00	0x2A, 0x2B	N/A	Output, timestamp
Reserved	N/A	N/A	0x00	0x2C to 0x2F	N/A	Reserved
X_GYRO_SCALE	R/W	Yes	0x00	0x30, 0x31	0x00000000	Calibration, scale, x-axis gyroscope
Y_GYRO_SCALE	R/W	Yes	0x00	0x32, 0x33	0x00000000	Calibration, scale, y-axis gyroscope
Z_GYRO_SCALE	R/W	Yes	0x00	0x34, 0x35	0x00000000	Calibration, scale, z-axis gyroscope
X_ACCL_SCALE	R/W	Yes	0x00	0x36, 0x37	0x00000000	Calibration, scale, x-axis accelerometer
Y_ACCL_SCALE	R/W	Yes	0x00	0x38, 0x39	0x00000000	Calibration, scale, y-axis accelerometer
Z_ACCL_SCALE	R/W	Yes	0x00	0x3A, 0x3B	0x00000000	Calibration, scale, z-axis accelerometer
Reserved	N/A	N/A	0x00	0x3C to 0x3F	N/A	Reserved
X_GYRO_BIAS	R/W	Yes	0x00	0x40, 0x41	0x00000000	Calibration, bias, x-axis gyroscope
Y_GYRO_BIAS	R/W	Yes	0x00	0x42, 0x43	0x00000000	Calibration, bias, y-axis gyroscope
Z_GYRO_BIAS	R/W	Yes	0x00	0x44, 0x45	0x00000000	Calibration, bias, z-axis gyroscope
X_ACCL_BIAS	R/W	Yes	0x00	0x46, 0x47	0x00000000	Calibration, bias, x-axis accelerometer
Y_ACCL_BIAS	R/W	Yes	0x00	0x48, 0x49	0x00000000	Calibration, bias, y-axis accelerometer
Z_ACCL_BIAS	R/W	Yes	0x00	0x4A, 0x4B	0x00000000	Calibration, bias, z-axis accelerometer
Reserved	N/A	N/A	0x00	0x4C to 0x51	N/A	Reserved
COMMAND	W	No	0x00	0x50, 0x51	N/A	Control, system level commands
CONFIG	R/W	Yes	0x00	0x52, 0x53	0x00000000	Control, miscellaneous correction
DECIMATE	R/W	Yes	0x00	0x54, 0x55	0x00000000	Control, output sample rate decimation
SYNC_SCALE	R/W	Yes	0x00	0x56, 0x57	0x00000FA0	Control, input clock scaling (scaled sync mode)
Reserved	N/A	N/A	0x00	0x5A to 0x5F	N/A	Reserved
USER_SCR1	R/W	Yes	0x00	0x60, 0x61	0x00000000	User Scratch Register 1
USER_SCR2	R/W	Yes	0x00	0x62, 0x63	0x00000000	User Scratch Register 2
USER_SCR3	R/W	Yes	0x00	0x64, 0x65	0x00000000	User Scratch Register 3
USER_SCR4	R/W	Yes	0x00	0x66, 0x67	0x00000000	User Scratch Register 4
Reserved	N/A	N/A	0x00	0x68 to 0x71	N/A	Reserved
ENDURANCE	R	N/A	0x00	0x72, 0x73	N/A	Endurance
LOT_NUM	R	N/A	0x00	0x74, 0x75	N/A	Lot number

USER REGISTER MEMORY MAP

Table 21. User Register Memory Map (Continued)

Register Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
SER_NUM	R	N/A	0x00	0x76, 0x77	N/A	Serial number
PROC_REV	R	N/A	0x00	0x78, 0x79	N/A	Digital signal processor (DSP) revision
FW_REV	R	N/A	0x00	0x7A, 0x7B	N/A	Firmware revision
FW_DATE	R	N/A	0x00	0x7C, 0x7D	N/A	Firmware programming date
PROD_ID	R	N/A	0x00	0x7E, 0x7F	0x000040A6	Output, product identification (16,550)
PAGE_ID	R/W	No	0x01	0x00, 0x01	0x00000000	Page identifier
Reserved	N/A	N/A	0x01	0x02 to 0x07	N/A	Reserved
COEFF_C0 to COEFF_C1	R/W	Yes	0x01	0x08, 0x09	N/A	FIR Filter Coefficient C0 and Filter Coefficient C1
COEFF_C2 to COEFF_C117	R/W	Yes	0x01	0x0A to 0x7C	N/A	FIR Filter Coefficient C2 through Filter Coefficient C117
COEFF_C118 to COEFF_C119	R/W	Yes	0x01	0x7D, 0x7E	N/A	FIR Filter Coefficient C118 and Filter Coefficient C119

USER REGISTER DEFINTIONS

PAGE NUMBER (PAGE_ID)

The contents in the PAGE_ID register (see Table 22 and Table 23) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x00000082 to select Page 0 to access most user configuration settings. See Table 21 for the page assignments associated with each user accessible register.

Table 22. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x00, 0x01	0x00000000	R/W	No

Table 23. PAGE_ID Bit Descriptions

Bits	Description
[31:4]	Reserved
[3:0]	Page number, binary numerical format

BURST READ CONFIGURATION (BURST_RD)

The BURST_RD register is used to configure the burst mode. The ADIS16550 responds to a read of Register 0x0A with an inertial data burst response (accelerometer and gyroscope data), it responds to a read of Register 0x0B with an integrated data burst response (delta velocity and delta angle). See Table 17, Table 18, and Figure 5 for more information on the BRF function.

Table 24. BURST_RD Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x0A, 0x0B	Not applicable	R	No

DATA AND SAMPLE COUNTER (DATA_CNT)

The DATA_CNT register (see Table 25 and Table 26) is a continuous, real-time, sample counter. This register starts at 0x00000000, increments every time the output data registers update, and wraps around from 0xFFFF (65,535 decimal) to 0x00000000 (0 decimal).

Table 25. DATA_CNT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0C, 0x0D	Not applicable	R	No

Table 26. DATA_CNT Bit Descriptions

Bits	Description
[31:16]	Reserved
[15:0]	Data counter, binary format

STATUS FLAGS (STATUS)

The STATUS register (see Table 27 and Table 28) provides various error flags. Reading this register causes all of its bits to return to 0, except for sticky bits. Bit 2, Bit 7, Bit 9, and Bit 11 are sticky and remain high as long as the error state persists. All other bits automatically reassert once an error condition occurs.

Table 27. STATUS Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0E, 0x0F	0x00000000	R	No

Table 28. STATUS Bit Descriptions

Bits	Description
31	Internal Regulator Error. Used to signal an error with the internal regulated supply voltage.
30	Internal Sensor Supply Error. Used to signal an error with the power supply to one or more of the internal inertial sensors.
29	External 5 V Supply Error. Used to signal an error with the 5 V power supply.
28	Internal Processor Supply Error. Used to signal an error with the power supply to the internal microcontroller.
[27:26]	Z-Axis Accelerometer Error. Used to determine which specific sensor and axis resulted in the sensor error bit being set.
[25:24]	Y-Axis Accelerometer Error. Used to determine which specific sensor and axis resulted in the sensor error bit being set.
[23:22]	X-Axis Accelerometer Error. Used to determine which specific sensor and axis resulted in the sensor error bit being set.
[21:20]	Z-Axis Gyroscope Error. Used to determine which specific sensor and axis resulted in the sensor error bit being set.
[19:18]	Y-Axis Gyroscope Error. Used to determine which specific sensor and axis resulted in the sensor error bit being set.
[17:16]	X-Axis Gyroscope Error. Used to determine which specific sensor and axis resulted in the sensor error bit being set.
15	Watchdog Timer Flag. A 1 indicates that the ADIS16550 automatically resets itself to clear an issue. A 0 indicates a normal operating condition. Note that a hardware reset is required to clear this flag.
[14:12]	Reserved.
11	Register NVM Error. A 1 indicates that unrecoverable data loss occurred in the NVM. A 0 indicates a normal operating condition.
10	Sync Unlock Error. A 1 indicates one or more of the following occurred when operating in scaled sync mode: ▶ The input sync frequency is outside the allowable range (1 Hz to 128 Hz). ▶ SYNC_SCALE is out of range (3000 Hz to 4500 Hz). ▶ The sample timing is not scaling correctly (phase error). ▶ The sync edge is not detected. A 0 indicates a normal operating condition.
9	Boot Memory Failure. A 1 indicates that the boot is from backup copy (replacement advised). A 0 indicates a normal operating condition.
8	Power Supply Failure. A 1 indicates an error condition for either the internal or external power supplies. A 0 indicates a normal operating condition.
7	Processing Overrun Error. A 1 indicates that data sampling has outpaced the ability of the unit to properly process data, and thus, the signal chain is corrupted. This error requires a reset to properly recover. A 0 indicates a normal operating condition.
6	SPI Communication Error. A 1 indicates that a SPI communication error occurred. A 0 indicates a normal operating condition.
5	Temperature Error. A 1 indicates an error condition with the internal temperature sensors. A 0 indicates a normal operating condition.
4	Sensor Error. A 1 indicates a sensor error. A 0 indicates a normal operating condition.

USER REGISTER DEFINTIONS

Table 28. STATUS Bit Descriptions (Continued)

Bits	Description
3	Overrange for Inertial Signals. A 1 indicates that an overrange event occurred. A 0 indicates a normal operating condition.
2	Flash Update Error. A 1 indicates an error while issuing a flash command or corruption of a single copy of the registers in the flash memory. A 0 indicates a normal operating condition.
1	Configuration and/or Calibration CRC Error. A 1 indicates that an error occurred within the configuration CRC or calibration CRC. A 0 indicates a normal operating condition.
0	Code CRC Error. A 1 indicates the calculated CRC of the code loaded in the SRAM does not match the CRC value stored during factory programming. A 0 indicates a normal operating condition.

INTERNAL TEMPERATURE (TEMP)

The TEMP register (see Table 29 and Table 30) provides a coarse measurement of the temperature inside of the ADIS16550. This data is useful for monitoring relative changes in the thermal environment. Table 31 provides several examples of the data format for the TEMP register.

Table 29. TEMP Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x10, 0x11	Not applicable	R	No

Table 30. TEMP Bit Descriptions

Bits	Description
[31:25]	Reserved.
24	Accelerometer temperature flag for z-axis and x-axis. This flag indicates an error with a temperature sensor that affects the z-axis and x-axis accelerometer channels.
23	Accelerometer temperature Flag for y-axis and z-axis. This flag indicates an error with a temperature sensor that affects the y-axis and z-axis accelerometer channels.
22	Accelerometer temperature flag for x-axis and y-axis. This flag indicates an error with a temperature sensor that affects the x-axis and y-axis accelerometer channels.
21	Gyroscope Temperature Flag 2 for z-axis. This flag indicates an error with a temperature sensor that affects the z-axis gyroscope channel.
20	Gyroscope Temperature Flag 1 for z-axis. This flag indicates an error with a temperature sensor that affects the z-axis gyroscope channel.
19	Gyroscope Temperature Flag 2 for y-axis. This flag indicates an error with a temperature sensor that affects the y-axis gyroscope channel.
18	Gyroscope Temperature Flag 1 for y-axis. This flag indicates an error with a temperature sensor that affects the y-axis gyroscope channel.
17	Gyroscope Temperature Flag 2 for x-axis. This flag indicates an error with a temperature sensor that affects the x-axis gyroscope channel.
16	Gyroscope Temperature Flag 1 for x-axis. This flag indicates an error with a temperature sensor that affects the x-axis gyroscope channel.
[15:0]	Temperature data; twos complement, 1°C per 250 LSB, 25°C = 0x00000000.

Table 31. TEMP Data Format Examples

Temperature (°C)	Decimal	Hexadecimal	Binary
+105	+20,000	0x4E20	0100 1110 0010 0000
+85	+15,000	0x3A98	0011 1010 1001 1000
+26	+250	0x00FA	0000 0000 1111 1010
+25	0	0x00000000	0000 0000 0000 0000
+24	−250	0xFF06	1111 1111 0000 0110
0	-6250	0xE796	1110 0111 1001 0110
−40	−16,250	0xC086	1100 0000 1000 0110

GYROSCOPE DATA

The gyroscopes in the ADIS16550 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 38 shows the orientation of each gyroscope axis, which defines the direction of rotation that produces a positive response in each of the angular rate measurements.

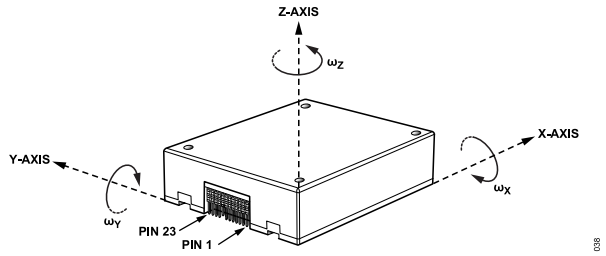

Figure 38. Gyroscope Axis and Polarity Assignments

Each gyroscope outputs 32-bit data in twos complement format split into an upper and lower register. The full 32-bit data-word can be retrieved by using a burst read to ensure that the upper and lower words are sampled at the same point in time.

Gyroscope Measurement Range and Scale Factor

Table 32 provides the range and scale factor (K_G) for the angular rate (gyroscope) measurements in each ADIS16550 model.

Table 32. Gyroscope Measurement Range and Scale Factors

Model	Range	K_G
ADIS16550	±300°/sec	For 16 bit, 80 LSB/°/sec, and for 32 bit, 5242880 LSB/°/sec

Gyroscope Resolution

Although 32-bit resolution is available, 16-bit mode is most commonly used because each DOUT response contains 16 bits of sensor data. Table 33 offers various numerical examples that demonstrate the format of the rotation rate data.

Table 33. 16-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hexadecimal	Binary
+409.5875[1]	+32,767	0x7FFF	0111 1111 1111 1111
+300	+24,000	0x5DC0	0101 1101 1100 0000
+1	+80	0x0050	0000 0000 0101 0000

USER REGISTER DEFINTIONS

Table 33. 16-Bit Gyroscope Data Format Examples (Continued)

Rotation Rate (°/sec)	Decimal	Hexadecimal	Binary
0	0	0x00000000	0000 0000 0000 0000
−1	−80	0xFFB0	1111 1111 1011 0000
−300	−24,000	0xA240	1010 0010 0100 0000
−409.6[1]	−32,768	0x8000	1000 0000 0000 0000

[1] The electrical clipping level of each gyroscope axis is ±409.6°/sec. The ADIS16550 is only guaranteed to remain within specification up to ±300°/sec as stated in Table 1.

X-Axis Gyroscope (X_GYRO)

The X_GYRO (see Table 34 and Table 35) register contains the gyroscope data for the x-axis.

Table 34. X_GYRO Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x12, 0x13	Not applicable	R	No

Table 35. X_GYRO Bit Descriptions

Bits	Description
[31:16]	X-axis gyroscope data (16-bit resolution); twos complement, 0°/sec = 0x00000000, see Table 32 for the scale factor
[15:0]	Lower 16 bits to achieve 32-bit resolution

Y-Axis Gyroscope (Y_GYRO)

The Y_GYRO (see Table 36 and Table 37) register contains the gyroscope data for the y-axis.

Table 36. Y_GYRO Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x14, 0x15	Not applicable	R	No

Table 37. Y_GYRO Bit Descriptions

Bits	Description
[31:16]	Y-axis gyroscope data (16-bit resolution); twos complement, 0°/sec = 0x00000000, see Table 32 for the scale factor
[15:0]	Lower 16 bits to achieve 32-bit resolution

Z-Axis Gyroscope (Z_GYRO)

The Z_GYRO (see Table 38 and Table 39) register contains the gyroscope data for the z-axis.

Table 38. Z_GYRO Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x16, 0x17	Not applicable	R	No

Table 39. Z_GYRO Bit Descriptions

Bits	Description
[31:16]	Z-axis gyroscope data (16-bit resolution); twos complement, 0°/sec = 0x00000000, see Table 32 for the scale factor
[15:0]	Lower 16 bits to achieve 32-bit resolution

ACCELERATION DATA

The accelerometers in the ADIS16550 measure both dynamic and static (response to gravity) acceleration along three orthogonal axes (x, y, and z). Figure 39 shows the orientation of each accelerometer axis, which defines the direction of linear acceleration that produces a positive response in each of the angular rate measurements.

Each accelerometer outputs 32-bit data in twos complement format split into an upper and lower register. The full 32-bit data-word can be retrieved by using a burst read to ensure that the upper and lower words are sampled at the same point in time.

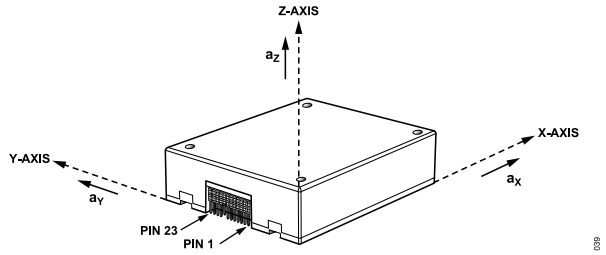

Figure 39. Accelerometer Axis and Polarity Assignments

X-Axis Accelerometer (X_ACCL)

The X_ACCL (see Table 40 and Table 41) register contains the accelerometer data for the x-axis.

Table 40. X_ACCL Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x18, 0x19	Not applicable	R	No

Table 41. X_ACCL Descriptions

Bits	Description
[31:16]	X-axis accelerometer data (16-bit resolution); twos complement, 0 *g* = 0x00000000, 1562.5 LSB/*g*
[15:0]	Lower 16 bits to achieve 32-bit resolution

Y-Axis Accelerometer (Y_ACCL)

The Y_ACCL (see Table 42 and Table 43) register contains the accelerometer data for the y-axis.

Table 42. Y_ACCL Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1A, 0x1B	Not applicable	R	No

Table 43. Y_ACCL Bit Descriptions

Bits	Description
[31:16]	Y-axis accelerometer data (16-bit resolution); twos complement, 0 *g* = 0x00000000, 1562.5 LSB/*g*
[15:0]	Lower 16 bits to achieve 32-bit resolution

USER REGISTER DEFINTIONS

Z-Axis Accelerometer (Z_ACCL)

The Z_ACCL (see Table 44 and Table 45) register contains the accelerometer data for the z-axis.

Table 44. Z_ACCL Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1C, 0x1D	Not applicable	R	No

Table 45. Z_ACCL Bit Descriptions

Bits	Description
[31:16]	Z-axis accelerometer data (16-bit resolution); twos complement, 0 *g* = 0x00000000, 1562.5 LSB/*g*
[15:0]	Lower 16 bits to achieve 32-bit resolution

Accelerometer Resolution

Although 32-bit resolution is available, 16-bit mode is most commonly used because each DOUT response contains 16 bits of sensor data. Table 46 offers various numerical examples that demonstrate the format of the linear acceleration data.

Table 46. 16-Bit Accelerometer Data Format Examples

Acceleration	Decimal	Hexadecimal	Binary
+14.0 *g*	+21,875	0x5573	0101 0101 0111 0011
+1.0 *g*	+1563	0x061B	0000 0110 0001 1011
+17.5 m*g*	+27	0x001B	0000 0000 0001 1011
0 m*g*	0	0x00000000	0000 0000 0000 0000
−17.5 m*g*	−27	0xFFE5	1111 1111 1110 0101
−1.0 *g*	−1563	0xF3CB	1111 0011 1100 1011
−14.0 *g*	−21,875	0xAA8D	1010 1010 1000 1101

DELTA ANGLES

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16550 also provides delta angle measurements that represent a computation of angular displacement between each sample update. Figure 40 shows the orientation of each delta angle output, which defines the direction of rotation that produces a positive response in each of the angular displacement (delta angle) measurements.

The delta angle outputs represent an integration of the gyroscope measurements, and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,\,nD} = \frac{1}{2 \times f_S} \times \sum_{d\,=\,0}^{D\,-\,1} \left(\omega_{x,\,nD\,+\,d} + \omega_{x,\,nD\,-\,d}\right) \quad (20)$$

where:
$\Delta\theta_x$ is the delta angle measurement for the x-axis.
n is the sample time before the decimation filter.
D is the decimation rate = DECIMATE + 1 (see Table 92).
f_S is the sample rate.
d is the incremental variable in the summation formula.
ω_x is the x-axis rate of rotation (gyroscope).

When using the internal sample clock, f_S is equal to 4000 SPS. When using the external clock option, f_S is equal to the frequency of the external clock. The range in the delta angle registers accommodates the maximum rate of rotation (±409.6°/sec), the nominal sample rate (4000 SPS), and an update rate of 1 Hz (DECIMATE = 0x00000F9F; divide by 3999 plus 1, see Table 92), all at the same time. When using an external clock that is slower than 4000 SPS, select a DECIMATE setting that avoids overranging the delta angle registers.

Each delta angle register contains 32-bit data in twos complement format.

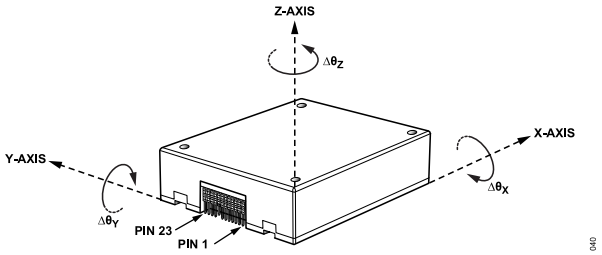

Figure 40. Delta Angle Axis and Polarity Assignments

X-Axis Delta Angle (X_DELTANG)

The X_DELTANG (see Table 47 and Table 48) register contains the delta angle data for the x-axis.

Table 47. X_DELTANG Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x1E, 0x1F	Not applicable	R	No

Table 48. X_DELTANG Bit Descriptions

Bits	Description
[31:16]	X-axis delta angle data (16-bit resolution); twos complement, 0° = 0x00000000, 45.511 LSB/°
[15:0]	Lower 16 bits to achieve 32-bit resolution

Y-Axis Delta Angle (Y_DELTANG)

The Y_DELTANG (see Table 49 and Table 50) register contains the delta angle data for the y-axis.

Table 49. Y_DELTANG Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x20, 0x21	Not applicable	R	No

Table 50. Y_DELTANG Bit Descriptions

Bits	Description
[31:16]	Y-axis delta angle data (16-bit resolution); twos complement, 0° = 0x00000000, 45.511 LSB/°
[15:0]	Lower 16 bits to achieve 32-bit resolution

USER REGISTER DEFINTIONS

Z-Axis Delta Angle (Z_DELTANG)

The Z_DELTANG (see Table 51 and Table 52) register contains the delta angle data for the z-axis.

Table 51. Z_DELTANG Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x22, 0x23	Not applicable	R	No

Table 52. Z_DELTANG Bit Descriptions

Bits	Description
[31:16]	Z-axis delta angle data (16-bit resolution); twos complement, 0° = 0x00000000, 45.511 LSB/°
[15:0]	Lower 16 bits to achieve 32-bit resolution

Delta Angle Resolution

Although 32-bit resolution is available, 16-bit mode is most commonly used because each DOUT response contains 16 bits of sensor data. Table 53 shows various numerical examples that demonstrate the format of the delta angle data.

Table 53. 16-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hexadecimal	Binary
+719.978	+32767	0x7FFF	0111 1111 1111 1111
+360	+16384	0x4000	0100 0000 0000 0000
+1	+46	0x002E	0000 0000 0010 1110
0	0	0x00000000	0000 0000 0000 0000
−1	−46	0xFFD2	1111 1111 1101 0010
−360	−16384	0xC000	1100 0000 0000 0000
−720	−32768	0x8000	1000 0000 0000 0000

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16550 also provides delta velocity measurements that represent a computation of linear velocity change between each sample update. Figure 41 shows the orientation of each delta velocity measurement, which defines the direction of linear velocity increase that produces a positive response in each of the delta velocity rate measurements.

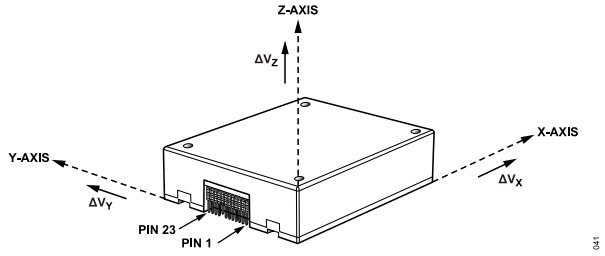

Figure 41. Delta Velocity Axis and Polarity Assignments

The delta velocity outputs represent an integration of the acceleration measurements, and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,\,nD} = \frac{1}{2 \times f_S} \times \sum_{d=0}^{D-1} \left(\alpha_{x,\,nD+d} + \alpha_{x,\,nD+d-1}\right) \quad (21)$$

where:
ΔV_X is the delta velocity measurement for the x-axis.
n is the sample time before the decimation filter.
D is the decimation rate = DECIMATE + 1 (see Table 92).
f_S is the sample rate.
d is the incremental variable in the summation formula.
a_x is the x-axis linear acceleration (accelerometer).

When using the internal sample clock, f_S is equal to 4000 SPS. When using the external clock option, f_S is equal to the frequency of the external clock. The range in the delta velocity registers accommodates an average linear acceleration of 12.75 *g*, the nominal sample rate (4000 SPS), and an update rate of 1 Hz (DECIMATE = 0x00000F9F; divide by 3999 plus 1, see Table 92), all at the same time. When using external clocks slower than 4000 SPS or when subjected to high accelerations, select a DECIMATE setting that avoids overranging the delta velocity registers. It is also important to note that if the integration period is too long (>1 second), the delta velocity registers rail.

Each delta velocity register contains 32-bit data in twos complement format.

X-Axis Delta Velocity (X_DELTVEL)

The X_DELTVEL (see Table 54 and Table 55) register contains the delta velocity data for the x-axis.

Table 54. X_DELTVEL Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x24, 0x25	Not applicable	R	No

Table 55. X_DELTVEL Bit Definitions

Bits	Description
[31:16]	X-axis delta velocity data (16-bit resolution); twos complement, 0 m/sec = 0x00000000, 262.144 LSB/m/sec
[15:0]	Lower 16 bits to achieve 32-bit resolution

Y-Axis Delta Velocity (Y_DELTVEL)

The Y_DELTVEL (see Table 56 and Table 57) register contains the delta velocity data for the y-axis.

Table 56. Y_DELTVEL Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x26, 0x27	Not applicable	R	No

Table 57. Y_DELTVEL Bit Definitions

Bits	Description
[31:16]	Y-axis delta velocity data (16-bit resolution); twos complement, 0 m/sec = 0x00000000, 262.144 LSB/m/sec
[15:0]	Lower 16 bits to achieve 32-bit resolution

USER REGISTER DEFINTIONS

Z-Axis Delta Velocity (Z_DELTVEL)

The Z_DELTVEL (see Table 58 and Table 59) register contains the delta velocity data for the z-axis.

Table 58. Z_DELTVEL Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x28, 0x29	Not applicable	R	No

Table 59. Z_DELTVEL Bit Definitions

Bits	Description
[31:16]	Z-axis delta velocity data (16-bit resolution); twos complement, 0 m/sec = 0x00000000, 262.144 LSB/m/sec
[15:0]	Lower 16 bits to achieve 32-bit resolution

Delta Velocity Resolution

Although 32-bit resolution is available, 16-bit mode is most commonly used because each DOUT response contains 16 bits of sensor data. Table 60 offer various numerical examples that demonstrate the format of the delta angle data.

Table 60. 16-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hexadecimal	Binary
+124.996	+32767	0x7FFF	0111 1111 1111 1111
+2	+524	0x020C	0000 0010 0000 1100
+1	+262	0x0106	0000 0001 0000 0110
0	0	0x00000000	0000 0000 0000 0000
−1	−262	0xFEFA	1111 1110 1111 1010
−2	−524	0xFDF4	1111 1101 1111 0100
−125	−32768	0x8000	1000 0000 0000 0000

TIMESTAMP

The TIMESTAMP register (see Table 61 and Table 62) provides the user with the elapsed time from most recent sync input to the current sample.

Table 61. TIMESTAMP Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x2A, 0x2B	0x00000000	R/W	No

Table 62. TIMESTAMP Bit Definitions

Bits	Description
[31:0]	Timestamp; twos complement, 1 LSB = 12.3 ns

USER BIAS AND SCALE ADJUSTMENT

The signal chain of each inertial sensor (accelerometers and gyroscopes) includes the application of unique correction formulas that come from extensive characterization of bias, sensitivity, and alignment over a temperature range of −40°C to +85°C for the ADIS16550. These correction formulas are not accessible, but the user does have the opportunity to adjust the bias and the scale factor for each sensor individually through user-accessible registers. These correction factors follow immediately after the factory derived correction formulas and sensor summing in the signal chain, which processes at a rate of 4000 Hz when using the internal sample clock (see f_{SM} in Figure 20 and Figure 21).

Gyroscope Scale Adjustment (X_GYRO_SCALE)

The X_GYRO_SCALE register (see Table 63 and Table 64) provides the user with the opportunity to adjust the scale factor for the x-axis gyroscopes. See Figure 42 for an illustration of how this scale factor influences the x-axis gyroscope data.

Table 63. X_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x30, 0x31	0x00000000	R/W	Yes

Table 64. X_GYRO_SCALE Bit Definitions

Bits	Description
[31:16]	Reserved
[15:0]	X-axis gyroscope scale correction; twos complement, 0x00000000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

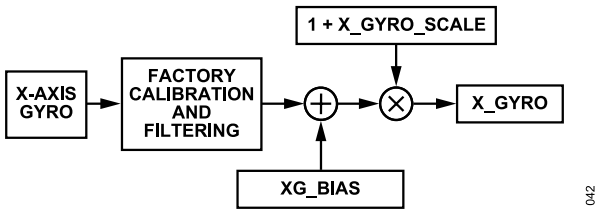

Figure 42. User Bias and Scale Adjustment Registers in Gyroscope Signal Path

Gyroscope Scale Adjustment (Y_GYRO_SCALE)

The Y_GYRO_SCALE register (see Table 65 and Table 66) allows the user to adjust the scale factor for the y-axis gyroscopes. This register influences the y-axis gyroscope measurements in the same manner that X_GYRO_SCALE influences the x-axis gyroscope measurements (see Figure 42).

Table 65. Y_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x32, 0x33	0x00000000	R/W	Yes

Table 66. Y_GYRO_SCALE Bit Definitions

Bits	Description
[31:16]	Reserved
[15:0]	Y-axis gyroscope scale correction; twos complement, 0x00000000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

Gyroscope Scale Adjustment (Z_GYRO_SCALE)

The Z_GYRO_SCALE register (see Table 67 and Table 68) allows the user to adjust the scale factor for the z-axis gyroscopes. This register influences the z-axis gyroscope measurements in the same

USER REGISTER DEFINTIONS

manner that X_GYRO_SCALE influences the x-axis gyroscope measurements (see Figure 42).

Table 67. Z_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x34, 0x35	0x00000000	R/W	Yes

Table 68. Z_GYRO_SCALE Bit Definitions

Bits	Description
[31:16]	Reserved
[15:0]	Z-axis gyroscope scale correction; twos complement, 0x00000000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

Accelerometer Scale Adjustment (X_ACCL_SCALE)

The X_ACCL_SCALE register (see Table 69 and Table 70) allows users to adjust the scale factor for the x-axis accelerometers. See Figure 43 for an illustration of how this scale factor influences the x-axis accelerometer data.

Table 69. X_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x36, 0x37	0x00000000	R/W	Yes

Table 70. X_ACCL_SCALE Bit Definitions

Bits	Description
[31:16]	Reserved
[15:0]	X-axis accelerometer scale correction; twos complement, 0x00000000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

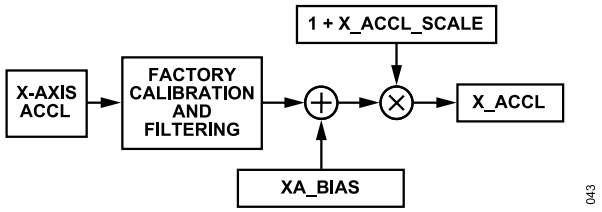

Figure 43. User Bias and Scale Adjustment Registers in Accelerometer Signal Path

Accelerometer Scale Adjustment (Y_ACCL_SCALE)

The Y_ACCL_SCALE register (see Table 71 and Table 72) allows the user to adjust the scale factor for the y-axis accelerometers. This register influences the y-axis accelerometer measurements in the same manner that X_ACCL_SCALE influences the x-axis accelerometer measurements (see Figure 43).

Table 71. Y_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x38, 0x39	0x00000000	R/W	Yes

Table 72. Y_ACCL_SCALE Bit Definitions

Bits	Description
[31:16]	Reserved
[15:0]	Y-axis accelerometer scale correction; twos complement, 0x00000000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

Accelerometer Scale Adjustment (Z_ACCL_SCALE)

The Z_ACCL_SCALE register (see Table 73 and Table 74) allows the user to adjust the scale factor for the z-axis accelerometers. This register influences the z-axis accelerometer measurements in the same manner that X_ACCL_SCALE influences the x-axis accelerometer measurements (see Figure 43).

Table 73. Z_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x3A, 0x3B	0x00000000	R/W	Yes

Table 74. Z_ACCL_SCALE Bit Definitions

Bits	Description
[31:16]	Reserved
[15:0]	Z-axis accelerometer scale correction; twos complement, 0x00000000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

Gyroscope Bias Adjustment (X_GYRO_BIAS)

The X_GYRO_BIAS (see Table 75 and Table 76) registers combine to allow the user to adjust the bias of the x-axis gyroscopes. The digital format examples in Table 33 also apply to the X_GYRO_BIAS register. See Figure 42 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

Table 75. X_GYRO_BIAS Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x40, 0x41	0x00000000	R/W	Yes

Table 76. X_GYRO_BIAS Bit Definitions

Bits	Description
[31:0]	X-axis gyroscope offset correction, twos complement, 0°/sec = 0x00000000, 5242880 LSB/°/sec (32-bit resolution)

Gyroscope Bias Adjustment (Y_GYRO_BIAS)

The Y_GYRO_BIAS (see Table 77 and Table 78) registers combine to allow users to adjust the bias of the y-axis gyroscopes. The digital format examples in Table 33 also apply to the Y_GYRO_BIAS register. These registers influence the y-axis gyroscope measurements in the same manner that the X_GYRO_BIAS registers influence the x-axis gyroscope measurements (see Figure 42).

Table 77. Y_GYRO_BIAS Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x42, 0x43	0x00000000	R/W	Yes

USER REGISTER DEFINTIONS

Table 78. Y_GYRO_BIAS Bit Definitions

Bits	Description
[31:0]	Y-axis gyroscope offset correction, twos complement, 0°/sec = 0x00000000, 5242880 LSB/°/sec (32-bit resolution)

Gyroscope Bias Adjustment (Z_GYRO_BIAS)

The Z_GYRO_BIAS (see Table 79 and Table 80) registers combine to allow users to adjust the bias of the z-axis gyroscopes. The digital format examples in Table 33 also apply to the Z_GYRO_BIAS register. These registers influence the z-axis gyroscope measurements in the same manner that the X_GYRO_BIAS registers influence the x-axis gyroscope measurements (see Figure 42).

Table 79. Z_GYRO_BIAS Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x44, 0x45	0x00000000	R/W	Yes

Table 80. Z_GYRO_BIAS Bit Definitions

Bits	Description
[31:0]	Z-axis gyroscope offset correction, twos complement, 0°/sec = 0x00000000, 5242880 LSB/°/sec (32-bit resolution)

Accelerometer Bias Adjustment (X_ACCL_BIAS)

The X_ACCL_BIAS (see Table 81 and Table 82) registers combine to allow the user to adjust the bias of the x-axis accelerometers. The digital format examples in Table 46 also apply to the X_ACCL_BIAS register. See Figure 43 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

Table 81. X_ACCL_BIAS Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x46, 0x47	0x00000000	R/W	Yes

Table 82. X_ACCL_BIAS Bit Definitions

Bits	Description
[31:0]	X-axis accelerometer offset correction, twos complement, 0 *g* = 0x00000000, 102400000 LSB/*g* (32-bit resolution)

Accelerometer Bias Adjustment (Y_ACCL_BIAS)

The Y_ACCL_BIAS (see Table 83 and Table 84) registers combine to allow the user to adjust the bias of the y-axis accelerometers. The digital format examples in Table 46 also apply to the Y_ACCL_BIAS register. These registers influence the y-axis accelerometer measurements in the same manner that the X_ACCL_BIAS registers influence the x-axis accelerometer measurements (see Figure 43).

Table 83. Y_ACCL_BIAS Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x48, 0x49	0x00000000	R/W	Yes

Table 84. Y_ACCL_BIAS Bit Definitions

Bits	Description
[31:0]	Y-axis accelerometer offset correction, twos complement, 0 *g* = 0x00000000, 102400000 LSB/*g* (32-bit resolution)

Accelerometer Bias Adjustment (Z_ACCL_BIAS)

The Z_ACCL_BIAS (see Table 85 and Table 86) registers combine to allow users to adjust the bias of the z-axis accelerometers. The digital format examples in Table 46 also apply to the Z_ACCL_BIAS register. These registers influence the z-axis accelerometer measurements in the same manner that the X_ACCL_BIAS registers influence the x-axis accelerometer measurements (see Figure 43).

Table 85. Z_ACCL_BIAS Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4A, 0x4B	0x00000000	R/W	Yes

Table 86. Z_ACCL_BIAS Bit Definitions

Bits	Description
[31:0]	Z-axis accelerometer offset correction, twos complement, 0 *g* = 0x00000000, 102400000 LSB/*g* (32-bit resolution)

SYSTEM LEVEL COMMAND (COMMAND)

The COMMAND register (see Table 87 and Table 88) provides trigger bits for several operations. Write a 1 to the appropriate bit in COMMAND to start a particular function. Note that only one function can be implemented at a time. Never set multiple bits at the same time in this register.

Table 87. COMMAND Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x50, 0x51	Not applicable	W	No

Table 88. COMMAND Bit Definitions

Bits	Description
[31:16]	Reserved
15	Software reset
[14:4]	Reserved
3	Flash update
2	Clear user calibration
1	On-demand self test
0	Write lock

Software Reset

COMMAND, Bit 15, triggers a software reset when set to a value of 1 (DIN = 0x8000508F). Following a software reset, the device behaves as if it is experiencing a power-on reset (POR). All user

USER REGISTER DEFINTIONS

settings reset, and the user must wait the start-up time before getting data from the ADIS16550 (see Figure 28).

Flash Update

COMMAND, Bit 3, triggers a flash update when set to a value of 1. A flash update is an update of all nonvolatile data and system configuration into memory. This command requires a stable power supply for the duration of this update. Note that a limit exists on the number of flash operations allowable over the life of the product (see Table 1).

Clear User Calibration

COMMAND, Bit 2, allows the user to clear all user calibration when set to a value of 1. This includes a reset of system level SCALE and BIAS registers to the initial factory settings. Data within the decimation and filter functions are reset as well with the availability of the next valid data depending upon the filter and decimation settings.

On-Demand Self Test

COMMAND, Bit 1, initiates an internal diagnostics check of all inertial sensors. Wait for 12 ms after the on-demand self test bit is asserted to verify its results or initiate the next command. Results are observable in the STATUS register.

Write Lock

COMMAND, Bit 0, locks the device from further configuration commands when set to 1. Before setting the write lock bit, the device is in its initialization phase upon power-up. During the initialization phase, the user can configure the various settings of the device. After setting the write lock bit, the device transitions to the run phase and no further configurations are possible. To return to initialization mode, perform a software or hardware reset.

MISCELLANEOUS CONFIGURATION (CONFIG)

The CONFIG register (see Table 89 and Table 90) provides configuration options for the clock modes, FIR filter control, and point of percussion alignment for the accelerometers (on/off).

Table 89. CONFIG Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x52, 0x53	0x00000000	R/W	Yes

Table 90. CONFIG Bit Definitions

Bits	Description
[31:5]	Reserved
4	Point of percussion alignment (1 = enabled)
3	Gyroscope FIR filter enable (1 = enabled)
2	Accelerometer FIR filter enable (1 = enabled)
1	SYNC mode (1 = scaled, 0 = direct)
0	SYNC enable (1 = enabled)

Point of Percussion

CONFIG, Bit 4 offers a point of percussion alignment function that maps the accelerometer sensors to the corner of the package identified in Figure 44. To activate this feature, set CONFIG, Bit 4 = 1 (DIN = 0x00045281).

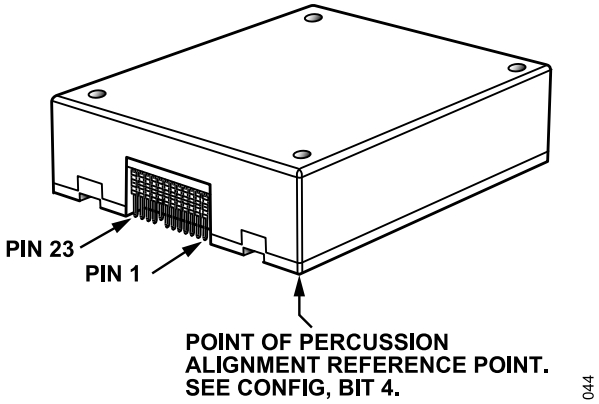

Figure 44. Point of Percussion Reference Point

Gyroscope FIR Filter Control (GYRO_FILTR_EN)

The GYRO_FILTR_EN bit, Bit 3 (see Table 90), provides the configuration control for the gyroscope FIR filter bank in the signal chain of each sensor (see Figure 23). This bit provides on/off control for the gyroscope FIR bank. To activate this filter, set CONFIG, Bit 3 = 1.

Accelerometer FIR Filter Control (ACCEL_FILTR_EN)

The ACCEL_FILTR_EN bit, Bit 2 (see Table 90), provides the configuration control for the accelerometer FIR filter bank in the signal chain of each sensor (see Figure 23). This bit provides on/off control for the accelerometer FIR bank. To activate this filter, set CONFIG, Bit 2 = 1.

Sync Mode Control (SYNC_MODE)

The SYNC_MODE bit, Bit 1 (see Table 90), provides the configuration control for the sync mode (direct or scaled). Direct sync mode uses the input sync frequency as the output data rate. Scaled sync mode generates a slower data rate than the input sync frequency. To activate the scaled sync mode, set CONFIG, Bit 1 = 1.

Sync Enable Control (SYNC_EN)

The SYNC_EN bit, Bit 0 (see Table 90), provides the configuration control for using an external clock instead of the internal clock. This bit provides on/off control for the sync mode. To activate the sync mode, set CONFIG, Bit 0 = 1.

USER REGISTER DEFINTIONS

DECIMATION FILTER (DECIMATE)

The DECIMATE register (see Table 91 and Table 92) provides user control for the final filter stage (see Figure 23), which averages and decimates the accelerometers and gyroscopes data, and extends the time that the delta angle and delta velocity track between each update. The output sample rate is equal to 4000/(DECIMATE + 1). For example, set DECIMATE = 0x00000027 (DIN = 0x0027A90C) to reduce the output sample rate to 100 SPS (4000 ÷ 40).

Table 91. DECIMATE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x54, 0x55	0x00000000	R/W	Yes

Table 92. DECIMATE Bit Definitions

Bits	Description
[31:12]	Reserved
[11:0]	Decimation rate, binary format, maximum = 4095

SCALING THE INPUT CLOCK, SCALED SYNC MODE (SYNC_SCALE)

The scaled sync mode (CONFIG, Bit 1 = 1 and Bit 0 = 1, see Table 90) supports the use of an input sync frequency that is slower than the data sample rates of the inertial sensors. This mode supports a frequency range of 1 Hz to 128 Hz for the input sync mode. In this mode, the data sample rate is equal to the product of the value in the SYNC_SCALE register (see Table 93 and Table 94) and the input sync frequency. Note that the product of the value stored in the SYNC_SCALE register and the input sync frequency must never exceed 4000 SPS:

$$SYNC\_SCALE \times \text{Input Sync Frequency} \leq 4000 \text{ SPS} \quad (22)$$

For example, the following command sequence sets the data collection and processing rate (f_{SM} in Figure 20 and Figure 21) to 4000 Hz (SYNC_SCALE = 0x0FA0) when using a 1 Hz signal on the sync line as the external clock input, and preserves the factory default configuration for the data ready signal:

1. Turn to Page 0
2. Set SYNC_SCALE, Bits[15:0] = 0x0FA0
3. Set CONFIG, Bits[15:0] = 0x0003

The allowable range for the SYNC_SCALE register is 3000 Hz to 4500 Hz. For upscale conditions set to higher than the maximum defined rate, the IMU reverts to ignoring sync pulses to maintain a reduced upscale boundary. If a lower scaled sync output is desired, the decimate function must be used. For example, to achieve a 2000 Hz scaled sync output rate, set SYNC_SCALE = 4000 and set DECIMATE = 1.

Table 93. SYNC_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x56, 0x57	0x00000FA0	R/W	Yes

Table 94. SYNC_SCALE Bit Definitions

Bits	Description
[31:0]	External clock scale factor (K_{ECSF}), binary format

SCRATCH REGISTERS (USER_SCR_X)

The USER_SCR_1 (see Table 95 and Table 96), USER_SCR_2 (see Table 97 and Table 98), USER_SCR_3 (see Table 99 and Table 100), and USER_SCR_4 (see Table 101 and Table 102) registers provide four locations for the user to store information.

Table 95. USER_SCR_1 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x60, 0x61	0x00000000	R/W	Yes

Table 96. USER_SCR_1 Bit Definitions

Bits	Description
[31:0]	User defined

Table 97. USER_SCR_2 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x62, 0x63	0x00000000	R/W	Yes

Table 98. USER_SCR_2 Bit Definitions

Bits	Description
[31:0]	User defined

Table 99. USER_SCR_3 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x64, 0x65	0x00000000	R/W	Yes

Table 100. USER_SCR_3 Bit Definitions

Bits	Description
[31:0]	User defined

Table 101. USER_SCR_4 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x66, 0x67	0x00000000	R/W	Yes

Table 102. USER_SCR_4 Bit Definitions

Bits	Description
[31:0]	User defined

FLASH MEMORY ENDURANCE COUNTER (ENDURANCE)

The ENDURANCE (see Table 103 and Table 104) registers combine to provide a 32-bit, binary counter that tracks the number of flash memory write cycles. In addition to the number of write cycles, the flash memory has a finite service lifetime, which depends on the junction temperature. Figure 45 provides guidance for estimating the retention life for the flash memory at specific junction temperatures. The junction temperature is approximately 7°C above the case temperature.

USER REGISTER DEFINTIONS

Table 103. ENDURANCE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x72, 0x73	Not applicable	R	Not applicable

Table 104. ENDURANCE Bit Definitions

Bits	Description
[32:0]	Flash memory write counter

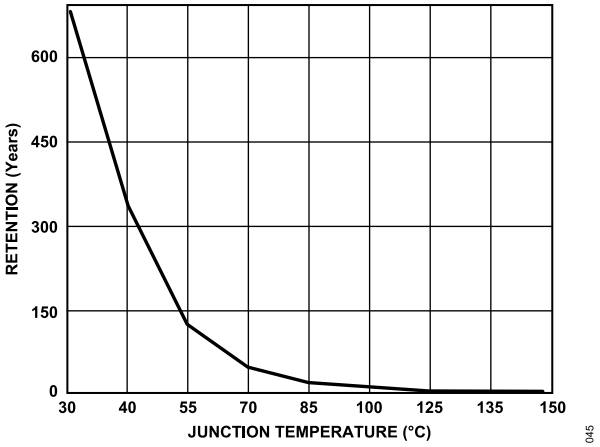

Figure 45. Flash Memory Retention

LOT SPECIFIC NUMBER (LOT_NUM)

Table 105. LOT_NUM Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x74, 0x75	Not applicable	R	Not applicable

Table 106. LOT_NUM Bit Definitions

Bits	Description
[31:0]	Lot specific number

SERIAL NUMBER (SERIAL_NUM)

Table 107. SERIAL_NUM Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x76, 0x77	Not applicable	R	Not applicable

Table 108. SERIAL_NUM Bit Definitions

Bits	Description
[31:0]	Serial number

PROCESSOR REVISION NUMBER (PROC_REV)

The PROC_REV register (see Table 109 and Table 110) contains the silicon revision. Because the boot code is burned into the ROM, the boot revision of the ADIS16550 processor core is traceable from the silicon revision.

Table 109. PROC_REV Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x78, 0x79	Not applicable	R	Not applicable

Table 110. PROC_REV Bit Definitions

Bits	Description
[31:4]	Reserved
[3:0]	Silicon revision number

FIRMWARE REVISION (FW_REV)

The FW_REV register (see Table 111 and Table 112) contains the firmware revision in XX.xx format.

Table 111. FW_REV Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x7A, 0x7B	Not applicable	R	Not applicable

Table 112. FW_REV Bit Definitions

Bits	Description
[31:16]	Reserved.
[15:8]	Major firmware revision number.
[7:0]	Minor firmware revision number. Tracks enhancements and bug fixes.

FIRMWARE REVISION (FW_DATE)

The FW_DATE register (see Table 113 and Table 114) contains the year, month, and day of the factory configuration date. FW_DATE, Bits[31:16], contain digits that represent the year of the factory configuration in a binary coded decimal (BCD) format. For example, the year 2019 is represented by FW_DATE, Bits[31:16] = 0x2019.

FW_DATE, Bits[15:8], contain digits that represent the month of the factory configuration in a binary coded decimal (BCD) format. For example, November is the 11th month in a year and is represented by FW_DATE, Bits[15:8] = 0x11.

FW_DATE, Bits[7:0], contain digits that represent the day of factory configuration in a BCD format. For example, the 27th day of the month is represented by FW_DATE, Bits[7:0] = 0x27.

Table 113. FW_DATE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x7C, 0x7D	Not applicable	R	Not applicable

Table 114. FW_DATE Bit Definitions

Bits	Description
[31:28]	Factory configuration year BCD code, thousands digit, numerical format = 4-bit binary, range = 0 to 9
[27:24]	Factory configuration year BCD code, hundreds digit, numerical format = 4-bit binary, range = 0 to 9
[23:20]	Factory configuration year BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[19:16]	Factory configuration year BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9
[15:12]	Factory configuration month BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 2
[11:8]	Factory configuration month BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

USER REGISTER DEFINTIONS

Table 114. FW_DATE Bit Definitions (Continued)

Bits	Description
[7:4]	Factory configuration day BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration day BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

PRODUCT IDENTIFICATION (PROD_ID)

The PROD_ID register (see Table 115 and Table 116) contains the numerical portion of the device number (16,550) in hexadecimal format.

Table 115. PROD_ID Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x7E, 0x7F	0x000040A6	R	Not applicable

Table 116. PROD_ID Bit Definitions

Bits	Description
[31:16]	Reserved
[15:0]	Product identification = 0x40A6

FIR FILTER BANK COEFFICIENTS (COEFF_C0 TO COEFF_C119)

The ADIS16550 provides an FIR filter bank with 120 taps that consume one page of memory (Page 1). Each 32-bit register in Page 1 is split into two independently signed 16-bit filter coefficients. The FIR filter has unity gain when the sum of all the coefficients is equal to 32,768. For filter designs that require less than 120 taps, write 0x0000 to all unused registers to eliminate the latency associated with that particular tap.

Table 117. FIR Filter Bank Register Definitions

Page	Addresses	Access	Register Contents
0x01	0x08, 0x09	R/W	FIR Coefficient C0 to C1
0x01	0x0A to 0x7C	R/W	FIR Coefficient C2 to C117
0x01	0x7D, 0x7E	R/W	FIR Coefficients C118 to C119

Table 118 and Table 119 provide detailed register and bit definitions for one of the FIR coefficient registers, COEFF_C71.

Table 118. COEFF_C70 and COEFF_C71 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x01	0x4E, 0x4F	0x02BE0353	R	Yes

Table 119. COEFF_C70 and COEFF_C71 Bit Definitions

Bits	Description
[31:16]	FIR Bank, Coefficient 70, twos complement
[15:0]	FIR Bank, Coefficient 71, twos complement

Table 120. Configuration Example, FIR Coefficient

DIN Command	Description
0x00010083	Select Page 1
0x03534E8D	COEFF_C70, Bits[15:0] = 0x0353
0x02BE4F8E	COEFF_C71, Bits[15:0] = 0x02BE

Table 121. Filter Bank Memory Map

PAGE_ID	Address	Register
0x01	0x00, 0x01	PAGE_ID
0x01	0x02 to 0x07	Not used
0x01	0x08, 0x09	COEFF_C0, COEFF_C1
0x01	0x0A to 0x7D	COEFF_C2 to COEFF_C117
0x01	0x7E, 0x7F	COEFF_C118, COEFF_C119

Default Filter Performance

The FIR filter bank is factory programmed to be a 100Hz low-pass filter with unity dc gain. Figure 46 shows an example of the frequency response characteristics. The phase delay is equal to ½ of the total number of taps.

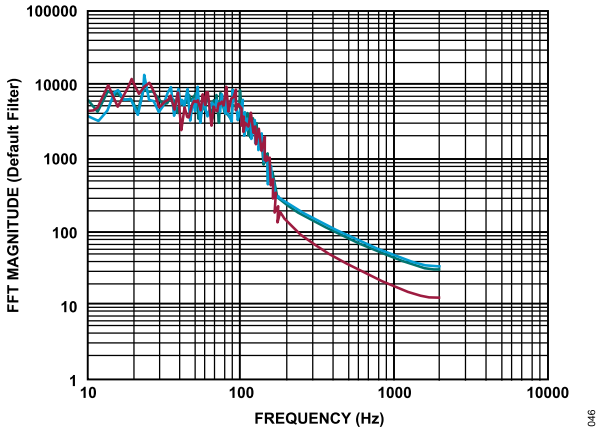

Figure 46. FIR Frequency Response Curve—Default 100 Hz Filter

APPLICATIONS INFORMATION

MOUNTING BEST PRACTICES

For the best performance, follow these guidelines when installing the ADIS16550 into a system:

- Eliminate opportunity for translational force (x-axis and y-axis direction, per Figure 39) application on the electrical connector.
- Use uniform mounting forces (see AN-1295) on all four corners. The suggested torque setting is 40 inch ounces (0.285 Nm).
- When the ADIS16550 rests on the PCB, which contains the mating connector (see Figure 47), use a diameter of at least 2.85 mm for the passthrough holes.
- Use alignment pins near the four corners of the package to optimize mounting accuracy of the ADIS16550 and to reduce system level cross axis sensitivity (see Figure 49).

These guidelines help prevent irregular force profiles, which can warp the package and introduce bias errors in the sensors. Figure 47 and Figure 48 provide details for mounting hole and connector alignment pin drill locations.

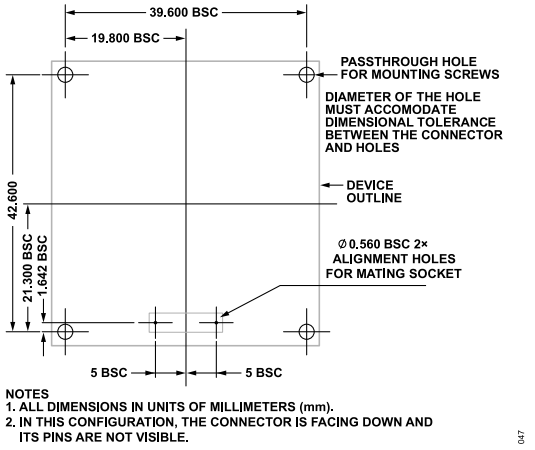

Figure 47. Suggested PCB Layout Pattern, Connector Down

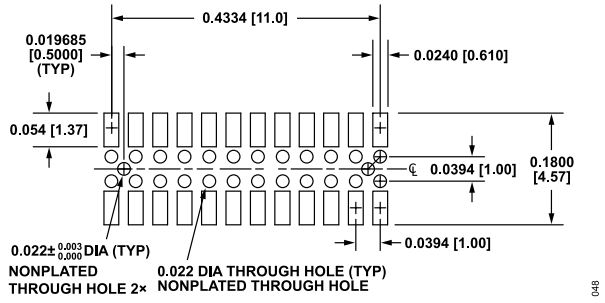

Figure 48. Suggested Layout and Mechanical Design when Using Samtec CLM-112-02-G-D-A for the Mating Connector

PREVENTING MISINSERTION

The ADIS16550 connector uses the same pattern as the ADIS16488A, but with Pin 12 and Pin 15 missing. This pin configuration enables a mating connector to plug these holes to help prevent misconnection of the ADIS16550. The ADIS16550 is physically pin compatible with the ADIS16495 but without some of the DIOx pin configurability. Samtec has a custom part number that provides this type of mating socket: ASP-193371-04.

EVALUATION TOOLS

Breakout Board, ADIS16IMU1/PCBZ

The ADIS16IMU1/PCBZ (sold separately) provides a breakout board function for the ADIS16550, which means that it provides access to the ADIS16550 through larger connectors that support standard 1 mm ribbon cabling. This board also provides four mounting holes for attachment of the ADIS16550 to the breakout board.

PC-Based Evaluation, EVAL-ADIS2

Use the EVAL-ADIS2 and ADIS16IMU1/PCBZ to evaluate the ADIS16550 on a PC-based platform.

POWER SUPPLY CONSIDERATIONS

The VDD power supply must charge 46 µF of capacitance (inside of the ADIS16550, across the VDD and GND pins) during its initial ramp and settling process. When the ADIS16550 begins its internal start-up process, it generates additional transient current demand. This transient current must be accounted for at the system level.

Note that the ADIS16550 module casing is not grounded. If desired, the user can do this by connecting the GND pins on the ADIS16550 to the threaded interconnect into which the mounting screws are inserted. Care must be taken when doing this to limit what the mounting screws connect to electrically to limit electrical noise being coupled into the electrical ADIS16550 GND pins.

OUTLINE DIMENSIONS

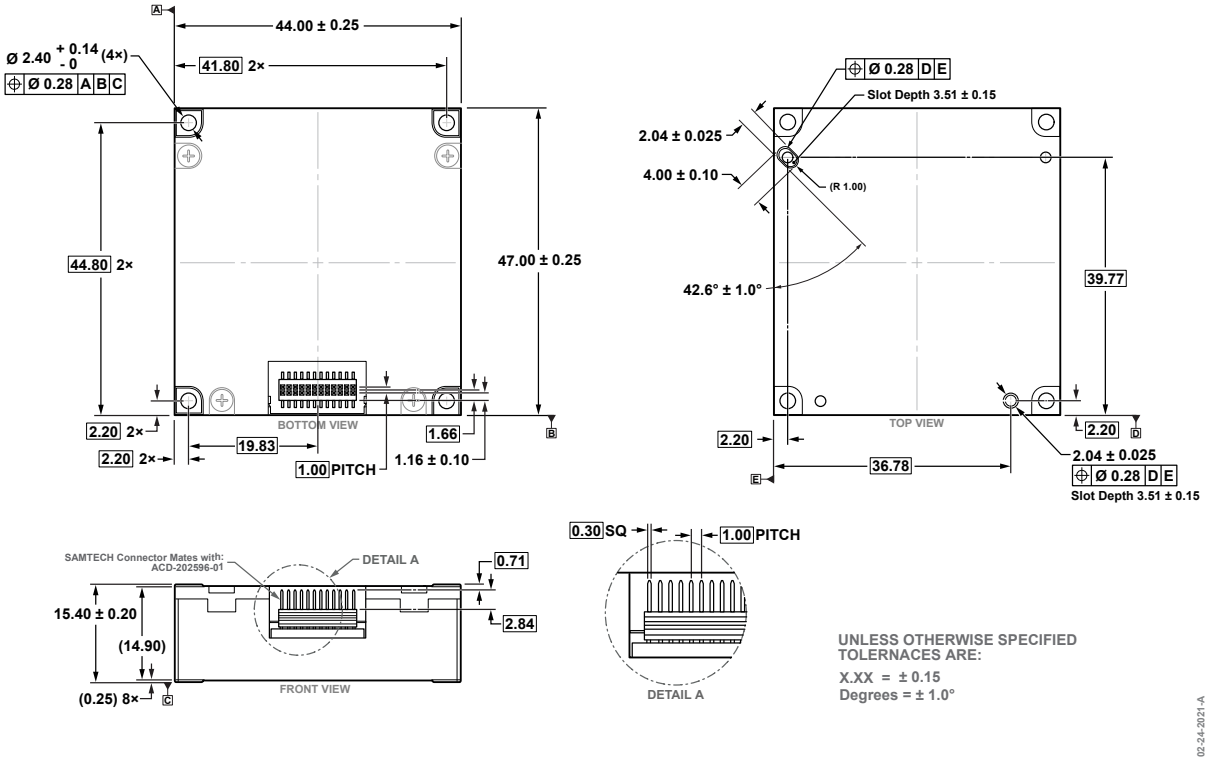

Figure 49. 24-Lead Module with Connector Interface [MODULE]
(ML-24-12)
Dimensions shown in millimeters

Updated: March 14, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16550BMLZ	−40°C to +105°C	24-Lead Module with Connector Interface	ML-24-2

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 122. Evaluation Boards

Model[1]	Description
ADIS161MU1/PCBZ	Breakout Board for the ADIS1613x, ADIS1637x, ADIS1648x and ADIS1649x
EVAL-ADIS2	EVAL-ADIS Evaluation System

[1] Z = RoHS-Compliant Part.