AK1595A
Bluetooth Low Energy transmitter

1. General Description

The AK1595A is a Bluetooth® transmitter IC that greatly simplifies the addition of wireless connectivity to a system. There is no need to develop complicated, proprietary micro controller code; Bluetooth Low Energy compliant advertising transmission can be achieved by simply configuring the transmission power, data, and transmission start trigger via the AK1595A's UART or I²C interface. The AK1595A can achieve extremely low system current consumption by using the built-in low power timer.
The AK1595A supports Direction finding data format which can be achieved by simply setting the AK1595A internal register.
Using the AK1595A to add wireless connectivity to a product can simplify system design and reduce BOM cost.

2. Features

- Bluetooth Low Energy
  - Bluetooth Low Energy compliant
  - Support 31 octets Advertising data length
  - Supports 2402MHz, 2426MHz, 2480MHz frequencies
  - Supports 1Mbps data rate
  - Supports Direction finding format
  - Built–in interface and test circuitry for Bluetooth certification tests

  Note: AK1595A does not support secondary advertising, LE2M, AoD options

- Microprocessor Interface
  - UART and I²C
  - UART Baud Rate: 9600bps or 115200bps

- RF transmission
  - Maximum RF power: 0dBm
  - RF power adjustable range: 0dBm to -32dBm
  - Initiate transmission via register or TXON pin

- Whitening, CRC, GFSK
  - Built–in data whitening feature and CRC compliant with Bluetooth Low Energy.
  - Support GFSK(1Mbps)

- Low power timer
  - Built-in Low power timer (0.5 μA typ.)

- Power-supply voltage
  - 2.0V to 3.6V

- Package
  - 20-pin HUQFN (3mm x 3mm x 0.5mm, 0.4mm pitch)

3. Table of Contents

4. Notation

Register names and pin names and their polarities are described below.

- NameA bit = “0” or “1” : Register
- NameB pin = “H” or “L” : Pin
- NameC, NameD bits : Multiple registers
- NameE, NameF pins : Multiple pins

To specify the bit width of a register or to indicate a specific 1-bit of the register data, describe as follows.

- NameG[2:0] bits = 3’b000
- NameG[1] bit = “0”

The address is written in the register that appears first for each page or chapter.

- <Address0x9A> NameD bits

The numerical values are expressed as follows

- 0x4D: Hexadecimal numbers
- 0d1234 or 1234: Decimal numbers
- 0b100 1101 0010: Binary numbers

Combination of bit number and numerical value

- 8'hAB: 8-bits hexadecimal data.
- 8'b1010 1011: 8-bits binary data.

ex)
6'h12 = 6'b01 0010
8'h12 = 8'b0001 0010

Terms and acronyms

- AdvA Advertiser's Device Address
- AoA Angle of Arrival
- AoD Angle of Departure
- CRC Cyclic Redundancy Check
- CTE Constant Tone Extension
- GFSK Gaussian Frequency Shift Keying
- I^2C Inter-Integrated Circuit
- LDO Low Drop Out
- LSB Least Significant Bit
- MCU Micro Controller Unit
- MSB Most Significant Bit
- PDU Protocol Data Unit
- PLL Phase Locked Loop
- PPM Part Per Million
- RF Radio Frequency
- RFU Reserved for Future Use
- SW Switch
- TX Transmit
- UART Universal Asynchronous Receiver Transmitter

These 3 terms describe the packet data of Bluetooth Low Energy Advertising channel. The data format is shown in Figure1.

- Payload
- AdvA
- AdvData

LSB MSB

Preamble	Access Address	PDU			CRC	Constant Tone Extension
		Header	Payload			
			AdvA	AdvData		
1octet	4octets	2octets	6octets	0 to 31octets	3octets	16 to 160 µs

Figure1. Bluetooth Low Energy Advertising Channel packet format

5. Block Diagram and Functions

5.1. Block Diagram

Power supply and ground pins are not included.

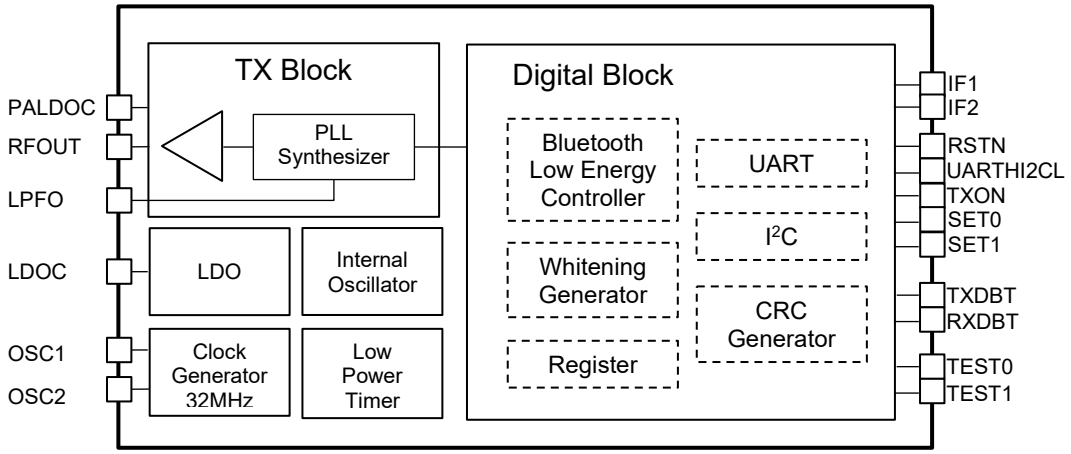


Figure 2. Overall Block Diagram

5.2. Functions

- Digital Block
  Write/read registers via the UART or I²C interface
  Power-down and timing control
  Generation of transmit data and CRC code
  Data whitening processing
  Bluetooth certification test

- Clock Generator 32MHz
  This block generates a reference oscillator frequency of 32MHz.

- Low Power Timer
  This block is a timer driven by ultra-low power consumption. This timer runs on the clock generated by the AK1595A internal oscillator.

- LDO
  This block generates power to the digital and TX Block from AVDD power supply.

- TX Block
  Configure the TX Block using PLLs and RFAMP. This block generates Bluetooth Low Energy advertising channels of 2402MHz, 2426MHz, and 2480MHz based on an external crystal oscillator and a 32MHz clock generated by the Clock Generator. GFSK is modulated based on the transmitted data generated by the digital block. The RFAMP amplifies and outputs the signals generated by the PLLs. The output power can be adjusted from 0dBm to -32dBm in the registers.

6. Pin Configurations and Functions

6.1. Pin Configurations

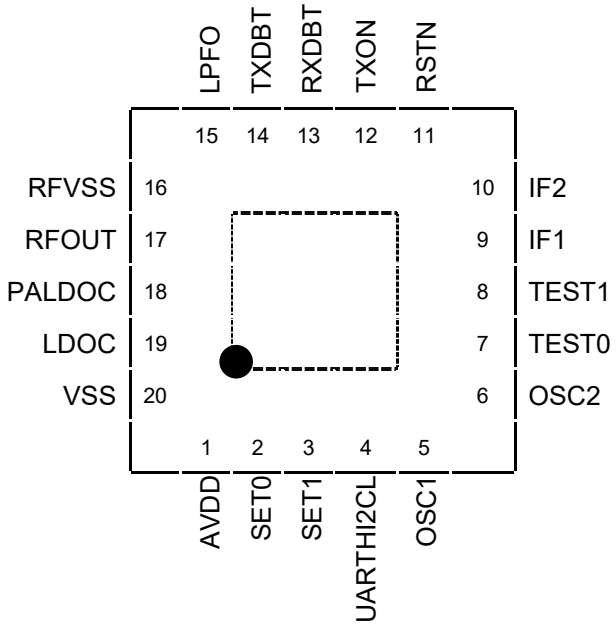


Figure 3. Pin configurations (Top view)

6.2. Functions

<The meaning of abbreviations used in the "I/O" column of the pin table is shown below>

AI:	Analog input pin	DO:	Digital output pin
AO:	Analog output pin	DIO:	Digital I/O pin
AIO:	Analog I/O pin	P:	Power supply pin
DI:	Digital input pin	G:	Ground pin

Pin #	Pin Name	I/O	Pin Functions	State after reset	Max. load capacitance	Pull-up/ Pull-down	Remarks
TX Section							
17	RFOUT	AO	RF signal output				
18	PALDOC	AO	Connection for an external TX output adjustment inductor to RFOUT pin.				
External Interface							
11	RSTN	DI	Reset pin				
9	IF1	DI	Interface input pin UART: RXD I^2C: SCL				Note 1
10	IF2	DIO	Interface input/output pin UART: TXD I^2C: SDA	UART: “H” I^2C: Hi-Z	UART:15 pF I^2C: 400 pF		Note 1
2	SET0	DI	Interface setting pin UART: UART Baud Rate setting “L”: 9,600bps “H”: 115,200bps I^2C: I^2C target address setting				
3	SET1	DI	Interface setting pin UART: UART interface Enable I^2C: I^2C target address setting				
13	RXDBT	DI	Low power timer Enable Inputs for Bluetooth certification tests				
14	TXDBT	DO	External MCU interrupt output Outputs pin for Bluetooth certification test	“H”	15pF		Note 2
4	UARTHI2CL	DI	Interface selection pin “H”: UART “L”: I^2C				
12	TXON	DI	RF transmit trigger pin				Note 3
7	TEST0	DI	For AKM Test			Pull-down	Note 3
8	TEST1	DI	For AKM Test			Pull-down	Note 3
Common Section							
19	LDOC	AO	Connection for external LDO output capacitor				Note 4
5	OSC1	AI	32MHz Crystal oscillator				
6	OSC2	AO	32MHz Crystal oscillator				
15	LPFO	AIO	Connection for an external capacitor for the loop filter				
Power Supply							
1	AVDD	P	Power supply				
16	RFVSS	G	Ground for RFAMP				
20	VSS	G	Ground				

Note 1 When using AK1595A with I^2C interface, the voltage to be pulled up must be the same as the AK1595A power supply voltage.
Note 2 Must be open if the pin is unused.
Note 3 Must be connect to VSS if the pin is unused.
Note 4 The LDOC pin must only be connected to a capacitor. Connecting it to any external device is prohibited.

Leave the exposed pad on the bottom surface of the package disconnected.

7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD	-0.3	4.0	V	Note 1
Ground Level	VSS	0	0	V	
Input Voltage 1	$V_{IN}1$	VSS-0.3	VDD+0.3	V	Note 1, Note 2
Input Voltage 2	$V_{IN}2$	VSS-0.3	2.0	V	Note 3
Input Current	I_{IN}	-50	+50	mA	
Output Current	I_{OUT}	-50	+50	mA	
Storage Temperature	Tstg	-55	+125	ºC	

Note 1 All voltages with respect to ground level (0V).
Note 2 Except LPFO pin
Note 3 LPFO pin

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

The specifications are applicable within the operating range (supply voltage/operating temperature) specified below.

Parameter	Symbol	Voltage	Ground Pin	Remarks
Ground Pin	VSS	0V	VSS, RFVSS	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating Temperature	Ta	-40		85	ºC	
Supply Voltage	VDD	2.0	3.0	3.6	V	AVDD pin

All voltages with respect to ground level (0V).
AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

9. Electrical Characteristics

The specifications below apply within the Recommended Operating Range (supply/operating temperatures).

9.1. Characteristics of RF Outputs

Parameter		Min.	Typ.	Max.	Unit	Remarks
Center Frequency Note1	Frequency 1	-	2402	-	MHz	
	Frequency 2	-	2426	-	MHz	
	Frequency 3	-	2480	-	MHz	
Output power	Maximum power setting		0		dBm	
	Minimum power setting		-32		dBm	
GFSK Note2	Average frequency deviation for 00001111 sequence (Δf).	±225	±250	±275	kHz	
	Ratio average frequency deviation (10101010 sequence / 00001111 sequence)	80	-	-	%	
	Minimum frequency deviation (Δfmin)	±185	-	-	kHz	
	Bit rate	-	1.0	-	Mbps	
	BT(Bandwidth-Time)	-	0.5	-		
	Modulation index (m)	0.45	0.50	0.55		m=(2*|Δf|) / (bit rate)
	In-band spurious emission			-20 -30	dBm dBm	1MHzBW @2MHz offset 1MHzBW @>3MHz offset

Note 1 Channel frequency means center frequency of modulation.
Note 2 GFSK characteristics based on Bluetooth Low Energy test specification (RF-PHY)

9.2. Current Consumptions

The specifications below apply within the Recommended Operating Range (supply/operating temperatures).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Full Power Down	SIDD1	Note1, Note 2		15		nA
Advertising	IDD1	Note1, Note 3		9.0		mA
Intermission	IDD2	Note1, Note 4		0.9		mA
Timer Active	IDD3	Note1, Note 5		0.5		μA

Note 1 VDD=3.0V, Room Temperature (25 ºC)
Note 2 RSTN pin = “L”
Note 3 TX_ch:2426MHz, RFOUT:0dBm
Note 4 <Address 0x08> EVENTNUM[2:0] bits ≠ 3'd1, UARTHI2CL pin =”H” and SET1 pin = “H”
Note 5 Low power timer active only. RSTN pin = "H" and RXDBT pin = "L" from full power down state.

9.3. Characteristics of 32 MHz Crystal Oscillator

Parameter	Min.	Typ.	Max.	Unit	Remarks
Oscillator Frequency		32.000		MHz	Note 1
Stabilization Time After Startup			2	msec	Note 2

Note 1 Frequency tolerance should be ±50ppm or less including external components.
Note 2 This is a reference value and not a guaranteed value.
Request a sample from the oscillator manufacturer for evaluation on the board, and check the oscillation characteristics before use.

9.4. Characteristics of Internal Oscillator

Parameter	Min.	Typ.	Max.	Unit	Remarks
Oscillator Frequency		8.192		kHz	
Oscillator Accuracy	-10		+10	%	Note 1, 3
	-50		+50	%	Note 2, 3, 4

Note 1 <Address 0x04> TIMER_CAL_DIS bit = “0”
Note 2 TIMER_CAL_DIS bit = “1”
Note 3 This is a reference value and not a guaranteed value.
Note 4 When transmitting with TXON pin, set the register to TIMER_CAL_DIS bit = “1”

9.5. Characteristics of Advertising IntervalTimer

Transmission interval

Parameter	Min.	Typ.	Max.	Unit	Remarks
Tch_int		Note 1		µsec	
advInterval	0.02		10.24	sec	15 control bits which is programmed by register Note 2
advDelay	0		10	msec	Randomly generated Note 2

Note 1 (8 + PDULEN bits) * 8 + 30 + 8 * CTE_LEN bits * CTE_ENB bit
When Bluetooth Low Energy RF-PHY certification testing, Tch_int = 625 or 1250 µsec, depending on <Address 0x09> RFPHY_INTVL bit.
Note 2 <Address 0x08> EVENTNUM[2:0] bits ≠ 3'd1

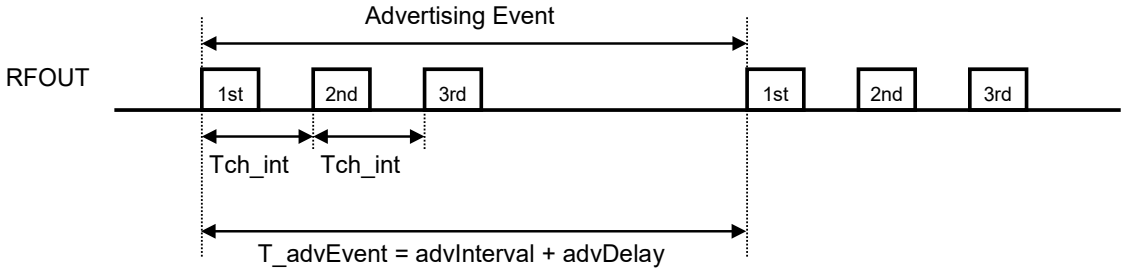


Figure 4. Interval of Advertising Event

10. Electric Characteristics of Digital Interface

The specifications are applicable within recommended operating range (supply voltage/operating temperature).

10.1. Digital DC Characteristics

Parameter	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	Note 1		0.7×VDD	-	-	V
Low Level Input Voltage	V_{IL}	Note 1		-	-	0.3×VDD	V
High Level Input Current	$I_{IH}1$	Note 1	V_{IH} = VDD	-10	-	+10	μA
Low Level Input Current	$I_{IL}1$	Note 1 Note 2	V_{IL} = VSS	-10	-	+10	μA
High Level Input Current	$I_{IH}2$	Note 2	V_{IH} = VDD	40	100	170	μA
High Level Output Voltage	V_{OH}	Note 3	I_{OH} = -100μA	0.8×VDD	-	-	V
Low Level Output Voltage (except SDA pin)	$V_{OL}1$	Note 3	I_{OL} = 100μA	-	-	0.2×VDD	V
Low Level Output Voltage for SDA pin	$V_{OL}2$	Note 4	I_{OL} = 3mA	-	-	0.4	V

Note 1 Digital input pins: RSTN, IF1, IF2, SET0, SET1, RXDBT, UARTHI2CL, TXON pins
Note 2 Digital input pins: TEST0, TEST1 pins
Note 3 Digital output pins: TXDBT, IF2(TXD) pins
Note 4 Digital output pin: IF2(SDA) pin

10.2. Digital AC Characteristics

Switchover timing of digital AC characteristics are specified at ½ VDD level unless otherwise noted.

10.2.1. System Reset

10.2.1.1. Hardware Reset

The AK1595A executes a hardware reset when the RSTN pin detects “L” for more than 1μsec and initializes all internal states. In order to ensure the AK1595A’s full hardware reset, the following setup and timing are required.

The AK1595A selects the UART interface;
IF1 pin = “H”, TXON pin = “L”.

The AK1595A selects the I^2C interface
IF1 pin = “H”, IF2 pin = “Hi-Z”, TXON pin = “L”.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Reset Pulse Width	tRSTN	1	-	-	μsec	

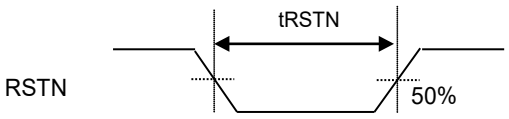


Figure 5. AC Timing of Hardware Reset

10.2.1.2. Software Reset

The AK1595A executes a software reset when <Address 0x3F>SOFTRST[7:0] bits are set to =8'b1010_1010 initializing internal digital blocks. The AK1595A state is changed to sleep when the I²C interface is used. It is changed to standby state when the UART interface is used. Therefore, the AK1595A needs reconfiguration of all blocks afterwards. The SOFTRST[7:0] bits automatically return to 8'b0000_0000 after software reset is executed. In order to ensure the AK1595A software reset, the following setup is required during reset period.

TXON pin = “L"

10.2.1.3. UART Interface Reset (UENABLE)

When the UART interface is selected, the UART I/F controller block is initialized when the SET1 pin (UENABLE) detects “Low” for more than 1µsec. In order to ensure the AK1595A UART interface is reset, the following setup and timing are required.

UARTHI2CL pin = “H” and IF1 pin = “H”

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
UART Reset Pulse Width	tURSTN	1	-	-	µsec	

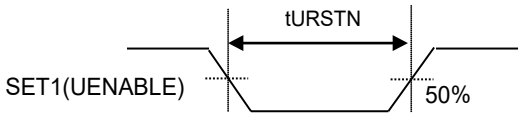


Figure 6. AC Timing of UART Interface Reset

10.2.2. TXON

The AK1595A starts transmission when the TXON pin detects “H” while the device is not in reset. The AK1595A stops transmission after a number of advertising events that as defined by <Address 0x08> EVENTNUM[2:0] bits ≠ 3'd0 even if TXON is set to “H”. The AK1595A will be able to start transmission again after TXON pin transitions from “L” to “H”. In this case, minimum 10 µsec low period is required.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
TXON "L" Pulse Width	tTXONL	10	-	-	µsec	

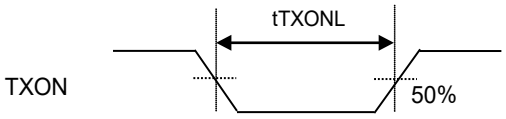


Figure 7. AC Timing of TXON

10.2.3. Serial Interface Timing of UART

When the UARTHI2CL pin is "H", the IF1 pin and IF2 pin operate as UART interfaces.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Baud Rate1	rBAUD	-	9,600	-	bps	SET0 pin: "L"
Baud Rate2	rBAUD	-	115,200	-	bps	SET0 pin: "H"
Baud Rate Accuracy (RXD)	bERR1	-	-	±2.5	%	Note 1
Baud Rate Accuracy (TXD)	bERR2			±2.5	%	Note 1
Byte Data Send Wait Time	tMIN	0	-	-	msec	
Command Turnaround Time	tTURN	0	-	-	msec	

Note 1 This is a reference value and not a guaranteed value.
While data is being received from the IF1 (RXD), the AK1595A does not transmitt from the IF2 (TXD).
Do not transmit data to the IF1 (RXD) while data is being transmitted from the IF2 (TXD).

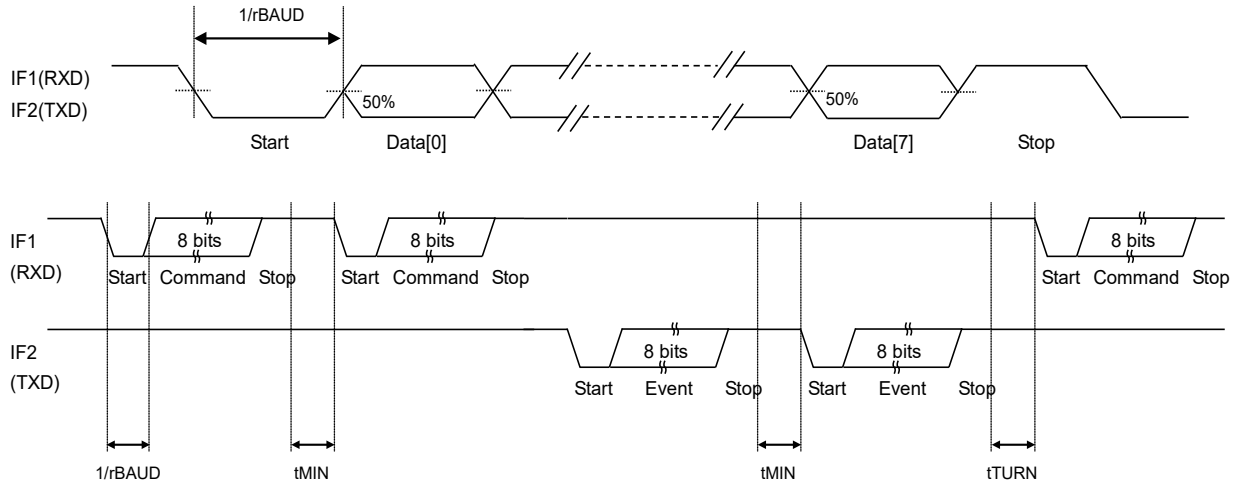


Figure 8. AC Timing of UART

10.2.4. Serial Interface Timing of I²C

When the UARTHI2CL pin is "L", the IF1 pin and IF2 pin operate as I²C interfaces. The AK1595A supports fast mode I²C interface (400kHz max.).

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µsec
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µsec
Clock Low Time	tLOW	1.3		-	µsec
Clock High Time	tHIGH	0.6		-	µsec
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µsec
SDA Hold Time from SCL Falling	tHD:DAT	0		-	µsec
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µsec
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µsec
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µsec
Setup Time for Stop Condition	tSU:STO	0.6		-	µsec
Capacitive load on bus	Cb	-		400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP			50	nsec

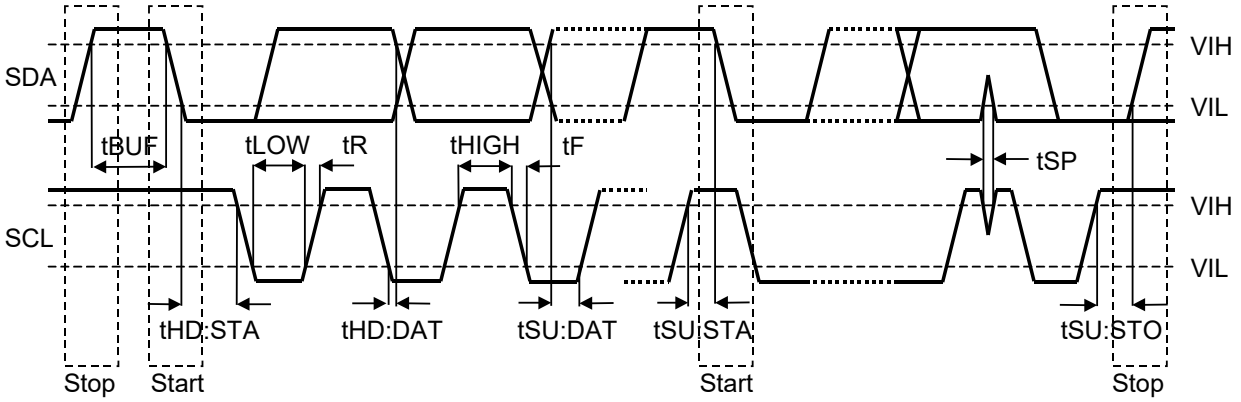


Figure 9. AC Timing of I²C

11. Serial Interface

The AK1595A supports UART and I²C interfaces and registers may be read from and written to using both interfaces. The AK1595A configures its selected interface by the UARTHI2CL, SET1, SET0 pins. The table below shows the interface configuration.

UARTHI2CL pin	Interface	SET1 pin	SET0 pin
L	I²C	I²C target address setting (CAD1)	I²C target address setting (CAD0)
H	UART	UART interface Enable (UENABLE)	UART Baud Rate setting (BRATE)

11.1. UART interface

11.1.1. Pin Condition

Connect the UARTHI2CL pin to VDD when the UART interface is used.
The IF1 pin = RX data (RXD)
The IF2 pin = TX data (TXD)
UART flow control is not supported.
The Baud Rate of the UART can be switched by the SET0 pin.
SET0 pin= “L”, 9600bps
SET0 pin= “H”, 115200bps

The UART interface is disabled when the SET1 pin (UENABLE) is set to "L". In this disable status, Data transfer from RXD and TXD both are disabled because the UART Interface control block is initialized.
When the AK1595A UART interface is used, the UART interface should be enabled by changing UENABLE “L” to “H”. At least 3 msec is required to start UART interface after UENABLE is set “L” to “H”.
Switching between UARTHI2CL pin and BRATE settings after reset release is prohibited. Switching between UARTHI2CL pin and BRATE settings during reset.

11.1.2. UART Format

The start bit is a single bit set to "0". The data is 8-bits and has no parity. The stop bit is a single bit, and this bit is set to 1. 8-bits data performs LSB first communication. Data received by the IF1 pin through the UART interface are defined as commands, and data sent by the IF2 pin are defined as events. The command and event formats are as follows:

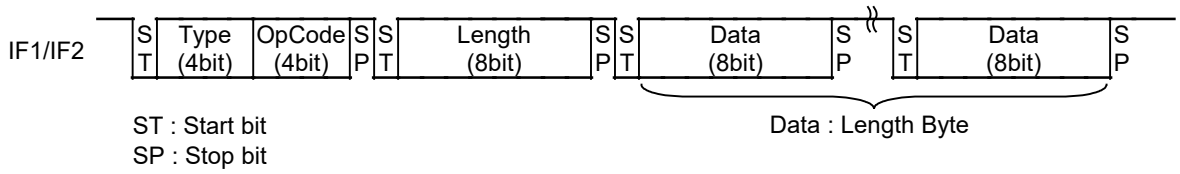


Figure 10. UART command/event format

The Type consists of 4-bits. When inputting commands from the RXD, set the Type bit to 4’b0001. Events from TXD are Type = 4’b0100.

Type	Function
4'b0001	Command
4'b0100	Event
Other than above	Prohibited

The OpCode consists of 4-bits. Specify an OpCode of 4'b0001 or 4'b0010 when accessing the register for Write or Read.

OpCode	Function
4'b0001	Write
4'b0010	Read
Other than above	Prohibited

The Length field shows the length of the subsequent command or data byte. The communication format for Data is specified in 11.1.3 General Description and 11.1.4 Read Access.

11.1.3. Write Access

The Figure 11 shows the format for write access to the AK1595A registers.

Type = 4'b0001
OpCode = 4'b0001.

The Length field shows total byte length of Start Address and Data for the write access. Total byte length is specified by the 6 LSBs (the two MSBs are Don't Care).

The Start Address byte specifies starting register access. Specify the register address with 6-bits of LSB. The first bit of MSB is "Don't Care" and the second MSB should be "0".

Data field specifies the data to be written to the register.

The AK1595A can write multi-byte data with a single operation. When the Length is set 3 or more and data is sent after the first one-byte transfer, the AK1595A's address counter is automatically incremented and data is written to the next address. The increment of the address counter stops at 6'h3D. It is prohibited to set the Length and Start Address to 6'h3D when the last data is received. In addition, the <Address 0x3F> SOFTRST bits cannot be written by counter increment. When accessing SOFTRST bits, set Length to 6'h02 and Start Address A[5:0] to 6'h3F

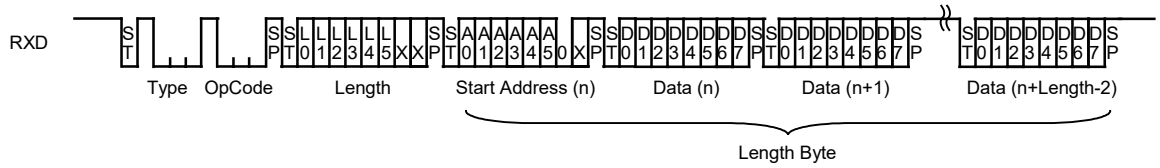


Figure 11. Write access command (RXD)

When the write access command is done, the TXD outputs events within 2 msec. The event format is as follows.

Type = 4'b0100
OpCode = 4'b0001
Length is 8'b0000_0001

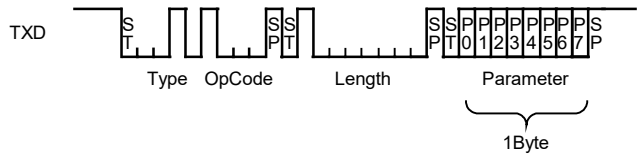


Figure 12. Write access event (TXD)

The parameter is as follows. When a command error occurs, the TXD output 8'b0000 0001 (command failed) as a parameter. Refer to 11.1.5 Command Failed for the command error conditions.

Parameter	Function
8'b0001_0000	Command succeeded
Other than above	Command failed

11.1.4. Read Access

The following format shows the read access to the registers from RXD.
Type = 4'b0001
OpCode = 4'b0010
The Length shows total byte length of Start Address and Stop Address for the read access. Total byte length is specified by the 6-bits LSBs (the two MSBs are Don't Care). 6'h02 should be specified in Length.

The Stop Address setting can be omitted by setting Length to 6'h01 when a single address is read. The Start Address is the byte that specifies starting register access. The Stop Address specifies ending register access. Specify register addresses with the six LSBs. The first MSB is "Don't Care" and the second MSB should be "0". When the same data is set to both the Start Address and Stop Address, a single address is read. When the Start Address and Stop Address are set to different addresses, the AK1595A supports multi-byte data read. Stop Address data should be higher than Start Address data.

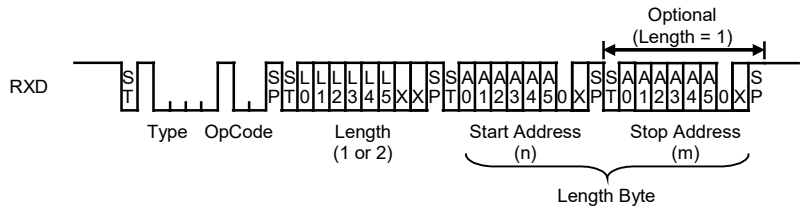


Figure 13. Read access command (RXD)

When the write access command is done, the TXD outputs events within 2 msec. The event format is as follows.
Type = 4 and b0100
OpCode = 4 b0010
The Length is total data from Start Address and Stop Address.

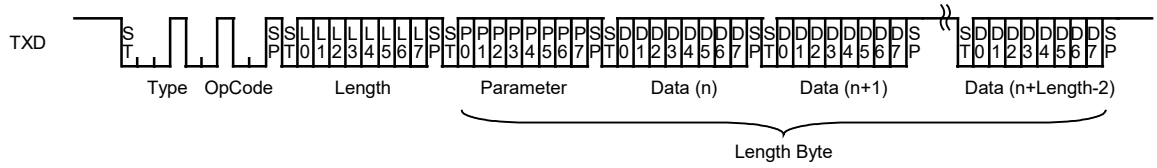


Figure 14. Read access event (TXD)

The Parameter is as follows. When a command error occurs, the TXD output 8'b0000 0001 as a Length and 8'b0000 0001 (command failed) as a parameter. In this case, the AK1595A outputs TXD to Parameter and data is not transmitted. Refer to Section 11.1.5 Command Failed for the condition of commands errors.

Parameter	Function
8'b0001_0000	Command succeeded
Other than above	Command failed

On command success, the AK1595A can read the data as specified by the Start Address and Stop Address. The AK1595A transfers one-byte of Data and then increments the address counter to read the next address's data. The incrementation of the address counter stops at 6'h3F. The result of reading an address not defined on on the Register Map or a write-only address is "0".

11.1.5. Command Failed

The following state shows error condition of Write or Read access to the AK1595A register. The TXD outputs 8'b0000 0001 (command failed) as an event parameter when command error occurs. The TXD outputs OpCode 4'b0000 when an error is caused by OpCode.

Error judgment item	Error condition of Write command	Error condition of Read command
Type	Other than 4' b0001	
OpCode	Other than 4' b0001 and 4'b0010	
Length	6'h00, 6'h01, 6'h3F	Other than 6'h01, 6'h02
Start Address	6'h3D or more	
Relation between Start Address and Stop Address	-	Start Address > Stop Address
Last value of address counter	6'h3D	-

11.1.6. Command and Event Timing

The commands to the RXD and the events from the TXD as follows. The TXD doesn't output data while the RXD is receiving data. It is not allowed to transmit Data to the RXD while the TXD is transmitting.
It is required to input whole byte data that is specified in Length to RXD. TXD doesn't output events unless commend transfer is finished. The TXD outputs events in 2 msec when all command, that is specified in Length, is received

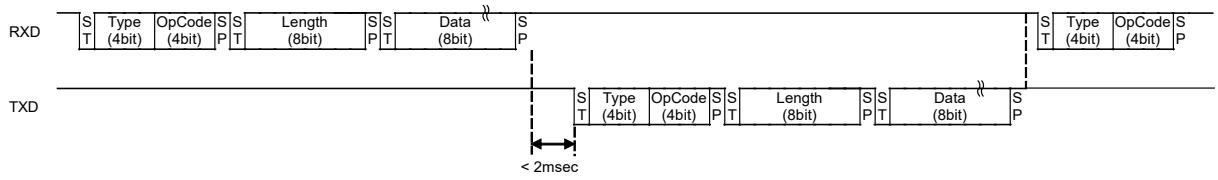


Figure 15. UART Command and Event Timing

If the start bit is not detected by TXD more than (1/rBAUD×10) sec when the Length specified bytes of data have not been transmitted, the following process is required.

To set ENABLE to "L"; This is to initialize I/F control block.
To set ENABLE to "H"
To wait minimum 3 msec
To resend commands

Or

Execute a hardware reset; This is to initialize all internal blocks.
Set all AK1595A setting again.

11.2. I²C interface

The I²C bus interface of AK1595A supports the standard mode (100 kHz max.) and the fast mode (400 kHz max.).

11.2.1. Pin Condition

When using the I²C interface, connect the UARTHI2CL pin to VSS. For the I²C interface, IF1 pin corresponds to the clock (SCL) and IF2 pin corresponds to the data (SDA). The lower 2-bits of the I²C target address of this IC can be switched by SET1, SET0 pin. The SET1 pin supports CAD0 by CAD1, SET0 pin. The target address is as follows:

CAD1 (SET1 pin)	CAD0 (SET0 pin)	I²C target address
0	0	7'b01010_00
0	1	7'b01010_01
1	0	7'b01010_10
1	1	7'b01010_11

It is prohibited to change the setting of UARTHI2CL pin and CAD1, CAD0 after reset. Change the settings while the hardware reset applied.

11.2.2. Data transfer

To access AK1595A on the bus, generate a start condition first.
Next, transmit a one-byte target address. The AK1595A compares the target address with its own address. If these addresses match, AK1595A generates an acknowledgement, and then executes Read or Wrte access. At the end of access, generate a stop condition.

11.2.2.1. Change of data

A change of data on the SDA line must be made during the “L” period of the clock on the SCL line. When the SCL line is “H”, the state of the SDA line must be stable. (Data on the SDA line can be changed only when the SCL line is “L”.)
While the SCL line is “H”, the state of data on the SDA line is changed only when a start condition or a stop condition is generated.

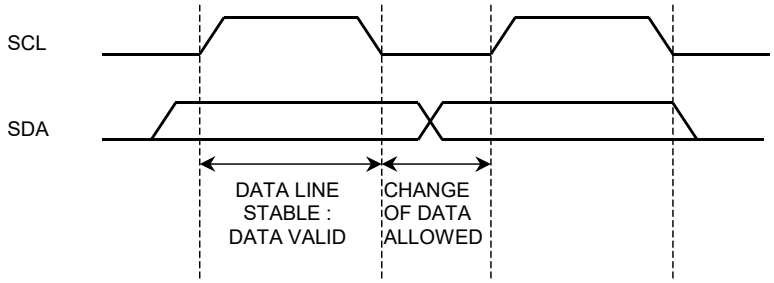


Figure 16. Data Change

11.2.2.2. Start / Stop Condition

If the SDA line is driven to “L” from “H” when the SCL line is “H”, a start condition is generated.
Every access starts with a start condition.
If the SDA line is driven to “H” from “L” when the SCL line is “H”, a stop condition is generated.
Every access stops with a stop condition.

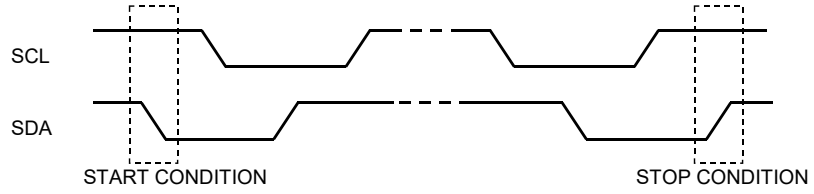


Figure 17. Start / Stop Conditions

11.2.2.3. Acknowledge

The IC that is transmitting data releases the SDA line (in the “H” state) after sending 1-byte data.
The IC that receives the data drives the SDA line to “L” on the next clock pulse. This operation is referred to as “acknowledge.” This operation may be used to verify that data has been transferred successfully.

AK1595A generates an acknowledge after reception of a start condition and target address.
When a Write access is executed, AK1595A generates an acknowledge after every byte is received.
When a Read access is executed, AK1595A generates an acknowledge then transfers the data stored at the specified address. Next, AK1595A releases the SDA line then monitors the SDA line. If a controller IC generates an acknowledge instead of a stop condition, AK1595A transmits the 8-bits data stored at the next address. If no acknowledge is generated, AK1595A stops data transmission.

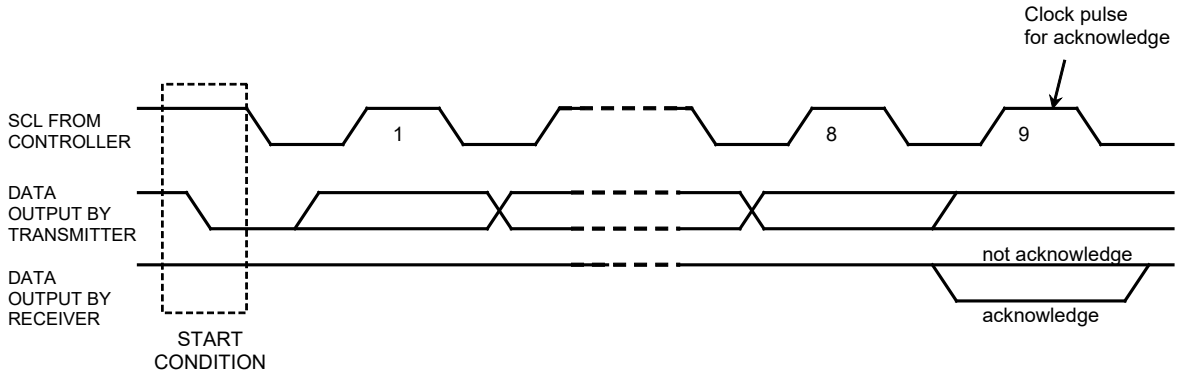


Figure 18. Generation of acknowledge

11.2.2.4. Target Address

The first byte, including the target address, is entered after the start condition, and the target address selects the IC on the bus to be accessed.
The target address consists of the upper 7-bits. The upper 5-bits are fixed to 5'b01110 and the lower 2-bits can be selected by SET1 pin or SET0 pin. When a target address is input, the IC that matches the target address generates an acknowledge and then executes the access. The 8th bit (LSB) of the first byte is R/W bit. When R/W bit = "1", the Read access is executed. When R/W bit = "0", the Write access is executed.

MSB 5 bit (fixed)					CAD1	CAD0	R/W bit
0	1	0	1	0	0/1	0/1	R/W

Figure 19. Structure of the first byte

11.2.3. Write Access

When the R/W bit is set to “0”, AK1595A performs a write operation.
In a write operation, AK1595A generates an acknowledge after receiving a start condition and the first byte (target address) then receives the second byte. The second byte is used to specify the register address and is based on the MSB-first configuration.
The second byte MSB 1st bit is don't care. The second byte MSB second bit is "0".

X	0	A5	A4	A3	A2	A1	A0

Figure 20. Configuration of the second byte (Register Address)

After receiving the second byte (register address), AK1595A generates an acknowledge then receives the third byte. The third and the following bytes represent data. Data consists of 8-bits and is based on the MSB-first configuration. AK1595A generates an acknowledge after every byte is received. Data transfer always stops with a stop condition generated by the controller.

D7	D6	D5	D4	D3	D2	D1	D0

Figure 21. Configuration of the 3rd byte or later (Data)

AK1595A can write multiple bytes of data at a time. After reception of the third byte (control data), AK1595A generates an acknowledge then receives the next data. If, after receiving one byte of data, additional data is received instead of a stop condition, the AK1595A’s address counter is automatically incremented and the data is written to the next address. The address is incremented from 0x00 to 0x3C. When the start address is “0x00”, the address is repeatedly incremented as. “0x00 -> 0x01 ->…-> 0x3B -> 0x3C -> 0x00 -> 0x01…
Address 0x3F cannot be written by the incrementing function. If accessing address 0x3F, set the address of the internal address counter to 6'h3F.

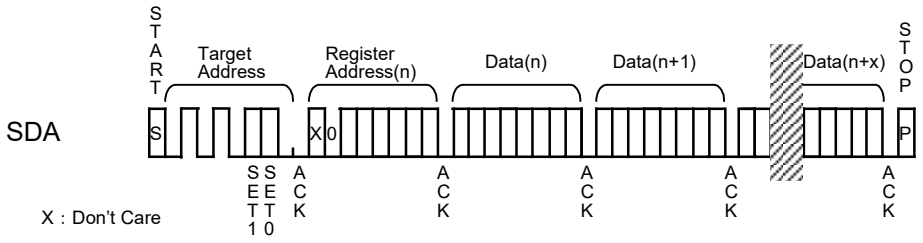


Figure 22. Write access

11.2.4. Read Access

When the R/W bit is set to “1”, AK1595A performs a read operation.
If a controller IC generates an acknowledge instead of a stop condition after AK1595A transfers the data at a specified address, the data at the next address can be read.
Address can be 0x00h to 0x3C.
The address is incremented 0x00 -> 0x01 ->…-> 0x3B -> 0x3C and the address goes back to 0x00 after 0x3C.

11.2.4.1. Current Address Read Access

In a current address read operation, the data at the address specified by the AK1595A’s address counter is read. The address counter holds the address that follows the most recently accessed address. For example, if the address most recently accessed (either Read or Write Access) is address “n”, and a current address read operation is attempted, the data at address “n+1” is read. In current address read operation, AK1595A generates an acknowledge after receiving a target address for the Read access (R/W bit = “1”). Next, AK1595A transfers the data specified by the address counter starting with the next clock pulse, then increments the address counter by one. If the controller IC generates a stop condition instead of an acknowledge after AK1595A transmits one byte of data, the read operation stops.

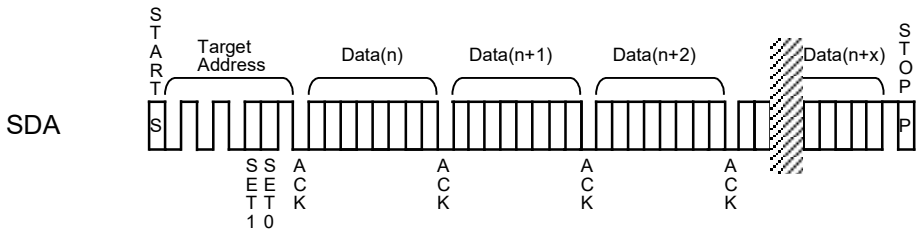


Figure 23. Current address read access

11.2.4.2. Random Read Access

By random address read operation, data at an arbitrary address can be read.
The random address read operation requires sending a dummy Write access before the target address for the Read access (R/W bit = “1”) is transmitted. In random read operation, a start condition is first generated then a target address for the Write access (R/W bit = “0”) and a read address are transmitted sequentially.
After AK1595A generates an acknowledge in response to this address transmission, a start condition and a target address for the Read access (R/W bit = “1”) are generated again. AK1595A generates an acknowledge in response to this target address transmission. Next, AK1595A transfers the data at the specified address then increments the address counter by one. If the controller IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.

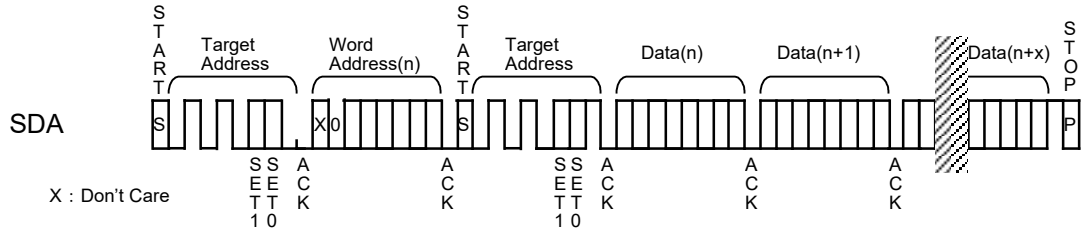


Figure 24. Random read access

12. RF Transmission

12.1. Start of Transimission

Writing <Address 0x3C>TX_ENB bit = “1” or switching the TXON pin from "L" to "H" generates an advertising event and allows the data set in the register to be transmitted by RF. When TXON pin is set to "H", 32-MHz clock is generated. TXON pin levels are detected after waiting 32768 clocks for clock stabilization.

If an advertising transmission is started by writing TX_ENB bit= ”1”, the burst transmission is terminated and the TX_ENB bit is initialized after the number of advertising events specified by the <Address 0x08> EVENTNUM bits.

When EVENTNUM[2:0] bits = 3'd0, after advertising transmission is started, burst transmission continues until TX_ENB bit = “0” and TXON pin is "L".

If the TXON pin is set to "H" to start transmission and the specified number of Interval of Advertising Event ends when EVENTNUM[2:0] bits ≠ 3'd0, transmission will not be performed again even if TXON pin remains "H". Transmission can be restarted by setting the TXON pin to "L" for 10 µsec or longer and then setting the TXON pin to "H" again.

If EVENTNUM[2:0] bits ≠ 3'd0, burst transmission can be forcibly terminated whenTX_ENB bit = “0” and TXON pin is "L"

Control by the TXON pin is disabled while RF transmission is being performed by the TX_ENB bit or <Address 0x3C> BLE_TEST_ENB bit. Control of RF transmission start/stop by the TX_ENB bit or BLE_TEST_ENB bit is also disabled while RF transmission is being performed by the TXON pin.

Whether or not the AK1595A has completed transmission can be checked by reading <Address 0x3C>TX_START bit.

12.2. Advertising Event

The number of advertising events can be set in the EVENTNUM bits. The AK1595A automatically enters sleep or standby after sending the specified number of times. The interval (advInterval) of the advertising event can be changed via the <Address 0x0A to 0x0B> ADVINTVL[14:0] bits. <Address 0x0A>ADVDELAY_ENB bit = "1", the advertising event time (T_advEvent) meets the Bluetooth Core Specifications. The current consumption during the interval is IDD2 intermission as described in 9.2 Current Consumptions.

Transmission interval can also be managed by the external MCU by setting EVENTNUM[2:0] bits=3'h1 to control the TXON pin or TX_ENB bit.

13. Power-up Flow

13.1. Operational Stats

The following states are managed by the power-down control and timing control block of the digital part.
For transition conditions, refer to 13.2 UART Power-up Flow and 13.3 I2C Power-up Flow.

State	Symbol	Description
Full power down	FPD	RSTN pin = “L”. All blocks are powered down. All registers have been initialized.
Sleep	SLP	(RSTN pin = “H” and UARTHI2CL pin = “L” or RSTN pin = “H” and UARTHI2CL pin = "L" and SET1 pin = "L") and No advertising event. The AK1595A holds the register value in the sleep state.
Stand-by	STB	RSTN pin = “H” and UARTHI2CL pin = “H” and SET1 pin = H and No advertising event
Advertising	ADV	<Address 0x3C> TX_ENB bit = “1” or TXON pin = “H” Transmitting RF during advertising.
Intermission	IMS	There are two types of intermission states. 1. (EVENTNUM[2:0] bits ≠ 3'd1 and TX_ENB bit = “1” or EVENTNUM[2:0] bits ≠ 3'd1 and TXON pin = "H”) and No RF transmission is being performed for the period from the end of the advertising state to the next advertising state. 2. In Bluetooth Certification mode, waiting for HCI command or, waiting for the duration of the period between the end of one advertising state and the next.

The term” burst transmission” means repeating the advertising and intermission states.

13.2. UART Power-up Flow

Figure 25 shows the status transition when the UART interface is selected (UARTHI2CL pin = "H"). The table below shows the transition conditions.

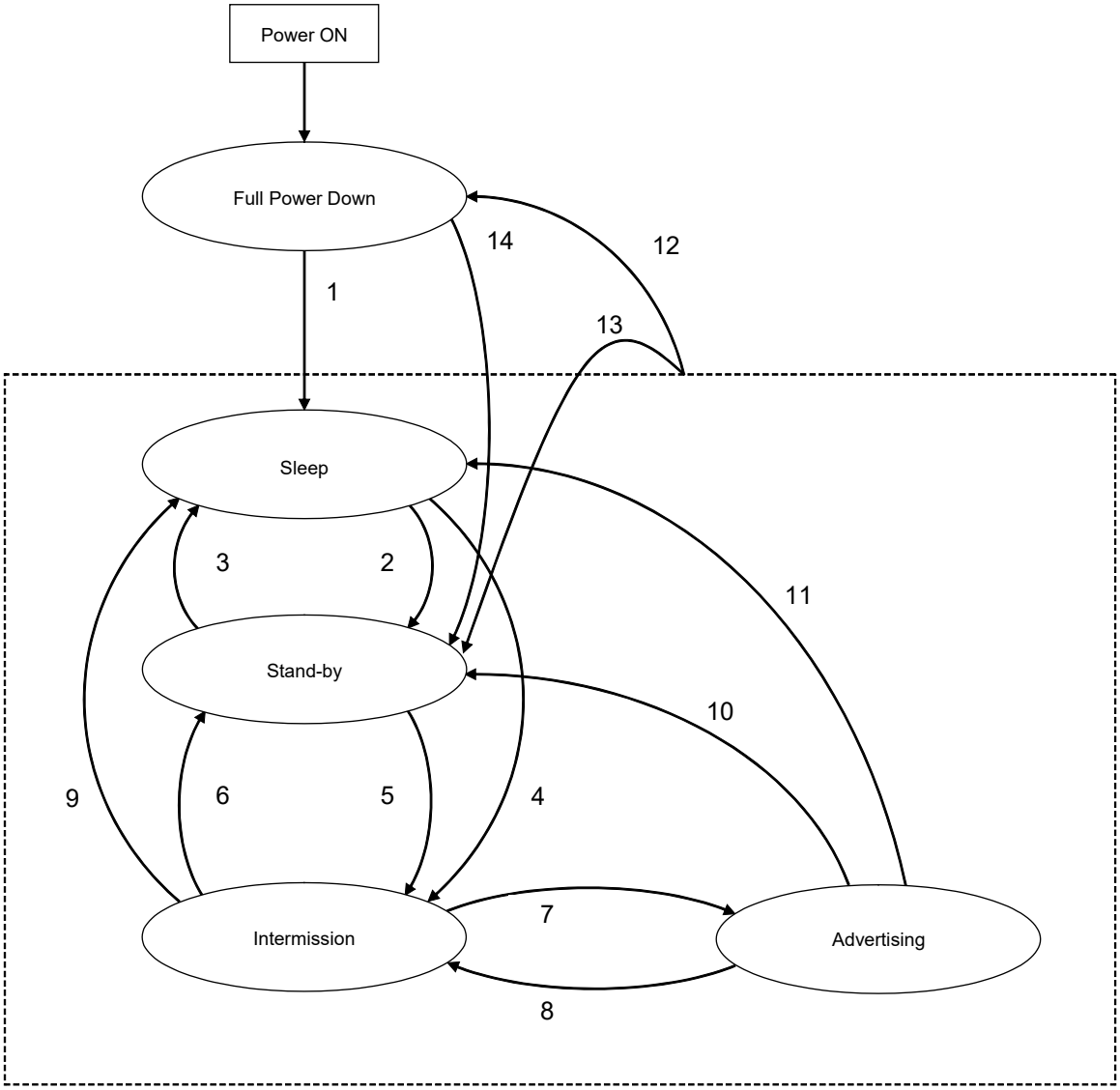


Figure 25. AK1595A UART power up flow

Transition	Transition condition
1	Release the reset when SET1 pin = "L" (RSTN pin = "H").
2	Enable UART interface (SET1 pin = "H").
3	Disable the UART interface (SET1 pin = "L").
4	Starts sending (TXONpin = "H")
5	Starts transmitting (either TXON pin = "H" or <Address 0x3C> TX_ENB bit = “1”) or Transition to Bluetooth certification test mode (<Address 0x3C> BLE_TEST_ENB bit = “1”)
6	When the UART interface is enabled (SET1 pin = "H"), Transmit stopped (TXON pin = "L" or TX_ENB bit = “0”) or End of Bluetooth certification test mode (BLE_TEST_ENB bit = “0”)
7	When the HCI LE Transmitter Test or HCI LE Set Advertising Enable (Enable) command is entered in the Bluetooth certification test mode, When the advertising interval ends because the number of events specified by the <Address 0x08> EVENTNUM bits has not been transmitted.
8	At the end of transmission of the selected advertising channel, <Address 0x03> The number of events specified by the EVENTNUM bits have not been transmitted, When HCI LE Test End or HCI LE Set Advertising Enable (Disable) or HCI Reset commands are inputted in Bluetooth certification test mode.
9	When the UART interface is disabled (SET1 pin = "L"), Transmit stopped (TXON pin = "L")
10	When the UART interface is enabled (SET1 pin = "H"), Transmission of the number of events specified by the EVENTNUM bits is completed at the end of transmission of the selected advertising channel, or Transmit stopped (TXON pin = "L" or TX_ENB bit = “0”) or When HCI LE Test End or HCI LE Set Advertising Enable (Disable) or HCI Reset commands are entered in the Bluetooth certification test mode.
11	When the UART interface is disabled (SET1 pin = "L"), At the end of transmission of the selected advertising channel, the transmission of the number of events specified by the EVENTNUM bits are completed, or Transmit stopped (TXON pin = "L")
12	Hardware reset with TXON pin = "L" (RSTN pin = "L") Note: Hardware resets are prohibited while TXON pin = "H".
13	Software reset (<Address 0x3F> SOFTRST[7:0] bits = 8'hAA) with TXON pin = "L" Note 1 Software reset is prohibited when TXON pin = "H". Note 2 The AK1595A initializes internal registers by the software reset.
14	Release the reset when SET1pin = "H" (RSTN pin = "H").

13.3. I²C Power-up Flow

Figure 26 shows the state transition when the I²C interface is selected (UARTHI2CL pin = "L"). The table below shows the transition conditions.

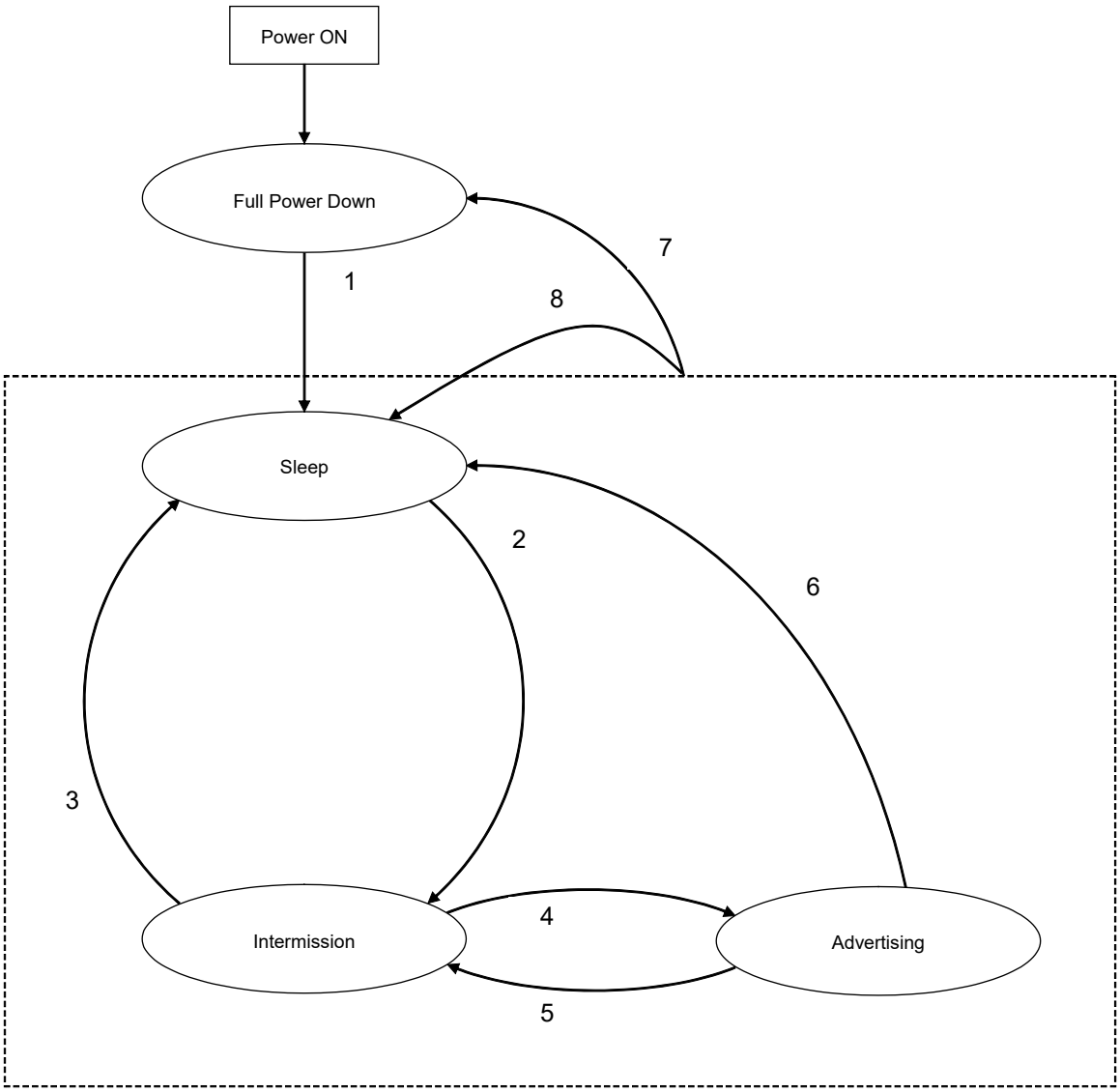


Figure 26. AK1595A I²C power up flow

Transition	Transition condition
1	Release of reset (RSTN pin = "H")
2	Starts transmitting (either TXON pin = "H" or <Address 0x3C> TX_ENB bit = “1”) or Transition to Bluetooth certification test mode (<Address 0x3C> BLE_TEST_ENB bit = “1”)
3	Transmit stopped (TXON pin = "L" or TX_ENB bit = “0”) or End of Bluetooth certification test mode (BLE_TEST_ENB bit = “0”)
4	When the HCI LE Transmitter Test or HCI LE Set Advertising Enable (Enable) command is entered in the Bluetooth certification test mode, When the advertising interval ends because the number of events specified by the <Address 0x08> EVENTNUM bits has not been transmitted.
5	At the end of transmission of the selected advertising channel, The number of events specified by the EVENTNUM bits have not been transmitted, When HCI LE Test End or HCI LE Set Advertising Enable (Disable) or HCI Reset commands are entered in Bluetooth certification test mode.
6	When transmission of the selected advertising channel ends for the number of events specified by the EVENTNUM bits. Or stop transmitting (TXON pin = "L" or TX_ENB bit = “0”).
7	Hardware reset (RSTN pin = "L") Note: It is prohibited to perform a hardware reset while TXON pin = "H".
8	Software reset (<Address 0x3F> SOFTRST[7:0] bits = 8'hAA). Note: It is prohibited to perform a software reset while TXON pin = "H

13.4. UART power up Sequence

Figure 27 shows a sample startup sequence using the UART interface.
Connect the UARTHI2CL pin to VDD. <Address 0x08> EVENTNUM[2:0] bits = 3'd1 setting.

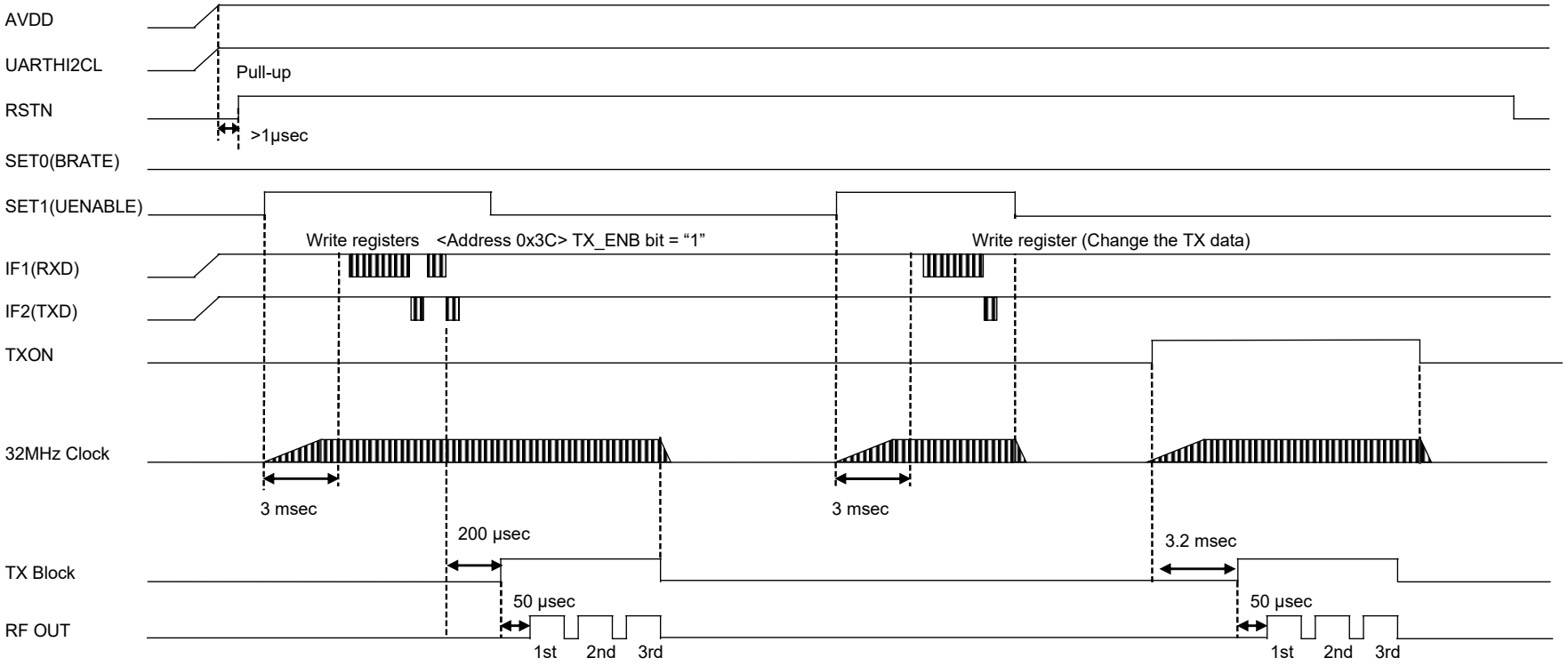


Figure 27. Flow of power up sequence (UART Interface)

13.5. I²C power up sequence

An example of the startup sequence using the I²C interface is shown in Figure 28.
Connect the UARTHI2CL pin to VSS. <Address 0x08> EVENTNUM[2:0] bits = 3'd2 setting.

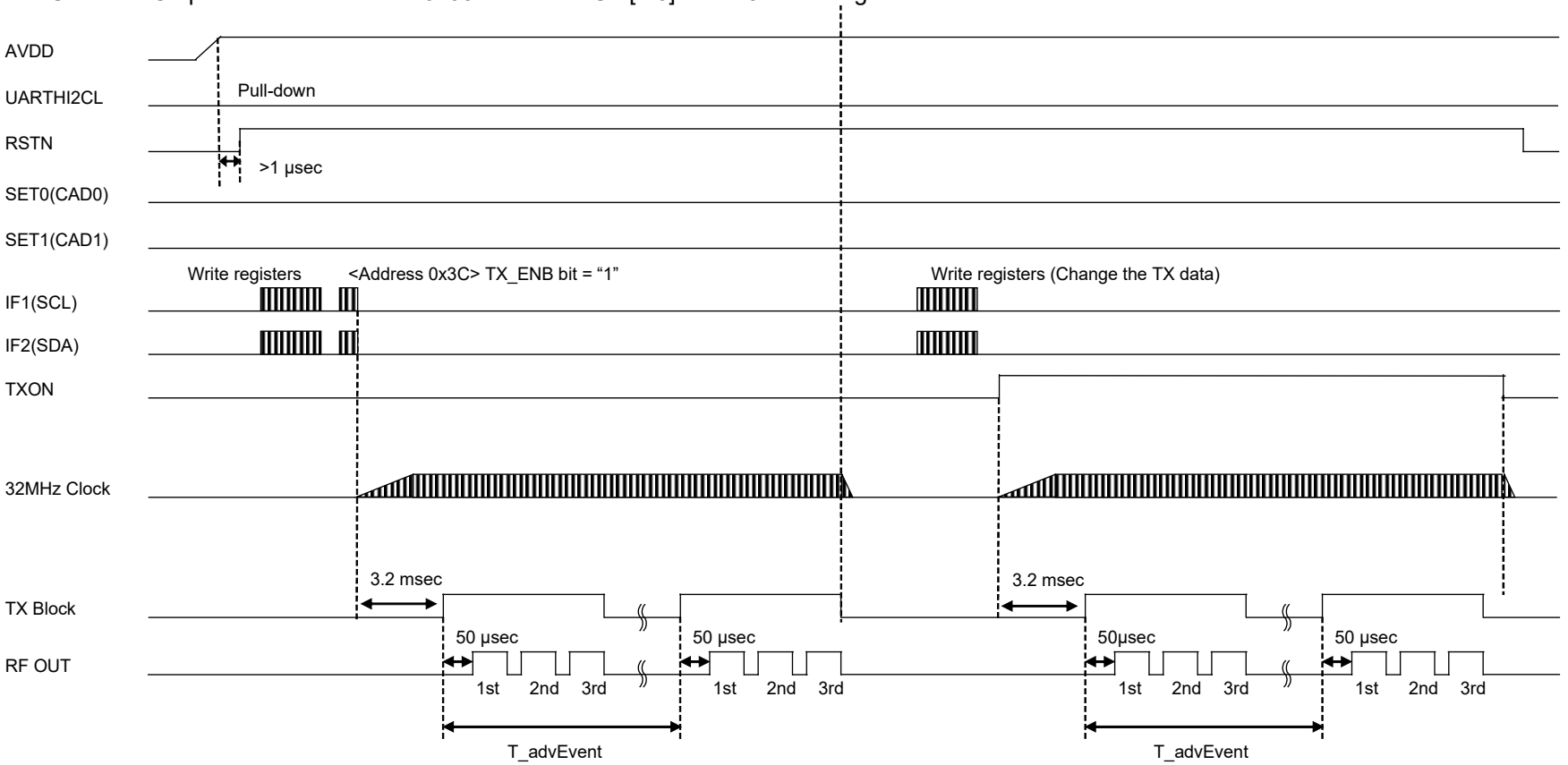


Figure 28. Flow of power up sequence (I²C Interface)

14. Transmission interval control with low current consumption

The AK1595A can manage the transmit interval time with ultra low current consumption by using internal low power timer.

14.1. Low power timer setting

The conditions under which the low power timer is enabled are as follows.

Low power timer	RSTN pin	RXDBT pin
Disable	L	Don't care
Disable	H	H
Enable	H	L

A low power timer set by <Address 0x04 to 0x05> TIMER_SET[11:0] bits.

TIMER_SET[11:0]	Timer setting [sec]
0000_0000_0000	2
0000_0000_0001	2
0000_0000_0010	2
0000_0000_0011	3
~	~
0111_1111_1111	2047
1000_0000_0000	2048 (default)
1000_0000_0001	2049
~	~
1111_1111_1110	4094
1111_1111_1111	4095

14.2. Low power timer calibration

The AK1595A can calibrate low power timers using 32MHz as a reference clock. Setting the <Address 0x04> TIMER_CAL_DIS bit = "0" enables the calibration of the low power timer.
Calibration of the low power timer is performed under the following conditions.

I^2C interface selected:
After the 32MHz crystal oscillator circuit starts up and outputs 4,096 clocks
Note: The 32MHz crystal oscillator will operate until calibration is complete

UART interface selected:
Set to <Address 0x3C> TX_ENB bit = "1"
When RF transimission automatically performed after the time set by TIMER_SET bits has elapsed with <Address 0x04> INTRPT_MODE bit = "0".
Note: The 32MHz crystal oscillator will operate until calibration is complete. When using UART, set SET1 pin = "L" except when accessing AK1595A registers.

14.3. Interrupt mode

The AK1595A can output an Interrupt signal from the TXDBT pin to the external MCU. The interrupt signal output has two modes, set by <Address0x04> INTRPT_MODE bit. The initial state of the TXDBT pin is “H”.

INTRPT_MODE bit = “0”

One second before the set time of <Address 0x04 to 0x05> TIMER_SET bits, the AK1595A outputs TXDBT pin “L” for 1 second, then returns to “H” output, and the AK1595A automatically RF transmit RF signal.

In this case, set <Address 0x08>EVENTNUM [2:0] bits = 3’h1. The number of RF transimissions can not be changed.

INTRPT_MODE bit = “1”

When the set time of TIMER_SET bits is reached, the AK1595A outputs TXDBT pin = “L”.

TXDBT pin returns to “H” when <Address 0x3C>TX_ENB bit = “1” is written. The AK1595A does not transmit RF signal until TX_ENB bit = “1” is written.

In this case, the number of RF transmissions can be changed according to the EVENTNUM bits. Note that once RF transmission is started, the 32MHz crystal oscillator circuit continues to operate until RF transmission is stopped, so be careful of current consumption.

14.4. Example of connecting the AK1595A and the External MCU

An example of connecting the AK1595A and the external MCU is shown below.

AK1595A pin	Direction	External MCU pin function
TXDBT	->	Interrupt
RSTN	<-	Reset
IF1	<-	I^2C or UART
IF2	<->	I^2C or UART
SET1 (UART only)	<-	UENABLE control (UART only)
RXDBT	<-	“L” output or Tie to GND

When using UART, set SET1 pin = “L” except when accessing AK1595A registers.

14.5. System Sequence

Figure 29 shows the system sequence with <Address 0x04> INTRPT_MODE bit = “0”.
After the external MCU internal reset and runs the program to access the AK1595A registers. Set <Address 0x08>EVENTNUM [2:0] bits = 3’h1.
After the MCU sets <Address 0x3C> TX_ENB bit = “1”, the AK1595A transmit RF signal. The MCU shifts to a power-down state due to waiting for an interrupt.
One second before the time set by <Address 0x04 to 0x05> TIMER_SET[11:0] bits, the AK1595A outputs TXDBT pin “L” for 1 second.
After AK1595A outputs TXDBT pin “L” for 1 second, the AK1595A changes TXDBT pin from “L” to “H” and transmits RF signal automatically.
The AK1595A settings and PDU data can be changed by accessing the AK1595A registers in the MCU interrupt program during the TXDBT pin = "L".
If there is no register access of the AK1595A during the interval when TXDBT pin = "L", the AK1595A send the same settings and data by RF at the time interval of TIMER_SET bits setting.

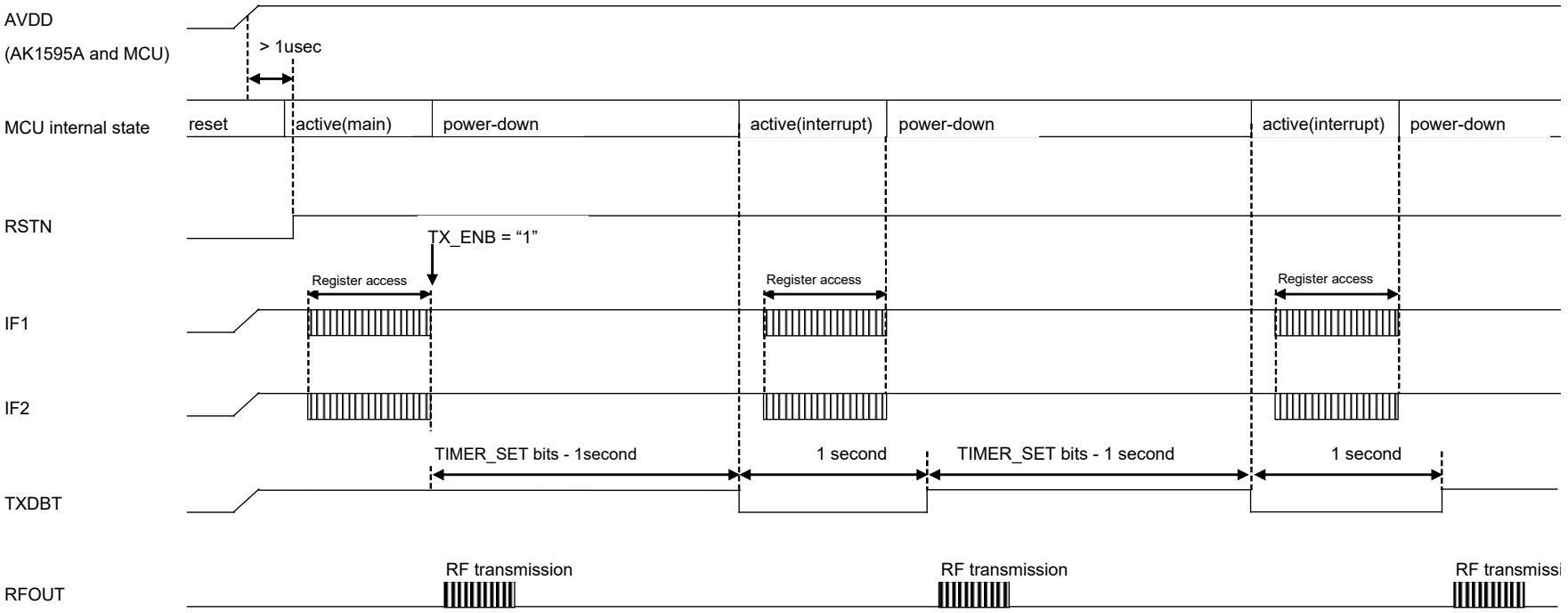


Figure 29. Flow of System Sequence (INTRPT_MODE bit = “0”)

Figure 30 shows the system sequence with <Address 0x04> INTRPT_MODE bit = “1”
After the external MCU internal reset and runs the program to access the AK1595A registers.
After the MCU sets <Address 0x3C> TX_ENB bit = “1”, the AK1595A transmit RF signal. The MCU shifts to a power-down state due to waiting for an interrupt.
The time set by <Address 0x04 to 0x05>TIMER_SET bits, the AK1595A change TXDBT pin “H” to “L”.
The TXDBT pin = “L” causes the interrupt program of the MCU to run and set the AK1595A register again. Then, the MCU shifts to the power-down state again.
When TX_ENB bit written “1” by MCU, The AK1595A TXDBT pin change “L” to “H” and transmit RF signal.

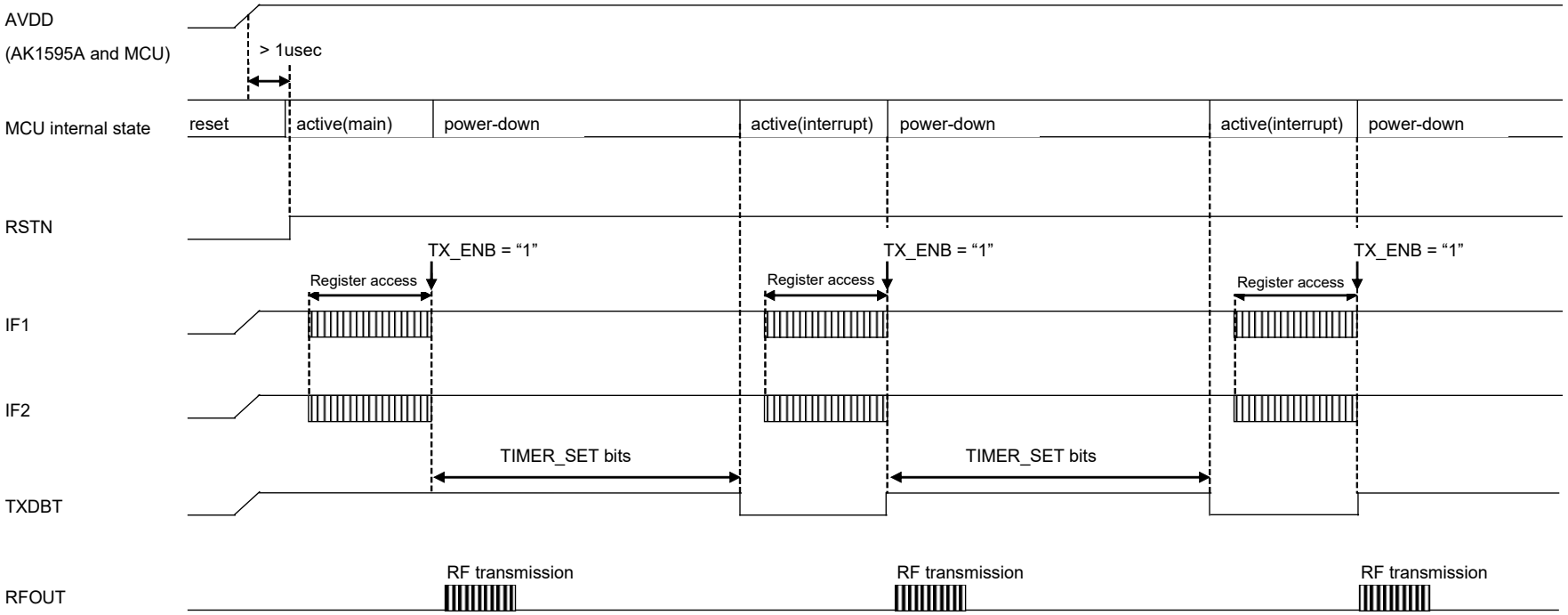


Figure 30. Flow of System Sequence (INTRPT_MODE bit = “1”)

15. Bluetooth Test Specification

15.1. Bluetooth Test Circuit

AK1595A integrated Bluetooth certification test function.
If performing a Bluetooth certification test, the AK1595A should be connected to the level shifter circuit and Bluetooth tester as shown in Figure 31, and set the<Address 0x3C> BLE_TEST_ENB bit = “1”.

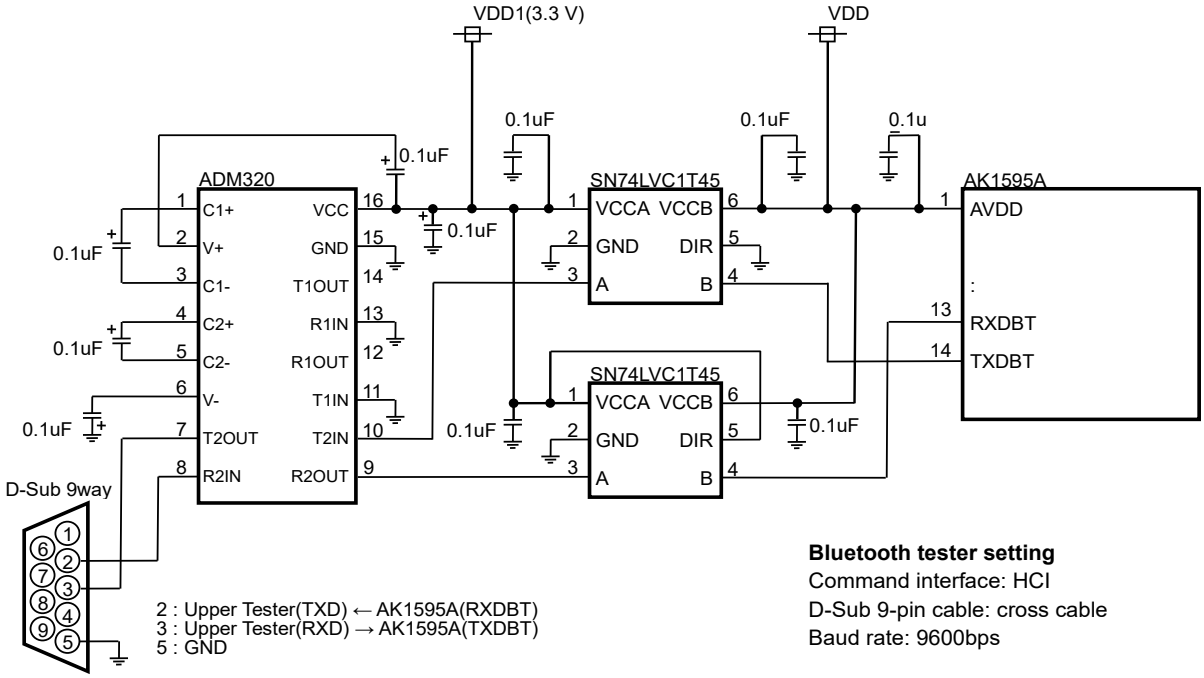


Figure 31. Bluetooth Test Setup

15.2. Test Plan

Bluetooth test plans except listed below are not guaranteed.

RF-PHY

Test Cases		Register Settings
RF-PHY/TRM-LE/CA/BV-01-C	Output power	RF-PHY1
RF-PHY/TRM-LE/CA/BV-03-C	In-band emissions	RF-PHY1
RF-PHY/TRM-LE/CA/BV-05-C	Modulation characteristics	RF-PHY1
RF-PHY/TRM-LE/CA/BV-06-C	Carrier frequency offset and drift	RF-PHY1
RF-PHY/TRM/BV-15-C	Output power, With Constant Tone Extension	RF-PHY2
RF-PHY/TRM/BV-16-C	Carrier frequency offset and drift, uncoded data at 1 Ms/s, Constant Tone Extension	RF-PHY2

15.3. Register Setting for Bluetoth test

The AK1595A register settings for Bluetooth certifiation testing are as follows.

ADDR	DATA		ADDR	DATA	
	RF-PHY1	RF-PHY2		RF-PHY1	RF-PHY2
0x00	0x00	0x00	0x20	0x00	0x00
0x01	0x00	0x00	0x21	0x00	0x00
0x02	0x00	0x00	0x22	0x00	0x00
0x03	0x00	0x00	0x23	0x00	0x00
0x04	0x08	0x08	0x24	0x00	0x00
0x05	0x00	0x00	0x25	0x00	0x00
0x06	0x0F	0x0F	0x26	0x00	0x00
0x07	0x00	0x00	0x27	0x00	0x00
0x08	0x00	0x00	0x28	0x00	0x00
0x09	0x14	0x74	0x29	0x00	0x00
0x0A	0x00	0x00	0x2A	0x00	0x00
0x0B	0x00	0x00	0x2B	0x00	0x00
0x0C	0x27	0x27	0x2C	0x00	0x00
0x0D	0x55	0x55	0x2D	0x00	0x00
0x0E	0x29	0x29	0x2E	0x00	0x00
0x0F	0x41	0x41	0x2F	0x00	0x00
0x10	0x76	0x76	0x30	0x00	0x00
0x11	0x71	0x71	0x31	0x00	0x00
0x12	0x00	0x00	0x32	0x00	0x00
0x13	0x25	0x25	0x33	0x00	0x00
0x14	0x00	0x00	0x34	0x00	0x00
0x15	0x00	0x00	0x35	0x00	0x00
0x16	0x00	0x00	0x36	0x00	0x00
0x17	0x00	0x00	0x37	0x00	0x00
0x18	0x00	0x00	0x38	0x00	0x00
0x19	0x00	0x00	0x39	0x55	0x55
0x1A	0x00	0x00	0x3A	0x55	0x55
0x1B	0x00	0x00	0x3B	0x55	0x55
0x1C	0x00	0x00	0x3C	0x00	0x00
0x1D	0x00	0x00	0x3F	0x00	0x00
0x1E	0x00	0x00	-	-	-
0x1F	0x00	0x00	-	-	-

15.4. Timing Chart for Bluetooth Specification Test Mode

The timing charts for the RF-PHY tests are shown below.

15.4.1. Bluetooth Specification Test Mode using UART Interface

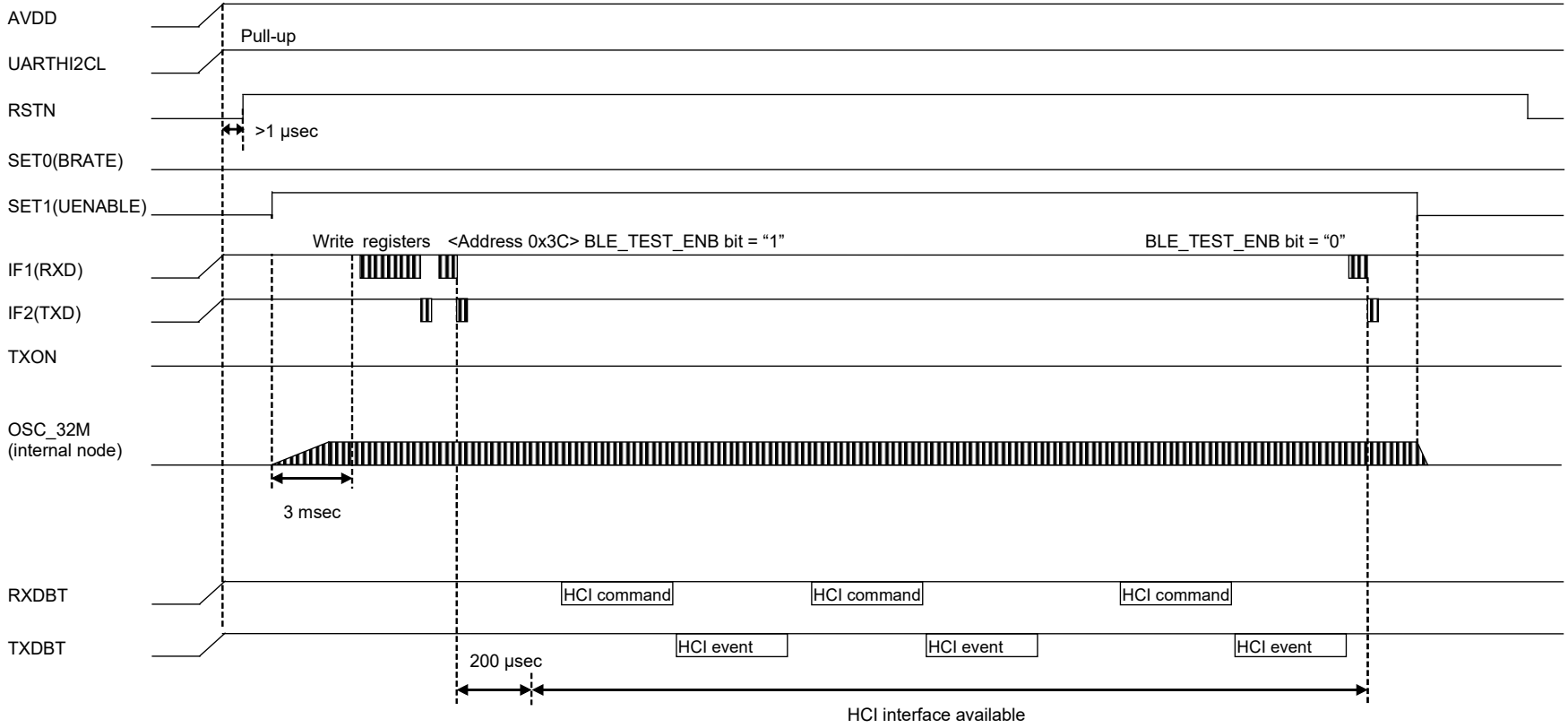


Figure 32. Timing chart of RF-PHY using UART Interface

15.4.2. Bluetooth Specification Test Mode using I²C Interface

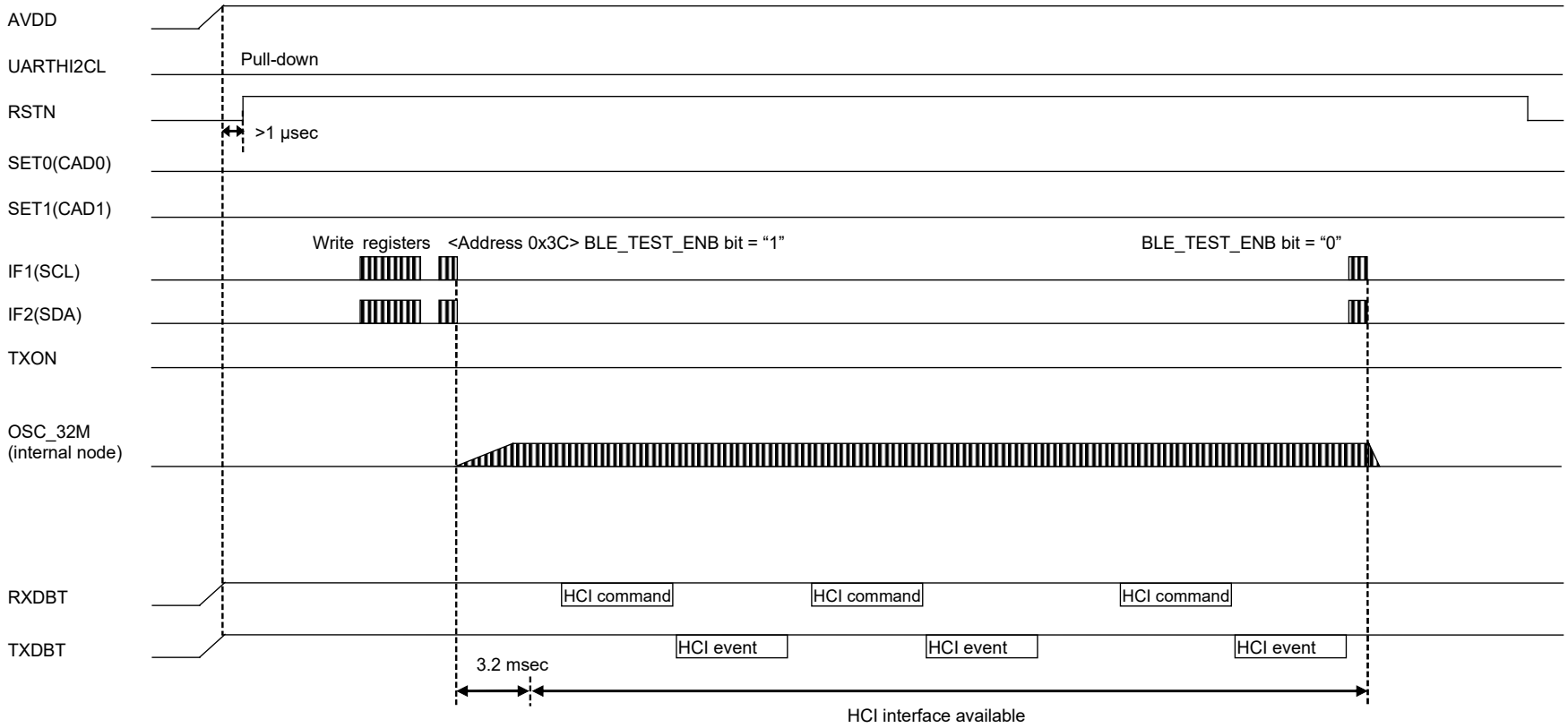


Figure 33. Timing chart of RF-PHY using I²C Interface

16. Register Function

16.1. Register Map

The AK1595A register address consists of 8-bits of data. Data is transferred to or received from the external MCU via the UART or I²C interface described previously.

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Reserved	0x00	R/W	FIXED"0"							
		defaults	0	0	0	0	0	0	0	0
Reserved	0x01	R/W	FIXED"0"							
		defaults	0	0	0	0	0	0	0	0
Reserved	0x02	R/W	FIXED"0"							
		defaults	0	0	0	0	0	0	0	0
Reserved	0x03	R/W	FIXED"0"							
		defaults	0	0	0	0	0	0	0	0
Setting1	0x04	R/W	FIXED"0"		INTRPT_MODE	TIMER_CAL_DIS	TIMER_SET[11:8]			
		defaults	0	0	0	0	1	0	0	0
Setting2	0x05	R/W	TIMER_SET[7:0]							
		defaults	0	0	0	0	0	0	0	0
Setting3	0x06	R/W	FIXED"0"		ADVCH1[1:0]		ADVCH2[1:0]		ADVCH3[1:0]	
		defaults	0	0	0	0	0	1	1	0
Setting4	0x07	R/W	FIXED"0"					POWERD[2:0]		
		defaults	0	0	0	0	0	0	0	0
Setting5	0x08	R/W	ADVDELAY_INSERT	ADVDELAY_POSI[1:0]		TXDATA_LOOP	TXDATA_CW	EVENTNUM[2:0]		
		defaults	0	0	0	0	0	0	0	0
Setting6	0x09	R/W	RFU	RFPHY_INTVL	CTE_ENB	CTE_LEN[4:0]				
		defaults	0	0	0	1	0	1	0	0
Setting7	0x0A	R/W	ADVDELAY_ENB	ADVINTVL[14:8]						
		defaults	1	0	0	0	0	0	0	0
Setting8	0x0B	R/W	ADVINTVL[7:0]							
		defaults	0	0	0	0	0	0	0	0
Setting9	0x0C	R/W	CRC_ENB	WHITE_ENB	PDULEN[5:0]					
		defaults	1	1	1	0	0	1	1	1
Preamble	0x0D	R/W	PRAMBL[7:0]							
		defaults	1	0	1	0	1	0	1	0
Access Address	0x0E	R/W	ACCS_ADRS1[7:0]							
		defaults	1	1	0	1	0	1	1	0
	0x0F	R/W	ACCS_ADRS2[7:0]							
		defaults	1	0	1	1	1	1	1	0

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Access Address	0x10	R/W	ACCS_ADRS3[7:0]							
		defaults	1	0	0	0	1	0	0	1
	0x11	R/W	ACCS_ADRS4[7:0]							
		defaults	1	0	0	0	1	1	1	0
PDU	0x12	R/W	PDU1[7:0]							
		defaults	0	0	0	0	0	0	1	0
	0x13	R/W	PDU2[7:0]							
		defaults	0	0	1	0	0	1	0	1
	0x14	R/W	PDU3[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x15	R/W	PDU4[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x16	R/W	PDU5[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x17	R/W	PDU6[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x18	R/W	PDU7[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x19	R/W	PDU8[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x1A	R/W	PDU9[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x1B	R/W	PDU10[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x1C	R/W	PDU11[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x1D	R/W	PDU12[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x1E	R/W	PDU13[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x1F	R/W	PDU14[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x20	R/W	PDU15[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x21	R/W	PDU16[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x22	R/W	PDU17[7:0]							
		defaults	0	0	0	0	0	0	0	0

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
PDU	0x23	R/W	PDU18[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x24	R/W	PDU19[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x25	R/W	PDU20[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x26	R/W	PDU21[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x27	R/W	PDU22[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x28	R/W	PDU23[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x29	R/W	PDU24[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x2A	R/W	PDU25[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x2B	R/W	PDU26[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x2C	R/W	PDU27[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x2D	R/W	PDU28[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x2E	R/W	PDU29[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x2F	R/W	PDU30[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x30	R/W	PDU31[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x31	R/W	PDU32[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x32	R/W	PDU33[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x33	R/W	PDU34[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x34	R/W	PDU35[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x35	R/W	PDU36[7:0]							
		defaults	0	0	0	0	0	0	0	0

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
PDU	0x36	R/W	PDU37[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x37	R/W	PDU38[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x38	R/W	PDU39[7:0]							
		defaults	0	0	0	0	0	0	0	0
CRC	0x39	R/W	CRC1[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x3A	R/W	CRC2[7:0]							
		defaults	0	0	0	0	0	0	0	0
	0x3B	R/W	CRC3[7:0]							
		defaults	0	0	0	0	0	0	0	0
MODE	0x3C	R/W	Blank	Blank	Blank	TX_START	Blank	Blank	BLE_TEST_ENB	TX_ENB
		defaults				0			0	0
SOFT RST	0x3F	W	SOFTRST[7:0]							
		defaults	0	0	0	0	0	0	0	0

Writing to registers with addresses from 0x00 to 0x3B is prohibited during the advertising and intermission states.

FIXED”0” bits must be used with zeroes. RFU registers can be Write/Read but do not affect IC operation and must be used with zeroes. Blank registers have no substance, always reads “0” and must be used with zeroes. Writing one to these locations is not supported.

16.1.1. <0x04 to 0x05> Setting1, 2

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Setting1	0x04	R/W	FIXED"0"		INTRPT_MODE	TIMER_CAL_DIS	TIMER_SET[11:8]			
		defaults	0	0	0	0	1	0	0	0
Setting2	0x05	R/W	TIMER_SET[7:0]							
		defaults	0	0	0	0	0	0	0	0

16.1.1.1. INTRPT_MODE

Interrupt mode setting

INTRPT_MODE	Function
0	Interrupt mode 0 (default)
1	Interrupt mode 1

This function detail refer to 14.3 Interrupt mode.

16.1.1.2. TIMER_CAL_DIS, TIMER_SET

Low power timer calibaration

TIMER_CAL_DIS	Function
0	Enables low power timer calibration (default)
1	Disables low power timer calibration

Setting TIMER_CAL_DIS bit from "1" to "0" is prohibited.
To change the TIMER_CAL_DIS bit from "1" to "0", execute a hardware reset.

Low power timer setting

TIMER_SET[11:0]	Timer setting [sec]
0000_0000_0000	2
0000_0000_0001	2
0000_0000_0010	2
0000_0000_0011	3
~	~
0111_1111_1111	2047
1000_0000_0000	2048 (default)
1000_0000_0001	2049
~	~
1111_1111_1110	4094
1111_1111_1111	4095

16.1.2. <0x06> Setting3, 4

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Setting3	0x06	R/W	FIXED"0"		ADVCH1[1:0]		ADVCH2[1:0]		ADVCH3[1:0]	
		defaults	0	0	0	0	0	1	1	0
Setting4	0x07	R/W	FIXED"0"					POWERD[2:0]		
		defaults	0	0	0	0	0	0	0	0

16.1.2.1. ADVCH1, ADVCH2, ADVCH3

Advertising channel 1st setting

ADVCH1[1]	ADVCH1[0]	Function
0	0	37ch :2402 MHz (default)
0	1	38ch : Center frequency 2426 MHz
1	0	39ch : Center frequency 2480 MHz
1	1	37ch : Center frequency 2402 MHz

Advertising channel 2nd setting

ADVCH2[1]	ADVCH2[0]	Function
0	0	37ch : Center frequency 2402 MHz
0	1	38ch : Center frequency 2426 MHz (default)
1	0	39ch : Center frequency 2480 MHz
1	1	No transmission output.

In case of ADVCH2[1:0] bits = 2'b11, the AK1595A doesn't output 2nd, 3rd advertising channel output.

Advertising channel 3rd setting

ADVCH3[1]	ADVCH3[0]	Function
0	0	37ch : Center frequency 2402 MHz
0	1	38ch : Center frequency 2426 MHz
1	0	39ch : Center Frequency 2480MHz (default)
1	1	No transmission output.

In case of ADVCH3[1:0] bits = 2'b11, the AK1595A doesn't output 3rd advertising channel output.

16.1.2.2. POWERD

TX output power setting

POWERD[2]	POWERD[1]	POWERD[0]	TX Power[dBm] typ.
0	0	0	0(default)
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-20
1	1	1	-32

16.1.3. <0x08> Setting5

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Setting5	0x08	R/W	ADVDELAY_INSERT	ADVDELAY_POSI[1:0]		TXDATA_LOOP	TXDATA_CW	EVENTNUM[2:0]		
		defaults	0	0	0	0	0	0	0	0

16.1.3.1. ADVDELAY_INSERT, ADVDELAY_POSI

Insert the advDelay value of 4-bits into the PDU.

ADVDELAY_INSERT	Function
0	advDelay insert disable (default)
1	advDelay insert enable

When ADVDELAY_INSERT bit = ”1”, the advInterval set in <Address 0x0A to 0x0B> ADVINTVL bits should also be inserted in the PDU. This function is intended to be used for reporting the advertising event time (T_advEvent) to the receiver.

Sets the location where the 4-bits advDelay value is inserted into the PDU.

ADVDELAY_POSI[1]	ADVDELAY_POSI[0]	Function
0	0	PDU13[7:0] bits LSB 4bit (PDU13[3:0]) (default)
0	1	PDU16[7:0] bits LSB 4bit (PDU16[3:0])
1	0	PDU19[7:0] bits LSB 4bit (PDU19[3:0])
1	1	PDU39[7:0] bits LSB 4bit (PDU39[3:0])

ADVDELAY_POSI bits enables when ADVDELAY_INSERT bit = “1”.
Set the PDU length that is longer than the value set by ADVDELAY_POSI bits.

16.1.3.2. TXDATA_LOOP, TXDATA_CW

The AK1595A transmits continuous signal via RFOUT pin when TXDATA_LOOP bit =”1”.
Channel frequencies are set by ADVCH1 bits.

TXDATA_LOOP	Function
0	Burst Transmission (default)
1	Continuous transmission

Set TXDATA_LOOP bit =”0” except regulatory testing.
Set <Address 0x09> CTE_ENB bit = “0” when TXDATA_LOOP bit = "1".

The AK1595A transmits non modulated signal via RFOUT pin when TXDATA_CW bit = "1".
Channel frequencies are set by ADVCH1, ADVCH2, ADVCH3 bits.

TXDATA_CW	Function
0	GFSK. (default)
1	Non modulated wave

Set TXDATA_CW bit =”0” except regulatory testing.

16.1.3.3. EVENTNUM

Set the number of advertising events

EVENTNUM[2]	EVENTNUM[1]	EVENTNUM[0]	Function
0	0	0	Repeat Advertising event(default)
0	0	1	1 time Advertising event
0	1	0	2 times Advertising event
0	1	1	3 times Advertising event
1	0	0	4 times Advertising event
1	0	1	5 times Advertising event
1	1	0	6 times Advertising event
1	1	1	7 times Advertising event

When TXON pin is changed from “H” to “L” or <Address 0x3C> TX_ENB bit = “0”, the AK1595A stops Advertising event output.
Set EVENTNUM[2:0] bits = 3’h1 when using the low power timer with <Address 0x04>INTRPT_MODE bit=”0”.
Refer to 14.3 Interrupt mode for details.

16.1.4. <0x09> Setting6

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Setting6	0x09	R/W	RFU	RFPHY_INTVL	CTE_ENB	CTE_LEN[4:0]				
		defaults	0	0	0	1	0	1	0	0

16.1.4.1. RFPHY_INTVL

LE Test packt interval setting

RFPHY_INTVLT	LE Test packet interval [µsec]
0	625 (default)
1	1250

This register bit used only Bluetooth certification test.
Set RFPHY_INTVLT bit = “1” when CTE_ENB bit = “1”.

16.1.4.2. CTE_ENB, CTE_LEN

Constant Tone Extension(CTE) enable

CTE_ENB	Function
0	CTE disable (default)
1	CTE enable

Set <Address 0x08> TXDATA_LOOP bit = “0” when CTE_ENB bit = “1”.

CTE length setting

CTE_LEN[4:0]	CTE length [µsec]
5’d0	Prohibited
5’d1	Prohibited
5’d2	16
5’d3	24
~	~
5’d19	152
5’d20	160
5’d21	Prohibited
5’d22	Prohibited
~	~
5’d31	Prohibited

This register enables when CTE_ENB bit = "1"

16.1.5. <0x0A to 0x0B> Setting7, 8

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Setting7	0x0A	R/W	ADVDELAY_ENB	ADVINTVL[14:8]						
		defaults	1	0	0	0	0	0	0	0
Setting8	0x0B	R/W	ADVINTVL[7:0]							
		defaults	0	0	0	0	0	0	0	0

16.1.5.1. ADVDELAY_ENB, ADVINTVL

AdvDelay Enable

ADVDELAY_ENB	Function
0	AdvDelay disable
1	AdvDelay enable (default)

AdvDelay changes for each advertising event.
ADVDELAY_ENB bit = "1", the advertising event time (T_advEvent) meets the Bluetooth Core Specifications.

Advertising interval setting

ADVINTVL[14:0]	Advertising Interval [msec]
000_0000_0000_0000	20.000(default)
000_0000_0000_0001	20.000
~	~
000_0000_0001_1111	20.000
000_0000_0010_0000	20.000
000 0000_0010_0001	20.625
~	~
000_0000_1001_1111	99.375
000_0000_1010_0000	100.000
000_0000_1010_0001	100.625
~	~
011_1111_1111_1110	10238.750
011_1111_1111_1111	10239.375
100_0000_0000_0000	10240.000
Other setting	10240.000

16.1.6. <0x0C> Settings9

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Setting9	0x0C	R/W	CRC_ENB	WHITE_ENB	PDULEN[5:0]					
		defaults	1	1	1	0	0	1	1	1

16.1.6.1. CRC_ENB, WHITE_ENB

CRC setting

CRC_ENB	Function
0	Use the value of <Address 0x39 to 0x3B> CRC1, CRC2, CRC3 bits as CRC
1	Generate CRC by internal calculation (default)

Set CRC_ENB =”1” except regulatory testing.
For details of CRC function, refer to Bluetooth specification

Data Whitening setting

WHITE_ENB	Function
0	Data whitening disable
1	Data whitening enable (default)

Set WHITE_EN bit =” 1” except regulatory testing.
For details of whitening function, refer to Bluetooth specification

16.1.6.2. PDULEN

PDU Length setting

PDULEN[5:0]	PDU Length [octet]
00_0000	Prohibited
00_0001	Prohibited
00_0010	2
00_0011	3
~	~
10_0101	37
10_0110	38
10_0111	39 (default)
Other setting	Prohibited

16.1.7. <0x0D to 0x3B> TX Data

Write TX data to the following addresses.
Preamble (<Address 0x0D>)
Access Address (<Address 0x0E to 0x11>)
PDU (<Address 0x12 to 0x38>),
CRC (<Address 0x39 to 0x3B>)

Maximum TX data size is 47 octets.
Unused sectors value must set “0”.

Data is sent in the following format.
Constant Tone Extension is sent only when <Address 0x09> CTE_ENB bit = ”1”.

LSB MSB

Preamble	Access Address	PDU			CRC	Constant Tone Extension
		Header	Payload			
			AdvA	AdvData		
1octet	4octets	2octets	6octets	0 to 31octets	3octets	16 to 160 µs

The output order of the data register address is 0x0D -> 0x0E -> … -> 0x3A -> 0x3B.
The output order of the data bits is as follows

<Name>	Addr.	R/W Defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
-	0x0D to 0x3B	R/W	Data[7]	Data[6]	Data[5]	Data[4]	Data[3]	Data[2]	Data[1]	Data[0]
		defaults								

Data[0] -> Data[1] -> Data[2] -> Data[3] -> Data[4] -> Data[5] -> Data[6] -> Data[7]

16.1.7.1. <0x0D> PRAMBL

Preamble setting. Set default values 0xAA except regulatory testing.

16.1.7.2. <0x0E to 0x11> ACCS_ADRS1 to ACCS_ADRS4

Access Address setting. Set following default values.
<Address 0x0E> ACCS_ADRS1[7:0] bits = 8'hD6
<Address 0x0F> ACCS_ADRS2[7:0] bits = 8'hBE
<Address 0x10> ACCS_ADRS3[7:0] bits = 8'h89
<Address 0x11> ACCS_ADRS4[7:0] bits = 8'h8E

16.1.7.3. <0x12 to 0x38> PDU1 to PDU39

The PDU setting. Set the send data that complies with Bluetooth Low Energy.
The PDU consists of the Header of 2 octets and the Payload of 0-37 octets. Note that there is a difference of 2 octets between the PDU length specified in the PDULEN bits and the Payload length defined in the Header Length.

16.1.7.4. <0x39 to 0x3B> CRC1 to CRC3

The CRC data setting.
When CRC_ENB bit = “1”, CRC(0x39 to 0x3B) is not need to be set.
When CRC_ENB bit = “0”, set CRC value that complies with Bluetooth Low Energy.

16.1.8. <0x3C> MODE

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
MODE	0x3C	R/W	Blank	Blank	Blank	TX_START	Blank	Blank	BLE_TEST_ENB	TX_ENB
		defaults				0			0	0

16.1.8.1. TX_START

Check AK1595A state (read-only)

TX_START	Function
0	The AK1595A state is either full power-down, sleep, or standby(default).
1	The AK1595A state is either advertising or intermission

TX_START bit is read-only.

16.1.8.2. BLE_TEST_ENB, TX_ENB

Bluetooth Test mode enable, RF transmission enable

BLE_TEST_ENB	TX_ENB	Function
0	1	Start RF transmission. This is the same operation mode as when TXON pin is set to "H".
1	0	The unit enters the Bluetooth certification test mode. This mode is used to perform a certification test. Refer to 15 Bluetooth Test Specification.
0	0	Stop RF transmission when TX_ENB bit is set “1” to “0”. Exit Bluetooth certification test mode when BLE_TEST_ENB bit is set “1” to “0”.
1	1	Prohibited

Set TXON pin = “L” while RF transmission is being performed by the TX_ENB bit or BLE_TEST_ENB bit. Set TX_ENB bit or BLE_TEST_ENB bit = “0” while RF transmission is being performed by the TXON pin.

16.1.9. <0x3F> SOFTRST

<Name>	Addr.	R/W defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
SOFT RST	0x3F	W	SOFTRST[7:0]							
		defaults	0	0	0	0	0	0	0	0

Software reset

SOFTRST[7:0]	Function
0xAA	Execute a software reset. This is to initialize the digital block. To set all AK1595A setting again. SOFTRST[7:0] bits automatically turns 0x00 after the software reset is completed.
Other than above	If a value other than the above is written, a software reset is not executed.

Default is 0x00. This register is write-only.

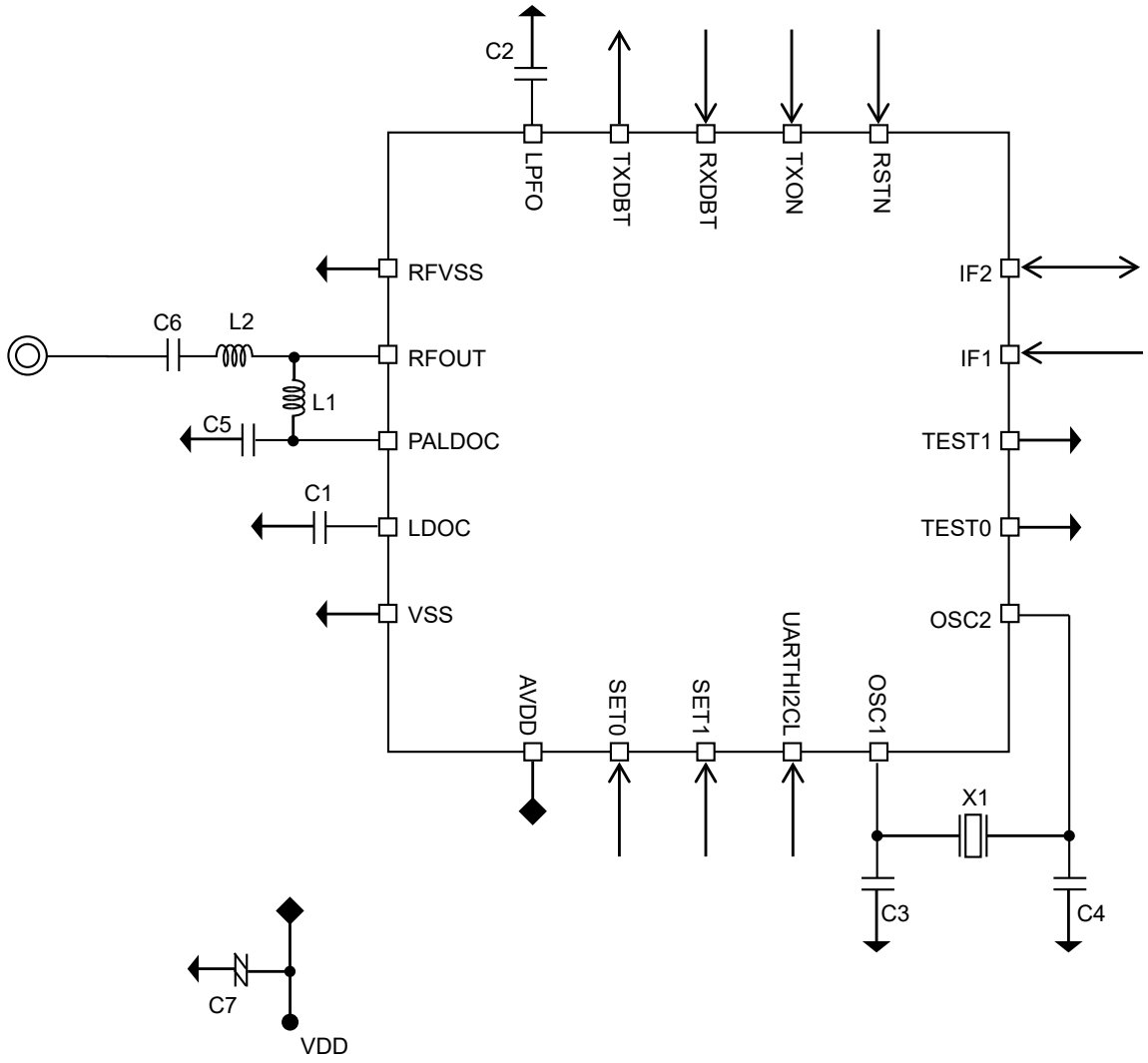
The AK1595A doesn’t generate an acknowledge when a software reset is executed by the I^2C interface. Even though the AK1595A doesn’t generate an acknowledge in this state, it is still necessary to provide all nine SCL clock cycles as usual (eight cycles for data + one cycle for the acknowledge).

The AK1595A doesn’t output an event when a software reset is executed via the UART interface.

In order to ensure the AK1595A software reset, TXON pin must be set “L” during the reset period.

17. Recommended External Circuits

17.1. Recommended External Circuits



RF specification, number of components and values may change depending upon the RF matching network and PCB design.

Figure 34. Recommended external circuits

17.2. Parts list

Number	Value	Part
C1	0.1μF	
C2	680pF	
C3	6.8pF	
C4	6.8pF	
C5	1000pF	
C6	0.8pF	
C7	0.1μF	
L1	22nH	
L2	6.8nH	
X1	32MHz(6pF)	EPSON, FA-128, Q22FA12800517xx

RF specification, number of components and values may change depending upon the RF matching network and PCB design.

18. Package

18.1. Outline Dimensions

20-pin HUQFN(3.0mm x 3.0mm x 0.5mm, 0.4mm pitch)

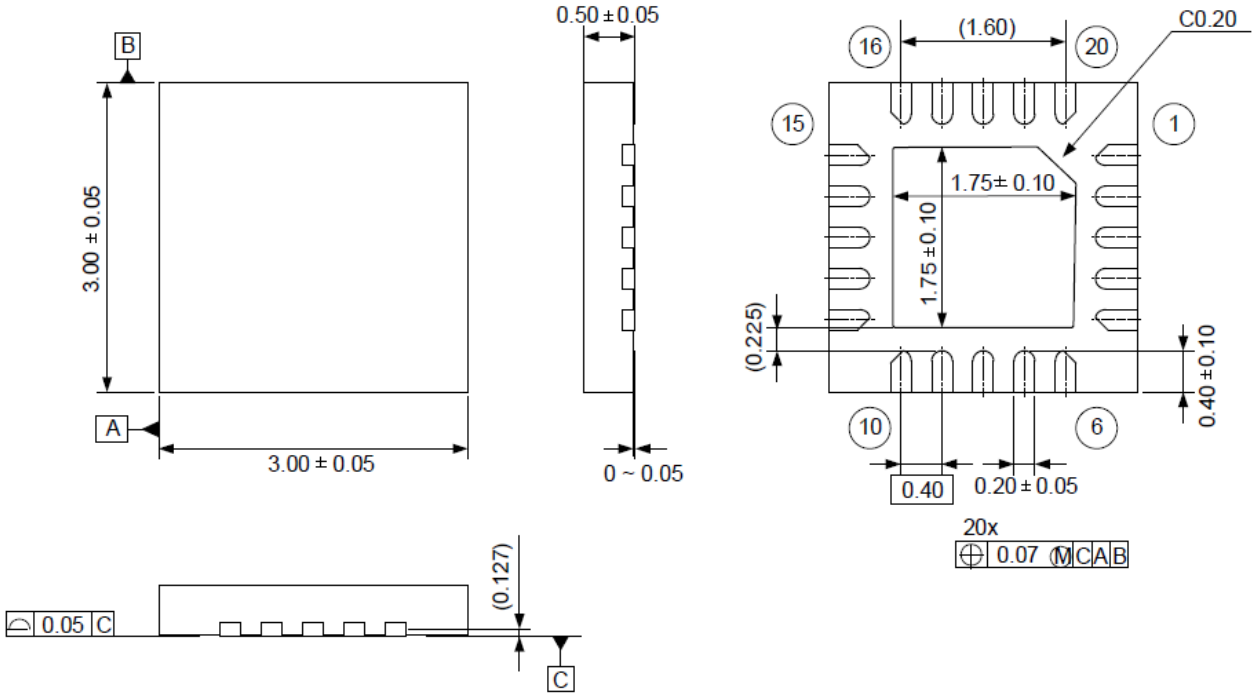
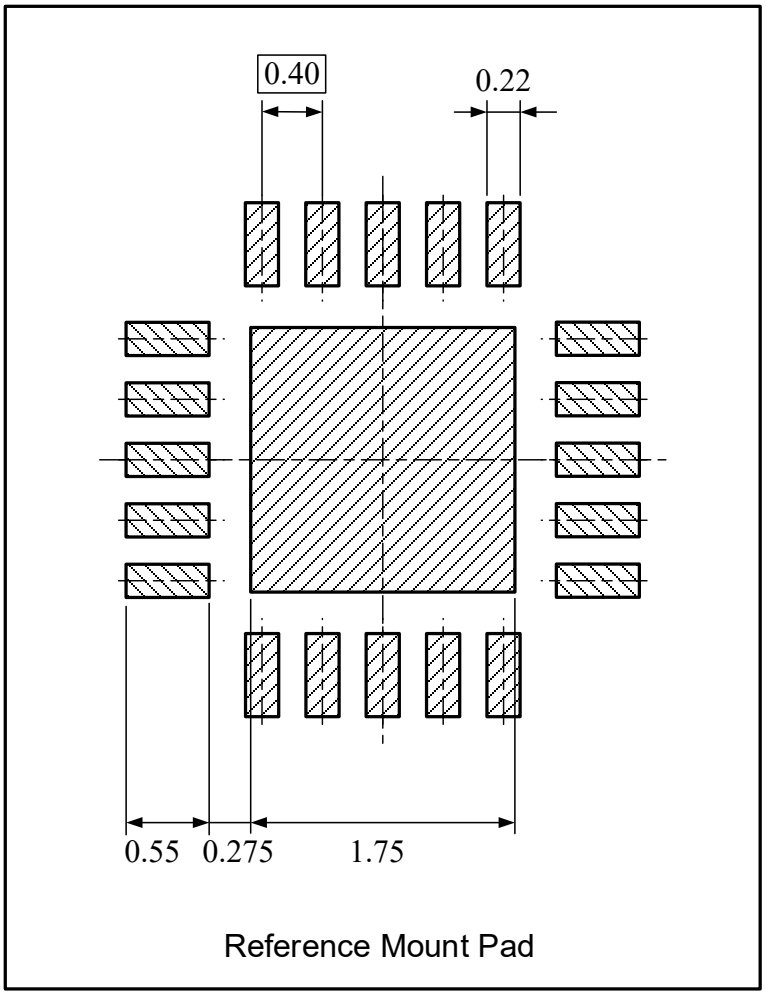


Figure 35. Package outer dimension

Leave the exposed pad on the bottom surface of the package unconnected.

18.2. Pad Dimensions (for reference)



Reference Mount Pad

The center mounting-pad should be covered with solder mask and the exposed pad of the AK1595A should be unconnected, not connected to VSS.

AKM's recommended Land-pattern is described above, however, please note that the most suitable dimension for mounting-pad will vary according to following conditions, :Materials of PCB, Kind of soldering paste, soldering method, accuracy of soldering machine, so on.
So, for your actual design for Land-pattern, we recommend you should optimize it to your actual condition.

18.3. Marking

a. Style : HUQFN
b. Number of pins : 20pins
c. A1 pin marking : Circle mark
d. Product number : 1595A
e. Date code : XXXX (4 digits)

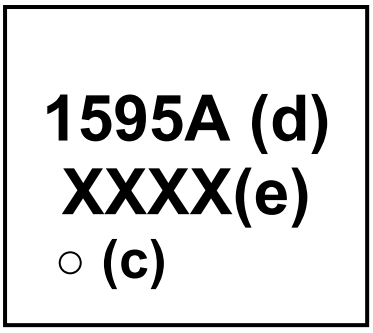


Figure 36. Marking

19. Ordering Guide

- AK1595A 20-pin HUQFN (3.0mm x 3.0mm x 0.5mm, 0.4mm pitch)
- AKD1595A AK1595A evaluation board

20. Revision history

Date (Y/M/D)	Revision	Reason	Page	Contents
2022/07/27	00	Initial version		

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