Low Spurious Multiclock Generator for Audio

AK8128MV

Features

- External Clock Input Frequencies:
  - 2.8224/3.072/11.2896/12.288/27.000MHz
- Two Frequency-Selectable Clock Outputs
- Selectable Clock Output Frequencies:
  - CLK1: 24.576/45.000/46.40625MHz
  - CLK2: 11.2896MHz/off
- Low Jitter Performance
  - Period Jitter (1σ):
    20 psec (Typ.) at CLK1-2
  - Long Term Jitter (1000 cycle, 1σ):
    40 psec (Typ.) at CLK1-2
- Low Current Consumption:
  8.0mA (Typ.) at 3.3V
- Output Load:
  15pF (Max.)
- Supply Voltage:
  3.0V to 3.6V
- Operating Temperature Range:
  -40°C to +85°C
- Package:
  10-pin TMSOP (lead-free)

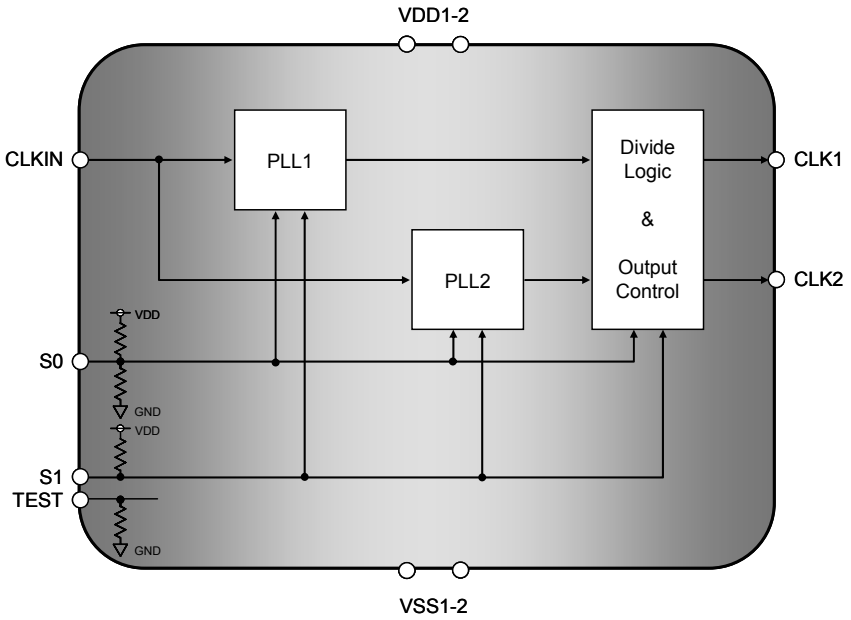
Description

The AK8128MV is a member of AKM's low power multi clock generator family designed for a high quality audio clock with high performance C/N. The AK8128MV generates different frequency clocks from external clock input. It provides them to up to two outputs configured by pin-setting. The circuitries of PLL in AK8128MV are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption. The AK8128MV is available in a 10-pin TMSOP package.

Applications

- Digital Television
- Personal Video Recorders
- Set-Top-Boxes
- Multi Media Receivers
- Digital Still Camera
- Digital Video Camera

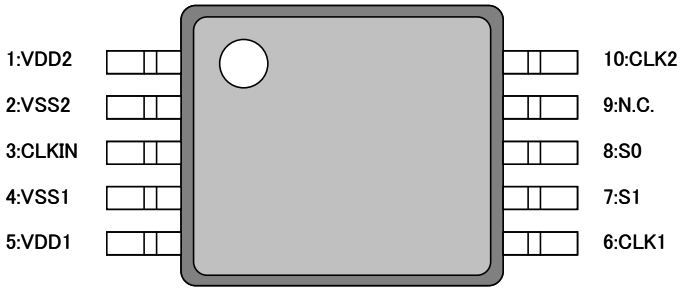
Block Diagram



AK8128MV Multi Clock Generator

Pin Descriptions

Package: 10-Pin TMSOP(Top View)



Pin No.	Pin Name	Pin Type	Description	
1	VDD2	--	Power Supply	
2	VSS2	--	Ground	
3	CLKIN	IN	External Clock Input. See table.1.	
4	VSS1	--	Ground	
5	VDD1	--	Power Supply	
6	CLK1	OUT	Clock Output. See table.1.	
7	S1	--	Frequency Select Pin 1. See table.1.	(1)
8	S0	IN	Frequency Select Pin 0. See table.1.	(1), (2)
9	TEST	--	Connect to GND	(2)
10	CLK2	OUT	Clock Output. See table.1.	

(1) Internal pull up 400kΩ (Typ.)

(2) Internal pull down 400kΩ (Typ.)

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8128MV	128MV	Tape and Reel	10-pin TMSOP	-40 to 85 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta	AK8128MV	-40		85	°C
Supply voltage (1)	VDD		3.0	3.3	3.6	V
Output Load Capacitance	Cpl	Pin: CLK1-2			15	pF

Note:

(1) Power to VDD1 and VDD2 requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be installed close to each VDD pin.

DC Characteristics

All specifications at VDD: over 3.0 to 3.6V, Ta = -40 to 85 ℃ unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High level input voltage 1	V_{IH1}	Pin: CLKIN, S1	0.7VDD			V
Low level input voltage 1	V_{IL1}	Pin: CLKIN, S1			0.3VDD	V
High level input voltage 2	V_{IH2}	Pin: S0	0.7VDD			V
Middle level input voltage 2	V_{IM2}	Pin: S0	0.45VDD	0.5VDD	0.55VDD	V
Low level input voltage 2	V_{IL2}	Pin: S0			0.3VDD	V
Input leak current 1	I_{L1}	Pin: CLKIN	-1		+1	μA
Input leak current 2	I_{L2}	Pin: S1	-20		+1	μA
Input leak current 3	I_{L3}	Pin: S0	-20		+20	μA
Input leak current 4	I_{L4}	Pin: TEST V_{IL}=GND	-1		+1	μA
High Level output voltage	V_{OH}	Pin: CLK1-2 I_{OH}=-4mA	0.8VDD			V
Low level output Voltage	V_{OL}	Pin: CLK1-2 I_{OL}=+4mA			0.2VDD	V
Current consumption	I_{DD}	Ta=25℃, No load S[0:1] = All Setting		8.0		mA

AC Characteristics

All specifications at VDD: over 3.0 to 3.6V, Ta = -40 to 85 ℃ unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
External clock frequency		Pin: CLKIN S[0:1] = “LL”		2.8224		MHz
		Pin: CLKIN S[0:1] = “ML”		3.072		MHz
		Pin: CLKIN S[0:1] = “LH”		11.2896		MHz
		Pin: CLKIN S[0:1] = “MH”		12.288		MHz
		Pin: CLKIN S[0:1] = “HL”, “HH”		27.000		MHz
Input Clock Duty Cycle		Pin: CLKIN At VDD/2	30		70	%
Output clock frequency		Pin: CLK1 S[0:1] = “LL”, “LH”, “ML”, “MH”		24.576		MHz
		Pin: CLK1 S[0:1] = “HL”		45.000		MHz
		Pin: CLK1 S[0:1] = “HH”		46.40625		MHz
		Pin: CLK2 S[0:1] = “LL”, “LH”, “ML”, “MH”		11.2896		MHz
		Pin: CLK2(1) S[0:1] = “HL”, “HH”		---		MHz
Period jitter (3)		Pin: CLK1, 2(2) S[0:1] = “LL”, “LH”, “ML”, “MH”		20		ps
		Pin: CLK1(2) S[0:1] = “HL”, “HH”		15		ps
Long Term jitter (3)		Pin: CLK1, 2(2) S[0:1] = “LL”, “LH”, “ML”, “MH” 1000cycles		40		ps
		Pin: CLK1(2) S[0:1] = “HL”, “HH” 1000cycles		30		ps
Output Clock Duty Cycle		Pin: CLK1-2(2)	45	50	55	%
Output clock rise time	t_{rise}	Pin: CLK1, 2(2)		1.5	3.0	ns
Output clock fall time	t_{fall}	Pin: CLK1, 2(2)		1.5	3.0	ns
Power-up Time (4)		Pin: CLK1, 2(2)		0.2		ms
Output Lock Time (5)		Pin: CLK1(2) S[0:1] = “HL” ⇔ “HH”		0.2		ms

(1) “L” Output

(2) Measured with load capacitance of 15pF

(3) 1σ in 10000 sampling or more

(4) The time to settle output into ±0.1% of specified frequency from the point that the power supply reaches VDD.

(5) The time to settle output into ±20ppm of specified frequency from the point that the S[0:1] is switched.

Output clock frequency selection

The AK8128MV generates a range of low-jitter and high-accuracy clock frequencies with two built-in PLLs and provides to up to two assigned outputs. A frequency selection at assigned output pin is configured by pin-setting of S0 (Pin8) and S1 (Pin7).
The selectable frequency is shown in Table1.

Table 1: CLK1-2 Clock output Frequency

Selection Pin		Clock Input Frequency (MHz)	Clock Output Frequency (MHz)	
S0 (Pin 8)	S1 (Pin 7)	CLKIN (Pin 3)	CLK1 (Pin 6)	CLK2 (Pin 10)
L	L	2.8224	24.576	11.2896
L	H	11.2896	24.576	11.2896
M	L	3.072	24.576	11.2896
M	H	12.288	24.576	11.2896
H	L	27.000	45.000	"L" Output
H	H	27.000	46.40625	"L" Output

Typical Connection Diagram

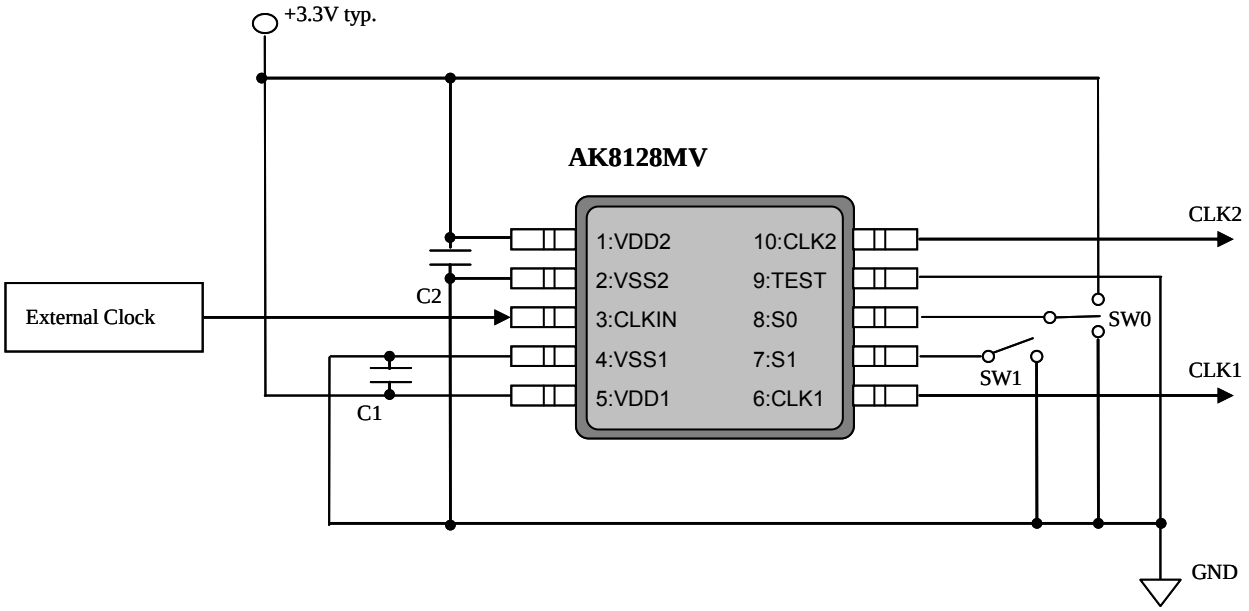


Figure 1: Typical Connection Diagram

C1-2 : 0.1μF
SW0 : Open is "H" and tied to GND is "L" for S0 because this pin has internal pull up resister.
SW1 : Open is "M", tied to VDD is "H" and tied to GND is "L" for S1 because this pin has internal pull down and up resister.

PCB Layout Consideration

The AK8128MV is a high-accuracy and low-jitter multi clock generator. For proper performances specified in this datasheet, careful PCB layout should be taken. The followings are layout guidelines based on the typical connection diagram shown in Figure 1

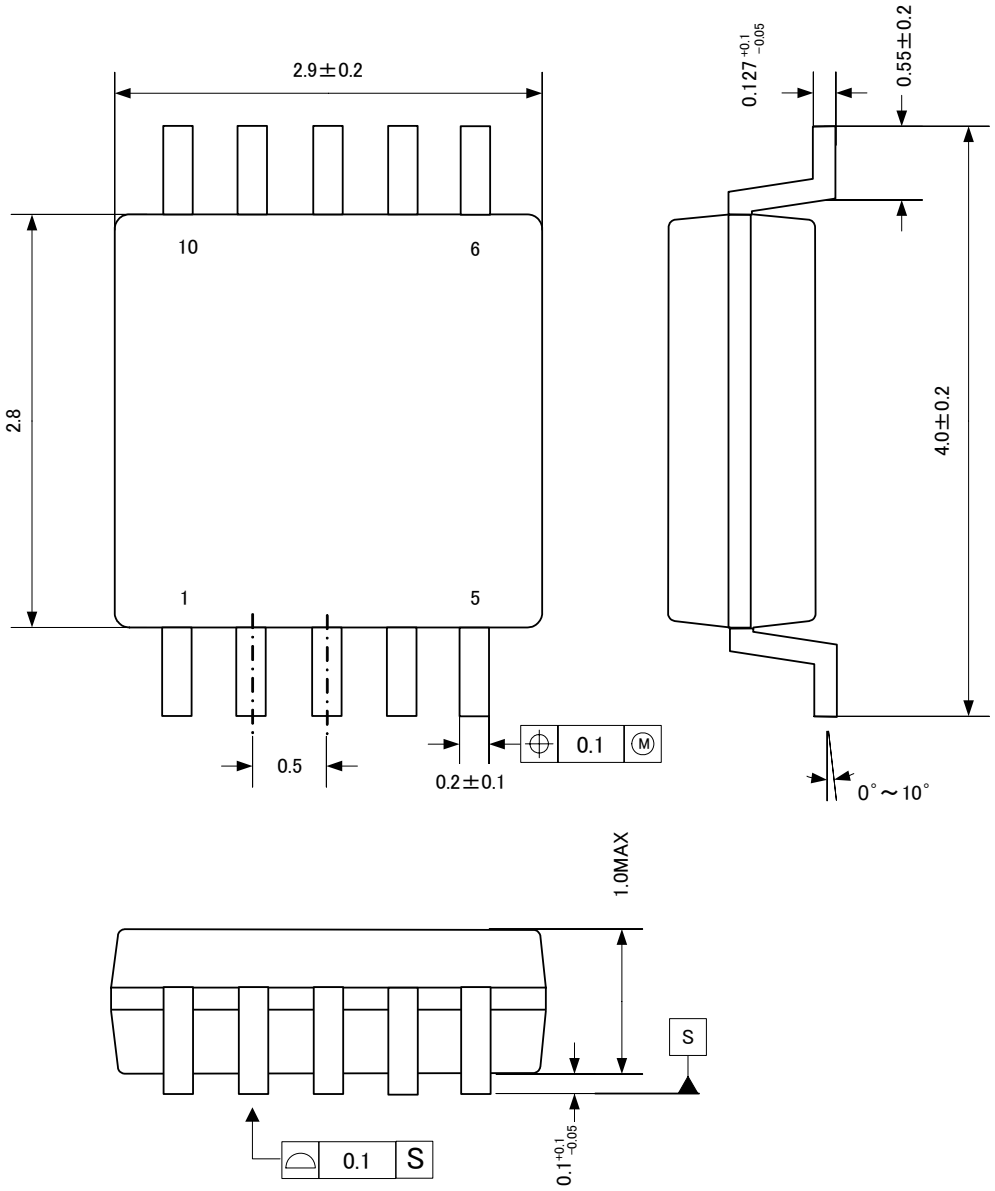
Power supply line – AK8128MV has two power supply pins (VDD1-2) which deliver power to internal circuitry segments. A 0.1μF decoupling capacitor should be placed as close to each VDD pin as possible.

Ground pin connection – AK8128MV has two ground pins (VSS1-2). These pin require connecting to plane ground which will eliminate any common impedance with other critical switching signal return. 0.1μF decoupling capacitors placed at VDD1 and VDD2 should be grounded at close to the VSS1 pin and the VSS2 pin, respectively.

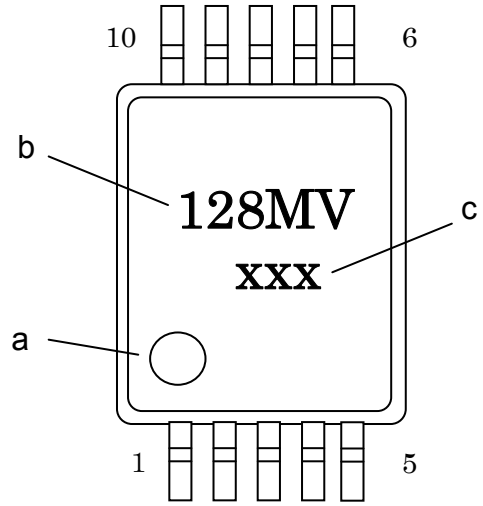
Package Information

- **Mechanical data**

10 TMSOP

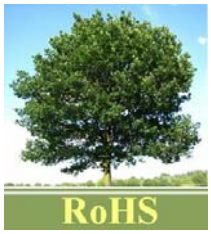


- **Marking**



a: #1 Pin Index
b: Part number
c: Date code (3 digits, Year/month/Lot No.)

- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with “Pb free” letter indication on product label posted on the anti-shield bag and boxes.

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