High Power Positive Hot Swap Controller with Power Monitor

FEATURES

- Drives two gates for high power applications
- Wide input supply voltage range: 6.5 V to 80 V
- Optimizes MOSFET SOA with multimode start-up sequencing and operation
- Monitors currents, voltages, power, and energy with the ADC
- Limits MOSFET temperature for overstress protection
- Adjustable, 6.6% accurate (5 mV) current limit with foldback
- BlackBox capturing and configuration using an optional external EEPROM
- SMBus 3.1 interface and PMBus-compliant command structure
- Parallelable controllers for high current levels
- Minimum and maximum ADC measurements logging with alerts
- Available in 48(39)-lead plastic QFN (7 mm × 7 mm) package
- Configurable current foldback

APPLICATIONS

- High availability server backplane systems
- 12 V/24 V/48 V/54 V distributed power systems
- Industrial

GENERAL DESCRIPTION

The LTC4287 is an integrated solution for hot swap applications that allows a board to be safely inserted and removed from a live backplane. The dual-gate drivers coupled with configurable multimode startup sequencing and operation optimize the metal-oxide semiconductor field-effect transistor (MOSFET) safe operating area (SOA) for a variety of power levels. The circuit breaker timer limits the MOSFET temperature for reliable protection against overstress.

The SMBus 3.1 interface, PMBus command structure, and onboard analog-to-digital converters (ADCs) with selectable resolution and speed allow monitoring of board current, voltage, power, energy, temperature, and fault status. An optional external, electrically erasable programmable read only memory (EEPROM) can be used for part configuration and provide BlackBox capturing of past fault conditions.

The LTC4287 has additional features to respond to input undervoltages and overvoltages, to interrupt the host when a fault has occurred, to notify when the output power is good, to detect insertion of a board, to turn off the MOSFET if an external supply monitor fails to indicate power-good within a timeout period, and to auto reboot after a programmable delay following a host commanded turn-off.

TYPICAL APPLICATION

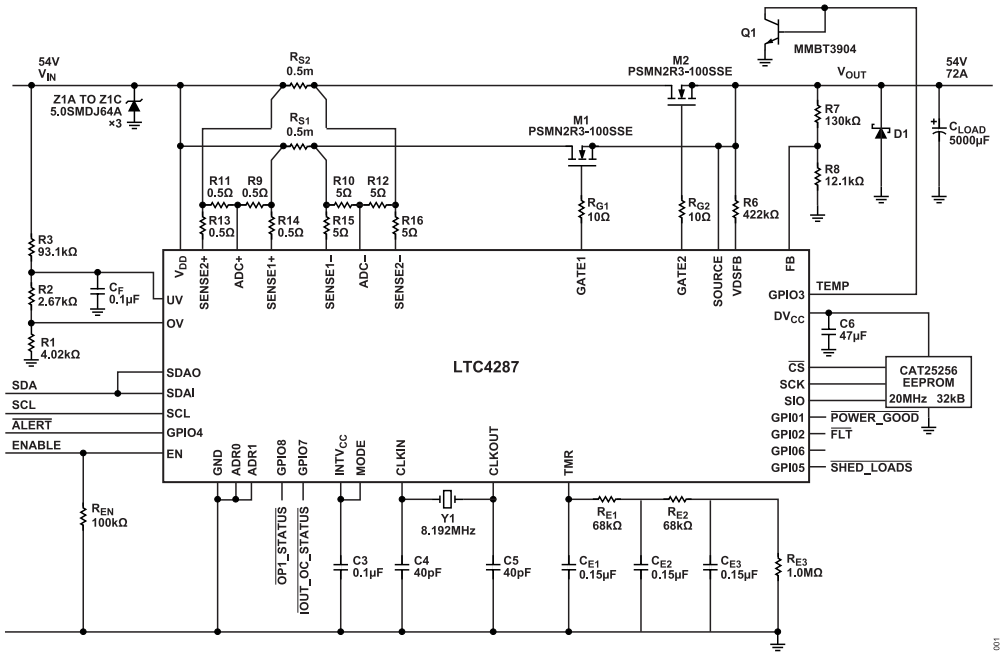

Figure 1. 54 V, 3900 W Hot-Swap Controller (Parallel Mode)

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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REVISION HISTORY

10/2023—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

Specifications apply over the full operating temperature range, unless otherwise noted. All currents into pins are positive, and all voltages are referenced to GND, unless otherwise specified.

Table 1. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Input Supply Range	V_{DD}		6.5		80	V
Input Supply Current	I_{DD}	No external resistor, input voltage (V_{IN}) to $INTV_{CC}$, no load on DV_{CC}		12	18	mA
		5 kΩ pull-up on $INTV_{CC}$ from V_{DD}, 48 V		1.8		mA
Input Supply Undervoltage Lockout	$V_{DD\ (UVLO)}$	V_{DD} rising	5	6	7	V
		V_{DD} falling	5	5.5	7	V
Input Supply Undervoltage Lockout Hysteresis	$\Delta V_{DD\ (HYST)}$			0.5		V
$INTV_{CC}$ Output Voltage	$INTV_{CC}$	V_{DD} = 8.5 V and 80 V, load current (I_{LOAD}) = 0 mA and −4 mA	4.5	5	5.5	V
$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC\ (UVLO)}$	$INTV_{CC}$ rising	3.6	4	4.5	V
		$INTV_{CC}$ falling	3.4	3.89	4.45	V
$INTV_{CC}$ Undervoltage Lockout Hysteresis	$\Delta INTV_{CC\ (UVLO)}$			115		mV
DV_{CC} Output Voltage	DV_{CC}	V_{DD} = 8.5 V and 80 V, I_{LOAD} = 0 mA	4.5	5	5.5	V
DV_{CC} Undervoltage Lockout	$DV_{CC\ (UVLO)}$	DV_{CC} rising	1.9	2.2	2.5	V
		DV_{CC} falling	1.7	2.0	2.3	V
Lockout Hysteresis				150		mV
GATE DRIVE						
External N-Channel Gate Drive at GATE1 and GATE2 (V_{GATE} − V_{SOURCE})[1]	$\Delta V_{GATE1}/\Delta V_{GATE2}$	V_{DD} = 8.5 V to 80 V, gate current (I_{GATE}) = 0 µA and −10 µA	10	12	14	V
GATE1 and GATE2 Pull-Up Current	$I_{GATE\ (UP)}$	Gate drive on, gate voltage (V_{GATE}) = source voltage (V_{SOURCE}) = 0 V	−35	−50	−70	µA
GATE1 and GATE2 Pull-Down Current	$I_{GATE\ (DN)}$	Gate drive off, V_{GATE} = 58 V, V_{SOURCE} = 48 V	6	10	15	mA
GATE1 and GATE2 Fast Pull-Down Current	$I_{GATE\ (FST)}$	Fast turn off, V_{GATE} = 58 V, V_{SOURCE} = 48 V		1		A
Gate Source Voltage for FET Bad and Power-Failed Faults and Turning on Low Stress FET	$V_{TH\ (GS)}$		6	8	10	V
ΔSENSE1/ΔSENSE2 High to GATE1 and GATE2 Low Propagation Delay	$t_{PHL(SENSE)}$	ILIM = 0000, ΔV_{SNS} = 0 mV step to 100 mV step, ΔV_{GATE} = 6 V, gate capacitance (C_{GATE}) = 10 nF		0.5	1	µs
GATE1 and GATE2 Propagation Delay—OV	$t_{PHL\ (GATE)\ OV}$					
Off		OV = high, ΔV_{GATE} = 6 V		1	2	µs
On		OV = low	0	5	10	µs
GATE1 and GATE2 Off Propagation Delay—UV	$t_{PHL\ (GATE)\ UV}$	UV = low, ΔV_{GATE} = 6 V gate open	0.3	2	3	µs
GATE1 and GATE2 Off Propagation Delay—EN	$t_{PHL\ (GATE)\ EN}$	EN = low, ΔV_{GATE} = 6 V gate open	15	40	70	µs
V_{DD} to Source Threshold Voltage for Turning on Low Stress FET Gate and Power Bad Faults	$V_{DS\ (LOW\text{-}STRESS\ FET)}$	V_{DD} to source falling	1.6	2.0	2.4	V
Propagation Delay for Turning Off Low Stress FET	$t_{PHL\ (LOW\text{-}STRESS\ FET)}$			13	30	µs
FET_BAD Fault Threshold (V_{DD} − SOURCE) to Start FET_BAD Timer	$V_{TH,\ FET\_BAD}$	V_{DD} to source rising				
		VDTH = 00	35	50	65	mV
		VDTH = 01	70	100	130	mV
		VDTH = 10	105	150	195	mV
		VDTH = 11	140	200	260	mV

ELECTRICAL CHARACTERISTICS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TIMING						
Power-Good Delay	$t_{DL\ (PG)}$	DB_DLY = 0	21.5	22.7	23.8	ms
		DB_DLY = 1	172	181	190	ms
Power-Good Watchdog Timer	$t_{DL\ (PGIWD)}$		551	580	609	ms
Debounce Delay, Auto-Retry Delay Following Undervoltage Fault	$t_{DL\ (DB)}$	DB_DLY = 0	10.8	11.3	11.9	ms
		DB_DLY = 1	86.1	90.6	95.2	ms
Auto-Retry Delay Following PGI Fault	$t_{DL\ (PGI\_RTRY)}$		0.551	0.580	0.609	Sec
FET_BAD Delay	$t_{DL\ (FET\_BAD)}$	FETBD_FLT_DL = 000	0.069	0.073	0.076	Sec
		FETBD_FLT_DL = 001	0.138	0.145	0.152	Sec
		FETBD_FLT_DL = 010	0.276	0.290	0.305	Sec
		FETBD_FLT_DL = 011	0.551	0.580	0.609	Sec
		FETBD_FLT_DL = 100	1.102	1.160	1.218	Sec
		FETBD_FLT_DL = 101	2.204	2.230	2.436	Sec
		FETBD_FLT_DL = 110	4.408	4.640	4.872	Sec
Auto-Retry Delay Following Overcurrent Fault (PIN_OP1_FAULT, PIN_OP2_FAULT, or FET_BAD_FAULT)	$t_{DL\ (RTRY)}$	COOLING_DL = 000	0.551	0.580	0.609	Sec
		COOLING_DL = 001	1.10	1.16	1.22	Sec
		COOLING_DL = 010	2.20	2.32	2.44	Sec
		COOLING_DL = 011	4.41	4.64	4.87	Sec
		COOLING_DL = 100	8.82	9.28	9.74	Sec
		COOLING_DL = 101	17.6	18.6	19.5	Sec
		COOLING_DL = 110	35.3	37.1	39.0	Sec
		COOLING_DL = 111	70.5	74.2	78.0	Sec
Auto-Retry Counter Reset Delay	$t_{DL\ (RTCRST)}$	VIN_UV_FAULT_RETRY, VIN_OV_FAULT_RETRY, OC_FAULT_RETRY, FET_BAD_RETRY, OT_FAULT_RETRY, PGI_RETRY, OP_FAULT_RETRY = 001 to 110	88.2	92.8	97.4	Sec
OP1 Fault Unit Delay	$t_{DL\ (OP1\text{-}UNIT)}$	Delay = OP_TIMER (Value) × Unit Delay	1.08	1.13	1.19	ms
Power Off Unit Delay	$t_{DL\ (PWROFF\ UNIT)}$	Delay = POWER_OFF_DELAY (Value) × Unit Delay	135	142	149	µs
Auto-Reboot Delay	$t_{DL\ (RBT)}$	After REBOOT is set to 1 via the PMBus command				
		RBT_DL = 000	0.551	0.580	0.609	Sec
		RBT_DL = 001	1.10	1.16	1.22	Sec
		RBT_DL = 010	2.20	2.32	2.44	Sec
		RBT_DL = 011	4.41	4.64	4.87	Sec
		RBT_DL = 100	8.82	9.28	9.74	Sec
		RBT_DL = 101	17.6	18.6	19.5	Sec
		RBT_DL = 110	35.3	37.1	39.0	Sec
		RBT_DL = 111	70.5	74.2	78.0	Sec
CURRENT LIMIT						
Current-Limit Sense Voltage Threshold ($V_{SENSE+} - V_{SENSE-}$)	ΔV_{SNS}	ILIM = 0000	4.67	5	5.33	mV
		ILIM = 1111	18.55	20	21.45	mV
Foldback Factor	α	10%	5	10	15	%
		30%	15	30	45	%
Current-Limit Sense Voltage Linearity				0	±100	µV
Fast Pull-Down Threshold Multiplier	$V_{(TH)FPD}$			3		Ratio
SENSE1+ and SENSE2+ Input Current	$I_{SENSE1+\ (IN)}$/ $I_{SENSE2+\ (IN)}$	SENSE1+ = SENSE2+ = SENSE1− = SENSE2− = 48 V	0	120	250	µA

ELECTRICAL CHARACTERISTICS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SENSE1− Input Current	$I_{SENSE1-(IN)}$	SENSE1− = SENSE1+ = 48 V, all other modes		0	±1	µA
		SENSE1− = SENSE1+ = 48 V, high stress staged start (HSSS) mode, Channel 2 off	4	5	6	µA
SENSE2− Input Current	$I_{SENSE2-(IN)}$	SENSE2− = SENSE2+ = 48 V		0	±1	µA
OVERCURRENT TIMER						
TMR Fault Threshold	$V_{TMR(H)}$	V_{TMR} rising	2.5	2.56	2.62	V
TMR Low Threshold	$V_{TMR(L)}$	V_{TMR} falling	0.18	0.2	0.22	V
TMR Thermal Pull-Up Current	$I_{TMR, THERM(UP)}$	V_{TMR} = 0 V, SENSE2+ − SENSE2− (ΔV_{SNS2}) = 10 mV, V_{DD} − VDSFB voltage (V_{VDSFB}) = 6 V	−120	−100	−80	µA
		V_{TMR} = 0 V, ΔV_{SNS2} = 0 mV, V_{DD} − V_{VDSFB} = 0 V	−5	0	+1	µA
		V_{TMR} = 0 V, ΔV_{SNS2} = 1.6 mV, V_{DD} − V_{VDSFB} = 12 V	−39	−32	−21	µA
		V_{TMR} = 0 V, ΔV_{SNS2} = 20 mV, V_{DD} − V_{VDSFB} = 50 mV	−2.5	−1.4	+1	µA
TMR Pull-Up Current	$I_{TMR(UP)}$	V_{TMR} = 0 V	−25	−20	−15	µA
TMR Pull-Down Current	$I_{TMR(DN)}$	V_{TMR} = 2.56 V	3	5	7	µA
INPUT PINS						
UV, OV, and FB Threshold Voltage	$V_{(TH)UV/OV/FB}$	$V_{UV}/V_{OV}/V_{FB}$ rising	2.51	2.56	2.61	V
OV Threshold Voltage	$V_{(TH)OV-F}$	OV voltage (V_{OV}) falling	2.3	2.5	2.6	V
OV Hysteresis	$\Delta V_{(HYST)OV}$			55		mV
FB Threshold Voltage	$V_{(TH)FBF}$	FB voltage (V_{FB}) falling	2.3	2.5	2.61	V
FB Hysteresis	$\Delta V_{(HYST)FB}$			79		mV
UV Threshold Voltage	$V_{(TH)UVF}$	UV voltage (V_{UV}) falling	2.15	2.2	2.25	V
UV Hysteresis	$\Delta V_{(HYST)UV}$			360		mV
UV Retry Threshold Voltage	$V_{(TH)UVR}$	V_{UV} falling	0.95	1.0	1.05	V
		V_{UV} rising	1	1.1	1.2	V
UV Retry Threshold Hysteresis	$\Delta V_{(HYST)UVR}$			100		mV
ADR0, ADR1, and MODE Input High Threshold	$V_{ADR, MODE(H)}$		$INTV_{CC}$ − 0.8	$INTV_{CC}$ − 0.5	$INTV_{CC}$ − 0.2	V
ADR0, ADR1, and MODE Input Low Threshold	$V_{ADR, MODE(L)}$		0.2	0.5	0.8	V
ADR0, ADR1, and MODE Input Current	$I_{ADR, MODE(IN)}$	$V_{ADR, MODE}$ = 1 V, V_{PIN} = $INTV_{CC}$ − 0.85 V			±10	µA
EN and GPIO1 to GPIO8 Input Threshold Voltage	$V_{EN/GPIO(TH)}$	$V_{EN/GPIO}$ rising	1.25	1.28	1.31	V
EN and GPIO1 to GPIO8 Hysteresis	$\Delta V_{EN/GPIO(HYST)}$			20		mV
VDSFB Internal Resistor	R_{VDSFB}		75	120	150	kΩ
VDSFB Leakage Current	$I_{LEAK, VDSFB}$	VDSFB = 0 V, V_{DD} = 80 V, FET off		0	±1	µA
SOURCE Input Current	I_{SOURCE}	V_{SOURCE} = 48 V, FET on			300	µA
		V_{SOURCE} = 0 V, FET off			−200	µA
		V_{SOURCE} = 2 V, FET off	0		500	µA
GPIO5 (COMM) Pin Threshold Voltage	$V_{GPIO5(TH)}$	Low 1, low stress staged start mode (LSSS) on	0.18	0.25	0.3	V
		Low 2, global on	1.05	1.55	1.9	V
		High, global electronic current limit (ECL) engaged	$INTV_{CC}$ − 2	$INTV_{CC}$ − 1.5	$INTV_{CC}$ − 1	V
GPIO5 (COMM) Pin Clamp Voltage	$V_{GPIO5(CLAMP)}$	Low	0.35	0.75	1.0	V
		Mid	2.3	2.56	2.7	V

ELECTRICAL CHARACTERISTICS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
GPIO5 (COMM) Pin,	I_{GPIO5}	Source current	−4	−5	−6	µA
		Sink current	3			mA
OV, UV, EN, and FB Input Current	I_{INPUT}	OV, UV, EN, and FB = 3 V		0	±1	µA
OUTPUT PINS						
GPIO1 to GPIO8 Output Low Voltage	$V_{OL, GPIO}$	GPIO1 to GPIO8 current ($I_{GPIO1\ to\ GPIO8}$) = 3 mA		0.2	0.5	V
GPIO1 to GPIO8 Leakage Current	$I_{LEAK, GPIO}$	GPIO4 and GPIO8 = 6 V, GPIO1, GPIO2, and GPIO6 = 80 V, GPIO3, GPIO5, GPIO7 = $INTV_{CC}$		0	±1	µA
GPIO3 Pull-Up Current	I_{PU_GPIO3}	GPIO3 configured as GPO or IOUT_OC_STATUS output	−8	−10	−12	µA
GPIO5 Pull-Up Current	I_{PU_GPIO5}	GPIO5 configured as GPO or SHED_LOADS output	−4	−5	−6	µA
ADC						
Resolution (No Missing Codes)[2]		All channels				
		15BIT = 0	12			Bits
		15BIT = 1	15			Bits
Full-Scale Voltage	V_{FS}	(ADC+ – ADC−), (SENSE1+/SENSE2+ – SENSE1−/SENSE2−)		32		mV
		V_{DS}		320		mV
		ADIN1 to ADIN2		2.56		V
		V_{IN} (V_{DD})/V_{OUT} (SOURCE), 25 V range		25.6		V
		V_{IN} (V_{DD})/V_{OUT} (SOURCE), 100 V range		102.4		V
LSB Step Voltage	LSB	(ADC+ – ADC−), (SENSE1+/SENSE2+ – SENSE1−/SENSE2−)				
		15_BIT_MODE = 0		7.8		µV
		15_BIT_MODE = 1		0.98		µV
		V_{DS}				
		15_BIT_MODE = 0		78		µV
		15_BIT_MODE = 1		9.8		µV
		ADIN1 to ADIN2				
		15_BIT_MODE = 0		0.625		mV
		15_BIT_MODE = 1		78		µV
		V_{IN} (V_{DD})/V_{OUT} (SOURCE), 25 V range				
		15_BIT_MODE = 0		6.25		mV
		15_BIT_MODE = 1		0.78		mV
		V_{IN} (V_{DD})/V_{OUT} (SOURCE), 100 V range				
		15 bit = 0		25		mV
		15 bit = 1		3.13		mV
Offset Error, 15BIT = 0	V_{OS}	ADC+ – ADC−, SENSE1+/SENSE2+ – SENSE1−/SENSE2−			±20	LSB
		V_{DD}/SOURCE, ADIN1 to ADIN2			±10	LSB
		V_{DS}	−50		+10	LSB
Integral Nonlinearity, 15BIT = 0	INL			±1		LSB
Full-Scale Error, 15BIT = 0	FSE	(ADC+ – ADC−), VDD/SOURCE, ADIN1 to ADIN2			±1	%
		(SENSE1+/SENSE2+ – SENSE1−/SENSE2−), V_{DS}	−3		+1	%

ELECTRICAL CHARACTERISTICS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Refresh Rate in Continuous Mode, Internal Oscillator	f_{CONV}	(ADC+ – ADC−), V_{DD}/SOURCE, ADIN1-2, POWER				
		15_BIT_MODE = 0	3.36	3.53	3.71	kHz
		15_BIT_MODE = 1	421	442	465	Hz
		(SENSE1+/SENSE2+ – SENSE1−/SENSE2−), V_{DS}				
		15_BIT_MODE = 0	1.68	1.77	1.86	kHz
		15_BIT_MODE = 1	210	221	232	Hz
Individual Channel Conversion Time, Internal Oscillator	t_{CONV}	(ADC+ – ADC−), (SENSE1+/SENSE2+ – SENSE1−/SENSE2−), V_{DS}				
		15_BIT_MODE = 0	269	283	310	µs
		15_BIT_MODE = 1	2.15	2.26	2.37	ms
		V_{DD}/SOURCE, ADIN1-2				
		15_BIT_MODE = 0	269	283	310	µs
		15_BIT_MODE = 1	2.15	2.26	2.37	ms
ADC+ Input Current	I_{ADC+}	ADC+ = V_{DD} = 48 V, ADC− = V_{DD} – 21.3 mV		73	132	µA
ADC− Input Current	I_{ADC-}	ADC+ = V_{DD} = 48 V, ADC− = V_{DD} – 21.3 mV		0	±1	µA
ADIN1 to ADIN2 Input Impedance, Single-Ended	$R_{ADIN (SE)}$	ADIN1 to ADIN2 = 2 V	2	10		MΩ
ADIN1 to ADIN2 Input Current, Single-Ended	$I_{ADIN (SE)}$	ADIN1 to ADIN2 = 2 V		0	±1	µA
TEMPERATURE MEASUREMENT						
Resolution (No Missing Codes)[2]				10		Bits
Refresh Rate in Continuous Mode	f_{TCONV}			3.45		Hz
Full-Scale Temperature Range	R_{TFS}		−273		+751	°C
Temperature Measurement Range	R_{TOP}		−55		+175	°C
Remote Temperature Error, η = 1.004	T_{RMT}	−40°C to +125°C[3]		±1	±10	°C
Temperature LSB Step	LSB_{TEMP}			1		°C
TEMP Current	I_{TEMP}	Low level		10		µA
		Midlevel		80		µA
		High level		150		µA
SMBus INTERFACE[4]						
SDAO Output Low Voltage	$V_{SDAO (OL)}$	I_{SDAO} = 20 mA		0.15	0.5	V
SDAO Input Current	I_{SDAO}	SDAO = 5 V		0	±1	µA
SDAI and SCL Input Threshold	$V_{SDAI, SCL (TH)}$		0.9	1.1	1.35	V
SDAI and SCL Input Current	$I_{SDAI, SCL}$	SDAI and SCL= 5 V		0	±1	µA
SMBus INTERFACE TIMING[24]						
SCL Clock Frequency	f_{SCL}		10		1000	kHz
SCL Low Period	t_{LOW}		0.40			µs
SCL High Period	t_{HIGH}		0.20			µs
Data Setup Time	$t_{SU, DAT}$		20			ns
Data Hold Time	$t_{HD, DAT}$		0			ns
Hold Time Start Bit	$t_{HD, STA}$		160			ns
Setup Time for Repeated Start	$t_{SU, STA}$		160			ns
Setup Time for Stop Bit	$t_{SU, STO}$		160			ns
SDAO Delay	$t_{DEL:SDAO}$	SDAO delay from SCL ↓ for maximum load capacitance (C_{LOAD}) = 550 pF				
		SEL_1M = 0	100	175	405	ns
		SEL_1M = 1	75	125	220	ns

ELECTRICAL CHARACTERISTICS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SCL or SDAI Pulse Spike Rejection[2]	t_{PW}		55	75	110	ns
PMBus Stuck Bus Timeout	$t_{D\ (STUCK)}$		25	30	35	ms
SCL and SDA Input Capacitance	C_X	SDAI tied to SDAO		5	10	pF
SERIAL PERIPHERAL INTERFACE (SPI)						
SIO Input Low Voltage	V_{IL}		−0.3		0.3 × DV_{CC}	V
SIO Input High Voltage	V_{IH}		0.7 × DV_{CC}		DV_{CC} + 0.3	V
$\overline{CS}$, SCK, and SIO Output Threshold Low Voltage	V_{OL}	Output low threshold current (I_{OL}) = 3 mA			0.4	V
$\overline{CS}$, SCK, and SIO Output Threshold High Voltage	V_{OH}	Output high threshold current (I_{OH}) = −1.6 mA	DV_{CC} − 0.8			V
$\overline{CS}$, SCK, and SIO Tristate Input Current	$I_{CS,\ SCK,\ SIO}$	CS, SCK, and SIO = 5 V		0	±1	µA
SIO, SCK, and $\overline{CS}$ Rise Time	t_{RISE}	C_{LOAD} = 50 pF			100	ns
SIO, SCK, and $\overline{CS}$ Fall Time	t_{FALL}	C_{LOAD} = 50 pF			40	ns
CONFIGURATION WITHOUT EEPROM						
SIO Input High Threshold Voltage	$V_{SIO-SU\ (H)}$	Only during device configuration at startup	$INTV_{CC}$ − 0.8	$INTV_{CC}$ − 0.5	$INTV_{CC}$ − 0.2	V
SIO Input Low Threshold Voltage	$V_{SIO-SU\ (L)}$	Only during device configuration at startup	0.2	0.5	0.8	V
SIO Input Current	$I_{SIO-SU\ (IN)}$	V_{SIO} = 1 V, V_{SIO} = $INTV_{CC}$ − 0.85 V, only during device configuration at startup	±10			µA
SCK Pin Input Current	I_{SCK-SU}	Only during device configuration at startup		0	±1	µA
$\overline{CS}$ Pin Input Current	I_{CS-SU}	Only during device configuration at startup	−8	−10	−12	µA
$\overline{CS}$ Input Threshold Voltage	$V_{CS-SU\ (TH)}$	Only during device configuration at startup				
		Low	0.9	1	1.1	V
		High	2.3	2.56	2.8	V
CRYSTAL OSCILLATOR						
CLKIN Rising Threshold	V_{TH}		0.3	0.6	0.9	V
CLKIN Pin Input Frequency	f_{XLKIN}		5.82	8.192	10.2	MHz
CLKIN Input Current	I_{CLKIN}	CLKIN voltage (V_{CLKIN}) = 0 V to 5 V, input resistance (R_{IN}) = 2 kΩ	−3		+3	mA
CLKOUT Output Current	I_{CLKOUT}	CLKOUT voltage (V_{CLKOUT}) = 0 V to 5 V	−10		+10	mA

1 An internal clamp limits the GATE pin to a minimum of 10 V above SOURCE. Driving this pin to voltages beyond the clamp can damage the device.

2 Guaranteed by design and characterization.

3 Remote diode temperature, not LTC4287 temperature. Guaranteed by design and test correlation.

4 The LTC4287 is fully compliant with SMBus 3.1 and operation up to 1 Mbps. In general, the chip can be used in I^2C bus systems using standard mode, fast mode, or fast mode plus as long as PMBus command protocols are followed. A V_{IH}/V_{IL} incompatibility between SMBus 3.1 and I^2C can lead to a DC level violation for I^2C buses running at 3.5 V or higher.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Value
Supply Voltages	
V_{DD}	−0.3 V to +100 V
$INTV_{CC}$ and DV_{CC}	−0.3 V to +5.5 V
Input Voltages	
SDAI and SCL	−0.3 V to +6 V
CLKIN	−0.3 V to +1 V
OV, UV, FB, and EN	−0.3 V to +100 V
VDSFB	−0.3 V to V_{DD} + 0.3 V
TMR, ADR0, ADR1, and MODE	−0.3 V to $INTV_{CC}$ + 0.3 V
ADC+, SENSE1+, and SENSE2+	V_{DD} − 4.5 V to V_{DD} + 0.3 V
ADC−, SENSE1−, and SENSE2−	V_{DD} − 4.5 V to V_{DD} + 0.3 V
SOURCE	−0.3 V to +100 V
GATE1/GATE2 – SOURCE[1]	−0.3 V to +10 V
Input Currents	
CLKIN	4 mA
Output Voltages	
SCK, SIO, and $\overline{CS}$	−0.3 V to DV_{CC} + 0.3 V
CLKOUT	−0.3 V to $INTV_{CC}$ + 0.3 V
GPIO1, GPIO2, and GPIO6	−0.3 V to +100 V
GPIO3, GPIO5, and GPOI7	−0.3 to $INTV_{CC}$ + 0.3 V
GATE1 and GATE2	−0.3 V to +100 V
SDAO, GPIO4, and GPIO8	−0.3 V to +6 V
Output Currents	
$INTV_{CC}$ and DV_{CC}	−5 mA
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C

[1] Internal clamps limit the GATE pins to a minimum of 10 V more than SOURCE. Driving the GATE pins to voltages beyond the clamps may damage the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
05-08-1792	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

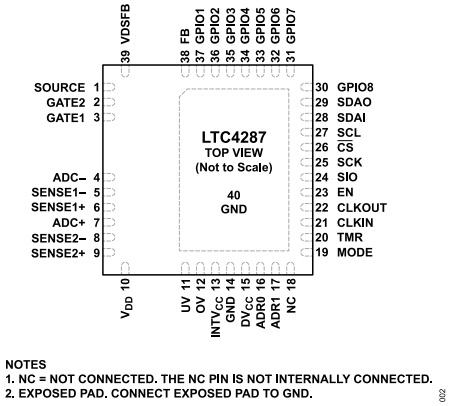

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SOURCE	N-Channel MOSFET Source and ADC Input. Connect the SOURCE pin to the source of the external N-channel MOSFET. The SOURCE pin provides a return for the GATEx pull-down circuit, and it is used as an input to the 200 mV and 2 V V_{DS} comparators that are used for the FET_BAD faults and power good, respectively. The SOURCE pin also serves as an ADC input to monitor the output voltage.
2	GATE2	Gate Drive Output for External N-Channel MOSFET. An internal 50 µA current source charges the gate of the MOSFET. No compensation capacitors are required on the GATE2 pin, but an RC network from the GATE2 pin to ground can be used to set the turn-on output voltage slew rate. During turn-off, there is a 10 mA pull-down current to SOURCE and a 1 mA pull-down current to GND. During a short-circuit or undervoltage lockout, UVLO, (V_{DD} and $INTV_{CC}$), a 1 A pull-down between GATE2 and SOURCE is activated. GATE2 is the start-up GATE for LSSS and the bypass GATE for HSSS. If only one MOSFET is used, leave the GATE2 pin open and connect SENSE2+ and SENSE2− to V_{DD}.
3	GATE1	Gate Drive Output for External N-Channel MOSFET. An internal 50 µA current source charges the gate of the MOSFET. No compensation capacitors are required on the GATE1 pin, but an RC network from the GATE1 pin to ground can be used to set the turn-on output voltage slew rate. During turn-off, there is a 10 mA pull-down current to SOURCE and a 1 mA pull-down current to GND. During a short-circuit or UVLO (V_{DD} and $INTV_{CC}$), a 1 A pull-down between GATE1 and SOURCE is activated. GATE1 is used when only one MOSFET is needed, and it is the start-up GATE for HSSS operation and the bypass GATE for LSSS operation.
4	ADC−	Negative Kelvin ADC Current Sense Input. Use a resistive divider between the two SENSE− pins to measure the average of the two SENSE− voltages. Tie to SENSE1− when using a single sense resistor.
5	SENSE1−	Negative Kelvin Current Sense Input. Connect this pin to the MOSFET side of the current sense resistor. The current-limit circuit controls the GATE1 pin to limit the sense voltage between the SENSE1+ and SENSE1− pins to the limit value selected by the SCK pin or ILIM register bits.
6	SENSE1+	Positive Kelvin Current Sense Input for GATE1. Connect this pin to the VDD side of the current sense resistor.
7	ADC+	Positive Kelvin ADC Current Sense Input. Use a resistive divider between the two SENSE+ pins to measure the average of the two SENSE+ voltages. Tie to SENSE1+ when using a single sense resistor. ADC+ must be connected to the same trace as V_{DD} or a resistive averaging network that adds up to 1 Ω to V_{DD}.
8	SENSE2−	Negative Kelvin Current Sense Input for GATE2. Connect the SENSE2− pin to the MOSFET side of the current sense resistor. The current-limit circuit controls the GATE2 pin to limit the sense voltage between the SENSE+ and SENSE− pins to the limit the values selected by the SCK pin or ILIM register bits. Tie to V_{DD} if unused.
9	SENSE2+	Positive Kelvin Current Sense Input for GATE2. Connect the SENSE2+ pin to the V_{DD} side of the current sense resistor. Tie to V_{DD} if unused.
10	V_{DD}	Supply Voltage Input. The V_{DD} pin has an UVLO threshold of 6 V. V_{DD} is an input for the FET_BAD comparator with a 50 mV to 200 mV threshold. V_{DD} is also an input for the power bad comparator with a 2 V threshold. The ADC can be configured to measure the voltage at the V_{DD} pin.
11	UV	Undervoltage Comparator Input. Connect the UV pin to an external resistive divider from V_{DD} to GND. If the UV pin falls to less than 2.2 V, an undervoltage occurs, and the MOSFET turns off. If the UV pin rises to more than 2.56 V, the MOSFET turns on after a configurable debounce delay of 11.3 ms or 90.6 ms. Pulling the UV pin to less than 1 V adds one retry to the retry counter for an overcurrent, FET_BAD, overtemperature, or overpower fault, which is linked to the $\overline{\text{FAULT}}$ GPIO output in MFR_FLT_CONFIG if that fault has zero remaining retries. If overcurrent auto-retry is required, tie the UV pin to the GPIO2 pin, which is configured as a $\overline{\text{FAULT}}$ output that reports overcurrent and FET_BAD faults by

PIN CONFIGURATION AND FUNCTION DESCRIPTION

Table 4. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
		default. Tie UV to $INTV_{CC}$ if unused or connect UV to a GPIOx pin with a 4.7 kΩ pull-up to $INTV_{CC}$ if only the auto-retry function is used.
12	OV	Overvoltage Comparator Input. Connect OV to an external resistive voltage divider from V_{DD} to GND. An overvoltage fault occurs if the OV pin is more than the 2.56 V threshold. When the OV pin voltage falls under the 2.5 V falling threshold, the GATE pin turns on again immediately. Tie OV to GND if unused.
13	$INTV_{CC}$	Internal Supply Decoupling Output. Connect a capacitor no smaller than 0.1 µF from the $INTV_{CC}$ pin to the ground. Up to 5 mA can be drawn from the $INTV_{CC}$ pin to power 5 V application circuitry. The $INTV_{CC}$ pin is current limited and drops to GND to reduce heating in an overcurrent condition. Overloading the $INTV_{CC}$ pin can disrupt internal operation. To reduce heating, the $INTV_{CC}$ pin can act as a shunt regulator by connecting a resistor to V_{DD} or another supply such that 10 mA flows to $INTV_{CC}$.
14	GND	Device Ground.
15	DV_{CC}	5 V Internal Logic Supply Output. The DV_{CC} pin is an output of the internal linear regulator with an UVLO threshold of 2 V. The voltage at the DV_{CC} pin powers up the logic control circuitry, SMBus interface, and EEPROM. Bypass the DV_{CC} pin with a 47 µF capacitor to provide DV_{CC} enough hold-up capacity to complete an EEPROM write if the V_{DD} supply collapses. When not using an external EEPROM, a 0.1 µF bypass is sufficient.
16, 17	ADR0, ADR1	Serial Bus Address Inputs. Tying the ADR0 and ADR1 pins to ground (low), open (NC), or $INTV_{CC}$ (high) configures one of the nine possible addresses. See Table 14.
18	NC	Not Connected. The NC pin is not internally connected.
19	MODE	Gate Drive Mode Configuration Input. When the MODE pin is tied to ground, GATE1 can be used as a single N-channel FET or used with GATE2 in a HSSS mode. GATE2 drives a second FET as a switch that turns on after GATE1 is enhanced and turns off whenever a fault condition occurs (Mode 1). When the MODE pin is open, the LSSS mode is selected (Mode 2). GATE2 drives a FET that turns on first and stands the stress during a fault condition. While GATE1 drives a second FET as a switch that turns on after GATE2 is enhanced and stays on during a fault condition to share the stress. When the MODE pin is tied to $INTV_{CC}$, the GATE1 and GATE2 pins are configured to drive two parallel FETs that turn on and turn off at the same time and share stresses (Mode 3). See Table 5 for more details. The status of the MODE pin can be read at any time in Table 12. When EEPROM is not present the MODE, SIO, SCK and $\overline{CS}$ pins select the start-up behavior for the device. See Configuration Without EEPROM.
20	TMR	Current-Limit Timer or SOA Timer Output. The mode of operation is set by the EEPROM, or when EEPROM is not present, the mode of operation is set by the MODE, SIO, SCK, and $\overline{CS}$ pins. In current-limit timer mode, connect a capacitor between the TMR pin and ground to set a 128 ms/µF duration for the current limit before the switch is turned off. In SOA timer mode, connect an RC network between the TMR pin and ground. The current charging the RC network is proportional to the power dissipation in the power path, which is equal to ΔV_{SENSE1} multiplied by the voltage difference between the V_{DD} and SOURCE pins as measured at the V_{DSFB} pin.
21	CLKIN	Crystal Oscillator Input. Connect the CLKIN pin to an optional external 8.192 MHz crystal oscillator circuit. Connect the CLKIN pin to ground if unused.
22	CLKOUT	Crystal Oscillator Output. Connect the CLKOUT pin to an optional external 8.192 MHz crystal oscillator circuit. Float the CLKOUT pin if unused.
23	EN	Enable Input. Hardware default is for active high EN. When active, the EN pin indicates that a board is present and allows the N-channel MOSFETs to turn on. When the EN pin is inactive, the MOSFETs are not allowed to turn on. Transitions on the EN pin set the EN_CHANGED bit in the MFR_SPECIFIC_STATUS register. A transition to the active level causes all faults to be cleared (except EN_CHANGED). See the On and Off Control with the EN Pin section.
24	SIO	SPI Data Input and Output for the SPI (Host) Interface to the External EEPROM. When the EEPROM is not present, the MODE, SIO, SCK, and $\overline{CS}$ pins select the start-up mode for the device. See Configuration Without EEPROM.
25	SCK	SPI Clock for the SPI (Host) Interface to the External EEPROM. When the EEPROM is not present, the MODE, SIO, SCK, and $\overline{CS}$ pins select the start-up mode for the device. See Configuration Without EEPROM section.
26	$\overline{CS}$	External EEPROM SPI Chip Select. When the EEPROM is not present, the $\overline{CS}$ pin configures the power-up state of the ON bit in the operation command. See the Configuration Without EEPROM section.
27	SCL	SMBus-Compatible Clock Input, High Impedance.
28	SDAI	Serial Bus Data Input. A high impedance input for shifting in the address, command, or data bits. Normally tied to SDAO to form the SDA line.
29	SDAO	Serial Bus Data Output. The open-drain output for sending data back to the controller or acknowledging a write operation. Normally tied to SDAI to form the SDA line. An external pull-up resistor or current source is required.
30	GPIO8	OP1_STATUS Indicator Output. The GPIO8 pin is pulled low when the ADCs measure a power level more than the Over Power 1 (OP1) threshold. Tie GPIO8 to GND if unused.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

Table 4. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
31	GPIO7	Comparator Output (CMPOUT). The GPIO7 pin is the output of the comparator on the GPIO6 pin. Tie GPIO7 to GND if unused.
32	GPIO6	Comparator Input (COMPIN). The GPIO6 pin has a 1.28 V threshold. The output of the comparator is available on GPIO7. Tie GPIO6 to GND if unused.
33	GPIO5	SHED_LOADS Input. In addition, configurable as a COMM bus. The GPIO5 pin has a 1.28 V threshold. Leave the GPIO5 pin open if unused.
34	GPIO4	IOUT_OC_STATUS Indicator Output. When the LTC4287 is in current limit, this open-drain output is pulled low to indicate an overcurrent condition. Tie GPIO4 to GND if unused.
35	GPIO3	Temperature (TEMP) Sensor Input. Connect GPIO3 to an MMBT3904 transistor for use as a remote temperature sensor. Tie GPIO3 to GND if unused.
36	GPIO2	$\overline{\text{FAULT}}$ Output. The GPIO2 pin pulls low when an overcurrent or FET_BAD fault occurs. The GPIO2 pin can be tied to the UV pin to clear faults and auto-retry after a fault occurs. Tie GPIO2 to GND if unused.
37	GPIO1	$\overline{\text{POWER\_GOOD}}$ Indicator Output. The GPIO1 open-drain pull-down pulls low when power is good, as determined by the FB pin and GATE pin voltages. Tie GPIO1 to GND if unused.
30 to 37	GPIO1 to GPIO8	General-Purpose Input and Output with Open-Drain Output Drivers. Several digital input and output functions are available for the GPIOx pins. Those functions can be assigned by configuration to any of the eight pins. With a few exceptions, the GPIOx pins behave identically. GPIO1, GPIO2, and GPIO6 can be externally pulled as high as V_{DD}. The GPIO3, GPIO4, GPIO5, and GPIO7 pins must not be pulled any higher than DV_{CC}. The external temperature sensor function is available on GPIO3 only, and the COMM function is available on GPIO5 only. The individual GPIOx pin descriptions further detail the hardware default configurations. By default, all alerts are disabled, and no GPIOx pins are assigned to ALERT, which can be changed after power-up by writing to the configuration registers.
38	FB	Power-Good Input. Connect the FB pin to an external resistive divider from SOURCE to GND. When the voltage at the FB pin drops to less than 2.56 V, power is not considered good. The power bad condition can result in a GPIOx pin $\overline{\text{POWER\_GOOD}}$ output pulling low or going high impedance depending on the GPIOx pin configuration. In addition, a power bad fault is logged in this condition if a GATEx pin is high. Tie FB to $INTV_{CC}$ if unused.
39	VDSFB	V_{DS} Foldback Sense Input. The VDSFB pin is used to monitor the drain to source voltage of the external MOSFETs, which is used by the SOA timer to monitor MOSFET power, as well as to set the foldback current limit. VDSFB is tied to SOURCE for 12 V applications, and an additional 10 kΩ/V is added for higher operating voltages to set the proper gain of the foldback circuit.
40	EPAD (GND)	Exposed Pad. Connect the exposed pad to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C and V_{DD} = 12 V, unless otherwise noted.

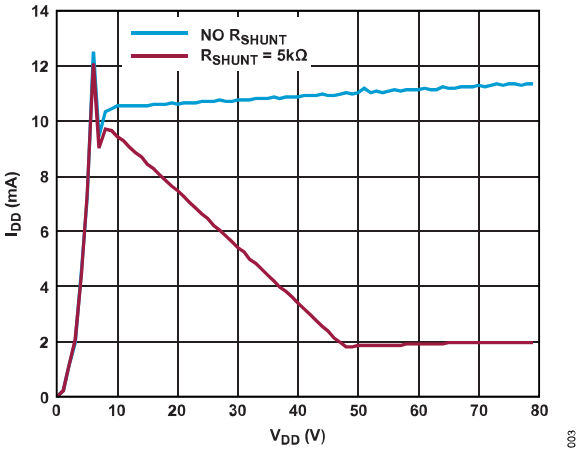

Figure 3. I_{DD} vs. V_{DD}

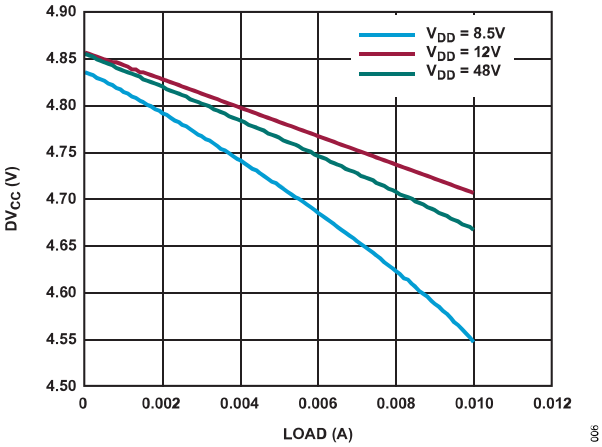

Figure 6. DV_{CC} vs. Load at V_{DD} = 8.5 V, 12 V, and 48 V

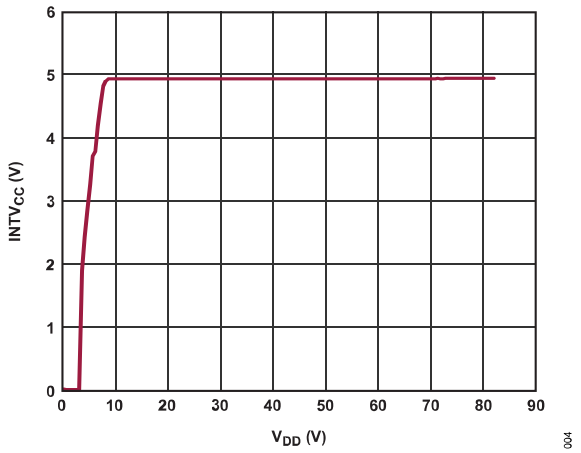

Figure 4. $INTV_{CC}$ vs. V_{DD}

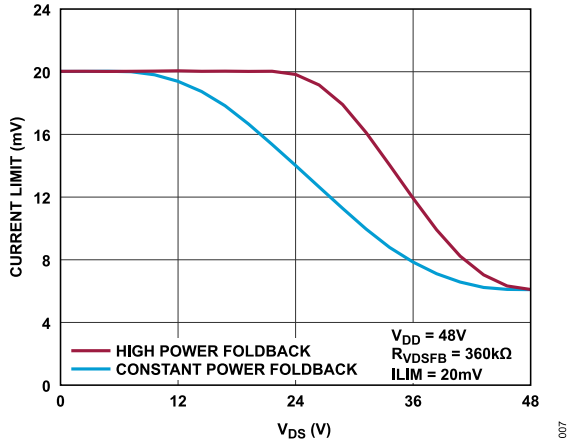

Figure 7. Current-Limit Foldback Profiles

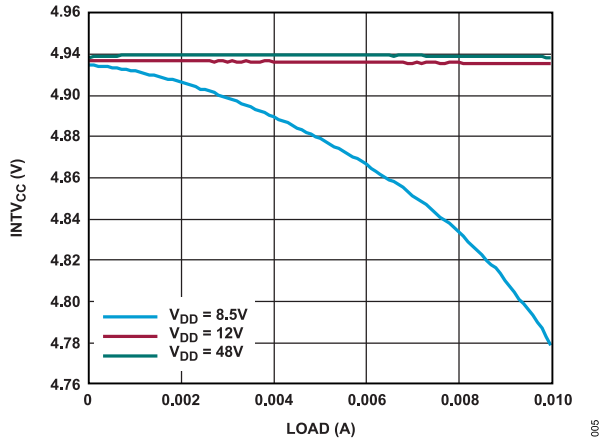

Figure 5. $INTV_{CC}$ vs. Load at V_{DD} = 8.5 V, 12 V, and 48 V

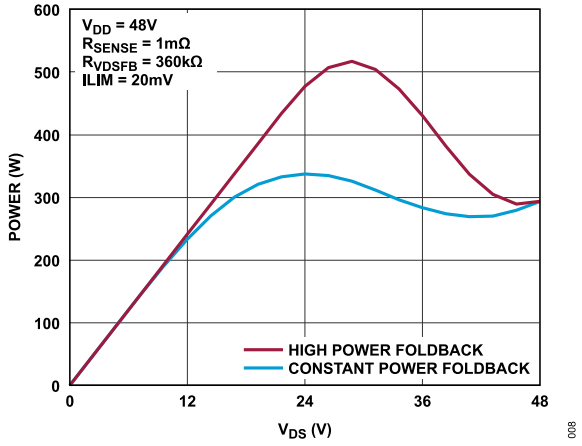

Figure 8. MOSFET Power vs. V_{DS}

TYPICAL PERFORMANCE CHARACTERISTICS

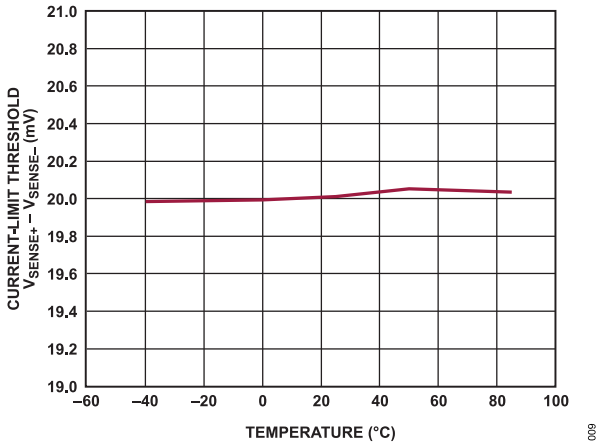

Figure 9. Current-Limit Threshold V_{SENSE+} – V_{SENSE-} vs. Temperature

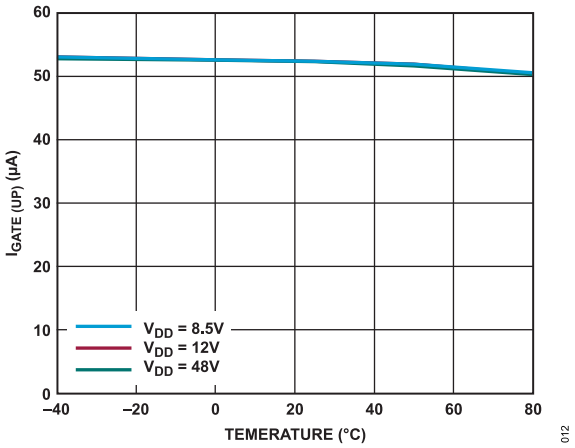

Figure 12. $I_{GATE\ (UP)}$ vs. Temperature

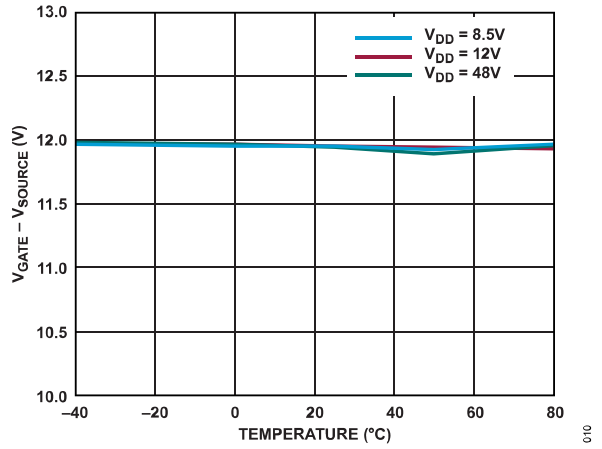

Figure 10. V_{GATE} – V_{SOURCE} vs. Temperature at V_{DD} = 8.5 V, 12 V, and 48 V

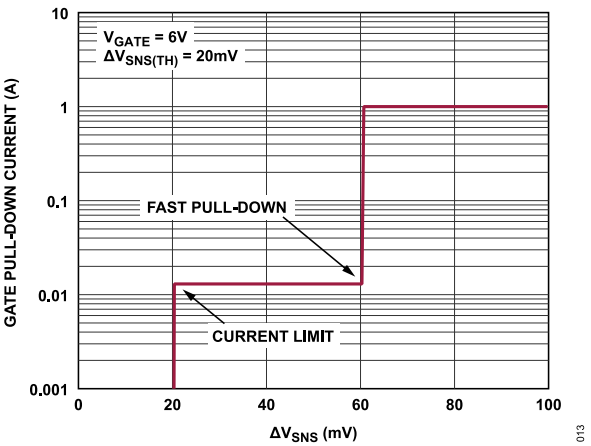

Figure 13. GATE Pull-Down Current vs. ΔV_{SNS}

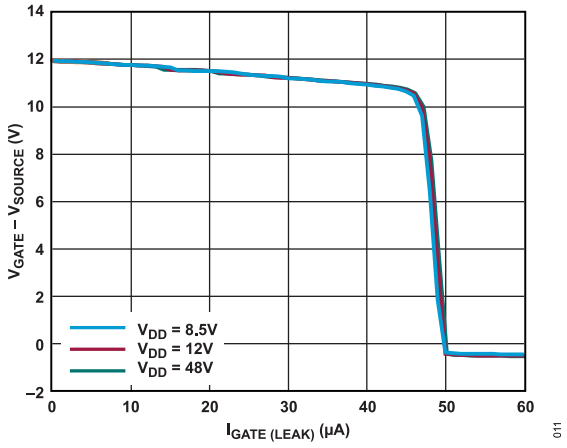

Figure 11. V_{GATE} – V_{SOURCE} vs. $I_{GATE\ (LEAK)}$ at V_{DD} = 8.5 V, 12 V, and 48 V

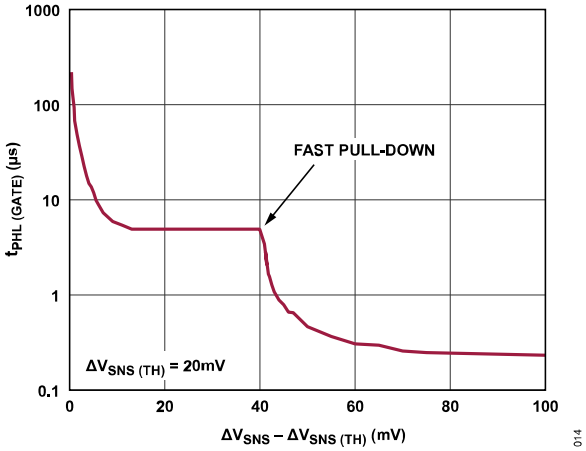

Figure 14. $t_{PHL\ (GATE)}$ vs. ΔV_{SNS} – $\Delta V_{SNS\ (TH)}$

TYPICAL PERFORMANCE CHARACTERISTICS

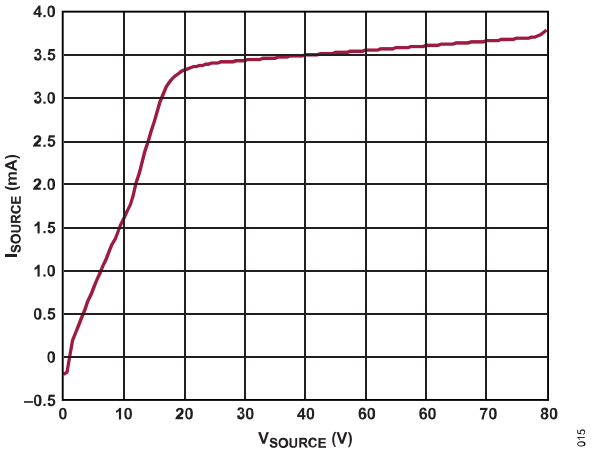

Figure 15. I_{SOURCE} vs. V_{SOURCE}

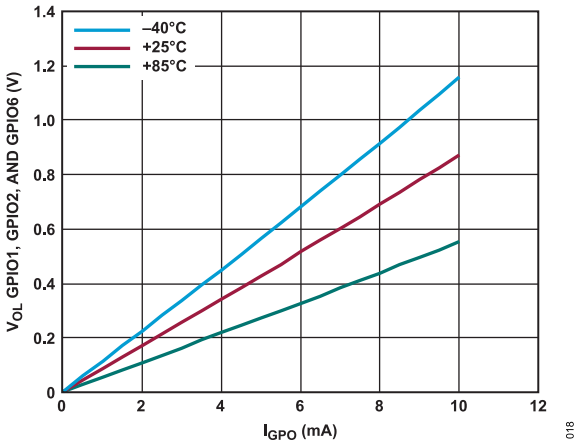

Figure 18. V_{OL} GPIO1, GPIO2, GPIO6 vs. I_{GPO} for Various Temperatures

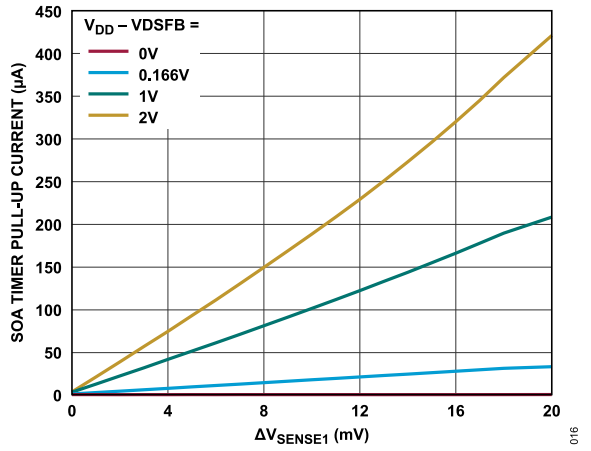

Figure 16. SOA Timer Pull-Up Current vs. ΔV_{SENSE1}

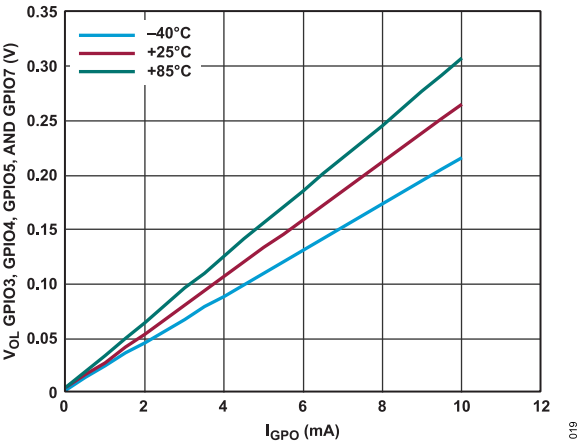

Figure 19. V_{OL} GPIO3, GPIO4, GPIO5, GPIO7 vs. I_{GPO}

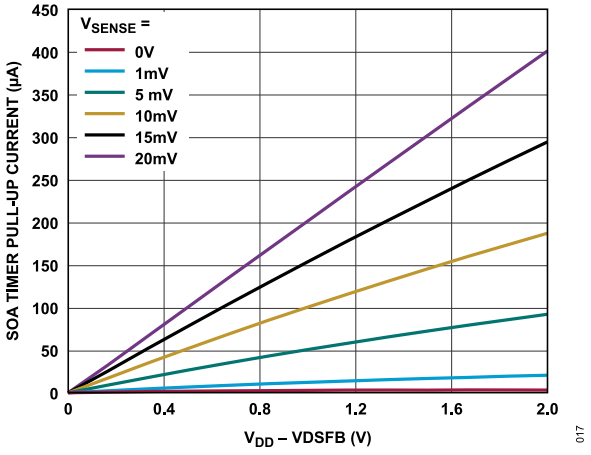

Figure 17. SOA Timer Pull-Up Current vs. V_{DD} – VDSFB

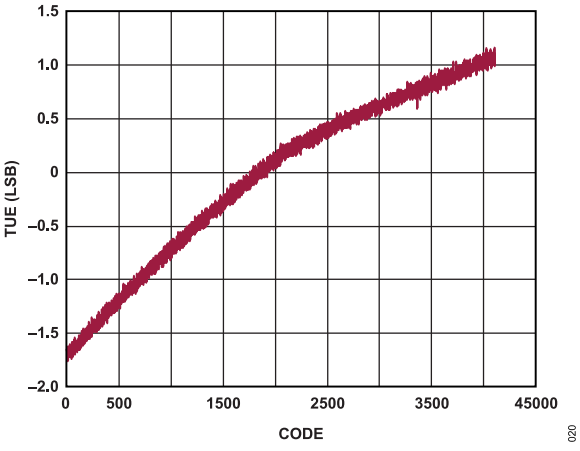

Figure 20. ADC TUE vs. Code (64× Average)

TYPICAL PERFORMANCE CHARACTERISTICS

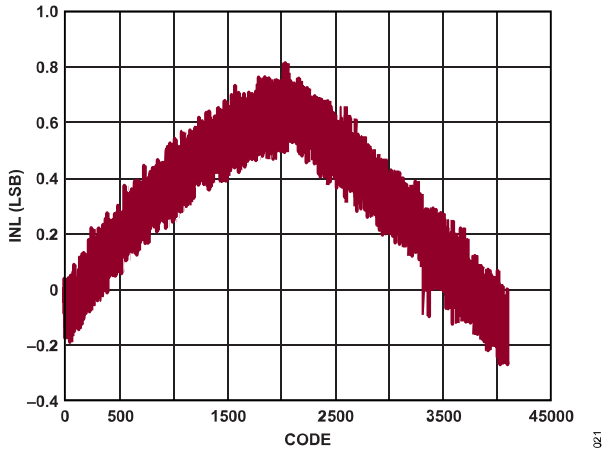

Figure 21. ADC INL vs. Code (64× Average)

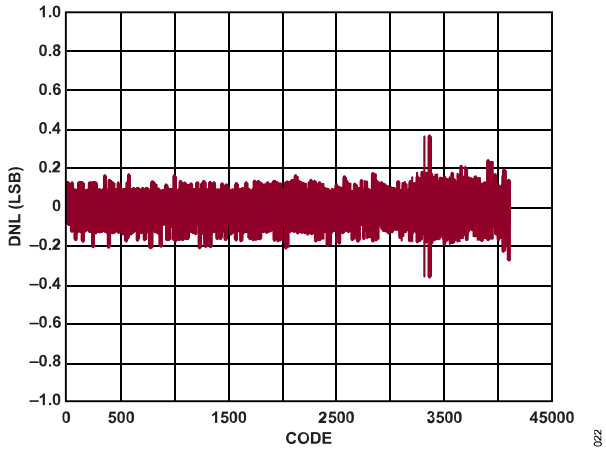

Figure 22. ADC DNL vs. Code (64× Average)

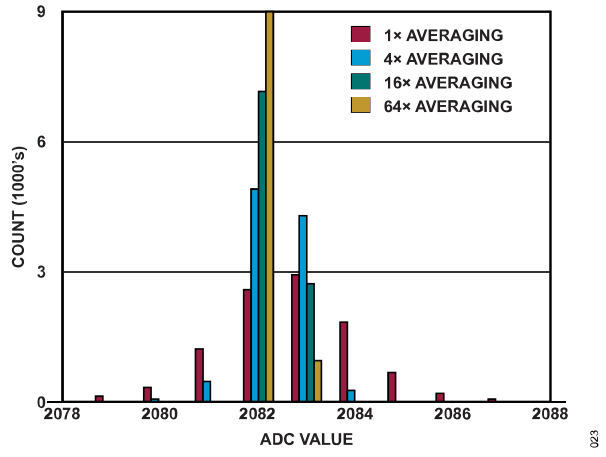

Figure 23. 12-Bit Current ADC Noise Histogram (No Averaging, 4×, 16×, and 64× Average)

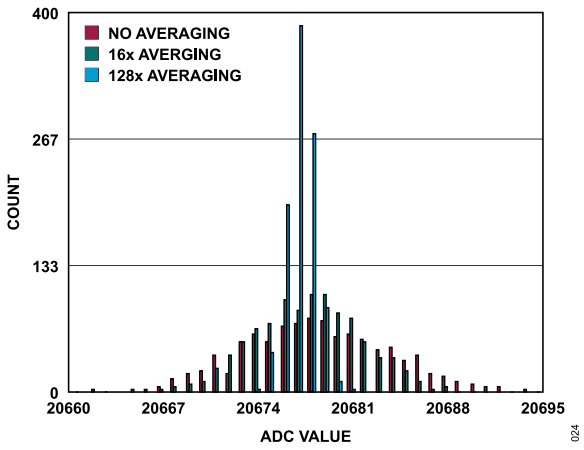

Figure 24. 15-Bit Current ADC Noise Histogram (No Averaging, 16×, and 128× Averaging)

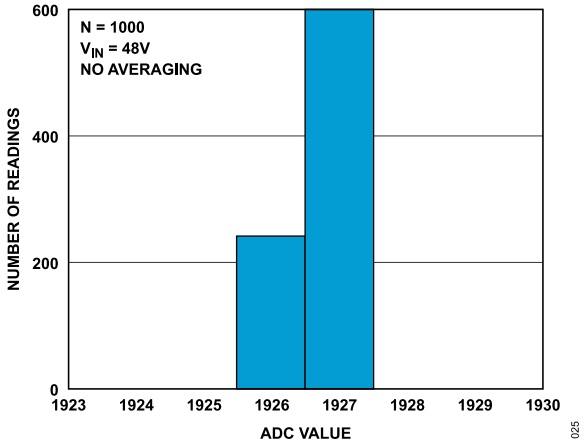

Figure 25. 12-Bit SOURCE ADC Noise Histogram

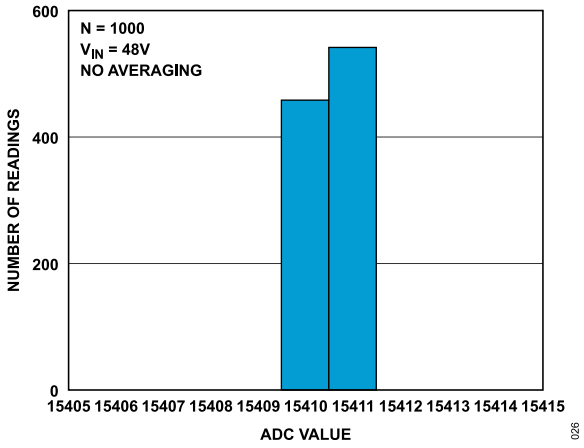

Figure 26. 15-Bit SOURCE ADC Noise Histogram

THEORY OF OPERATION

The LTC4287 is designed to turn the supply voltage of a board on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. During normal operation, the charge pumps and gate drivers turn on a pair of parallel external N-channel MOSFET gates to pass power to the load. The gate drivers use charge pumps that derive their power from the V_{DD} pin. The gate drivers also include internal 14 V GATEx to SOURCE clamps to protect the oxide of the external MOSFETs. The device features four distinct operation modes: single driver, parallel, HSSS, and LSSS. Each of these modes addresses specific application requirements for SOA, $R_{DS(ON)}$, and cost.

Figure 27 shows the monitoring blocks of the LTC4287. The group of comparators on the right side includes the UV, OV, and EN comparators. These comparators determine if the external conditions are valid prior to turning on the gates. However, first, the three undervoltage lockout circuits, UVLO1, UVLO2, and UVLO3, validate the input supply and the internally generated 5 V supplies, $INTV_{CC}$ and DV_{CC}. UVLO3 also generates the power-up initialization to the logic circuits and reads the contents of the EEPROM to the operating memory as DV_{CC} crosses this rising threshold.

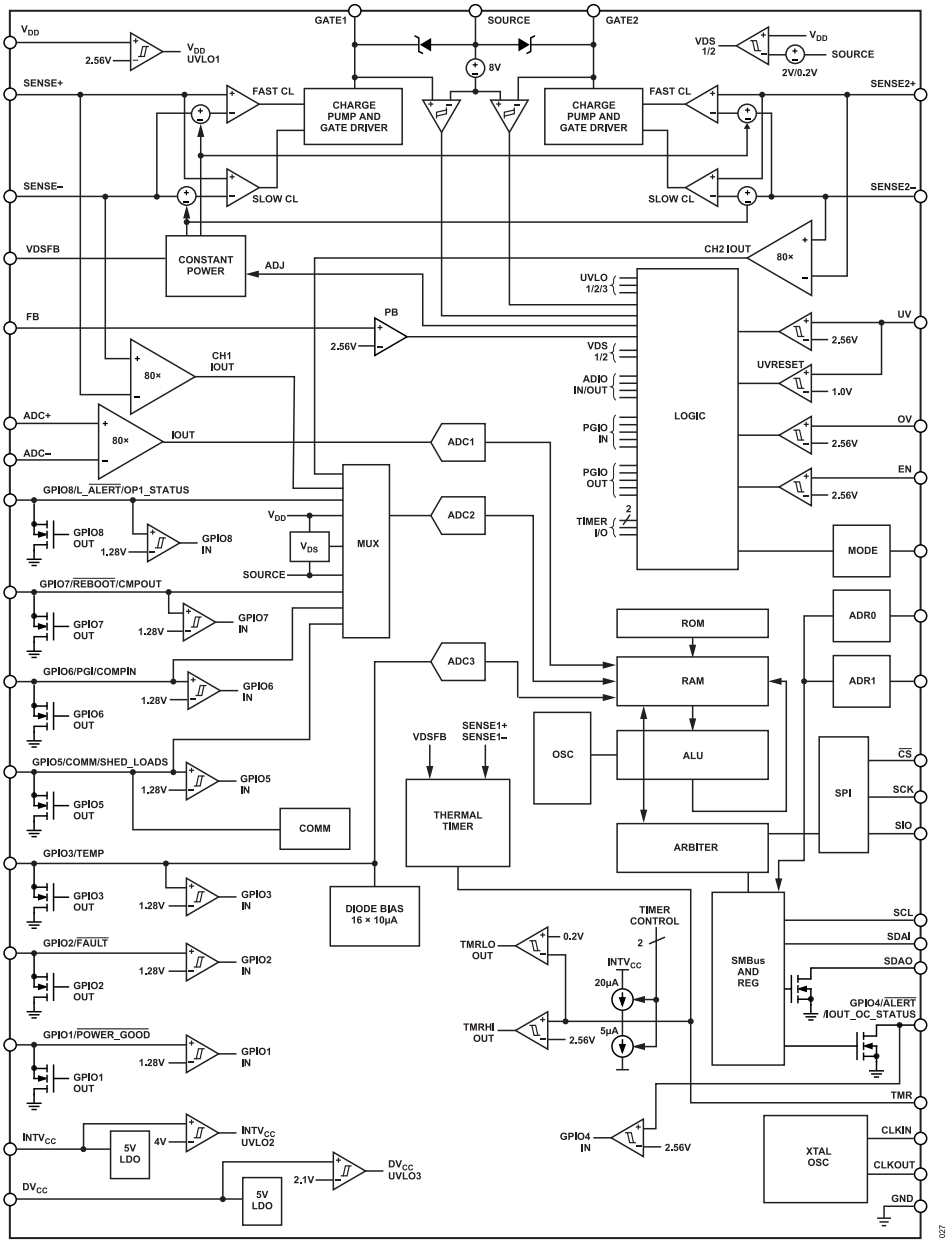

Figure 27. Functional Block Diagram

THEORY OF OPERATION

In normal operation, the LTC4287 turns on the external N-channel MOSFETs after a start-up debounce delay, passing power to the load. A precise current-limit value can be set from 5 mV to 20 mV in 1 mV steps using the SCK pin voltage or bits in the MFR_CONFIG1 register. During startup, the voltage between SENSE+ and SENSE− can be controlled to be no higher than 10% of the current-limit threshold or to the current-limit threshold with foldback (α). The start-up current can be set to even lower values with an external gate RC network.

An overcurrent fault at the output can result in excessive MOSFET power dissipation during active current limiting (ACL). To limit this power in each channel, the ACL amplifiers regulate the voltage between the SENSE1+ and SENSE1− and the SENSE2+ and SENSE2− pins by reducing the GATEx to SOURCE voltages in an active control loop when the sense voltages exceed the current-limit value. When the drain to source voltage of the MOSFET is high, power dissipation is further reduced by folding back the current limit to 30% of nominal. In the event of a catastrophic output short, fast current-limit comparators immediately pull the GATEx pins down with 1 A when the sensed current is three times of the nominal current limit.

The LTC4287 provides two ways of limiting the time that the system is exposed to overstress conditions: a MOSFET SOA timer or a current-limit timer. Make this selection via the MFR_CONFIG1 register or the state of the external EEPROM pins. If an EEPROM is not used, see Configuration Without EEPROM. If the MOSFET SOA timer is chosen, the TMR pin is pulled up by a current that is proportional to the power dissipation in the MOSFET driven by GATE1. With an RC network representing the thermal behavior of this MOSFET, the TMR voltage is proportional to the MOSFET temperature rise. When the TMR voltage reaches its threshold of 2.56 V (representing $T_{J(MAX)}$ of the MOSFET), the overcurrent fault is triggered. Both gates turn off to protect the MOSFETs based on their SOA. If the current-limit timer is chosen, the TMR pin is configured to drive a single capacitor and ramp up with 20 µA when active current limiting is engaged. If the TMR pin reaches its 2.56 V threshold, the LTC4287 turns off both gates and the IOUT_OC_FAULT bit is set. Then, the TMR pin ramps down using a 5 µA current source until the voltage drops to less than 0.2 V. If overcurrent auto-retry is enabled by tying the GPIO2 pin in its default $\overline{\text{FAULT}}$ configuration to the UV pin, the LTC4287 allows the MOSFETs to cool and then turn on again at the end of the selected COOLING_DL time, which is 9.28 sec by default.

The output voltage is monitored using the SOURCE pin and the power-good comparator to determine if the power is available for the load. The power-good condition can be signaled by one of the GPIOx pins using an open-drain pull-down transistor.

Included in the LTC4287 are three ADCs, and the first two ADCs operate at a 12-bit or a 15-bit resolution, and the last ADC operates at a 10-bit resolution. One data converter continuously monitors the ADC+ to ADC− voltage, sampling every 1 µs and producing a 12-bit result of the average sense voltage every 283 µs, while the other data converter synchronizes to the first one and measures the GPIOx voltage and SOURCE voltage during the same time period. Every time the ADCs finish taking a measurement, the sense voltage is multiplied by the measurement of the SOURCE pin to provide a power measurement. Every time power is measured, it is added to the energy accumulator that keeps track of how much energy has been transmitted to the load. The energy accumulator can generate an optional alert upon overflow. An accumulator also keeps track of how many times the power meter has been incremented, dividing the results of the energy accumulator by the time accumulator gives the average system power over a period up to 13 days at 12-bit resolution. The third data converter measures temperature on an external or internal diode with a 10-bit resolution and 1°C LSB. The minimum and maximum GPIOx, SOURCE, SENSE+ to SENSE−, ADC+ to ADC−, power, V_{DS}, and temperature measurements are stored, and optional alerts may be generated if a measurement is above or below user configurable 15-bit thresholds.

An external EEPROM provides nonvolatile configuration of the behavior of the LTC4287 and records fault information and data converter results for offline analysis.

A PMBus interface is provided to read the analog-to-digital registers. This interface also allows the host to poll the device and determine if faults have occurred. If a GPIOx pin is configured as an ALERT interrupt, the host is enabled to respond to faults in real time. The PMBus device target address is decoded using the ADR0 and ADR1 pins. These inputs have three different states that decode into a total of nine device addresses.

APPLICATIONS INFORMATION

A typical LTC4287 application is in a high availability system in which a positive voltage supply is distributed to power individual boards. The device measures board voltages and currents and records past and present fault conditions. The LTC4287 stores minimum and maximum ADC measurements, calculates power and energy, and can be configured to generate alerts based on measurement results, avoiding the need for the system to poll the device on a regular basis. The LTC4287 can use external nonvolatile EEPROM, allowing it to be configured during board level testing and avoid having to configure the hot-swap at every insertion.

APPLICATION 1: PARALLEL MODE

A typical application in parallel mode of the LTC4287 is shown in Figure 28. The following sections detail turn-on, turn-off, and various faults that the LTC4287 detects and acts upon. External component selection is discussed in detail in the Design Examples section.

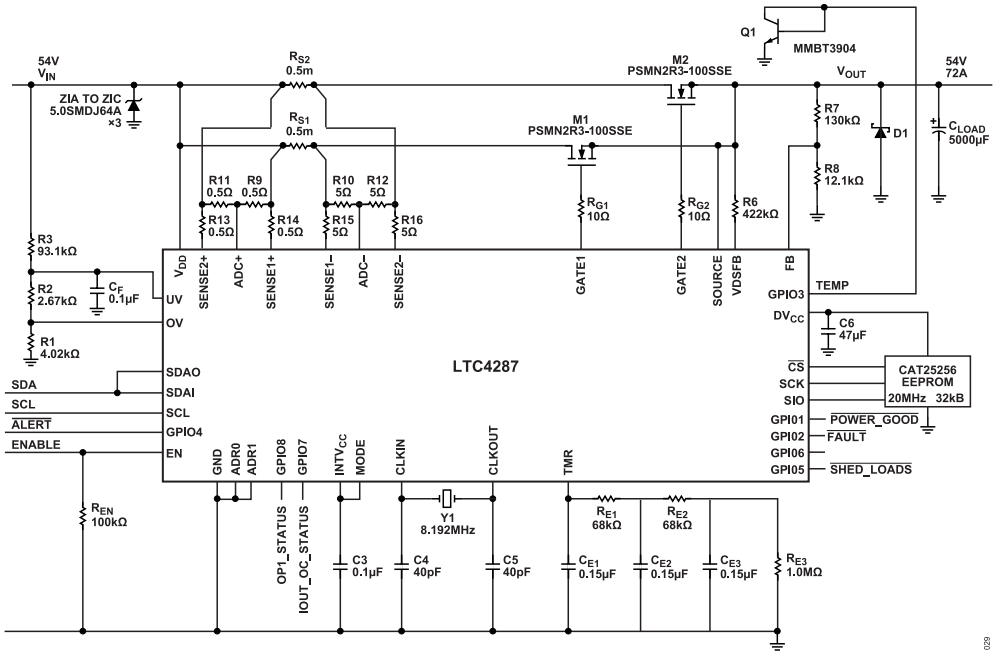

Figure 28. Typical Application in Parallel Mode

APPLICATIONS INFORMATION

Turn-On Sequence

The power supply on a board is controlled by using a pair of N-channel MOSFETs, M1 and M2, placed in the power path. Note that the RS1 and RS2 registers provide current detection. The R9, R10, R11, and R12 resistors provide a weighted average of the two sense voltages for ADC measurements. The R1, R2, and R3 registers define undervoltage and overvoltage levels. RG1 and RG2 prevent high frequency self oscillations in the MOSFETs. R7 and R8 set the power-good threshold, and R6 scales the current-limit foldback to the intended operating voltage.

Several conditions must be present before the external MOSFETs turn on. First, the external supply, V_{DD}, must exceed its 6.0 V UVLO level. Next, the internally generated supplies, $INTV_{CC}$ and DV_{CC}, must cross their 4 V and 2.2 V undervoltage thresholds, respectively, which generates a power-on reset, and the LTC4287 proceeds to load the configuration data from the external EEPROM, if one is present.

After a power-on reset, the UV and OV pins verify that input power is within the acceptable range, and the EN pin must be made active to indicate that the board is seated or that the LTC4287 was commanded to turn on. The state of the UV and EN comparators must be stable for at least 10 ms to qualify for turn-on. When these conditions are satisfied, turn-on is initiated.

In this application, the 10% current limit is used to control the inrush current. The 10% current-limit startup guarantees that both of the MOSFETs in a parallel mode application share the stress when charging the load capacitor, which is the preferred method of inrush control in parallel mode applications.

The MOSFETs are then turned on by charging up the GATEx pins with 50 µA current sources. When the GATEx pin voltage reaches the MOSFET threshold voltage, the MOSFET begins to turn on, and the SOURCE voltage then follows the GATEx voltages as it increases.

While the MOSFETs turn on, the power dissipation in the current limit for each MOSFET is limited to a fixed value by a foldback profile (see Figure 29). The current-limit foldback profile configured here is a constant current profile. As the SOURCE voltage rises, the VDSFB and FB pins follow as set by the R6, R7, and R8 resistors. Once the MOSFETs are fully on, both MOSFET gate to source voltages (V_{GS}) exceed their 8 V thresholds, and the FB pin exceeds its 2.56 V threshold, a GPIOx pin configured as a power-good output releases high after a power-good delay to indicate that power is good, and the load can be activated.

The time from the EN signal qualifying to both of the V_{GS} voltages crossing the 8 V threshold must be less than the FET_BAD delay time (FETBD_FLT_DL) set in the MFR_FET_FAULT_RESPONSE register.

At the minimum input supply voltage of 8.5 V, the minimum GATEx to SOURCE driver voltage is 10 V. The GATEx to SOURCE voltage is clamped to less than 14 V to protect the gates of 20 V N-channel MOSFETs.

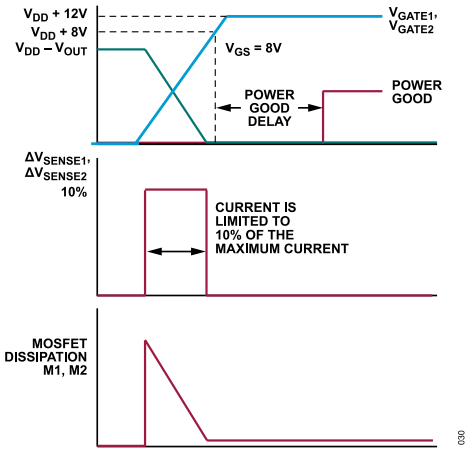

Figure 29. Power-Up Waveforms

Turn-Off Sequence

A normal turn-off sequence is initiated by card withdrawal when the backplane connector short pin connected to EN opens, causing the EN pin to change state. Additionally, several fault conditions turn off the GATEx pins.

Overcurrent Protection

The LTC4287 features two levels of protection from short-circuit and overcurrent conditions. Load current is monitored by the SENSE+ and SENSE– pins across the current sense resistors. There are two distinct thresholds for the current sense voltages, an active current-limit threshold and a fast current-limit comparator threshold. The fast current-limit comparator threshold is always three times the nominal current-limit threshold. If the sense voltage of a channel reaches the current-limit threshold, the corresponding GATEx is pulled down until the associated active current-limit loop is engaged. In the event of a catastrophic short-circuit or a sudden input step, where the sense voltage of a channel reaches the fast current-limit comparator threshold, the corresponding GATEx is immediately pulled to SOURCE to limit peak current through the MOSFET. When the sense voltage drops to the current-limit threshold, the active current-limit loop is engaged.

Current-Limit Foldback

The LTC4287 features an adjustable current limit with foldback that protects the MOSFETs from excessive power dissipation. During active current limiting, the available current is reduced as a function of the voltage across the MOSFET sensed by the V_{DD} and VDSFB pins. The higher the voltage across the MOSFET, the lower the current-limit threshold is. The lowest foldback value (α) after startup is 30% of the nominal voltage. The nominal voltage of the LTC4287 current-limit threshold is set between 6 mV and 20 mV in 2 mV steps via the SCK pin if an external EEPROM is not used, or

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between 5 mV and 20 mV in 1 mV steps via the ILIM bits in the MFR_CONFIG1 register, which can be loaded from the external EEPROM and adjusted manually. Adjusting the current limit can be used to achieve a given current limit with the limited selection of standard sense resistor values available around 1 mΩ. Parallel arrays of resistors are used to create low values. Low values of ILIM reduce the power dissipation in the current-sense resistors. Using low value current-sense resistors reduces the resolution and accuracy of the current telemetry.

Two current-limit foldback profiles are available to meet different application needs, constant power and high power. Refer to Table 8 for the foldback configurations. The constant power profile is shaped such that the power in the MOSFET is constant while current limiting, regardless of V_{DS}, to simplify the SOA design of the application and make the safe dissipation time a constant for various voltage and current conditions. Constant power foldback works well with the current-limit timer on the TMR pin. However, the constant power foldback profile starts to fold back at small V_{DS}, which can occur during an input step. For that reason, the high power profile is also available, and this profile does not start to fold back until the V_{DS} is around 50% of the nominal input voltage to prevent the current limit from folding back after an input step and collapsing the output because it is less than the load current. Because the power dissipation in the MOSFET is not constant for the high power profile, the worst-case power dissipation usually occurs when half of the nominal supply voltage is across the MOSFET. Figure 7 and Figure 8 show the current limit and power vs. the voltage across the MOSFETs. Additionally, to ease startup, the LTC4287 features a configurable option for a start-up current at 10% of the full current limit. The LTC4287 stays at 10% until the power-good conditions are met, at which point, it switches to the normal foldback profile and current limit. In many cases, the 10% current limit eliminates the need for an RC network on the GATEx pins to limit the inrush current.

Configurations using the 10% current limit for startup usually use the SOA timer and are only available with the SOA timer when starting up without an EEPROM or manual preconfiguration. This timer provides the flexibility to allow a long current-limit timeout at the low power levels during startup, and a short current-limit timeout during a fault after startup.

Constant Current Startup Using the GATEx RC Networks

An optional series RC network from GATEx to GND (R_{G4} and C_{G1} in Figure 33) provides an inrush current less than the current limit by limiting the slew rate of the GATEx pin. The current-limit timer does not run because the current limit is not engaged during startup. Thus, a small timer capacitor can be used that allows the use of MOSFETs with smaller SOA. Power-good signals when the FB pin crosses its 2.56 V threshold and the ΔV_{GATEx} voltages cross their 8 V thresholds. When these two conditions are met and the impedance back to the supply through the MOSFET is low, the output voltage is suitable for the load to be turned on. A GPIOx pin configured as power-good releases high to indicate that power is good. Choose the gate resistance (R_G) such that the gate current (I_{GATE}) × R_G is less than the threshold voltage of the MOSFET to avoid an initial inrush current spike. However, increasing R_G improves the stability of the current-limit servo loop (see the Current-Limit Stability section for additional details). If the voltage of the 50 µA I_{GATE} across R_G is higher than the threshold of the MOSFET, a diode can be added in parallel with the large R_G to limit its voltage while charging up C_{G1} (see Figure 33). For staged start architectures, an RC network can be used on a trickle MOSFET or stress MOSFET. In the parallel architecture, identical RC networks can be used on both MOSFETs. Bypass MOSFETs do not need the current limiting function of an RC network, but an RC network can be used in LSSS mode to improve the undershoot recovery time of the bypass MOSFETs.

Current-Limit Stability

For many applications, the LTC4287 current-limit loop is stable without additional components. However, there are certain conditions where additional components may be needed to improve stability. The dominant pole of the current-limit circuit is set by the capacitance at the gate of the external MOSFET, and larger gate capacitance makes the current-limit loop more stable. The 27 nF GATEx to SOURCE capacitance, C_{GS}, is enough for stability and is provided by inherent MOSFET C_{GS}. The stability of the loop is degraded by reducing the size of the resistor on a gate to ground RC network if one is used, which may necessitate additional GATEx to SOURCE capacitance. The worst case for current-limit stability occurs when the output is shorted to ground after a normal startup. Board level short-circuit testing is highly recommended because board layout can also affect transient performance.

In some systems, surges or input steps may trigger the fast pull-down, turning off the external MOSFET, and it is important to turn it on again quickly to ride through the event without downstream disturbance. In such cases a GATEx to SOURCE series RC network may be used to improve the current limit undershoot recovery time by providing a brief extra pull-up on the GATEx pin. The capacitor must be 2× to 4× the total capacitance connected to the GATEx pin through less than 1 kΩ, and the time constant of the RC network must be 150 µs, resulting in resistors between 1 kΩ and 4.7 kΩ. The GATEx to SOURCE RC network and the capacitor within also functions as the compensation capacitor for the current-limit circuit.

Parasitic MOSFET Oscillations

Not all circuit oscillations can be ascribed to the current-limit loop. Some higher frequency oscillations can arise from the MOSFETs themselves. (For further details, see AnalogDialogue's *Rarely Asked Questions, Issue #151*, High-Side Current Sensing). There are two possible parasitic oscillation mechanisms. The first type of oscillation occurs at high frequencies, typically more than 1 MHz. This high frequency oscillation is easily damped with gate

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resistors, R_{G1} and R_{G2}, as shown in Figure 28. In some applications, these resistors help in short-circuit transient recovery as well. However, too large of a resistor slows down the turn-off time. The recommended R_{G1} to R_{G2} range is between 5 Ω and 500 Ω. Note that 10 Ω provides stability without affecting the turn-off time. These resistors must be located next to the MOSFET gate pin with no other connections between them. A second type of parasitic oscillation occurs at frequencies between 200 kHz and 800 kHz when the MOSFET source is loaded with less than 10 µF, and the drain is fed with an inductive impedance such as contributed by wiring inductance. To prevent this second type of oscillation, load the SOURCE with more than 10 µF and bypass the input supply with a series 10 Ω, 100 nF snubber to ground.

Overcurrent Fault with a Basic Current-Limit Timer

During active current limit, the power dissipation in the MOSFET is large. If this power dissipation persists, the MOSFET can reach temperatures that cause damage. A basic current-limit timer has a single capacitor connected between the TMR pin and GND and sets a maximum time for the MOSFET to operate in current-limit mode. When this timer expires, an overcurrent fault is generated and the MOSFET is turned off to protect it from overheating. Current limiting begins when the current-sense voltage between the SENSE+ and SENSE– pins reaches the current-limit threshold level (which depends on foldback and the ILIM bits in the MFR_CONFIG1 register). The corresponding GATEx pin is then pulled down and regulated to limit the current-sense voltage to the current-limit value. In parallel mode, if either GATEx is in current limit during startup, the current-limit timer starts to run. The external timer capacitor at the TMR pin charges with a 20 µA pull-up current. After startup, only when both GATEx pins are regulated in current limit does the current-limit timer start to run. If at least one of the GATEx pins stops limiting current before the TMR pin reaches the 2.56 V threshold, the TMR pin discharges with 5 µA. For HSSS, LSSS, or single driver modes, if the current-sense voltage between the SENSE1+ and SENSE1– pins reaches the current-limit threshold level, the current limit-timer starts to run. For a given current-limit time delay (t_{ACL}), use the following equation for setting the value of the timing capacitor:

$$\textit{TMR Capacitance } (C_{TMR}) = t_{ACL} \times 8 \text{ nF/ms}$$

When the TMR pin reaches its 2.56 V threshold, the LTC4287 turns off both gates and generates an overcurrent fault. The MOSFETs are turned off with a 10 mA current from GATEx to SOURCE and a 1 mA current from GATEx to ground. The GPIO2 pin, configured as an open-drain $\overline{\text{FAULT}}$ output by default, also pulls low. After the fault, the TMR pin begins discharging with a 5 µA pull-down current and must reach 200 mV before the LTC4287 is allowed to turn on again. The overcurrent cool-down time is set by the COOLING_DL bits in the MFR_CONFIG1 register, which can be set from 580 ms to 74.2 sec to allow the system to cool before reapplying power.

An overcurrent fault can be cleared by pulling the UV pin to less than its 1 V UV reset threshold, which happens automatically if the GPIO2 pin is in its default configuration as a $\overline{\text{FAULT}}$ output and is tied to the UV pin. When the TMR completes the cool down delay, the MOSFETs turn on if the fault is cleared. Additionally, the LTC4287 can be configured to auto-retry automatically after an overcurrent fault by configuring the IOUT_OC_FAULT_RESPONSE register. If the LTC4287 turned off due to an OC fault, the appropriate code is set in the MFR_SD_CAUSE register.

MOSFET manufacturers specify the safe limits on operating voltage, current, and time as a set of curves referred to as the SOA. The proper timer capacitance must be set to allow the worst-case operating condition to stay within the SOA limits. The worst-case operating condition could be completely charging a large bypass capacitor at the output during startup or riding through a large input step. With a basic current-limit timer, once a timer capacitance is set, the MOSFET must be selected to withstand the worst-case SOA condition that occurs during any possible normal operating condition or fault condition.

The waveform in Figure 30 shows how the output turns off following a short circuit.

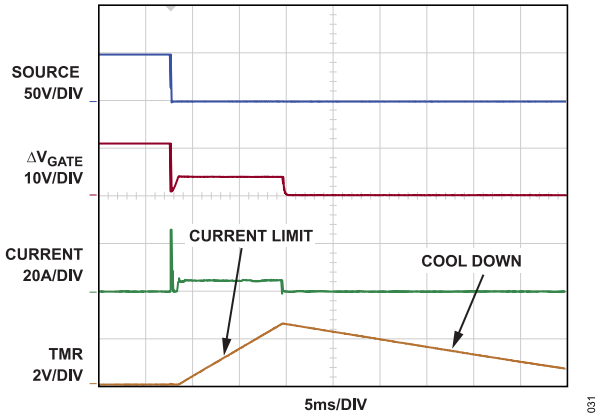

Figure 30. ΔV_{GATE}, SOURCE, and TMR Current vs. Time

Overcurrent Fault with the SOA Timer

The LTC4287 features another mode for the TMR pin, SOA timer, which better protects the MOSFETs when the power dissipated in the MOSFETs varies widely. Instead of a constant 20 µA current, the TMR outputs a current proportional to the power dissipation in the MOSFETs driven by GATE1 and the 5 µA internal TMR pull-down current is disabled. The assumption is made that in parallel mode that the MOSFETs of both channels see similar stresses. In other modes, the MOSFET at Channel 1 sees more stress. The TMR pin mode is set by the THERM_TMR bit of the MFR_CONFIG1 register, which is loaded from the EEPROM or the state of the MODE and SIO pins if an EEPROM is not used (see Configuration Without EEPROM).

The SOA timer requires an RC network representing the MOSFET thermal model to be connected to TMR (Figure 28). At least two

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resistors and two capacitors are required for minimum accuracy of the thermal behavior. More RC elements provide better accuracy. Thus, the cost and board area are larger than the single-capacitor timer. The SOA timer voltage represents the real-time rise in the junction temperature of the Channel 1 MOSFET and its trip threshold of 2.56 V represents the maximum allowable peak temperature of the MOSFET. With the SOA timer, the selection of MOSFETs is much simpler. The MOSFETs must meet the worst-case operation requirements. In fault conditions such as output short, the SOA timer automatically protects the MOSFETs by turning them off once the maximum allowable peak temperature is reached (TMR tripped). With the single capacitor timer, the minimum capacitor must first be selected to keep the MOSFETs on during worst-case operating conditions, then the MOSFETs must be selected to withstand the worst-case SOA conditions during normal operating and fault conditions. The cost of MOSFETs selected based on the single capacitor timer for parallel mode or HSSS mode may be substantially higher than that using the SOA timer. It is recommended to use the SOA timer for high power applications using parallel mode or HSSS mode, especially for those with large input steps.

During all modes of operation, an internal multiplier drives TMR with a current proportional to V_{SENSE1} multiplied by the voltage difference between the V_{DD} and SOURCE pin as measured by the VDSFB pin as follows:

$$I_{TMR} = \frac{400\ \mu A \times V_{SENSE1} \times (V_{DD} - VDSFB)}{20\ mV \times 12\ V} \quad (1)$$

For example, the TMR pin produces 100 µA when V_{SENSE1} = 10 mV and V_{DD} – VDSFB = 6 V. When the TMR voltage crosses its 2.56 V threshold, the MOSFETs are shut off and an overcurrent fault is detected. When the multiplier output current is low, the TMR voltage drops as the RC network discharges. When it drops to less than 0.2 V, the overcurrent fault is cleared, and the MOSFETs can turn on if the GPIO2 pin is in its default configuration as a $\overline{FAULT}$ output and is connected to UV. For the SOA timer to work properly, 12 V is expected between V_{DD} and VDSFB when V_{DD} is at its nominal and SOURCE is at ground. Note that there is 120 kΩ of resistance internally from V_{DD} to VDSFB. For 12 V systems, VDSFB must be simply connected to SOURCE. For input voltages larger than 12 V, add a resistor of 10 kΩ/V between the VDSFB and SOURCE pins. For example, for 54 V systems, a 422 kΩ resistor must be added between the two pins. Note that the SOA timer is independent of the current limit set via the SCK pin. The current limit can be adjusted with the SCK pin without the need to modify the thermal RC network. However, if the sense resistor value is changed, a modified thermal RC network is required. Using a large current-limit threshold, such as 20 mV, achieves the greatest accuracy and dynamic range from the SOA timer. See Figure 16 and Figure 17 for the SOA TMR pull-up currents at different ΔV_{SENSE1} and different V_{DD} – VDSFB voltages. The configuration of the thermal RC network for a particular MOSFET starts with the selection of a desired number of resistive and capacitive elements. The values of these elements are decided based on the thermal impedance plot provided by the MOSFET manufacturer. Three resistors and three capacitors are usually enough to fit the plot fairly well from 10 µs to 100 ms (see Figure 28), which covers the timing range of typical operating and fault conditions. If better fitting accuracy or a wider fitting range is desired, more elements can be used. After the thermal RC network is configured, the thermal quantities are then converted to electric quantities according to the following equations:

$$R_E = k \times R_\theta$$
$$C_E = \frac{C_\theta}{k} \quad (2)$$

where:
R_E and C_E are electric resistance and capacitance, respectively.
R_θ and C_θ are thermal resistance and capacitance, respectively.
The conversion constant k is given by the following:

$$k \frac{V_{DS,MAX} \times I_{D,MAX}}{I_{TIMER(UP)MAX}} \times \frac{V_{TIMER(TH)}}{\Delta T_{MAX}} \quad (3)$$

where:
$V_{DS,MAX}$ is the maximum drain-to-source voltage that results in VDSFB at 12 V less than V_{DD}.
$I_{D,MAX}$ = 20 mV/R_{SENSE1}.
$I_{TIMER(UP),MAX}$ is the TMR pull-up current corresponding to the maximum power dissipation (P_{MAX} = $V_{DS,MAX}$ × $I_{D,MAX}$).
$V_{TMR(TH)}$ is the TMR rising threshold (2.56 V).
ΔT_{MAX} is the maximum allowable temperature rise of the MOSFET.

For example, if $V_{DS,MAX}$ = 58 V, $I_{D,MAX}$ = 40 A, $I_{TIMER(UP)MAX}$ = 400 µA, and ΔT_{MAX} = 110°C (175°C T_{JMAX} – 65°C T_A), k = 1.35 × 10^5 (V^2/°C). A thermal RC network consisting of three resistors and capacitors that represent the thermal behavior of the PSMN2R3-100SSE is shown in Figure 28.

After an overcurrent fault with the thermal timer, the LTC4287 is not allowed to turn on again until the TMR pin decays to 200 mV, and the device automatically retries and waits for a cooling delay in the same manner as with a traditional timer.

Dual-Gate Operation Modes

The LTC4287 features dual gate drivers that are configured by the MODE pin into four distinct operation modes: single driver, parallel, HSSS, and LSSS. As shown in Table 1, each mode features specific SOA or $R_{DS(ON)}$ benefits, gate on/off behavior, power-good signaling, and fault detection logic. All modes except LSSS support starting up with a resistive load such as a heating element or incandescent lamp. When using an external EEPROM, the mode is chosen with the MODE pin while foldback and the TMR pin behavior are configured independently in the EEPROM. When not using an external EEPROM, the modes of the dual gate drivers are selected together with the foldback profile and TMR behavior by the status of the MODE and SIO pins as shown in Table 5.

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Parallel

High current applications often demand several power MOSFETs in parallel to reach a target $R_{DS(ON)}$ under 1 mΩ that is unavailable in a single MOSFET. In addition, dividing the load current among multiple devices alleviates the PCB current crowding problem with the use of a single MOSFET.

Parallel MOSFETs with their gate pins tied together share current well when their gate to source voltages are fully enhanced. However, when the MOSFETs are limiting current, the mismatch between gate thresholds causes the MOSFET with the lowest threshold to carry more current than the others. Because threshold voltage has a negative temperature coefficient, as this MOSFET heats, it can carry even more current. Eventually, all of the load current can be carried by a single MOSFET. For this reason, when a group of MOSFETs are operated in parallel, only the SOA of a single MOSFET is guaranteed.

The LTC4287 resolves this problem by offering two gate drivers, each with an independent current-limit circuit and associated current-sense pins. When the MODE pin is tied to $INTV_{CC}$, these two gate drivers operate in parallel mode, in which GATE1 and GATE2 are turned on or off simultaneously. In this mode, the LTC4287 allows a group of parallel MOSFETs to be divided into two channels. During current limiting in an overcurrent event, such as an output short or an input step, the independent gate control of the two channels divides the current evenly between them, resulting in twice the SOA performance of a hot-swap controller with a single current-limit circuit, which allows the use of smaller, less expensive MOSFETs, can start up a load twice as big, or increase SOA margins. In addition, multiple LTC4287 devices can be connected in parallel using the GPIO5 pin configured as a COMM input and output to coordinate turn on, turn off, and fault behavior to further improve SOA.

Figure 28 shows an application example providing 3.6 kW operating in parallel mode. Two MOSFETs in each channel are used so that the power dissipation in each MOSFET is less than 3.8 W when fully enhanced. After startup, when the voltage across the drain and source of the MOSFETs is less than 2 V, the GATEx to SOURCE voltages for both MOSFETs are higher than 8 V, the FB voltage is higher than 2.56 V, and the power is considered good. After the power-good delay, a GPIOx pin configured as a power-good output is then released to go high. After that, if the FB falls to less than 2.48 V, the GPIOx pin resets to low. If the current-limit timer is selected with parallel mode, it runs if either channel is in current limit during startup. Once startup is finished, the power good is asserted, and the current-limit timer runs only if both channels are in current limit. If the SOA timer is selected, the RC network represents the thermal behavior of a single MOSFET because the TMR pull-up current is only related to the power dissipation in the Channel 1 MOSFET. When TMR reaches 2.56 V (representing the maximum allowable temperature rise in the MOSFET), both GATE1 and GATE2 turns off, and the overcurrent fault status pulls down the GPIO2 pin in its default configuration as a $\overline{FAULT}$ output.

APPLICATION 2: HSSS MODE

The two GATE drivers of the LTC4287 can also be configured to operate in HSSS mode by grounding the MODE pin. In this mode, GATE1 drives a high SOA MOSFET (M1) for startup and to withstand overstresses, and GATE2 drives less expensive bypass MOSFETs (M2A and M2B) with low $R_{DS(ON)}$ and relaxed SOA requirements to carry the load, as shown in Figure 33. The HSSS mode works well for systems where large input steps or supply surges can occur. M1 must be selected with large enough SOA to withstand these conditions, in which, M1 not only carries the full load current but also must deliver the current to charge up the load capacitance.

At power-up, GATE1 is turned on first to charge the load, and GATE2 is held off. As shown in Figure 31, GATE2 is turned on when GATE1 is fully enhanced (GATE1 is more than 8 V higher than the SOURCE pin), the MOSFET drain to source voltage is lower than 2 V, and Channel 1 is not in current limit. After GATE2 is more than 8 V higher than the SOURCE pin, a GPIOx pin configured as a power-good output is latched high given that the FB pin is higher than 2.56 V. Most of the load current is delivered by M2A and M2B, which usually have much lower $R_{DS(ON)}$ than M1.

In this mode, the current-sense resistor is connected between SENSE1+ and SENSE1–, while SENSE2+ and SENSE2– are connected to SENSE1+ to disable the current-limit circuit of GATE2. During overcurrent events, such as an output short or an input step, the LTC4287 immediately switches off GATE2 to protect M2A and M2B from overstress, leaving the current limit of GATE1 to regulate the load current through Q1. In this condition, the TMR pull-up current is turned on. When the TMR voltage reaches 2.56 V, GATE1 is turned off, and an overcurrent fault is logged.

HSSS mode decouples the SOA requirement from the $R_{DS(ON)}$ requirement. The MOSFET driven by GATE1 (M1) is selected so that its SOA is large enough to withstand stresses in all operating conditions. The $R_{DS(ON)}$ of M1 is not a major concern but must keep the MOSFET drain to source voltage lower than 2 V when GATE2 is off; otherwise, GATE2 does not turn on. The MOSFETs driven by GATE2 (M2A and M2B) are selected so that their $R_{DS(ON)}$ minimizes the I^2R power dissipation, typically less than or close to 2.3 W. The SOA of M2A and M2B does not need to be large because GATE2 is switched off when either GATE1 is in current limit, GATE1 is low (GATE1 is less than 8 V more than the SOURCE pin), or the MOSFET drain to source is higher than 2 V. In this way, the selection of MOSFETs for each channel is easier, and the overall cost of MOSFETs can be lower than parallel mode.

In HSSS mode, the FET_BAD timer starts to run when either GATE1 is low but Channel 1 is not in active current limit, GATE2 is enabled but low, or the MOSFET drain to source voltage is higher than the VDTH threshold, which is 200 mV by default. When the FET_BAD timer expires, a FET_BAD fault triggers.

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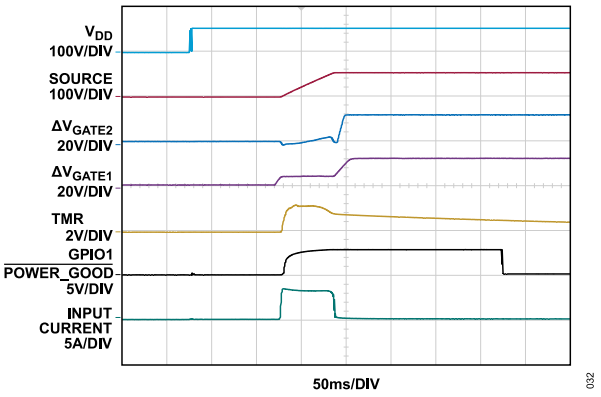

Figure 31. HSSS Mode Application: Normal Start-Up Waveform

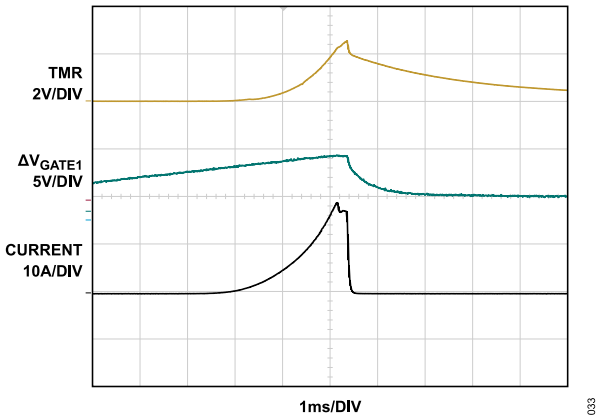

Figure 32. HSSS Mode Application: Start-Up into Short-Circuit

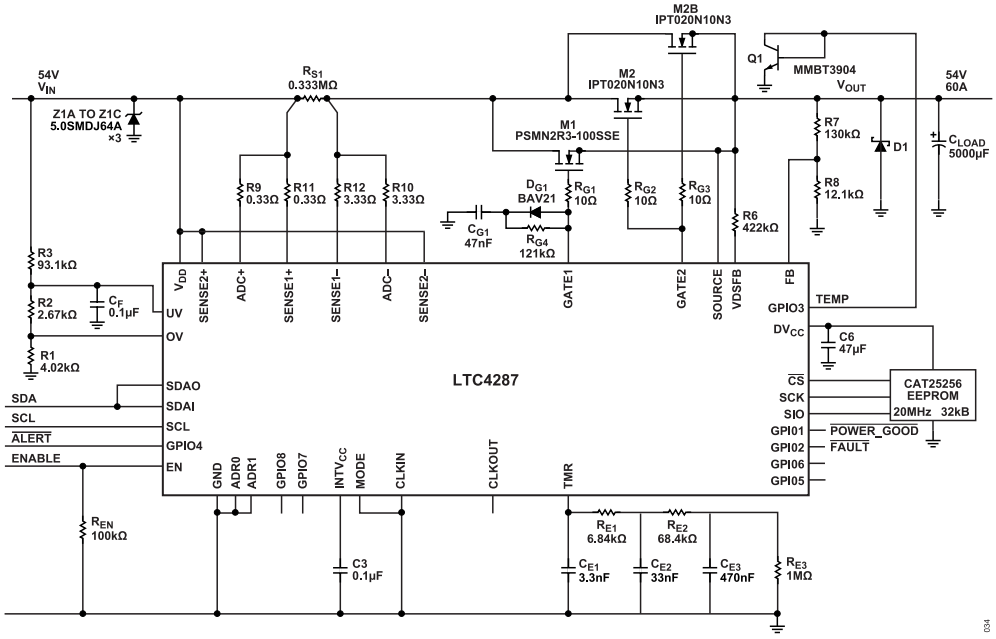

Figure 33. 54 V, 60 A Application Circuit with T_A = 65°C

APPLICATIONS INFORMATION

APPLICATION 3: LSSS MODE

LSSS mode is well suited for applications with a tightly regulated supply voltage. In such a system without significant input voltage steps, the worst-case operating condition for the MOSFET SOA occurs when charging the load capacitance during startup. By limiting the start-up inrush current to a low level, the SOA demand for the start-up MOSFET is greatly alleviated. Additionally, the bypass path that turns on after startup only needs an inexpensive, switching regulator class MOSFET. Therefore, this architecture minimizes the cost of MOSFETs to achieve a given load current and $R_{DS(ON)}$. However, LSSS mode has limited capability to ride through an input step or a sustained load surge in current limit. Due to the low start-up current, it also cannot start up a large resistive load such as a heating element or incandescent lamp.

Figure 36 shows an application circuit for a 1.9 kW system operating in LSSS mode. This mode is enabled by floating the MODE pin. In this mode, GATE2 drives a compact, inexpensive MOSFET (M2) with a small SOA as a trickle charging device for startup. GATE1 drives parallel, low $R_{DS(ON)}$, low SOA MOSFETs (M1A thru M1F) with a high current limit to deliver the full load current. The turn-on sequence is the opposite of that in the HSSS mode as shown in Figure 34: M2 turns on first and delivers a low inrush current due to the large sense resistor, R_{S2}. Once the load is fully charged (FB pin is higher than 2.56 V) and the start-up MOSFET is fully enhanced (VGATE2 > 8 V) and not in active current limit, GATE1 turns on. When the MOSFETs of both channels are fully enhanced, the drain to source voltage is lower than 2 V and the FB pin voltage is higher than 2.56 V, power-good is asserted.

The current-sense pins for both current-limit circuits on GATE1 and GATE2 must be connected to their corresponding sense resistors. If an overcurrent event occurs, both GATE1 and GATE2 stay in current limit to share the stress. GATE1 turns off if the FB pin drops to less than 2.48 V or GATE2 turns off due to a fault, which is different from the HSSS mode where GATE2 turns off if GATE1 is in current limit.

The condition to start the FET_BAD fault timer in this mode is the same as in the parallel mode (see Table 1). Because the FET_BAD fault timer is running during the trickle startup while the load is slowly charged, the timer duration must be programmed long enough to avoid turning off M2 too early.

If the current-limit timer is chosen, the TMR capacitor is charged only when Channel 1 is in current limit. A single, small TMR capacitor as shown in Figure 36 can be used to configure a brief delay that must be within the worst SOA of M1A, M1F, and M2. If the SOA timer is chosen, an RC network that represents the electric model for the thermal behavior of M1A thru M1Fmust be connected to TMR. Note that during startup when M1A thru M1F is turned off, the TMR pull-up current still relates to the power dissipation in M1A thru M1F, which is zero. M2 must be selected so that its SOA allows it to be in current limit longer than M1A thru M1F. In this way, M2 is automatically protected when M1A thru M1F turn off in an overcurrent condition.

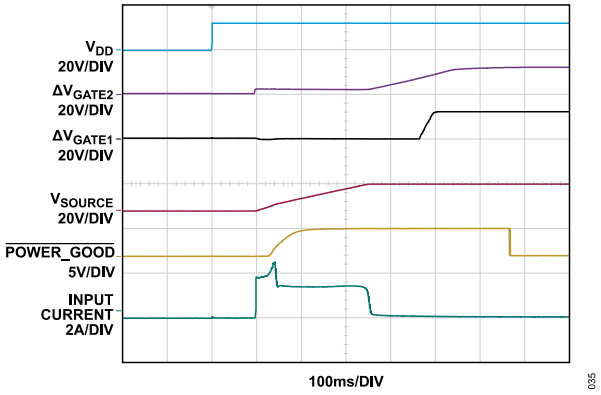

Figure 34. LSSS Mode Application: Normal Start-Up Waveform

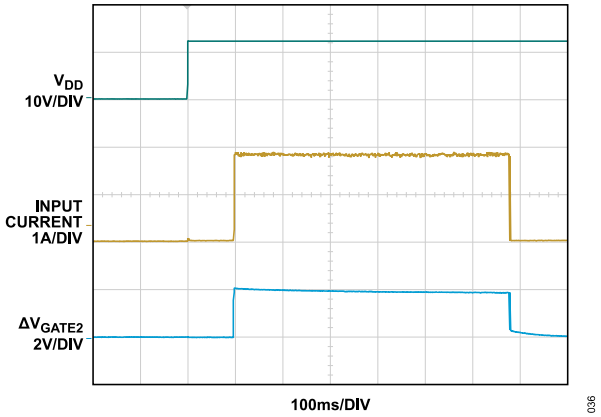

Figure 35. LSSS Mode Application: Start-Up into Short-Circuit

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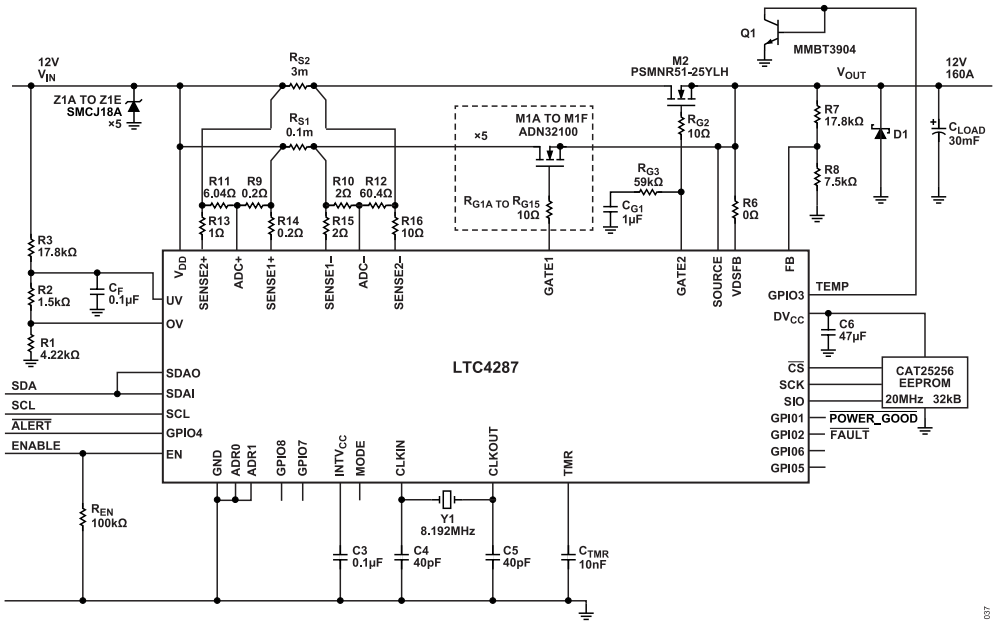

Figure 36. 12 V, 160 A Application Circuit with T_A = 65°C

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SINGLE DRIVER MODE

Figure 39 shows a single MOSFET application. Configured in HSSS mode, this implementation behaves as other single, hot-swap controllers, such as the LTC4260, LTC4286, or ADM1272, when the bypass MOSFETs are not stuffed, and the GATE2 pin is open.

In this application, the LTC4287 is configured without using an EEPROM. The voltage divider on the SCK pin is used to set the current limit.

The traditional timer is used.

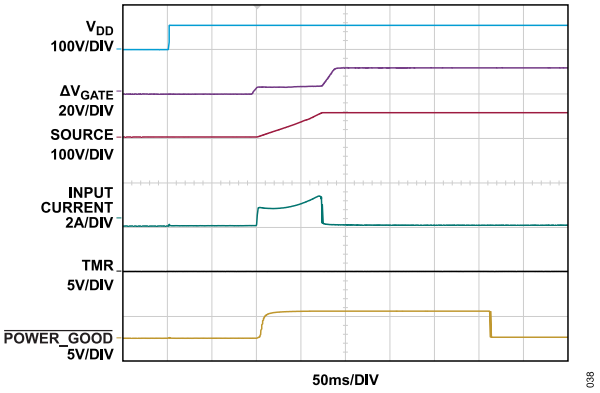

Figure 37. Start 1 mF

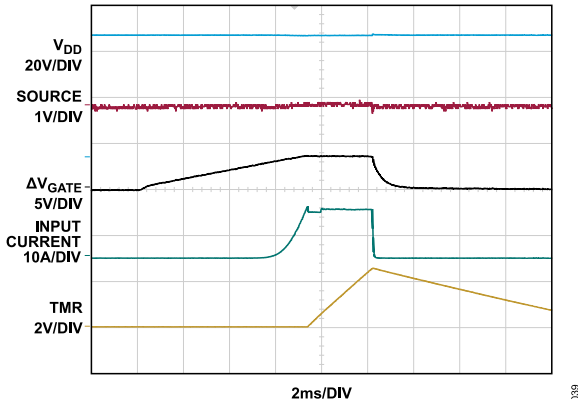

Figure 38. Start Short-Circuit

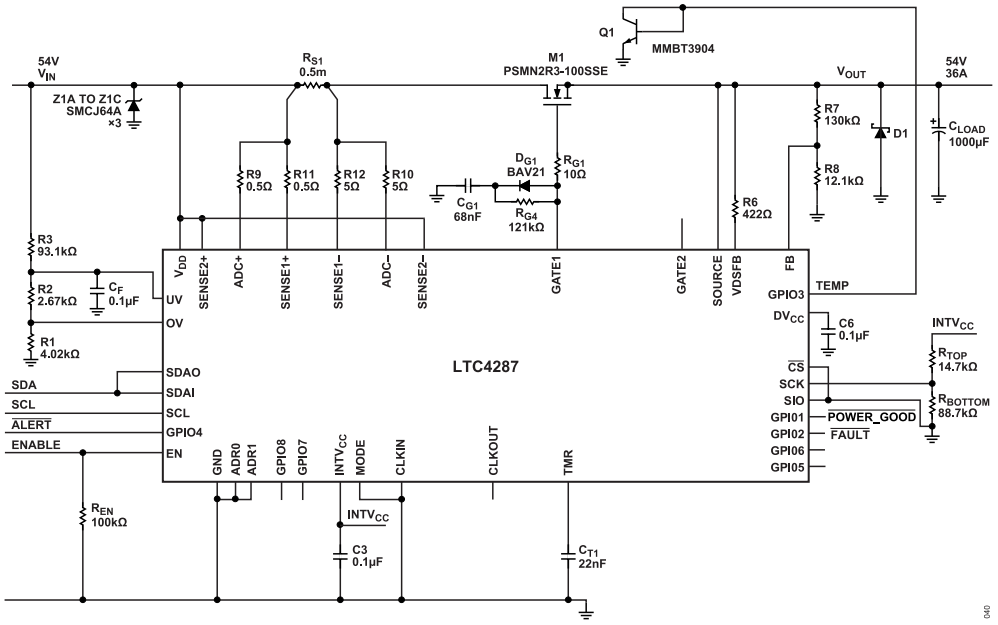

Figure 39. 54 V, 36 A, Single MOSFET Implementation with HSSS Mode

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Table 5. LTC4287 Dual Gate Operation Modes and Behaviors

Mode	Single Driver	Parallel	HSSS	LSSS
Feature	Simple.	SOA is double, and $R_{DS(ON)}$ is halved.	GATE1 drives high SOA MOSFET, and GATE2 drives low $R_{DS(ON)}$ MOSFET.	GATE1 drives low $R_{DS(ON)}$, small SOA MOSFET, and GATE2 drives small SOA MOSFET.
Turn-On Sequence		GATE1 and GATE2 turn on at the same time.	GATE1 turns on first, and GATE2 turns on after GATE1 turns high and $V_{DD} - V_{SOURCE} < 2$ V and Channel 1 is not in ACL.	GATE2 turns on first, and GATE1 turns on if $V_{FB} > 2.56$ V once GATE2 turns high.
Power-Good Latch				
Set	V_{DD} − SOURCE < 2 V, and V_{FB} > 2.56 V, and ΔV_{GATE1} > 10 V, and (ΔV_{GATE2} > 10 V or disabled).	V_{DD} − SOURCE < 2 V, and V_{FB} > 2.56 V, and ΔV_{GATE1} > 10 V, and (ΔV_{GATE2} > 10 V or disabled).	V_{DD} − SOURCE < 2 V, and V_{FB} > 2.56 V, and ΔV_{GATE1} > 10 V, and (ΔV_{GATE2} > 10 V or disabled).	V_{DD} − SOURCE < 2 V, and V_{FB} > 2.56 V, and ΔV_{GATE1} > 10 V, and (ΔV_{GATE2} > 10 V or disabled).
Reset	Feedback drops to less than 256 V	Feedback drops to less than 256 V.	Feedback drops to less than 256 V.	Feedback drops to less than 256 V or V_{COMM} drops to less than 0.2 V.
GATE1 Turn-Off	V_{COMM} < 1.4 V	V_{COMM} < 1.4 V.	V_{COMM} < 1.4 V.	V_{COMM} < 0.2 V or V_{FB} < 2.56 V.
GATE2 Turn-Off	ΔV_{GATE1} < 8 V or V_{DD} − SOURCE > 2 V or Channel 1 is in ACL.	V_{COMM} < 1.4 V.	ΔV_{GATE1} < 8 V or V_{DD} − SOURCE > 2 V or Channel 1 is in ACL.	V_{COMM} < 0.2 V.
Current-Limit Timer	Runs if V_{COMM} > 3.5 V or Channel 1 is in ACL.	Runs if VCOMM > 3.5 V or during startup if either channel is in ACL. After startup, both channels are in ACL.	Runs if V_{COMM} > 3.5 V or Channel 1 is in ACL.	Runs if V_{COMM} > 3.5 V or Channel is in ACL.
FET_BAD Timer	Runs if V_{COMM} > 1.4 V and ((V_{DD} − SOURCE > 100 mV) or (ΔV_{GATE1} < 8 V and not in ACL) or (ΔV_{GATE2} < 8 V and enabled)).	Runs if V_{COMM} > 1.4 V and ((V_{DD} − SOURCE > 100 mV) or (ΔV_{GATE1} < 8 V and not in ACL) or (ΔV_{GATE2} < 8 V and enabled)).	Runs if V_{COMM} > 1.4 V and ((V_{DD} − SOURCE > 100 mV) or (ΔV_{GATE1} < 8 V and not in ACL) or (ΔV_{GATE2} < 8 V and enabled)).	Runs if V_{COMM} > 1.4 V and ((V_{DD} − SOURCE > 100 mV) or (ΔV_{GATE1} < 8 V and not in ACL) or (ΔV_{GATE2} < 8 V and enabled)).

FET_BAD FAULT AND AUTO-RETRY

A damaged MOSFET can have leakage from gate to drain or have degraded $R_{DS(ON)}$. Debris on the board can also produce leakage or a short from the GATEx pin to the SOURCE pin, the MOSFET drain, or to ground. In these conditions, the LTC4287 may not be able to pull the GATEx pin high enough to fully enhance the MOSFET, or the MOSFET may not reach the intended $R_{DS(ON)}$ when the GATEx pin is fully enhanced, which can put the MOSFET in a condition where the power in the MOSFET is higher than its continuous power handling capability, even though the current is less than the current limit. The LTC4287 monitors the integrity of the MOSFETs in two ways and acts on both of them in the same manner. First, the LTC4287 monitors the voltage between the V_{DD} and SOURCE pins. A comparator detects a high drain to source voltage (V_{DS}) whenever the V_{DD} to SOURCE voltage is greater than a configurable 50 mV to 200 mV threshold, as selected in the MFR_CONFIG1 register. Second, the LTC4287 monitors the GATEx voltage. The GATEx voltage may not fully enhance with a damaged MOSFET. A gate low condition is detected if gate-to-source voltage is lower than 8 V, and that channel is not in an active current limit. When either a high drain to source voltage or a gate low condition is present for either or both MOSFETs while they are commanded on, the FET_BAD timer starts to run. The logic determining the FET_BAD condition is in Figure 40. The FET_BAD condition causes an internal timer to run, the duration and auto-retry configuration of the FET_BAD timer is available in the MFR_FET_FAULT_RESPONSE register. The available configurations are to ignore or respond to the fault, to auto-retry 0 times to 6 times, or to auto-retry forever, and the FET_BAD time can be selected from 267 ms to 2.13 sec.

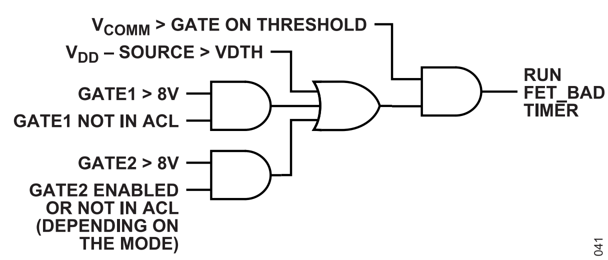

Figure 40. Logic Diagram for FET_BAD Timer

Note that during startup, the V_{DS} high condition is present because the voltage from drain to source is greater than the FET_BAD (TH). To avoid undesired turn-off, the FET_BAD timer duration must be long enough for the largest allowable load to start up.

The LTC4287 treats a FET_BAD fault similar to an overcurrent fault. A GPIOx pin configured as an $\overline{FAULT}$ output pulls low and can be tied to the UV pin to auto-retry. The cool-down after a FET_BAD fault is the same as for an overcurrent fault, which is set by the

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COOLING_DL bits in the MFR_CONFIG1 register. If the LTC4287 turns off due to a FET_BAD fault, the appropriate code is set in the MFR_SD_CAUSE register.

OVERVOLTAGE FAULT

An overvoltage fault occurs when the OV pin voltage goes more than its rising threshold of 2.56 V for longer than 12 µs, which shuts off the GATEx pins with a 10 mA current to SOURCE and a 1 mA current to ground and latches the VIN_OV_FAULT bit in the STATUS_INPUT register to 1. The live unlatched state of the OV pin is provided by the VIN_OV_STATUS bit in the MFR_PADS_LIVE_STATUS register. If the voltage falls back to less than the threshold, the GATEx pins turn on again if configured to do so in the VIN_OV_FAULT_RESPONSE register. If the LTC4287 turns off due to the OV pin rising, the appropriate code sets in the MFR_SD_CAUSE register.

UNDERVOLTAGE FAULT

An undervoltage fault occurs when the UV pin falls less than its 2.2 V threshold, which shuts off the GATEx pins with a 10 mA current to SOURCE and a 1 mA current to ground and latches the VIN_UV_FAULT bit in the STATUS_INPUT register to 1. The live unlatched state of the UV pin is provided by the VIN_UV_STATUS bit in the MFR_PADS_LIVE_STATUS register. If the voltage falls back to less than the threshold, the GATEx pins turn on again if configured to do so in the VIN_OV_FAULT_RESPONSE register, after a delay of 11 ms or 91 ms as selected by the DB_DLY bit in the MFR_CONFIG2 register. If the LTC4287 turns off due to the UV pin falling, the appropriate code sets in the MFR_SD_CAUSE register. The UV and OV signals can be filtered by placing a capacitor on the UV pin.

ON AND OFF CONTROL WITH THE EN PIN

When the EN pin is configured as active low ($\overline{EN}$), the input can detect card insertion with a short pin.Figure 41 through Figure 43 show examples where the EN pin is used to detect insertion. The debounce delay from the EN pin becoming active until the GATEx pins begin to rise is set by two bits in the MFR_CONFIG2 register. The DB_EN_ON_EN bit enables the debounce delay, and the DB_DLY bit selects between a 11.3 ms and 90.6 ms debounce delay. After the EN pin debounce delay, the system is allowed to start up.

If the LTC4287 turns off due to the EN pin going inactive, the appropriate code is set in the MFR_SD_CAUSE register. In addition, when the EN pin goes inactive to indicate that the board is unseated, the shed loads the GPIOx pin to go high immediately (if a GPIOx pin is configured as a shed load output) to tell the host to shed the load. This is followed by a turn-off delay before the GATEx pin driver turns off the MOSFET (turn-off delay varies from 0 ms to 36.1 ms with a linear 0.142 ms step size and is specified in the POWER_OFF_DELAY bits of the MFR_ON_OFF_CONFIG register. No delay is also an option.

The status of the EN pin is available at the EN_INPUT bit in the MFR_PADS_LIVE_STATUS register. The EN_INPUT status bit is set when EN is at the active status (allowing the MOSFET to turn on). If the RESET_FAULT_ENABLE bit in the MFR_CONFIG2 register is set, once the plug-in card is reinserted, the following faults are reset: IOUT_OC_FAULT, OT_FAULT, VIN_OV_FAULT, VIN_UV_FAULT, and all the bits in the STATUS_MFR_SPECIFIC register except the EN_CHANGED bit. If the RESET_FAULT_ENABLE bit is not set, faults are not cleared, and the LTC4287 does not turn on if an active fault has no remaining auto-retries.

If the system shuts down due to a fault, it is desirable to restart the system simply by removing and reinserting a load card. In cases where the LTC4287 and the switch reside on a backplane or midplane and the load resides on a plug-in card, the EN pin detects when the plug-in card is removed. If a connection sense on the plug-in card is driving the EN pin, insertion or removal of the card can cause the EN pin voltage to bounce, resulting in the clearing of the fault bits when the card is removed. The EN pin can be debounced using a filter capacitor, C_{EN}, on the EN pin as shown in Figure 41 through Figure 43.

Unlike the UV and OV pins, the EN pin always auto-retries indefinitely.

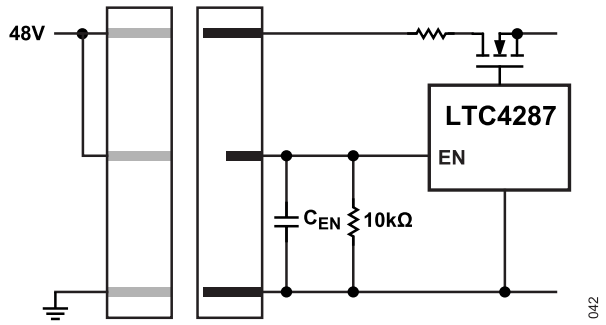

Figure 41. Connection Sense Configuration with the EN Pin (EN Configured as Active High, Default)

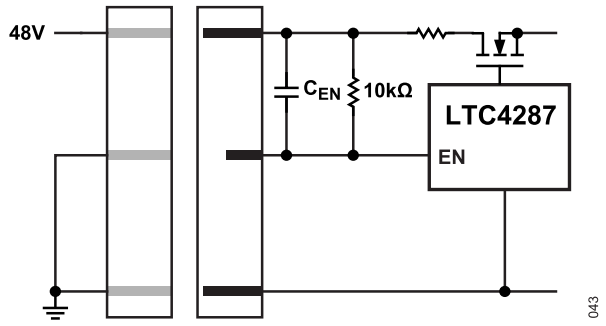

Figure 42. Connection Sense Configuration with the EN Pin (EN Configured as Active Low)

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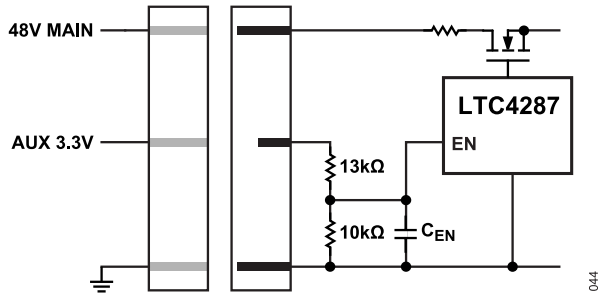

Figure 43. Connection Sense Configuration with the EN Pin (EN Pin Sensing of AUX Supply and EN Pin Configured Active High, Default)

POWER GOOD AND POWER FAILED

The default power good behavior of the LTC4287 is to indicate POWER_GOOD on the GPIO2 pin (active low). The PG_STATUS# bit, in the STATUS_WORD register, is set when the FB pin voltage is less than its 2.483 V falling threshold. To indicate POWER_GOOD on a GPIOx pin, one or both GATEx pins must first exceed their 8 V V_{GS} thresholds (GATE_HIGH) after startup for the delay time set by the DB_DLY bits in the MFR_CONFIG2 register. This requirement prevents POWER_GOOD from asserting during startup when the FB pin first crosses its threshold. The latch that indicates that the GATEx pins have gone high can be reset either by the FB pin falling to less than its 2.483 V threshold (FB pin status = 0), or the LTC4287 turning off (ON = 0 in the OPERATION register), and is selected by the PWRGD_RESET_CONTROL bit in the MFR_CONFIG2 register. After startup, the GPIOx pin outputs the value of the FB comparator so that POWER_GOOD stays high even in cases such as an input voltage step that causes the GATEx pins to briefly dip to less than 8 V V_{GS} (see Figure 44). A power-failed warning is generated when the FB pin is low and one or both GATEx pins are high, preventing power-failed faults when both GATEx to SOURCE voltages are low during power-up or power-down. Power failed is indicated by the latched POWER_FAILED_WARNING bit in the MFR_SYSTEM_STATUS2 register and the live POWER_FAILED_STATUS bit in the MFR_PADS_LIVE_STATUS register.

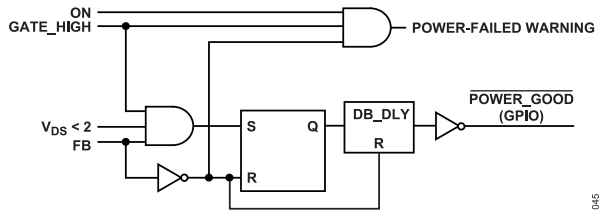

Figure 44. Power-Good Logic

PGI FAULT

Following the assertion of POWER_GOOD, a power-good watchdog timer (580 ms) starts. If a GPIOx pin is configured as a power-good input (PGI) by the PGI_EN and PGI_SEL bits of the MFR_GPI_SEL register, the GPIOx pin configured as a PGI must be driven either high or low, as selected by the PGI_INV bit in the MFR_GPIO_INV register, by a supply monitor that has validated the downstream supplies. If the PGI has transitioned to the correct state before the 580 ms timer expires, the LTC4287 remains on. If the PGI configured GPIOx pin does not reach the correct state by the time the timer expires, the LTC4287 produces a PGI fault and responds as configured in the MFR_PGI_FAULT_RESPONSE register. The options are to ignore the fault or turn off in response to the fault, and after turning off due to a fault, to latch off or auto-retry one time to six times, or auto-retry indefinitely. The LTC4287 waits at least 580 ms before turning on again after a PGI fault.

The statuses of the GPIOx pin are indicated by the PGI_STATUS bit in the MFR_PADS_LIVE_STATUS register. When the PGI_STATUS bit is set to 1, it indicates that the downstream loads have not yet satisfied their supply monitor, and when this bit is set to 0, it indicates that the downstream loads are good. If the LTC4287 turns off due to the PGI fault, the appropriate code is set in the MFR_SD_CAUSE register.

FET SHORT FAULT

A FET short fault is reported if the data converter measures a current-sense voltage greater than or equal to 2 mV while the GATEx pins are turned off. This condition sets the FET_SHORT_STATUS bit in the MFR_PADS_LIVE_STATUS register, and the FET_SHORT_WARNING bit in the MFR_SYSTEM_STATUS2 register. FET short faults can only occur when the hot-swap is off; therefore, this fault does not turn the MOSFET off. In practice, a shorted MOSFET is also likely to have an oxide failure that results in a FET_BAD fault that turns off the LTC4287. To latch the LTC4287 off following a FET short fault, a GPIOx pin is configured as an ALERT output, the FET short alerts are enabled by setting the FET_SHORT_WARNING alert mask bit in MFR_SYS_ALERT_MASK1 register, and then the ALERT configured GPIOx pin is tied to the UV pin or EN pin.

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PARALLEL CONTROLLERS USING THE COMM FUNCTION OF THE GPIO5

The LTC4287 has a COMM function available on the GPIO5 pin that communicates the status of the LTC4287 so that multiple LTC4287 devices can operate in parallel. Tie the COMM function of the GPIO5 pins of a group of devices together to allow these pins to operate in tandem. A small capacitor can be connected to COMM node to improve noise immunity if necessary. The COMM function has the following four states:

- A 0 V means that none of the devices can turn on. Any device with a fault present pulls the GPIO5 pin to 0 V to turn off the entire bank.
- A 0.8 V indicates that only the start-up channel of the devices configured with LSSS mode are allowed to turn on. Those devices regulate GPIO5 at an 0.8 V voltage with a 10 µA pull-up current until the start-up MOSFET is fully enhanced.
- A 2.5 V at the GPIO5 indicates that all of the devices can turn on. The devices that have no faults present regulate at 2.5 V with a 10 µA pull-up current. The devices that are on and in current limiting disable the 2.5 V regulator, allowing the GPIO5 voltage to rise.
- A 5 V means that all the devices are in current limit.

When configured as a current-limit timer, only one LTC4287 must have a capacitor connected to the TMR pin. When the GPIO5 voltage is within 1.5 V of $INTV_{CC}$, the current-limit TMR integrates. The remaining LTC4287 devices can have their TMR pins grounded to disable overcurrent faults. When using thermal networks, each individual device has its own thermal network and can generate a thermal fault regardless of the state of the GPIO5 pin. When multiple LTC4287 devices work together by having the GPIO5 pins connected, care must be taken to ensure that all the LTC4287 devices see the same solid ground potential. Ground bounce can corrupt COMM function or possibly damage the LTC4287 if the Absolute Maximum Ratings are violated. Putting a current-limiting resistor in series with the GPIO5 pins, or putting a Zener clamp between GPIO5 and ground, can mitigate ground noise.

The LTC4238 has a COMM pin and features that are compatible with the LTC4287. An LTC4287 can be used as a supply monitor and for digital on and off control, while one or more LTC4238 devices provide additional MOSFET drivers for current sharing in high power applications.

REBOOT BIT

The LTC4287 allows a reboot of the configuration and registers when the REBOOT bit in the MFR_REBOOT_CONTROL register is set high. The auto-reboot turn-on delay can be set from 0.580 sec to 74.2 sec in binary steps by the RBT_DL bits. The RBT_INIT bits select the initialization options. The default setting is for the reboot to cause a complete chip reset and to load configuration registers from the EEPROM.

A GPIOx pin can be configured as a reboot (or $\overline{\text{REBOOT}}$) input pin with the MFR_GPI_SEL register. If the $\overline{\text{REBOOT}}$ configured GPIOx pin has a high to low transition, a reboot sequence initiates.

DATA CONVERTERS

The LTC4287 incorporates a pair of Σ-Δ ADCs that are configurable to 12 bits or 15 bits, and a third ADC that monitors temperature with a 1°C LSB. One ADC continuously samples the current-sense voltage, while the other ADCs monitor the input voltage, output voltage, and the voltage on GPIOx inputs. The Σ-Δ architecture inherently averages signal noise during the measurement period. The ADCs can run in a 12-bit or 15-bit mode, which is selected by 15_BIT_MODE bit in the MFR_ADC_CONFIG register. The second ADC can be configured to measure V_{IN} at the V_{DD} pin, V_{OUT} at the SOURCE pin, the sense current on both channels, two of the GPIOx pins, and/or the voltage across the MOSFET by selecting the related bits in the MFR_ADC_CONFIG register. The ADC full scale is 32 mV for the current-sense voltage, a choice of 102.4 V or 25.6 V for V_{DD} and V_{SOURCE}, 2.56 V for GPIOx, and 320 mV for the V_{DD} − SOURCE measurement.

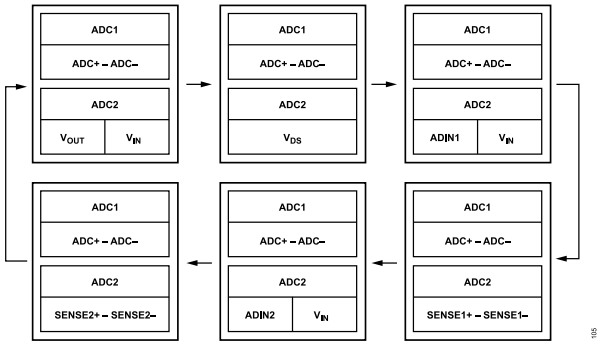

Figure 45. LTC4287 ADC Measurement Pattern in 12- Bit and 15-Bit Continuous Mode, Assuming All AUX Channels Selected

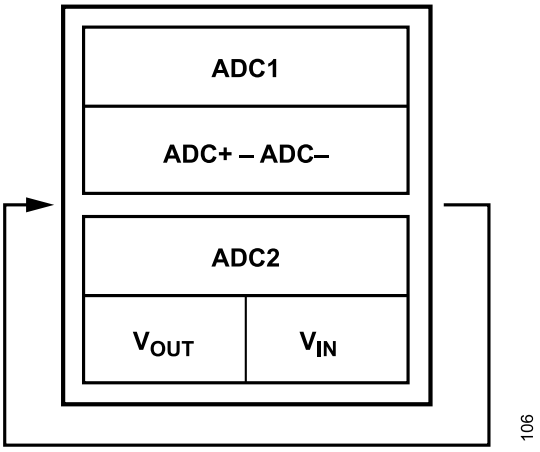

Figure 46. LTC4287 ADC Measurement Pattern in 12- Bit and 15-Bit Continuous Mode, Assuming No AUX Channels Selected

The ADC+ and ADC– input pins allow the ADC to measure the average voltage across the two sense resistors using resistive

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dividers. Some applications can use parallel sense resistors to achieve a specific resistance, in which case, the averaging resistors can be selected with the same ratio as the sense resistors they connect to, which allows the ADC to still measure current accurately (see Figure 47). In this case, the effective ADC sense resistor is R_S in parallel with k × R_S for the current limit. Scaling the averaging resistors, R_A, by the same scaling factor, k, allows the ADC to measure the correct sense voltage for this effective sense resistor. The smallest averaging resistor on the ADC+ or SENSE+ side must not exceed 1 Ω.

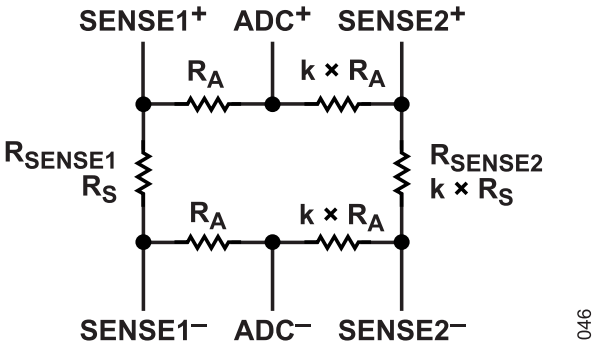

Figure 47. Weighted Averaging Current Sense Voltages

The two ADCs are synchronized, and after each current measurement conversion, the measured current is multiplied by the measured V_{DD} or V_{SOURCE}, as selected by the VPWR_SELECT bit in the MFR_CONFIG1 register, to yield input or output power. After each conversion, the measurement results and power are compared to the recorded minimum and maximum values. If the measurement is a new minimum or maximum, those registers are updated. The measurements are also compared to the minimum and maximum warning thresholds and set the corresponding ADC warning bits in the MFR_SYSTEM_STATUS2 register and generate an alert if configured to do so in the MFR_STAT2_ALERT_MASK register. After each measurement, calculated power is added to an accumulator that meters energy. Because the current is continuously monitored by a dedicated ADC, the current is sampled every 1 µs, ensuring that the energy meter accurately meters noisy loads up to 500 kHz noise frequency. The 6-byte energy meter is capable of accumulating 20 days of power at full scale, which is several months at a nominal power level. An optional alert can be generated when the meter overflows.

A time counter keeps track of how many times power is added into the energy meter. Dividing the energy by the number in the counter yields the average power over the accumulation interval. The 4 byte time counter keeps count for 10 years in the 12-bit mode before overflowing and can generate an alert at full scale to indicate that the counter is about to roll over. Multiplying the value in the counter by t_{CONV} yields the time that the energy meter has been accumulating. Both the energy accumulator and time counter are writable, allowing them to be preloaded with a given energy and/or time before overflow so that the LTC4287 generates an overflow alert after either a specified amount of energy is delivered or time has passed. The following formulas are used to convert the values in the ADC result registers into physical units. The data in the 12-bit mode is left justified, and the same equations apply to both 12-bit mode and 15-bit mode.

To calculate the GPIOx voltage, use the following equation:

$$V = \frac{CODE_{(WORD)} \times 2.56}{2^{15} - 1} \quad (4)$$

To calculate the input and output voltage, use the following equation:

$$V = \frac{CODE_{(WORD)} \times V_{FS(OUT)}}{2^{15} - 1} \quad (5)$$

where $V_{FS(OUT)}$ is 25.6 V or 102.4 V, depending on the device being in 25 V mode or 100 V mode, respectively.

To calculate the current in amperes, use the following equation:

$$I = \frac{CODE_{(WORD)} \times 0.032V}{\left(2^{15} - 1\right) \times R_{SENSE}} \quad (6)$$

To calculate V_{DD} – SOURCE in volts, use the following equation:

$$V = \frac{CODE_{(WORD)} \times 0.32V}{2^{15} - 1} \quad (7)$$

To calculate power in watts, use the following equation:

$$P = \frac{CODE_{(WORD)} \times 0.032V \times V_{FS(OUT)} \times 2^{15}}{\left(2^{15} - 1\right)^2 \times R_{SENSE}} \quad (8)$$

To calculate energy in joules, use the following equation:

$$E = \frac{CODE\left(48\ \text{Bits}\right) \times 0.032\ \text{V} \times V_{FS(OUT)} \times t_{CONV} \times 2^8}{\left(2^{15} - 1\right)^2 \times R_{SENSE}} \quad (9)$$

Where t_{CONV} = ($1/f_{CONV}$) is 0.000283 sec for the 12-bit mode and 0.00226 sec in the 15-bit mode.

To calculate the average power over the energy accumulation period, use the following equation:

$$P_{AVG} = \frac{E}{t_{CONV} \times CODE_{(COUNTER)}} \quad (10)$$

OVERPOWER FAULTS AND TURBO MODE

In addition to overpower warnings, the LTC4287 can also produce two overpower faults from the ADC power measurements.

The current-to-voltage load characteristics with operating regions are shown in Figure 48. Figure 48 demonstrates a 6 kW scenario, where at 40 V (supply minimum), the current limit of 150 A provides the upper bound for the operating current. Less than 40 V, the current limit (represented by the solid line) is governed by the V_{DS} foldback profile. This region between the 6 kW and the 4 kW level is the turbo mode region.

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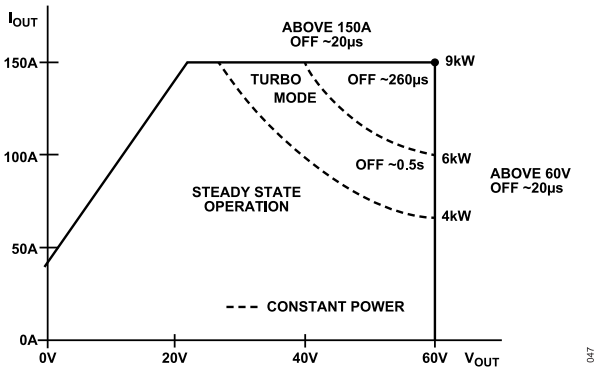

Figure 48. Example Load Current to Voltage Characteristics with 4 kW Turbo Mode

The power detection method uses the product of the voltage and current measured by the ADCs to identify when the LTC4287 is in the turbo mode region or exceeds 6 kW. The 4 kW and 6 kW thresholds are adjustable and set by the value in the two following command registers, respectively: MFR_PIN_OP1_FAULT_LIMIT and MFR_PIN_OP2_FAULT_LIMIT.

In the turbo mode region, the device uses an internal timer to turn off after an adjustable timeout from 0 ms to 2.32 sec with a linear 1.13 ms step size set in the MFR_OP_FAULT_RESPONSE register.

The timer uses an up and down method that counts up twice as fast when the output power is greater than 4 kW compared to when it is less than 4 kW. After the timeout a GPIOx pin pulls low immediately (if a GPIOx pin is configured as a shed load output, see Table 3) as an early warning for load shedding followed by a turn-off delay before the LTC4287 turns off the MOSFET gate (turn off delay varies from 0 ms to 36.1 ms with a linear 0.142 ms step size and is specified in the POWER_OFF_DELAY bits in the MFR_ON_OFF_CONFIG register. No delay is also an option.

After the timeout status bit, PIN_OP1_FAULT, is set in the STATUS_MFR_SPECIFIC register (see Table 31). This fault can hold the gate off until the device retries. The retry response is specified in the MFR_OP_FAULT_RESPONSE register, Bits[4:3] and Bits[2:0] (see Table 5). The response options include ignoring the fault and not turning off the gate, latching the gate off until the fault is cleared, or retrying turning on the gate from 1 time to 6 times or infinite times. The fault may also activate a GPIOx pin configured as a FAULT output if the OP_TO_FAULT bit is set in the MFR_FLT_CONFIG register (see Table 2). The GPIO output indicates the fault condition (either FAULT or $\overline{\text{FAULT}}$) once configured. See Table 16, Table 17, and Table 18 for the configurations available in the MFR_GPIO_INV, MFR_GPO_SEL41, and MFR_GPO_SEL85 registers, respectively.

If the power exceeds the 4 kW limit, it can be observed real-time in the OP1_STATUS bit of the MFR_PADS_LIVE_STATUS register (see Table 7). OP1_STATUS is also viewable on any GPIOx pin if configured as an output.

If the power exceeds 6 kW, the shed loads GPIOx pin pulls low immediately (with an ADC 283 µs latency). As in the 4 kW case, the shed loads GPIOx pin pulls low as an early warning for load shedding before the MOSFET gate turns off after the POWER_OFF_DELAY. The power is limited to 9 kW by the 150 A current limit at the 60 V maximum supply.

After the power exceeds 6 kW, the PIN_OP2_FAULT bit is set in the STATUS_MFR_SPECIFIC register (see Table 31). This fault can also hold the gate off until the device retries. The retry response is the same as the PIN_OP1_FAULT and is specified in the MFR_OP_FAULT_RESPONSE register (see Table 5). The response options include ignoring the fault and not turning off the gate, latching the gate off until the fault is cleared, or retrying turning on the gate from 1 time to 6 times or infinite times. The fault may also indicate on the fault GPIOx pin if the OP_TO_FAULT bit is set in the MFR_FLT_CONFIG register (see Table 2) if the GPIOx pin is configured as a fault output.

If the load current exceeds 150 A or the supply voltage exceeds 60 V, the current limiting amplifier and the overvoltage comparator turn off the gate and pull down the shed loads GPIOx pin within 20 µs.

The LTC4287 also provides warnings when the power is more than the ADC measured threshold specified in the PIN_OP_WARN_LIMIT register or less than the under power threshold in MFR_PIN_UP_LIMIT. These warnings appear in the PIN_OP_WARNING bit of the STATUS_INPUT register (see Table 27) and the PIN_UP_WARNING bit in the MFR_SYSTEM_STATUS2 register (see Table 3).

All faults and warnings can be enabled to appear as alerts in the ALERT and L_ALERT bits in the MFR_SYSTEM_STATUS1 register (see Table 2). These alert register bits can be configured to drive the SMBus alert GPIOx pin and the latched alert GPIOx pin, respectively. The L_ALERT bit and GPIOx pin are not cleared by the SMBus alert protocol.

CONFIGURATION WITHOUT EEPROM

The LTC4287 can be used without the optional external EEPROM with a limited set of default options that are chosen by tying the $\overline{\text{CS}}$, SCK, SIO, and MODE pins to certain voltages. Before the LTC4287 begins to boot from the EEPROM, it first sets the SCK and SIO pins as high impedance inputs and then checks that $\overline{\text{CS}}$ is high impedance by attempting to pull this pin more than 2.56 V with 10 µA. If the $\overline{\text{CS}}$ pin does not pull more than 2.56 V, booting from the EEPROM is skipped, and the input voltages of the $\overline{\text{CS}}$, SCK, SIO, and MODE pins are used to configure the LTC4287.

The $\overline{\text{CS}}$ pin is used to select if the LTC4287 starts up automatically after power-up or waits for a PMBus host controller to command it to turn on. If the $\overline{\text{CS}}$ pin is grounded, it turns on, and if it is set to 1.6 V by a resistive divider, this pin remains off and waits for further instructions (see Table 6).

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Table 6. Using the $\overline{CS}$ Pin to Configure the Default On and Off State

$\overline{CS}$ at Power-Up	On Bit
>2.56	Loaded from EEPROM
<1 V	On
>1 V, <2.56 V	Off

Next, the current limit is set with a resistive divider on the SCK pin. Note that the internal registers are capable of 1 mV resolution, while the SCK pin provides a 2 mV resolution. These options are shown in Table 7. The voltage on the SCK pin is read only during the boot-up sequence. Note that changing the voltage on the SCK pin after the boot-up sequence has no effect on the ILIM setting. After boot-up, the ILIM setting can be changed by writing to the MFR_CONFIG1 register (see Table 14).

Finally, the three-state MODE and SIO pins are tied high, low, or left floating to configure the operating mode and foldback behavior according to Table 8.

Note that the full suite of digital configurations available from the EEPROM may be set manually by the host PMBus controller after power-up in applications without an EEPROM.

Table 7. Configuring the Current Limit with the SCK Pin ($INTV_{CC}$ = 5 V Used)

		SCK Thresholds Compared with				
$\Delta V_{SNS(TH)}$ (mV)	V_{SCK} (V)	Lower (V)	Upper (V)	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	$R_{BOTTOM}/(R_{TOP} + R_{BOTTOM})$
6	0	Not applicable	0.357	Open	Short	0.000
8	0.714	0.357	1.071	88.7	14.7	0.143
10	1.429	1.071	1.786	73.2	29.4	0.286
12	2.143	1.786	2.5	59.0	44.2	0.429
14	2.857	2.5	3.214	44.2	59.0	0.571
16	3.571	3.214	3.929	29.4	73.2	0.714
18	4.286	3.929	4.643	14.7	88.7	0.857
20	5	4.643	Not applicable	Short	Open	1.000

Table 8. Mode and Foldback Configurations Without EEPROM

$\overline{CS}$ at Power-Up	MODE Pin	SIO Pin	Mode	Foldback Configuration Running	Foldback at Startup	Timer
>2.56	0	X	HSSS	EEPROM	EEPROM	EEPROM
>2.56	1	X	Parallel	EEPROM	EEPROM	EEPROM
>2.56	Z	X	LSSS	EEPROM	EEPROM	EEPROM
<2.56	0	0	HSSS	High power	Same as running	Traditional
<2.56	0	Z	HSSS	Constant power	Fixed 10% limit	Thermal
<2.56	0	1	HSSS	High power	Same as running	Thermal
<2.56	1	1	Parallel	High power	Same as running	Traditional
<2.56	1	Z	Parallel	Constant power	Same as running	Thermal
<2.56	1	0	Parallel	Constant power	Fixed 10% limit	Thermal
<2.56	Z	0	Parallel	High power	Same as running	Thermal
<2.56	Z	1	LSSS	Constant power	Same as running	Traditional
<2.56	Z	Z	LSSS	Constant power	Same as running	Thermal

DESIGN EXAMPLES

The design flow starts with specifying the maximum load power and the operating voltage limits. If redundant supplies are used, the system usually has a wide supply range and can experience large input steps when switching. An operation mode is then selected based on the approximate guidelines Table 9.

Table 9. Guidelines for Mode Selection

Mode	Power Level	Supply Range
Single Driver	<1500 W	Narrow or wide
Parallel	<4000 W	Narrow or wide
HSSS	>1500 W	Wide
LSSS	>1500 W	Narrow
Two or More LTC4287 Devices Using the COMM Function of the GPIO5 Pin	>4000 W	Narrow or wide

EXAMPLE 1: PARALLEL MODE WITH CURRENT LIMIT START-UP AND SOA TIMER

As a design example, use the following specifications: V_{IN} = 54 V ±10%, the maximum load power of 1.4 kW, start in active current limit, and C_{LOAD} = 5000 µF. The parallel mode is chosen based on the guideline above in Table 9. In parallel mode, GATE1 and GATE2 drive two parallel channels of MOSFETs to charge the load capacitor simultaneously at startup, share the load current after startup, and turn off simultaneously upon a fault condition such as output overload or short-circuit. Because the input voltage varies between 38 V and 58 V, the high power profile is selected for foldback to cope with input variations without folding back the current-limit threshold. In addition, the SOA timer is picked for the TMR pin to protect the MOSFETs more effectively. This completed design is shown in Figure 28. The maximum load current is calculated by the following:

$$I_{L(MAX)} = \frac{P_{L(MAX)}}{V_{UV(ON)}} = \frac{2700\ \text{W}}{38\ \text{V}} \approx 72\ \text{A} \quad (11)$$

Because there are two channels, the maximum current each channel carries is 36 A.

1. Configure current limit and select current-sense resistors. A 18 mV sense voltage with a 0.5 mΩ sense resistance is picked to provide 36 A for each channel. When a specific design is actually built, there can be small inaccuracies in the current sensing owing to contact and copper trace resistances. An immediate remedy without changing sense resistors is to readjust the sense voltage in 2 mV steps. For instance, moving sense voltage from 18 mV to 20 mV gives a 11% increase in current. Some designers can use parallel-sense resistors to achieve a specific resistance. In which case, the averaging resistors, R_A, must be selected with the same ratio, k, as the sense resistors they connect to (see Figure 47), which allows the current-limit circuit to measure the correct sense voltage for this effective sense resistor. The smallest averaging resistor must not exceed 1 Ω.
2. Select the MOSFETs. The MOSFET must be sized to handle the power dissipation during the inrush charging of C_{LOAD}. In addition, the $R_{DS(ON)}$ must be low enough to carry maximum the load current. To determine the power, use the following equation:

$$E_c = \frac{1}{2}CV^2 = \frac{1}{2}(5000\ \mu\text{F}) \times (58\ \text{V})^2 \approx 8.4\ \text{J} \quad (12)$$

During start-up, the 10% foldback current limits the average power dissipation in the MOSFET of each channel to the following:

$$P_{DISS(AVE),START-UP} = \frac{18\ \text{mV} \times 10\ \% \times 58\ \text{V}}{0.5\ \text{m}\Omega \times 2} \approx 104\ \text{W} \quad (13)$$

Calculate the time it take to charge up C_{LOAD} by using the following equation:

$$t_{CHARGEUP} = \frac{E_C}{P_{DISS(AVE),STARTUP} \times 2\ \text{MOSFETs}} = \frac{8.4\ \text{J}}{104\ \text{W} \times 2} \approx 40.4\ \text{ms} \quad (14)$$

The SOA curves of candidate MOSFETs must be evaluated to ensure that heat capacity of the package can tolerate this power for 40.4 ms. The SOA curve of the Nexperia PSMN2R3-100SSE shows it can sustain 9 A with 60 V across it for 10 ms, satisfying this requirement. The worst-case MOSFET drain to SOURCE voltage with full load is the following:

$$V_{DS,MAX} = I_{CH(MAX)} \times R_{DS(ON),MAX} = 36 \times 3.9\ \text{m}\Omega = 140\ \text{mV} \quad (15)$$

There is enough margin with the full current load for V_{DD} – SOURCE before reaching the FET_BAD threshold of 200 mV.

Because PSMN2R3-100SSE has about 15 nF of gate capacitance, it is likely to be stable, but the short-circuit stability of the current-limit loop must be checked and improved by adding capacitors from GATEx to SOURCE if needed.

3. Select the RC network for the SOA timer following the procedure detailed in the Overcurrent Fault with the SOA Timer section. Three thermal capacitors and three thermal resistors provide fairly good curve fitting for the thermal impedance plot of the chosen MOSFET, PSMN2R3-100SSE, in the range between 100 µs and 100 ms (wide enough for typical operating conditions of this application).

$C_{\theta1}$ = 0.0013 J/°C, $R_{\theta1}$ = 0.025°C/W, $C_{\theta2}$ = 0.015 J/°C, $R_{\theta2}$ = 0.25°C/W, $C_{\theta3}$ = 0.15 J/°C, and $R_{\theta3}$ = 30°C/W.

The conversion constant is given by the following:

$$k = \frac{V_{DS,MAX} \times I_{LIM,MAX}}{I_{TMR(UP),MAX} \times R_{SENSE}} \times \frac{V_{TMR(TH)}}{\Delta T_{MAX}} = \frac{58\ \text{V} \times 20\ \text{mV}}{400\ \mu\text{A} \times 0.5\ \text{m}\Omega} \times \frac{2.56\ \text{V}}{175°C - 65°C} = 1.35 \times 10^5 \left(\frac{V^2}{°C}\right) \quad (16)$$

DESIGN EXAMPLES

where ΔT_{MAX} is the maximum allowable temperature rise and chosen to be 110°C, which corresponds to a maximum MOSFET temperature of 175°C at an operating temperature of 65°C. The thermal R and C values are then converted to electric R and C values as detailed in the Overcurrent Fault with the SOA Timer section. After the electrical R and C values are computed, choose the closest next-larger available resistor value and the closest next-smaller available capacitor value. Then, the resistance corresponding to the thermal resistance of the board is added to the termination resistance (the largest one). Assuming a 25°C/W board thermal resistance in this application, it is converted to 25 × 1.35 × 10^5 = 3.3 MΩ. If the computed resistance for the board thermal resistance is over 1 M, choose 1 M, which avoids accuracy degradation due to board leakage currents. The resulting electrical capacitors and resistors are C_{E1} = 0.15 µF, R_{E1} = 68 kΩ, C_{E2} = 0.15 µF, R_{E2} = 68 kΩ, C_{E3} = 0.15 µF, and R_{E3} =1.0 MΩ, as shown in Figure 28. After the SOA timer is configured, run simulations in LTSpice to ensure TMR does not reach its 2.56 V trip point in any operating conditions including start-up and input step. When it trips in fault conditions, such as output overload or short-circuit, verify the peak temperature of the MOSFET matches the proposed maximum temperature. Iterations of the previous procedure may be needed before the RC network is finalized.

4. Design the FET_BAD timer. During start-up, the FET_BAD timer is running. The load capacitor must be fully charged before this timer expires, or the gate outputs turn off once a FET_BAD fault is triggered. For a start-up time of 40.5 ms, the default FET_BAD timer of 145 ms is sufficient and is set by writing zeroes to the FETBD_FLT_DL bits in the MFR_FET_FAULT_RESPONSE register (see Table 4).
5. Select resistive dividers for UV, OV, and power-good inputs. $V_{UV(ON)}$ = 38 V, $V_{OV(OFF)}$ = 63 V, and $V_{POWER\_GOOD(UP)}$ = 30 V. To solve for the UV and OV resistor string values, use the following method. To keep the error due to 1 µA of leakage to less than 1%, choose a divider current of at least 200 µA. R1 < 2.56 V/200 µA = 12.8 kΩ. Then, calculate by using the following equations:

$$R2 = \frac{V_{OV(OFF)}}{V_{UV(ON)}} \times R1 \times \frac{UV_{TH(RISING)}}{OV_{TH(FALLING)}} - R1$$
$$R3 = \frac{V_{UV(ON)} \times (R1 + R2)}{UV_{TH(RISING)}} - R1 - R2 \quad (17)$$

In this case, R1 is 4.02 kΩ to give a resistor string current greater than 200 µA. Then, solving the equations results in R2 = 2.67 kΩ and R3 = 93.1 kΩ. A 0.1 µF capacitor, C_F, is placed on the UV pin to prevent supply glitches from turning off the GATEx via UV or OV.

The FB divider is solved by picking R8 and solving for R7, choosing 12.1 kΩ for R8.

$$R7 = \frac{V_{POWER\_GOOD(UP)}}{FB_{TH(RISING)}} \times R8 - R8$$
$$R7 = 130\ \text{kΩ} \quad (18)$$

Because the fast current-limit comparator is engaged at 216 A, the input TVS must be capable of clamping a 216 A surge at a voltage more than the OV threshold but less than the 100 V absolute maximum rating of the LTC4287 for about 1 µs. The TVS diodes, SMCJ64A, clamp 51.7 A at 96.8 V for 1 ms and can dissipate 23 kW for 10 µs. Three of these diodes are required to sink 216 A current.

In addition, a 0.1 µF ceramic bypass capacitor is placed on the $INTV_{CC}$ pin. No bypass capacitor is required on the V_{DD} pin.

EXAMPLE 2: LSSS MODE WITH A BASIC TIMER

The second example has a line regulated 12 V supply with the voltage variation of ±10%. The output is a 1.6 kW constant power load. $V_{UV(ON)}$ = 10.5 V and $V_{OV(OFF)}$ = 14.25 V (see Figure 36) and C_L = 30 mF. The LSSS mode is chosen for this example because there is no concern of large input steps. In LSSS mode, the FET_BAD timer runs if GATE1 is low and not in ACL (see Table 5), which can happen when the power-good voltage has not been reached. Therefore, the power-good voltage is recommended to be lower than the input UV voltage. In this example, $V_{POWER\_GOOD(UP)}$ is set to 8.64 V. The current in Channel 2 is usually only a small fraction of the maximum load current, such as 10% or lower. For this reason, its current contribution during normal operation can be ignored for the first phase of the design. When designing Channel 1, Channel 2 can be accounted for or sized to make up for any shortfalls in the high current (Channel 1) path so that full power (1600 W) can be supplied at minimum input voltage (10 V).

Calculate the maximum load current as follows:

$$I_{MAX} = \frac{P_{L(MAX)}}{V_{S(MIN)}} = \frac{1600\ \text{W}}{10\ \text{V}} \approx 160\ \text{A} \quad (19)$$

With the two channels decoupled (Channel 2 dedicated to start up and Channel 1 dedicated to passing the load current), the overall design flow and design considerations in some individual steps of the LSSS mode are different from parallel mode. Take the following steps to complete the design:

1. Select sufficient bypass MOSFETs to carry the maximum load current. For the maximum channel current of 160 A, six AONS32100 ($R_{DS(ON)}$ < 1.1 mΩ) devices result in 0.78 W per package, an acceptable dissipation with airflow.

   With full load, the worst-case voltage across the MOSFET is about 160 A × (1.1/6) mΩ = 24 mV. The default threshold for starting the FET_BAD timer is 200 mV. Note that there is sufficient margin to account for inaccuracies before enabling the TMR FET pull-up current. See detailed design considerations in Step 2 in the Example 1: Parallel Mode With Current Limit Start-Up and SOA Timer section.
2. Configure the current limit and select the current-sense resistors. The current limit in this example must cover the maximum load current with enough margin to account for device tolerances. Pick the minimum resistance available for a single-sense

DESIGN EXAMPLES

resistor, 500 µΩ, which is a metal element resistor. Select the current-limit threshold voltage by first assuming Channel 1 carries the maximum load current, then add a small current carried by the start-up channel for the margin. Use five resistors in parallel to make a 100 µΩ current-sense resistor.

$$\Delta V_{SENSE(MIN)} = R_{S1} \times I_{L(MAX)} = 100\ \mu\Omega \times 160\ \text{A} \approx 16\ \text{mV} \quad (20)$$

The resistor power dissipation of Channel 1 is given by the following equation:

$$P_{S1} = \Delta V_{SENSEI(MIN)} \times I_{L(MAX)} = 16\ \text{mV} \times 160\ \text{A} = 2.56\ \text{W} \quad (21)$$

The power dissipation per resistor is 2.56 W/5 = 512 mW, which is well within the power limit for a metal element sense resistor.

A 3 mΩ sense resistor must then be chosen for the Channel 2 current as follows:

$$I_{LIM1} = \frac{\Delta V_{SENSE}}{R_{S2}} = \frac{12\ \text{mV}}{4\ \text{m}\Omega} = 5.3\ \text{A} \quad (22)$$

Then, calculate the total current limit as follows:

$$I_{LIM} = I_{LIM1} + I_{LIM2} = \frac{16\ \text{mV}}{100\ \mu\Omega} + 5.3\ \text{A} = 165.3\ \text{A} \quad (23)$$

Taking all tolerances into account, this limit provides sufficient margin for the maximum load current of 160 A.

3. Design the TMR behavior. Because there is no concern about a large input step, a short timer delay is chosen for overcurrent turn-off. In LSSS mode, the TMR function is a filtered circuit breaker and a single timer capacitor on TMR that works for this purpose. Channel 1 dictates the timer capacitor selection because it carries most of the load current. All of the Channel 1 current can be concentrated into a single MOSFET. The current limit of Channel 1 is 160 A, in this example, and the MOSFET AONS32100 can handle 12 V and 160 A for 1 ms. Note that 20 µs of circuit breaker filtering is sufficient to reject noise encountered in most systems; therefore, the chosen MOSFET is up to the task. The TMR pull-up current is 20 µA with a voltage threshold of 2.56 V.

   Use the following equation to calculate the timer capacitance, C_T, for a 20 µs filter delay:

$$C_{TMR} = \frac{I_{TMR(UP),MAX} \times t_{FILTER}}{V_{TMR(TH)}} = \frac{20\ \mu\text{A} \times 20\ \mu\text{s}}{2.56\ \text{V}} = 156\ \text{pF} \quad (24)$$

   Select the next larger available capacitance: C_{TMR} = 180 pF.

4. Design the start-up channel (Channel 2) and the FET_BAD timer. At startup in LSSS mode, Channel 2 charges the load capacitance with a small trickle current. The trickle current is controlled by limiting the dv/dt on the gate.

   Calculate the trickle current as follows:

$$I_{INRUSH} = I_{GATE(UP)} \times \frac{C_{LOAD}}{C_{G1}} = 50\ \mu\text{A} \times \frac{30\ \text{mF}}{1\ \mu\text{F}} = 1.5\ \text{A} \quad (25)$$

   The FET_BAD timer must be set longer than the time required to charge GATE2 to V_{SOURCE} + 8 V as follows:

$$T_{STARTUP} = \frac{V_{IN(MAX)} + C_{G1}}{I_{GATEUP}} = \frac{(14\ \text{V} + 8\ \text{V}) \times 1\ \mu\text{F}}{50\ \mu\text{A}} = 440\ \text{ms} \quad (26)$$

   Meanwhile, the FET_BAD timer cannot be too long so that the FET picked for Channel 2 can handle the start-up current with the full drain-to-source voltage for this duration. For a start-up time of 440 ms, the minimum FET_BAD timer of 580 ms is sufficient and is set by writing 011 to the FETBD_FLT_DL bits in the MFR_FET_FAULT_RESPONSE register (see Table 4).

   Because the start-up current is relatively low, a small, low cost device can be used. The PSMNR51-25YLH, which can stand the 30% foldback of 5.3 A at 14 V for the duration of the FET_BAD timer, was selected for this trickle channel. Note that the $R_{DS(ON)}$ of the PSMNR51-25YLH is no higher than 1.01 mΩ. After startup, the worst-case power dissipation in this channel is $(5.3\ \text{A})^2 \times 1.01\ \text{m}\Omega = 28\ \text{mW}$, which is well within the MOSFET capability.

5. Run simulations to verify temperature rises in both the Channel 1 and Channel 2 MOSFETs under all operating and fault conditions, which is a necessary step when using a single capacitor, current-limit timer as selected in Step 3.

   First, check the temperature rise in the Channel 2 MOSFET (M2) during startup. The conditions include normal startup into current limit to fully charge the 3 mF load capacitor at the maximum input voltage. If temperature rise is too high in a normal start-up condition, a larger MOSFET can be selected for Channel 2. For the fault condition, the worst-case power dissipated in the MOSFET is the same as the maximum voltage (14 V) across the MOSFET with 30% of the full current limit because the constant power profile is selected for foldback. If the temperature rise is too high, the start-up current limit can be reduced by selecting a larger sense resistor (R_{S2}). Using the conditions for this example, the worst-case temperature rise in M2 either in a normal start-up condition or with fault resistors is lower than 50°C, which verifies that the selected Channel 2 MOSFET, PSMNR51-25YLH, has more than enough SOA to handle the worst-case dissipation.

   Second, check the temperature rise in Channel 1 after startup when TMR times out under different overload conditions. In this example, the AONS32100 can take 160 A with 14 V across the MOSFET for 800 µs. The temperature rise in 20 µs is insignificant under overload conditions. If the worst-case

DESIGN EXAMPLES

temperature rise in Channel 1 is too high, larger MOSFETs must be selected.

LAYOUT CONSIDERATIONS

For high current applications, PCB layout plays a critical role in minimizing current congestion as well as partitioning the current between two channels. In parallel mode, to achieve the even split of current flow between the two channels, ensure that the two high current paths have similar layouts for the R_{SENSE} and MOSFET placements. To achieve accurate current sensing, Kelvin connections are also required. Lay out the SENSE+ and SENSE– lines as a differential signal pair. Make the trace lengths to the LTC4287 pins as short as possible. The minimum trace width for 1 oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1 oz copper exhibits a sheet resistance of approximately 530 µΩ per square. Small resistances add up quickly in high current applications. To improve noise immunity, place the resistive voltage dividers for the UV, OV, and FB pins close to the device and keep traces to V_{DD} and GND short. It is also important to put the $INTV_{CC}$ bypass capacitor as close as possible between $INTV_{CC}$ and GND. A 0.1 µF capacitor, C_F, from the UV pin (and the OV pin through the R2 resistor) to GND also helps reject supply noise. The EVAL-LTC4287 evaluation board shows a layout that addresses these issues (see the EVAL-LTC4287 User Guide). Note that a surge suppressor, Z1, is placed between the supply and ground using wide traces. It is recommended to avoid placing the ground plane under the power MOSFETs. If the MOSFETs overheat, the insulation can fail between the input voltage at their drains and an underlying ground plane, which can create a catastrophic short across the supply.

CHIP TICK TIMER AND ADC TIMING

The LTC4287 internal tick timer increments once every 2,320 clock cycles. The USER_TIME register increments at the tick timer rate. At the nominal 8.192 MHz clock rate, USER_TIME increments once per 283 µs. In 12-bit ADC mode voltage, current, power, and energy readings are updated once per tick increment. In 15-bit mode, the readings are updated once per eight tick increments.

The internal oscillator is overridden if a crystal or external signal is present at the CLKIN input. The frequency of the clock source can be combined with the ADC_AVERAGE_SELECT bits to optimize ADC readings for power-line noise rejection. The default ADC_AVERAGE_SELECT setting of 5 is optimum for this purpose. In this setting, averaged ADC results are presented once per 64 ticks in 12-bit mode, and the time between new readings is 148,480 clock cycles.

With the internal oscillator, new averages of 64 readings are returned at a rate of 55.2 Hz. For averages at a 60 Hz rate, use an 8.91 MHz clock. For averages at a 50 Hz rate, use an 7.42 MHz clock. In 15-bit mode, use the same clock speeds; however, ADC_AVERAGE_ SELECT must be 2.

With the internal oscillator, the tick field for READ_EIN rolls over in approximately 1.3 hours, and the tick field for MFR_READ_EIN rolls over in approximately 14 days.

As detailed in the MFR_READ_EIN (0xFA) section, the product of two 15-bit values is added to the energy accumulator once per ADC reading after shifting left by one bit. The maximum value added is 0x7FFF × 0x7FFF × 2 or approximately 2.1×10^9. With 64 bits of energy accumulator, the energy field in MFR_READ_EIN rolls over in no less than 28 days (with the internal oscillator).

The energy field in READ_EIN is based on the lower 47 bits of energy accumulator, and it rolls over in no less than 18 seconds. For 15-bit ADC mode, the energy accumulator rollover time is 8 times as long as in 12-bit mode.

LATCHED STATUS AND MASK COMMANDS

OVERVIEW

Latched status is kept in the following command locations:

- STATUS_BYTE
- STATUS_WORD
- STATUS_VOUT
- STATUS_IOUT
- STATUS_INPUT
- STATUS_TEMPERATURE
- STATUS_CML
- STATUS_OTHER
- STATUS_MFR_SPECIFIC
- MFR_SYSTEM_STATUS1
- MFR_SYSTEM_STATUS2

The status bits have three categories:

- Faults: conditions that cause GATE1 and GATE2 to turn off
- Warnings: conditions that could lead to a fault
- Events: errors and other information not related to faults

Once set, each status bit remains set until one of the following:

- A chip reset or reboot.
- A CLEAR_FAULTS command clears all.
- The ON bit in the OPERATION command is cleared then set again.
- All fault bits only clear if the RESET_FAULT_ENABLE bit is set (see Table 15) and an active edge is seen on the EN pin.
- A 1 bit is written to the corresponding location in the status command to clear it.

The LTC4287 also provides a method for software to set latched status bits. To support this, a parallel list of commands is defined. Writing 1 bits to these commands sets the corresponding status bits.

Each of the latched status bits is able to generate an SMBus alert condition by pulling down on a selected open-drain output (see Table 17 and Table 18 for details).

Status bits are combined with corresponding mask bits before activating the alert. If the mask bit is 1, the status bit does not contribute to the alert. The LTC4287 power-on default is for all status bits to be masked off, preventing alert indication. Software can write the mask commands to unmask selected status bits. The mask commands are configured automatically when an external EEPROM is used.

Table 10 details how the commands for latched status are related.

Table 10. Latched Status Commands

Main (R/W1C)[1]	Code	Mirror (R/W1S)[1]	Code	Mask (R/W)[1]	Code
STATUS_BYTE	0x78	MFR_STATUS_BYTE	0xFEC0	MFR_BYTE_ALERT_MASK	0xFED0
STATUS_WORD	0x79	MFR_STATUS_BYTE	0xFEC0	MFR_BYTE_ALERT_MASK	0xFED0
		MFR_STATUS_WORD_HIGH	0xFEC1	Not applicable	Not applicable
STATUS_VOUT	0x7A	MFR_STATUS_VOUT	0xFEC2	MFR_VOUT_ALERT_MASK	0xFED2
STATUS_IOUT	0x7B	MFR_STATUS_IOUT	0xFEC3	MFR_IOUT_ALERT_MASK	0xFED3
STATUS_INPUT	0x7C	MFR_STATUS_INPUT	0xFEC4	MFR_INPUT_ALERT_MASK	0xFED4
STATUS_TEMPERATURE	0x7D	MFR_STATUS_TEMP	0xFEC5	MFR_TEMP_ALERT_MASK	0xFED5
STATUS_CML	0x7E	MFR_STATUS_CML	0xFEC6	MFR_CML_ALERT_MASK	0xFED6
STATUS_OTHER	0x7F	MFR_STATUS_OTHER	0xFEC7	Not applicable	Not applicable
STATUS_MFR_SPECIFIC	0x80	MFR_SPECIFIC_STATUS	0xFEC8	MFR_SPECIFIC_ALERT_MASK	0xFED8
MFR_SYSTEM_STATUS1	0xE0	MFR_SYS_STAT1_SET	0xFECA	MFR_STAT1_ALERT_MASK	0xFEDA
MFR_SYSTEM_STATUS2	0xE1	MFR_SYS_STAT2_SET	0xFECC	MFR_STAT2_ALERT_MASK	0xFEDC

[1] R/W1C means read or write 1s to clear, R/W1S means read or write 1s to set, and R/W means read and write.

EXTERNAL EEPROM

OVERVIEW

The LTC4287 can optionally access an external EEPROM using a private SPI bus. To do this, connect the EEPROM CS# and SCK pins directly to the $\overline{CS}$ and SCK pins on the LTC4287. Tie the EPROM SO and SI pins together and connect these pins to the LTC4287 SIO pin. The drivers on the SIO pin are timed to avoid conflict with the EEPROM SO pin. For proper SPI bus levels, connect the DV_{CC} of the LTC4287 to the EEPROM V_{CC} pin.

The EEPROM must be 256 Kbits organized as 32 Kbytes. In addition, the EEPROM must have 64 byte page buffers. The LTC4287 has been thoroughly tested with the ON Semiconductor CAT25256; however, the specifications appear compatible with all generic SPI 256 Kbit EEPROMs. Compatible EEPROMs are also available from ST Micro, Microchip, Rohm, and ABLIC, as well as On Semiconductor.

The LTC4287 only uses the command codes listed in Table 11, which are supported by all 256 Kbit SPI EEPROM chips.

Table 11. Used EEPROM Codes

Code	Mnemonic	Meaning
0x06	WREN	Write enable
0x03	READ	Read data
0x02	WRITE	Write data
0x05	RDSR	Read status

No proprietary EEPROM features are used, including write protection. EEPROM write protection is implemented inside the LTC4287. Tie the EEPROM WP# and HOLD# pins high to disable those features in the EEPROM.

Logging features are discussed in the Logging section. The LTC4287 supports writing a log entry to the EEPROM after an impending power loss is detected ($INTV_{CC}$ is less than $INTV_{CC(UVLO)}$). In this case, the digital logic can still operate while DV_{CC} remains more than $DV_{CC(UVLO)}$). Three things are required for this feature:

- The EEPROM must support operation at 1.8 V.
- An external capacitor must be attached to DV_{CC} to hold the charge long enough to write a log entry (up to 50 ms if another log write is already in progress).
- The PL_LOG_EN bit must be set in the MFR_LOG_CONTROL register.

During EEPROM transfers, the SCK frequency is half the clock speed (either internal RC or external crystal) of the LTC4287. The highest supported crystal is 10 MHz; therefore, SCK speed is 5 MHz at the highest. For a log write on power loss, the SCK speed is reduced to 3.3 MHz.

EEPROM DATA USAGE

The LTC4287 splits the EEPROM into 128 logical pages of 256 bytes each (numbered 0 to 127). Logical Page 0 through Logical Page 125 are used for logging, Logical Page 126 is used to store chip configuration, and Logical Page 127 is reserved.

Each log entry occupies one logical page. Page 126 is split into two halves, each half containing a copy of the register configuration information of the LTC4287. The use of two copies allows protection from errors. If one copy of the configuration data has a problem, the LTC4287 can use the other copy to get the configuration. In addition, a simple version control system can be set up using the two configurations. See the MFR_CFG_VERS description for additional details (see Table 6).

DATA ACCESS METHODS

The following four methods are available for accessing external EEPROM data using the LTC4287. Note that these methods are mutually exclusive. Any attempt to mix these methods causes error statuses to be reported on the PMBus.

1. STORE and RESTORE commands. The PMBus standard STORE_USER_ALL and RESTORE_USER_ALL commands can be used to write or read back the configuration data, respectively, through Logical Page 126 in the EEPROM. STORE_USER_ALL writes the contents of all configurable registers to the EEPROM, and RESTORE_USER_ALL reads those registers back. At power-up or after a reboot, the LTC4287 initializes configurable registers with an automatic RESTORE_USER_ALL operation. These commands are available only when the EEPROM is locked (see the MFR_EE_UNLOCK (0xBD) section) and the EEPROM is not busy doing anything else. Also, the commands are blocked if automatic logging is enabled even if a log write is not taking place right now (see the Logging section).
2. MFR_EE fly by interface. This method is common to many Analog Devices, Inc., power products and is used by LTpowerPlay. In contrast with the STORE and RESTORE method, data transfers do not involve the configurable registers directly. The transfers fly by those registers. Use of this method starts by unlocking the EEPROM for access by using the MFR_EE_UNLOCK command (see the MFR_EE_UNLOCK (0xBD) section). MFR_EE_UNLOCK cannot be used if logging is enabled or if the EEPROM is already busy.

   The 2-byte unlock sequences allow access to configuration data in Logical Page 126. The 3-byte unlock sequences allow read only access to the entire EEPROM.

   Once the EEPROM is unlocked, MFR_EE_ERASE and MFR_EE_DATA (see the MFR_EE_ERASE (0xBE) section and the MFR_EE_DATA (0xBF) section, respectively) are available.

   Note that to use this access method requires detailed knowledge of the EEPROM data format including a cyclic redundancy check (CRC).
3. Log write and read. The writing of log data to Logical Pages 0 to Logical Page 125 in the EEPROM is managed through MFR_LOG_CONTROL (see Table 9). Using the NV_LOG_EN bits, log writes can be automatically triggered based on alerts, warnings, or faults in the LTC4287. In addition, the FORCE_LOG bit can be set to manually request a log write

EXTERNAL EEPROM

at any time. Automatic or manual log writing are allowed only when the EEPROM is not busy and is in the locked state.

Log data can be read back using the MFR_DATA_LOG command. This command returns a 255-byte block containing all the data for a selected log entry. The log entry returned is determined by the contents of MFR_LOG_RIDX, in which, Bits[6:0] select the logical page number.

MFR_DATA_LOG can be used even when automatic log writes are enabled. If a log write begins during the execution of MFR_DATA_LOG, the read operation is aborted and the error status returns. The log write completes normally.

4. Direct access to the EEPROM. The NV_HIZ bit in the MFR_LOG_CONTROL register (see Table 9) can be set to provide direct access to the EEPROM pins. The LTC4287 stops driving $\overline{CS}$, SCK, and SIO in response to a high on NV_HIZ. The bit can only be set when the EEPROM is locked and not busy with anything else.

LOGGING

As previously mentioned, the LTC4287 has a logging feature. Each log entry occupies one 256-byte logical page in the EEPROM. Log entry writes can be done manually or automatically in response to conditions in the LTC4287.

Each log entry consists of the following:

- Identifying information about this log entry
- Chip status at the time of the log write
- Current information for the selected ADC channels
- Historical data for the same selected ADC channels

ADC channels for logging are selected with the MFR_LOG_CONFIG command (see Table 10). When setting bits in the MFR_LOG_CONFIG command, ensure that the ADC channels are also selected in the MFR_ADC_CONFIG command (see Table 6).

Byte 1 is the log trigger event. This byte has flags that indicate why the log write took place. It is possible that two or three of the bits detailed in Table 12 can be set for the same log entry, which can happen because the LTC4287 optimizes to reduce the number of separate log entry writes.

Table 12. Log Trigger Event Byte Detail

Bit	Meaning
5	Loss of power (write only occurs if the PL_LOG_EN bit is set)
4	Reboot triggered by GPIOx input
3	FORCE_LOG bit set
2	Fault set
1	Latched warning set
0	Unmasked alert set

Byte 2 and Byte 3 are MFR_LOG_WIDX. This command indicates where the log entry is written in the EEPROM. The bytes are stored LSB first. Bits[6:0] specify the logical page number for the log entry.

The upper bits are not significant, but the LTC4287 increments these upper bits as MFR_LOG_WIDX and MFR_LOG_RIDX follow each other in the circular buffer. This supports accurate detection of log full vs. log empty conditions. If the log is full, or if the pointers are inconsistent, no log writes take place.

Byte 4 to Byte 23 is the status information.

Byte 32 to Byte 253 is the ADC data plus history.

The current ADC information appears first, with 6 bytes for each channel selected in MFR_LOG_CONFIG.

Table 13. ADC Log Data Format

Offset	Size	Name and Function
0	2	Instantaneous value
2	2	Minimum value
4	2	Maximum value

The channels appear in order of the MFR_LOG_CONFIG bits, LSB first.

History data appears after the current ADC data section. Only the instantaneous values are written in the history and no minimum or maximum values.

During normal operation, history data is stored in the internal RAM (128 words). The LOG_INTERVAL bits of the MFR_LOG_CONFIG register specify how often history data must be sampled (see Table 10). The channel list and the LOG_INTERVAL bits in the MFR_LOG_CONFIG register must be adjusted carefully to optimize the resolution and amount of history data that can be saved. Whenever MFR_LOG_INTERVAL is written, the 128 words of history in RAM are marked invalid (0xFFFF). If a log is written quickly after this, the log can contain 0xFFFF in some history locations.

Byte 254 and Byte 255 is the CRC.

DIGITAL INTERFACE

PMBUS SERIAL DIGITAL INTERFACE

The LTC4287 communicates with a host using the standard PMBus serial bus interface. PMBus is an extension of SMBus, and most of the timing and command structure comes from SMBus. The PMBus timing diagram shows the timing relationship of the signals on the bus. The SDAI and SDAO pins are usually tied together to form an SDA line. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The LTC4287 is a target device. The host can communicate with the LTC4287 using the following formats:

- Host transmitter, target receiver
- Host receiver, target transmitter

The following SMBus commands are supported:

- Write byte, write word, send byte
- Read byte, read word, block read
- Alert response address

Figure 49 to Figure 61 illustrate the aforementioned SMBus protocols. All transactions support packet error check (PEC) and group command protocol (GCP). The block read supports 255 bytes of returned data. For this reason, the SMBus timeout may be extended using the MFR_CONFIG_ ALL_LONGER_PMBUS_TIMEOUT setting.

PMBUS

PMBus is an industry standard that defines a means of communication with power conversion devices. This standard is composed of an industry standard SMBus serial interface and the PMBus command language.

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I^2C with some minor differences in timing, DC parameters, and protocol. The SMBus protocols are more robust than simple I^2C byte commands because these protocols provide timeouts to prevent bus hangs and optional PEC to ensure data integrity. In general, a host device that can be configured for I^2C communication can be used for PMBus communication with little or no change to hardware or firmware.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to the PMBus Specification Part 1 Revision 1.1: Section 5: Transport.

For a description of the differences between SMBus and I^2C, refer to System Management Bus (SMBus) Specification Version 3.1: Appendix B—Differences between SMBus and I^2C.

When using an I^2C controller to communicate with a PMBus part, it is important that the controller be able to write a byte of data without generating a stop, which allows the controller to properly form the repeated start of a PMBus read command by concatenating a start command byte write with an I^2C read.

PMBUS COMMAND SUMMARY

Nine distinct bus addresses are available using two three-state address pins, ADR0 and ADR1. Table 14 shows the correspondence between pin states and addresses. In addition, the LTC4287 responds to two special addresses. Address 0x1E is a mass write address that writes to all LTC4287 devices, regardless of their individual address settings. Mass write can be disabled by setting the MASS_WRITE_ENABLE in the MFR_CONFIG2 register to zero. Address 0x19 is the SMBus alert response address. If the ALERT bit in MFR_SYSTEM_STATUS1 is set, the LTC4287 acknowledges this address by broadcasting its target address and clearing the ALERT bit.

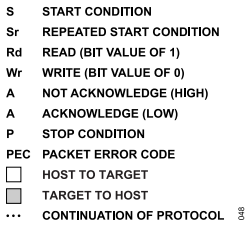

Figure 49. PMBus Packet Protocol Diagram Element Key

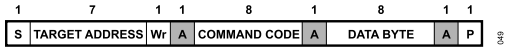

Figure 50. Write Byte Protocol

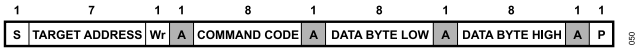

Figure 51. Write Word Protocol

Figure 52. Write Byte Protocol with PEC

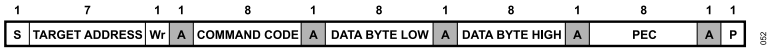

Figure 53. Write Word Protocol with PEC

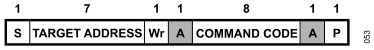

Figure 54. Send Byte Protocol

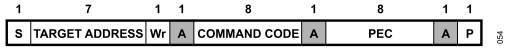

Figure 55. Send Byte Protocol with PEC

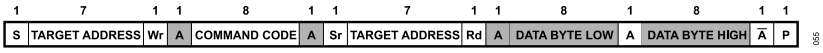

Figure 56. Read Word Protocol

Figure 57. Read Word Protocol with PEC

Figure 58. Read Byte Protocol

PMBUS COMMAND SUMMARY

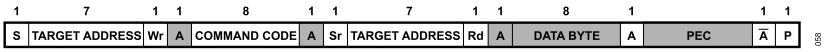

Figure 59. Read Byte Protocol with PEC

Figure 60. Block Read

Figure 61. Block Read with PEC

Table 14. LTC4287 Device Addressing

	HEX Device Address		Binary Device Address								LTC4287 Address Pins	
Description	**7-bit[1]**	**8-bit[2]**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**R/$\overline{W}$[3]**	**ADR1**	**ADR0**
Mass Write	0F	1E	0	0	0	1	1	1	1	0	X	X
Alert Response	0C	19	0	0	0	1	1	0	0	1	X	X
0	40	80	1	0	0	0	0	0	0	X	L	L
1	41	82	1	0	0	0	0	0	1	X	L	NC
2	42	84	1	0	0	0	0	1	0	X	L	H
3	43	86	1	0	0	0	0	1	1	X	NC	L
4	44	88	1	0	0	0	1	0	0	X	NC	NC
5	45	8A	1	0	0	0	1	0	1	X	NC	H
6	46	8C	1	0	0	0	1	1	0	X	H	L
7	47	8E	1	0	0	0	1	1	1	X	H	NC
8	11	22	0	0	1	0	0	0	1	X	H	H

[1] The 7-bit hexadecimal address with MSB 7 = 0.

[2] The 8-bit hexadecimal address with the LSB R/W bit = 0.

[3] H = tie to $INTV_{CC}$, L = tie to GND, NC = no connect or open, and X = don't care.

Table 15. LTC4287 PMBus Command Summary

Command Name	CMD Code	Description	Type	Data Format	Unit	NVM	Default Value
PAGE	0x00	Any value can be written to PAGE, but the value is not used by the chip internally. The value written can be read back.	R/W byte	Register	N/A	Yes	0x00
OPERATION	0x01	This command requests the hot swap to turn on or off.	R/W byte	Register	N/A	Yes	N/A
CLEAR_FAULTS	0x03	This command clears all latched status bits (all bits shaded in orange or pink in Figure 62). MFR_PMB_STAT and MFR_SD_CAUSE are also cleared by this commend (see Table 4) and Table 13, respectively.	Send byte	N/A	N/A	N/A	N/A
WRITE_PROTECT	0x10	Protects the device against unintended PMBus modifications.	R/W byte	Register	N/A	Yes	0x00
STORE_USER_ALL	0x15	Stores configuration data to the EEPROM. Can be written to only when NV_LOG_EN = 0.	Send Byte	N/A	N/A	N/A	N/A

PMBUS COMMAND SUMMARY

Table 15. LTC4287 PMBus Command Summary (Continued)

Command Name	CMD Code	Description	Type	Data Format	Unit	NVM	Default Value
RESTORE_USER_ALL	0x16	Restores configuration data from the EEPROM. Can be written to only when NV_LOG_EN = 0.	Send byte	N/A	N/A	N/A	N/A
CAPABILITY	0x19	Summary of supported optional PMBus features.	R byte	Register	N/A	N/A	0xD0
VOUT_OV_WARN_LIMIT	0x42	Sets the overvoltage warning limit for the voltage at V_{OUT} (SOURCE pin).	R/W word	Direct	V	Yes	0x7FFF
VOUT_UV_WARN_LIMIT	0x43	Sets the undervoltage warning limit for the voltage at V_{OUT} (SOURCE pin).	R/W word	Direct	V	Yes	0V0x0000
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W byte	Register	N/A	Yes	0xC0
IOUT_OC_WARN_LIMIT	0x4A	Sets overcurrent warning limit for IOUT ADC reading	R/W word	Direct	A	Yes	32 mV/R_{SENSE}, 0x7FFF
OT_FAULT_LIMIT	0x4F	Sets overtemperature fault limit for temperature ADC reading.	R/W word	Direct	℃	Yes	0x7FFF
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an overtemperature fault is detected.	R/W byte	Register	N/A	Yes	0x80
OT_WARN_LIMIT	0x51	Sets overtemperature warning limit for temperature ADC reading.	R/W word	Direct	℃	Yes	0x7FFF
UT_WARN_LIMIT	0x52	Sets undertemperature warning limit for temperature ADC reading.	R/W word	Direct	℃	Yes	0x0000
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W byte	Register	N/A	Yes	0xB8
VIN_OV_WARN_LIMIT	0x57	Sets the overvoltage warning limit for the voltage at the V_{IN} (V_{DD} pin).	R/W word	Direct	V	Yes	0x7FFF
VIN_UV_WARN_LIMIT	0x58	Sets the undervoltage warning limit for the voltage at the V_{IN} (V_{DD} pin).	R/W word	Direct	V	Yes	0V0x0000
VIN_UV_FAULT_RESPONSE	0x5A	Action to be taken by the device when an input undervoltage fault is detected.	R/W byte	Register	N/A	Yes	0xB8
PIN_OP_WARN_LIMIT	0x6B	Sets the overpower warning limit for the MFR_PIN ADC reading.	R/W word	Direct	W	Yes	3.2768/R_{SENSE}, 0x7FFF
STATUS_BYTE	0x78	One byte summary of the fault condition of the unit.	R/W byte	Register	N/A	N/A	0x00
STATUS_WORD	0x79	Two byte summary of the fault condition of the unit.	R/W word	Register	N/A	N/A	0x0000
STATUS_VOUT	0x7A	Provides status information for faults and warnings related to V_{OUT} (SOURCE pin).	R/W byte	Register	N/A	N/A	0x00
STATUS_IOUT	0x7B	Provides status information for faults and warnings related to I_{OUT}.	R/W byte	Register	N/A	N/A	0x00
STATUS_INPUT	0x7C	Provides status information for the faults and warnings related to V_{IN} and the MFR_PIN (V_{DD} pin).	R/W byte	Register	N/A	N/A	0x00
STATUS_TEMPERATURE	0x7D	Provides status information for faults and warnings related to temperature.	R/W byte	Register	N/A	N/A	0x00
STATUS_CML	0x7E	Provides status information for faults and warnings related to communication faults.	R/W byte	Register	N/A	N/A	0x00
STATUS_OTHER	0x7F	Provides other status faults.	R/W byte	Register	N/A	N/A	0x00
STATUS_MFR_SPECIFIC	0x80	Provides status information for manufacturer-specific faults and warnings.	R/W byte	Register	N/A	N/A	0x00
READ_EIN	0x86	Reads the energy metering registers in a single operation to ensure time consistent data.	R block, 6 bytes	Direct	J	N/A	N/A
READ_VIN	0x88	Reads the input voltage V_{IN} (V_{DD} pin).	R word	Direct	V	N/A	N/A
READ_VOUT	0x8B	Reads the output voltage V_{OUT} (SOURCE pin).	R word	Direct	V	N/A	N/A
READ_IOUT	0x8C	Reads I_{OUT}.	R word	Direct	A	N/A	N/A
READ_TEMPERATURE_1	0x8D	Reads the temperature measured by the device.	R word	Direct	℃	N/A	N/A

PMBUS COMMAND SUMMARY

Table 15. LTC4287 PMBus Command Summary (Continued)

Command Name	CMD Code	Description	Type	Data Format	Unit	NVM	Default Value
READ_PIN	0x97	Reads the calculated input power, P_{IN}.	R word	Direct	W	N/A	N/A
PMBUS_REVISION	0x98	PMBus revision supported. Current Revision is Version 1.3.	R byte	Register	N/A	N/A	0x33
MFR_ID	0x99	Returns string identifying the manufacturer of the device.	R block, 3 bytes	ASCII	N/A	N/A	LTC
MFR_MODEL	0x9A	Returns string identifying the specific model of the device.	R block, 7 bytes	ASCII	N/A	N/A	LTC4287
MFR_REVISION	0x9B	Returns string identifying the hardware revision of the device.	R block, 1 byte	Binary	N/A	N/A	0x11
IC_DEVICE_ID	0xAD	Returns string identifying the specific model of the device.	R block, 7 bytes	ASCII	N/A	N/A	LTC4287
IC_DEVICE_REV	0xAE	Returns string identifying the hardware revision of the device.	R block, 1 byte	Binary	N/A	N/A	0x11
USER_DATA_00	0xB0	Manufacturer reserved for LTpowerPlay.	R/W word	Register	N/A	N/A	N/A
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W word	Register	N/A	Yes	N/A
USER_DATA_02	0xB2	OEM reserved.	R/W word	Register	N/A	N/A	N/A
USER_SCRATCH_1	0xB3	Scratchpad Location Word 1.	R/W word	Register	N/A	Yes	0x0000
USER_SCRATCH_2	0xB4	Scratchpad Location Word 2.	R/W word	Register	N/A	Yes	0x0000
USER_SCRATCH_3	0xB6	Scratchpad Location Word 3.	R/W word	Register	N/A	Yes	0x0000
USER_SCRATCH_4	0xB7	Scratchpad Location Word 4.	R/W word	Register	N/A	Yes	0x0000
USER_TIME	0xB9	Cleared at power-on reset, increments at the internal tick timer rate. Can be written to set time.	R/W block 6 bytes	Register	N/A	Yes	0x000000
MFR_EE_UNLOCK	0xBD	Unlocks user EEPROM for bulk programming by MFR_EE_DATA (see MFR_EE_DATA (0xBF)).	R/W byte	Register	N/A	N/A	N/A
MFR_EE_ERASE	0xBE	Initializes user EEPROM for bulk programming by MFR_EE_DATA (see MFR_EE_DATA (0xBF)).	R/W byte	Register	N/A	N/A	N/A
MFR_EE_DATA	0xBF	Data transferred to and from the EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W word	Register	N/A	N/A	N/A
MFR_FLT_CONFIG	0xD2	Selects output for GPIOx pin configured as a fault output.	R/W byte	Register	N/A	Yes	0x00
MFR_PGI_FAULT_RESPONSE	0xD5	Action to be taken in response to PGI inactive.	R/W byte	Register	N/A	Yes	0x80
MFR_FET_FAULT_RESPONSE	0xD6	Action to be taken in response to FET_BAD condition.	R/W byte	Register	N/A	Yes	0x41
MFR_OP_FAULT_RESPONSE	0xD7	Selects device response to overpower fault.	R/W word	Register	N/A	Yes	0xFFE0
MFR_ADC_CONFIG	0xD8	Configures ADC mode and channels.	R/W byte	Register	N/A	Yes	0x01
MFR_AVG_SEL	0xD9	Selects ADC averaging rate, also enables display of averaged values in READ_VIN, READ_VOUT, READ_IOUT, and READ_PIN commands.	R/W byte	Register	N/A	Yes	0x85
MFR_SS_CONTROL	0xDA	Controls single-channel snapshot mode.	R/W byte	Register	N/A	Yes	0x00
MRF_LOFF	0xDC	Status of faults that are latched off. The seven bits in this register each correspond to a fault condition that is presently latched off (no retries available). Writing a 1 to any of the bits adds one retry if the fault is latched off.	R/W byte	Register	N/A	N/A	0x00
MFR_SYSTEM_STATUS1	0xE0	Provides manufacturer specific warning information.	R/W word	Register	N/A	N/A	N/A
MFR_SYSTEM_STATUS2	0xE1	Provides manufacturer system status information.	R/W word	Register	N/A	N/A	N/A
MFR_PMB_STAT	0xE2	Provides detailed status for latest PMBus transfers that failed.	R/W byte	Register	N/A	N/A	0x00

PMBUS COMMAND SUMMARY

Table 15. LTC4287 PMBus Command Summary (Continued)

Command Name	CMD Code	Description	Type	Data Format	Unit	NVM	Default Value
MFR_CLEAR_MIN_MAX	0xE3	This command sets all maximum values to 0x0000 and all minimum values to 0x7FFF. While this command executes, PMB_BUSY goes to 0 indicating further commands cannot be accepted, except the group of always ready commands.	Send byte	N/A	N/A	N/A	N/A
MFR_CFG_VERS	0xE4	Provides for version control of configuration data for use with the STORE_USER_ALL and RESTORE_USER_ALL commands.	R/W byte	Register	N/A	N/A	0x00
MFR_PADS_LIVE_STATUS	0xE5	State of the input and output pads and live status bits.	R word	Register	N/A	N/A	N/A
MFR_SPECIAL_ID	0xE7	This register contains the manufacturer ID, 0x7020, for the LTC4287.	R word	Register	N/A	N/A	0x7020
MFR_METER_CONTROL	0xE9	Controls energy meter block.	R/W byte	Register	N/A	Yes	0x00
MFR_LOG_CONTROL	0xEA	Controls data logging block.	R/W byte	Register	N/A	Yes	0x00
MFR_LOG_CONFIG	0xEB	Configures channels and speed for RAM history buffer. A write to this command clears the buffer. Can be written only when NV_LOG_EN = 0.	R/W word	Register	N/A	Yes	0x0000
MFR_LOG_RIDX	0xEC	Number of next EEPROM log entries to read. Can be written only when NV_LOG_EN = 0.	R/W word	Register	N/A	Yes	0x0000
MFR_LOG_WIDX	0xED	Number of next EEPROM log entries to be written. Can be written only when LV_LOG_EN = 0.	R/W word	Register	N/A	Yes	0x0000
MFR_DATA_LOG	0xEE	Reads next 255-byte data log block from the EEPROM.	R block	Register	N/A	Yes	N/A
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple Analog Devices chips.	R byte	Register	N/A	N/A	N/A
MFR_LIVE_STATUS2	0xF0	Provides additional live status bits.	R byte	Register	N/A	N/A	N/A
MFR_SD_CAUSE	0xF1	Cause of last hot-swap shutdown.	R byte	Register	N/A	Yes	0x00
MFR_CONFIG1	0xF2	Configures current limit, foldback, delays, and FET_BAD threshold and calculates the power input.	R/W word	Register	N/A	Yes	0x5572
MFR_CONFIG2	0xF3	Miscellaneous configuration.	R/W word	Register	N/A	Yes	0x00EF
MFR_GPIO_INV	0xF4	Sets polarity of GPIOx inputs and outputs.	R/W word	Register	N/A	Yes	0x009B
MFR_GPO_SEL41	0xF5	Configures GPIO1 to GPIO4 output functions.	R/W word	Register	N/A	Yes	0x5F43
MFR_GPO_SEL85	0xF6	Configures GPIO5 to GPIO8 output functions.	R/W word	Register	N/A	Yes	0x8207
MFR_GPI_SEL	0xF7	Configures GPIO1 to GPIO8 input functions.	R/W word	Register	N/A	Yes	0x0005
MFR_GPI_DATA	0xF8	Input values for GPIO1 to GPIO8.	R byte	Register	N/A	N/A	N/A
MFR_GPO_DATA	0xF9	Output values for GPIO1 to GPIO8.	R/W byte	Register	N/A	Yes	0xFF
MFR_READ_EIN	0xFA	Reads full versions of tick counter and energy meter.	R block 12 bytes	Register	J	N/A	0x00 x 12
MFR_READ_BLK	0xFB	Reads a time-coherent copy of several PMBus variables.	R block 16 bytes	Direct	N/A	N/A	0x00 x 16
MFR_ON_OFF_CONFIG	0xFC	Controls delay from fault detection to GATE1 and GATE2 pulled low.	R/W word	Register	N/A	Yes	0x001D
MFR_REBOOT_CONTROL	0xFD	Enables reboot and configures reboot delay.	R/W byte	Register	N/A	N/A	0x00
MFR_IOUT	0xFE00	I_{OUT} value, no averaging.	R word	Direct	A	N/A	N/A
MFR_IOUT_AVG	0xFE01	I_{OUT} value with averaging.	R word	Direct	A	N/A	N/A
MFR_IOUT_MIN	0xFE02	Saved minimum I_{OUT} value.	R/W word	Direct	A	N/A	0x7FFF
MFR_IOUT_MAX	0xFE03	Saved maximum I_{OUT} value.	R/W word	Direct	A	No?	0x0000
MFR_IOUT_UC_LIMIT	0xFE04	Limit for I_{OUT} undercurrent warning.	R/W word	Direct	A	Yes	0x0000
MFR_IOUT_OC_LIMIT	0xFE05	Limit for I_{OUT} overcurrent warning.	R/W word	Direct	A	Yes	0x7FFF
MFR_PIN	0xFE08	Measured power value, no averaging.	R word	Direct	W	N/A	N/A

PMBUS COMMAND SUMMARY

Table 15. LTC4287 PMBus Command Summary (Continued)

Command Name	CMD Code	Description	Type	Data Format	Unit	NVM	Default Value
MFR_PIN_AVG	0xFE09	The MFR_PIN value with averaging.	R word	Direct	W	N/A	N/A
MFR_PIN_MIN	0xFE0A	Saved minimum the MFR_PIN value.	R/W word	Direct	W	N/A	0x7FFF
MFR_PIN_MAX	0xFE0B	Saved maximum the MFR_PIN value.	R/W word	Direct	W	N/A	0x0000
MFR_PIN_UP_LIMIT	0xFE0C	Limit for the MFR_PIN underpower warning.	R/W word	Direct	W	Yes	0x0000
MFR_PIN_OP_LIMIT	0xFE0D	Limit for the MFR_PIN overpower warning.	R/W word	Direct	W	Yes	0x7FFF
MFR_VIN	0xFE10	V_{IN} value, no averaging.	R word	Direct	V	N/A	N/A
MFR_VIN_AVG	0xFE11	V_{IN} value with averaging.	R word	Direct	V	N/A	N/A
MFR_VIN_MIN	0xFE12	Saved minimum V_{IN} value.	R/W word	Direct	V	N/A	0x7FFF
MFR_VIN_MAX	0xFE13	Saved maximum V_{IN} value.	R/W word	Direct	V	N/A	0x0000
MFR_VIN_UV_LIMIT	0xFE14	Limit for V_{IN} undervoltage warning.	R/W word	Direct	V	Yes	0x0000
MFR_VIN_OV_LIMIT	0xFE15	Limit for V_{IN} overvoltage warning.	R/W word	Direct	V	Yes	0x7FFF
MFR_VOUT	0xFE18	V_{OUT} value, no averaging.	R word	Direct	V	N/A	N/A
MFR_VOUT_AVG	0xFE19	V_{OUT} value with averaging.	R word	Direct	V	N/A	N/A
MFR_VOUT_MIN	0xFE1A	Saved minimum V_{OUT} value.	R/W word	Direct	V	N/A	0x7FFF
MFR_VOUT_MAX	0xFE1B	Saved maximum V_{OUT} value.	R/W word	Direct	V	N/A	0x0000
MFR_VOUT_UV_LIMIT	0xFE1C	Limit for V_{OUT} undervoltage warning.	R/W word	Direct	V	Yes	0x0000
MFR_VOUT_OV_LIMIT	0xFE1D	Limit for V_{OUT} overvoltage warning.	R/W word	Direct	V	Yes	0x7FFF
MFR_VDS	0xFE20	V_{DS} value, no averaging.	R word	Direct	V	N/A	N/A
MFR_VDS_AVG	0xFE21	V_{DS} value with averaging.	R word	Direct	V	N/A	N/A
MFR_VDS_MIN	0xFE22	Saved minimum V_{DS} value.	R/W word	Direct	V	N/A	0x7FFF
MFR_VDS_MAX	0xFE23	Saved maximum V_{DS} value.	R/W word	Direct	V	No?	0x0000
MFR_VDS_UV_LIMIT	0xFE24	Limit for V_{DS} undervoltage warning.	R/W word	Direct	V	Yes	0x0000
MFR_VDS_OV_LIMIT	0xFE25	Limit for V_{DS} overvoltage warning.	R/W word	Direct	V	Yes	0x7FFF
MFR_CH1	0xFE28	Channel 1 value, no averaging.	R word	Direct	A	N/A	N/A
MFR_CH1_AVG	0xFE29	Channel 1 value with averaging.	R word	Direct	A	N/A	N/A
MFR_CH1_MIN	0xFE2A	Saved minimum Channel 1 value.	R/W word	Direct	A	N/A	0x7FFF
MFR_CH1_MAX	0xFE2B	Saved maximum Channel 1 value.	R/W word	Direct	A	N/A	0x0000
MFR_CH1_UC_LIMIT	0xFE2C	Limit for Channel 1 undercurrent warning.	R/W word	Direct	A	Yes	0x0000
MFR_CH1_OC_LIMIT	0xFE2D	Limit for Channel 1 overcurrent warning.	R/W word	Direct	A	Yes	0x7FFF
MFR_CH2	0xFE30	Channel 2 value, no averaging.	R word	Direct	A	N/A	N/A
MFR_CH2_AVG	0xFE31	Channel 2 value with averaging.	R word	Direct	A	N/A	N/A
MFR_CH2_MIN	0xFE32	Saved minimum Channel 2 value.	R/W word	Direct	A	N/A	0x7FFF
MFR_CH2_MAX	0xFE33	Saved maximum Channel 2 value.	R/W word	Direct	A	N/A	0x0000
MFR_CH2_UC_LIMIT	0xFE34	Limit for Channel 2 undercurrent warning.	R/W word	Direct	A	Yes	0x0000
MFR_CH2_OC_LIMIT	0xFE35	Limit for Channel 2 overcurrent warning.	R/W word	Direct	A	Yes	0x7FFF
MFR_ADIN1	0xFE38	ADIN1 value, no averaging.	R word	Direct	V	N/A	N/A
MFR_ADIN1_AVG	0xFE39	ADIN1 value with averaging.	R word	Direct	V	N/A	N/A
MFR_ADIN1_MIN	0xFE3A	Saved minimum ADIN1 value.	R/W word	Direct	V	N/A	0x7FFF
MFR_ADIN1_MAX	0xFE3B	Saved maximum ADIN1 value.	R/W word	Direct	V	N/A	0x0000
MFR_ADIN1_UV_LIMIT	0xFE3C	Limit for ADIN1 undervoltage warning.	R/W word	Direct	V	Yes	0x0000
MFR_ADIN1_OV_LIMIT	0xFE3D	Limit for ADIN1 overvoltage warning.	R/W word	Direct	V	Yes	0x7FFF
MFR_ADIN2	0xFE40	ADIN2 value, no averaging.	R word	Direct	V	N/A	N/A
MFR_ADIN2_AVG	0xFE41	ADIN2 value with averaging.	R word	Direct	V	N/A	N/A
MFR_ADIN2_MIN	0xFE42	Saved minimum ADIN2 value.	R/W word	Direct	V	N/A	0x7FFF
MFR_ADIN2_MAX	0xFE43	Saved maximum ADIN2 value.	R/W word	Direct	V	N/A	0x0000
MFR_ADIN2_UV_LIMIT	0xFE44	Limit for ADIN2 undervoltage warning.	R/W word	Direct	V	Yes	0x0000

PMBUS COMMAND SUMMARY

Table 15. LTC4287 PMBus Command Summary (Continued)

Command Name	CMD Code	Description	Type	Data Format	Unit	NVM	Default Value
MFR_ADIN2_OV_LIMIT	0xFE45	Limit for ADIN2 overvoltage warning.	R/W word	Direct	V	Yes	0x7FFF
MFR_TEMP	0xFE48	Temperature value, no averaging.	R word	Direct	℃	N/A	N/A
MFR_TEMP_AVG	0xFE49	Temperature value with averaging.	R word	Direct	℃	N/A	N/A
MFR_TEMP_MIN	0xFE4A	Saved minimum temperature value.	R/W word	Direct	℃	N/A	0x7FFF
MFR_TEMP_MAX	0xFE4B	Saved maximum temperature value.	R/W word	Direct	℃	N/A	0x0000
MFR_TEMP_UT_LIMIT	0xFE4C	Limit for temperature undertemperature warning.	R/W word	Direct	℃	Yes	0x0000
MFR_TEMP_OT_LIMIT	0xFE4D	Limit for temperature overtemperature warning.	R/W word	Direct	℃	Yes	0x7FFF
MFR_PIN_OP1_FAULT_LIMIT	0xFE58	Limit for the MFR_PIN overpower timed fault.	R/W word	Direct	W	Yes	0x7FFF
MFR_PIN_OP2_FAULT_LIMIT	0xFE59	Limit for the MFR_PIN overpower immediate fault.	R/W word	Direct	W	Yes	0x7FFF
MFR_STATUS_BYTE	0xFEC0	One byte summary of the fault condition of the unit.	R/W byte	Register	N/A	N/A	0x00
MFR_STATUS_WORD_HIGH	0xFEC1	Upper byte of STATUS_WORD.	R/W byte	Register	N/A	N/A	0x00
MFR_STATUS_VOUT	0xFEC2	Provides status information for faults and warnings related to V_{OUT} (SOURCE pin).	R/W byte	Register	N/A	N/A	0x00
MFR_STATUS_IOUT	0xFEC3	Provides status information for faults and warnings related to I_{OUT}.	R/W byte	Register	N/A	N/A	0x00
MFR_STATUS_INPUT	0xFEC4	Provides status information for faults and warnings related to V_{IN} and PIN (V_{DD} pin).	R/W byte	Register	N/A	N/A	0x00
MFR_STATUS_TEMP	0xFEC5	Provides status information for faults and warnings related to temperature.	R/W byte	Register	N/A	N/A	0x00
MFR_STATUS_CML	0xFEC6	Provides status information for faults and warnings related to communication faults.	R/W byte	Register	N/A	N/A	0x00
MFR_STATUS_OTHER	0xFEC7	Provides other status faults.	R/W byte	Register	N/A	N/A	0x00
MFR_SPECIFIC_STATUS	0xFEC8	Provides status information for manufacturer specific faults and warnings.	R/W byte	Register	N/A	N/A	0x00
MFR_SYS_STAT1_SET	0xFECA	Provides manufacturer specific warning information.	R/W word	Register	N/A	N/A	0x0000
MFR_SYS_STAT2_SET	0xFECC	Provides manufacturer system status information.	R/W word	Register	N/A	N/A	0x0000
MFR_BYTE_ALERT_MASK	0xFED0	Alert mask for STATUS_BYTE.	R/W byte	Register	N/A	Yes	0x80
MFR_VOUT_ALERT_MASK	0xFED2	Alert mask for STATUS_VOUT.	R/W byte	Register	N/A	Yes	0x60
MFR_IOUT_ALERT_MASK	0xFED3	Alert mask for STATUS_IOUT.	R/W byte	Register	N/A	Yes	0xA0
MFR_INPUT_ALERT_MASK	0xFED4	Alert mask for STATUS_INPUT.	R/W byte	Register	N/A	Yes	0xF1
MFR_TEMP_ALERT_MASK	0xFED5	Alert mask for STATUS_TEMPERATURE.	R/W byte	Register	N/A	Yes	0xE0
MFR_CML_ALERT_MASK	0xFED6	Alert mask for STATUS_CML.	R/W byte	Register	N/A	Yes	0xE3
MFR_SPECIFIC_ALERT_MASK	0xFED8	Alert mask for STATUS_MFR_SPECIFIC.	R/W byte	Register	N/A	Yes	0xFF
MFR_STAT1_ALERT_MASK	0xFEDA	Alert mask for MFR_SYSTEM_STATUS1.	R/W word	Register	N/A	Yes	0x3CFE
MFR_STAT2_ALERT_MASK	0xFEDC	Alert mask for MFR_SYSTEM_STATUS2.	R/W word	Register	N/A	Yes	0xCFFF

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Table 16. OPERATION (0x01) Read/Write

Bit(s)	Name	Default	Operation
7	ON	N/A	Indicates on and off command of the FET. 1 = FET commanded on. 0 = FET commanded off. A 0 to 1 edge for this bit clears all orange and pink shaded bits in Figure 62. If no external EEPROM is attached, the ON bit is selected based on the $\overline{CS}$ input (see the Configuration Without EEPROM section). If an external EEPROM is present and has valid data, the ON bit is initialized according to the EEPROM data. If an external EEPROM is present but has no valid data, the ON bit clears. EN must also be active to turn on.
[6:0]	Reserved	0000000	Always returns 0000000.

Table 17. WRITE_PROTECT (0x10) Read/Write

Bit(s)	Name	Default	Operation
7	WP1	0	Disables all writes except WRITE_PROTECT, PAGE, STORE_USER_ALL, and MFR_EE_UNLOCK commands. 1 = disable writes. 0 = enable writes.
6	WP2	0	Disables all writes except WRITE_PROTECT, PAGE, STORE_USER_ALL, MFR_EE_UNLOCK, OPERATION, CLEAR_FAULTS, and MFR_CLEAR_MIN_MAX commands. 1 = disable writes. 0 = enable writes.
[5:0]	Reserved	000000	Always returns 000000.

Table 18. CAPABILITY (0x19) Read Only

Bit(s)	Name	Default	Operation
7	PEC	1	Indicates that PEC supported.
[6:5]	MAX_BUS_SPEED	10	Indicates 1 MHz maximum bus speed supported.
4	SMBALERT#	1	Indicates SMBus alert response supported.
3	IEEE	0	Indicates that numeric data is linear or direct format.
2	AVSBUS	0	Indicates that the adaptive voltage scaling bus (AVSBus) is not supported.
[1:0]	Reserved	00	Always returns 00.

Table 19. IOUT_OC_FAULT_RESPONSE (0x47) Read/Write

Bit(s)	Name	Default	Operation	
[7:6]	OC_FAULT_RESPONSE	11	Configures response options for the OC fault.	
			Value	**Meaning**
			00	Ignore fault
			11	Device shuts down and responds according to retry settings
[5:3]	OC_FAULT_RETRY	000	Configures retry options for the OC fault.	
			Value	**Meaning**
			000	Latchoff
			001	1 retry
			010	2 retries
			011	3 retries
			100	4 retries
			101	5 retries
			110	6 retries
			111	∞ retries
[2:0]	Reserved	000	Always returns 000	

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Table 20. OT_FAULT_RESPONSE (0x50) Read/Write

Bit(s)	Name	Default	Operation	
[7:6]	OT_FAULT_RESPONSE	10	Configures response options for the OT fault.	
			Value	**Meaning**
			00	Ignore fault
			10	Device shuts down and responds according to retry settings
[5:3]	OT_FAULT_RETRY	000	Configures retry options for the OT fault.	
			Value	**Meaning**
			000	Latchoff
			001	1 retry
			010	2 retries
			011	3 retries
			100	4 retries
			101	5 retries
			110	6 retries
			111	∞ retries
[2:0]	Reserved	000	Always returns 000.	

Table 21. VIN_OV_FAULT_RESPONSE (0x56) Read/Write

Bit(s)	Name	Default	Operation	
[7:6]	VIN_OV_FAULT_RESPONSE	10	Configures response options for the OV fault.	
			Value	**Meaning**
			00	Ignore fault
			10	Device shuts down and responds according to retry settings
[5:3]	VIN_OV_FAULT_RETRY	111	Configures retry options for the OV fault.	
			Value	**Meaning**
			000	Latchoff
			001	1 retry
			010	2 retries
			011	3 retries
			100	4 retries
			101	5 retries
			110	6 retries
			111	∞ retries
[2:0]	Reserved	000	Always returns 000.	

Table 22. VIN_UV_FAULT_RESPONSE (0x5A) Read/Write

Bit(s)	Name	Default	Operation	
[7:6]	VIN_UV_FAULT_RESPONSE	10	Configures response options for the UV fault.	
			Value	**Meaning**
			00	Ignore fault
			10	Device shuts down and responds according to retry settings
[5:3]	VIN_UV_FAULT_RETRY	111	Configures retry options for the UV fault.	
			Value	**Meaning**
			000	Latchoff
			001	1 retry
			010	2 retries
			011	3 retries

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Table 22. VIN_UV_FAULT_RESPONSE (0x5A) Read/Write (Continued)

Bit(s)	Name	Default	Operation	
			100	4 retries
			101	5 retries
			110	6 retries
			111	∞ retries
[2:0]	Reserved	000	Always returns 000.	

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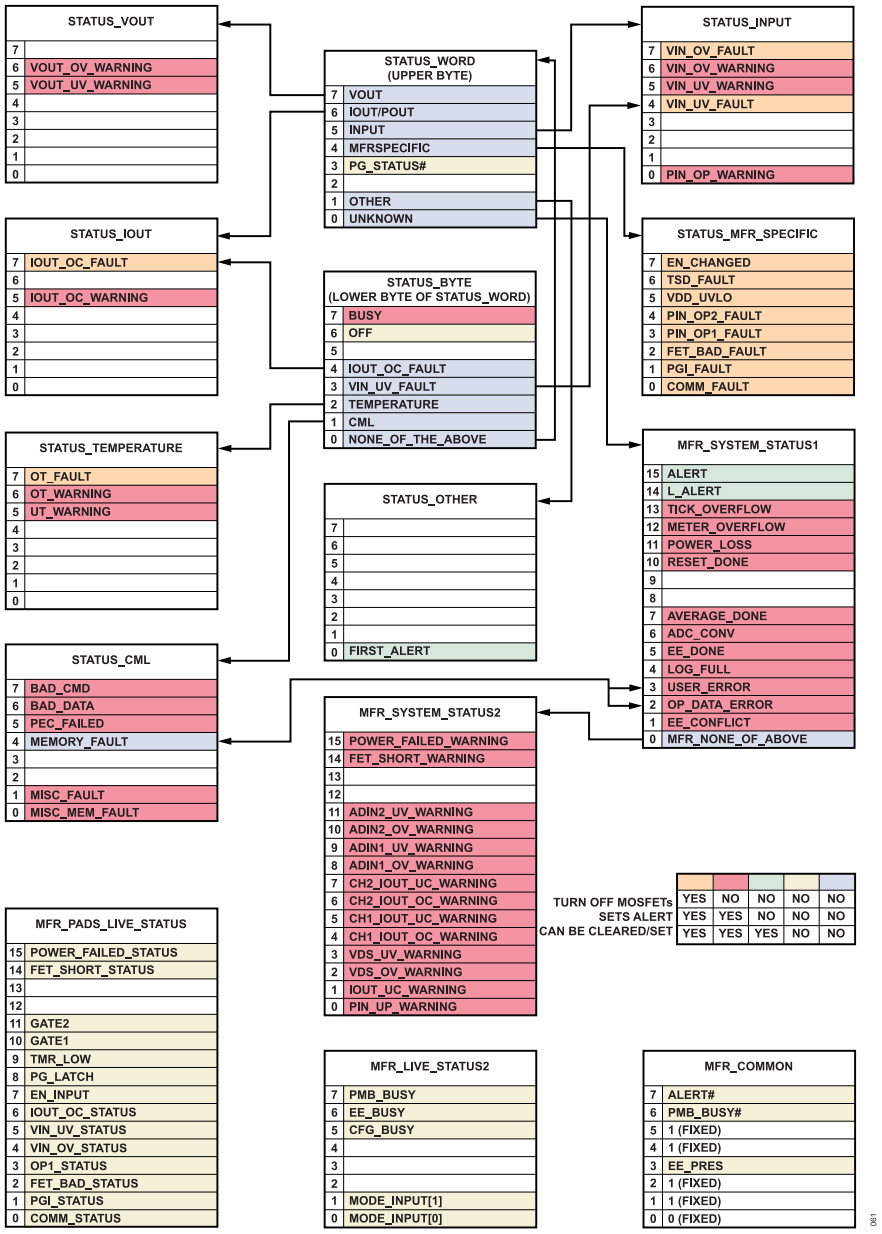

Figure 62. LTC4287 Status Register Summary

Table 23. STATUS_BYTE (0x78) Read/W1C, MFR_STATUS_BYTE (0xFEC0) Read/W1S, and MFR_BYTE_ALERT_MASK (0xFED0) Read/Write

Bit(s)	Name	Default	Operation
7	BUSY	0	Bit set if the device is busy and cannot respond to a PMBus access.

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Table 23. STATUS_BYTE (0x78) Read/W1C, MFR_STATUS_BYTE (0xFEC0) Read/W1S, and MFR_BYTE_ALERT_MASK (0xFED0) Read/Write (Continued)

Bit(s)	Name	Default	Operation
6	OFF	0	Hot-swap gate is off. 1 = gate is disabled. 0 = gate is enabled.
5	Reserved	0	Always returns 0.
4	IOUT_OC_FAULT	0	Copy of IOUT_OC_FAULT bit in STATUS_IOUT.
3	VIN_UV_FAULT	0	Copy of VIN_UV_FAULT in STATUS_VIN.
2	TEMPERATURE	0	Temperature fault or warning. 1 = there are one or more active status bits in the STATUS_TEMPERATURE. 0 = there are no active status bits.
1	CML	0	CML fault or warning. 1 = there are one or more active status bits in the STATUS_CML. 0 = there are no active status bits.
0	NONE_OF_THE_ABOVE	0	None of the above. 1 = one or more status bits not listed in Bits[7:1] are set.

Table 24. STATUS_WORD (0x79) Read/W1C, MFR_STATUS_BYTE/MFR_STATUS_WORD_HIGH (0xFEC0/0xFEC1) Read/W1S, and MFR_BYTE_ALERT_MASK (0xFED0) Read/Write

Bit(s)	Name	Default	Operation
15	VOUT	0	V_{OUT} (SOURCE pin) fault or warning. 1 = there are one or more active status bits in the STATUS_VOUT. 0 = there are no active status bits.
14	IOUT/POUT	0	I_{OUT} fault or warning. 1 = there are one or more active status bits in the STATUS_IOUT. 0 = there are no active status bits.
13	INPUT	0	V_{IN} (V_{DD} pin) status warning. 1 = there are one or more active status bits in the STATUS_INPUT. 0 = there are no active status bits.
12	MFRSPECIFIC	0	Manufacture specific fault or warning. 1 = there are one or more active faults, Bits[7:3] in the STATUS_MFR_SPECIFIC. 0 = there are no active fault bits.
11	PG_STATUS#	0	Bit is high if the FB input pin is less than 2.56 V, indicating the MOSFET output voltage is not high enough for the PG_LATCH status.
10	Reserved	0	Always returns 0.
9	OTHER	0	Status is present in the STATUS_OTHER byte.
8	UNKNOWN	0	Bit is high to indicate one or more bits in MFR_SYSTEM_STATUS1 are set.
7	BUSY	0	Bit set if the device is busy and cannot respond to a PMBus access.
6	OFF	0	Hot-swap gate is off. 1 = gate is disabled. 0 = gate is enabled.
5	Reserved	0	Always returns 0.
4	IOUT_OC_FAULT	0	Copy of the IOUT_OC_FAULT bit in STATUS_IOUT.
3	VIN_UV_FAULT	0	Copy of the VIN_UV_FAULT in STATUS_VIN.
2	TEMPERATURE	0	Temperature fault or warning. 1 = there are one or more active status bits in the STATUS_TEMPERATURE. 0 = there are no active status bits.
1	CML	0	CML fault or warning. 1 = there are one or more active status bits in the STATUS_CML. 0 = there are no active status bits.

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Table 24. STATUS_WORD (0x79) Read/W1C, MFR_STATUS_BYTE/MFR_STATUS_WORD_HIGH (0xFEC0/0xFEC1) Read/W1S, and MFR_BYTE_ALERT_MASK (0xFED0) Read/Write (Continued)

Bit(s)	Name	Default	Operation
0	NONE_OF_THE_ABOVE	0	None of the above. 1 = one or more status bits not listed in Bits[7:1] are set.

Table 25. STATUS_VOUT (0x7A) Read/W1C, MFR_STATUS_VOUT (0xFEC2) Read/W1S, and MFR_VOUT_ALERT_MASK (0xFED2) Read/Write

Bit(s)	Name	Default	Operation
7	Reserved	0	Always returns 0
6	VOUT_OV_WARNING	0	V_{OUT} overvoltage warning. 1 = detected overvoltage by the voltage ADC measuring the SOURCE pin. 0 = no OV detected.
5	VOUT_UV_WARNING	0	V_{OUT} undervoltage warning. 1 = detected undervoltage by the voltage ADC measuring the SOURCE pin. 0 = no UV detected.
[4:0]	Reserved	0	Always returns 0.

Table 26. STATUS_IOUT (0x7B) Read/W1C, MFR_STATUS_IOUT (0xFEC3) Read/W1S, and MFR_IOUT_ALERT_MASK (0xFED3) Read/Write

Bit(s)	Name	Default	Operation
7	IOUT_OC_FAULT	0	I_{OUT} overcurrent fault (latched). 1 = detected overcurrent past the TMR pin time limit. 0 = no OC fault detected.
6	Reserved	0	Always returns 0.
5	IOUT_OC_WARNING	0	I_{OUT} overcurrent warning. 1 = detected overcurrent warning by the current ADC (VSENSE+ – VSENSE—). 0 = no OC detected.
[4:0]	Reserved	0	Always returns 0.

Table 27. STATUS_INPUT (0x7C) Read/W1C, MFR_STATUS_INPUT (0xFEC4) Read/W1S, and MFR_INPUT_ALERT_MASK (0xFED4) Read/Write

Bit(s)	Name	Default	Operation
7	VIN_OV_FAULT	0	V_{IN} overvoltage fault (latched). 1 = detected overvoltage on the OV pin. 0 = no OV detected.
6	VIN_OV_WARNING	0	V_{IN} overvoltage warning. 1 = detected overvoltage by the VOLTAGE ADC measuring the V_{DD} pin. 0 = no OV detected.
5	VIN_UV_WARNING	0	V_{IN} undervoltage warning. 1 = detected overvoltage by the voltage ADC measuring the V_{DD} pin. 0 = no UV detected.
4	VIN_UV_FAULT	0	V_{IN} undervoltage fault (latched). 1 = detected undervoltage on the UV pin. 0 = no UV detected.
[3:1]	Reserved	0	Always returns 000.
0	PIN_OP_WARNING	0	Calculated input power, PIN, overpower warning; 1 = detected overpower, 0 = no OP detected

Table 28. STATUS_TEMPERATURE (0x7D) Read/W1C, MFR_STATUS_TEMP (0xFEC5) Read/W1S, and MFR_TEMP_ALERT_MASK (0xFED5) Read/Write

Bit(s)	Name	Default	Operation
7	OT_FAULT	0	Overtemperature fault (latched). 1 = detected overtemperature fault by the temperature ADC. 0 = no overtemperature detected.

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Table 28. STATUS_TEMPERATURE (0x7D) Read/W1C, MFR_STATUS_TEMP (0xFEC5) Read/W1S, and MFR_TEMP_ALERT_MASK (0xFED5) Read/Write (Continued)

Bit(s)	Name	Default	Operation
6	OT_WARNING	0	Overtemperature warning. 1 = detected overtemperature warning by the temperature ADC. 0 = no OT detected.
5	UT_WARNING	0	Undertemperature warning. 1 = detected undertemperature warning by the temperature ADC. 0 = no undertemperature detected.
[4:0]	Reserved	00000	Always returns 00000.

Table 29. STATUS_CML (0x7E) Read/W1C, MFR_STATUS_CML (0xFEC6) Read/W1S, and MFR_CML_ALERT_MASK (0xFED6), Read/Write

Bit(s)	Name	Default	Operation
7	BAD_CMD	0	Invalid or unsupported command received.
6	BAD_DATA	0	Invalid or unsupported data received.
5	PEC_FAILED	0	PEC failed or PEC byte missing where is it required (MFR_EE_UNLOCK, MFR_EE_ERASE or MFR_EE_DATA).
4	MEMORY_FAULT	0	Set when USER_ERR or OP_DATA_ERR bit set in MFR_SYSTEM_STATUS1.
[3:2]	Reserved	00	Always returns 00.
1	MISC_FAULT	0	Miscellaneous communications fault occurred.
0	MISC_MEM_FAULT	0	Set when the EEPROM operation attempted is not allowed.

Table 30. STATUS_OTHER (0x7F) Read/W1C and MFR_STATUS_OTHER (0xFED7) Read/W1S

Bit(s)	Name	Default	Operation
[7:1]	Reserved	0000000	Always returns 0000000.
0	FIRST_ALERT	0	Bit set if this chip is the first to assert ALERT# low.

Table 31. STATUS_MFR_SPECIFIC (0x80) Read/W1C, MFR_SPECIFIC_STATUS (0xFEC8) Read/W1S, and MFR_SPECIFIC_ALERT_MASK (0xFED8) Read/Write

Bit(s)	Name	Default	Operation
7	EN_CHANGED	0	Indicates that the $\overline{EN}$ pin changed state. 1 = $\overline{EN}$ changed state. 0 = $\overline{EN}$ unchanged.
6	TSD_FAULT	0	Latched to a 1 if a thermal shutdown condition is detected. 0 = no thermal shutdown.
5	VDD_UVLO	0	Latched to a 1 if the V_{DD} input goes to less than the VDD_UVLO limit. 0 = no UVLO condition on V_{DD}.
4	PIN_OP2_FAULT	0	Indicates that the MFR_PIN has exceeded the limit for the immediate fault.
3	PIN_OP1_FAULT	0	Indicates that the timer has expired for the timed MFR_PIN fault limit.
2	FET_BAD_FAULT	0	Latched to a 1 if FET_BAD fault occurred. 0 = no FET_BAD fault.
1	PGI_FAULT	0	When GPIO pin is configured as PGI# or PGI, this bit is latched to a 1 if the GPIO pin input does not match the expected value when the PGI watchdog timer expires. 1 = GPIOx pin mismatch detected. 0 = no GPIOx pin mismatch detected.
0	COMM_FAULT	0	Latched to a 1 if GATE1 and GATE2 are disabled due to a low level found on the COMM function of the GPIO5 pin.

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Table 32. READ_EIN Format, 6-Byte Block Read

Byte	7	6	5	4	3	2	1	0
0	Energy, Bits[31:24]							
1	0	Energy, Bits[38:32]						
2	Energy, Bits[46:39]							
3	Tick, Bits[7:0]							
4	Tick, Bits[15:8]							
5	Tick, Bits[23:16]							

The READ_EIN (0x86) command returns abbreviated versions of the internal energy meter and tick counters in the standard PMBus format. See MFR_READ_EIN (0xFA) for an alternate version with greater resolution. This command is in block read format.

The 0 in Byte 1, Bit 7 is a sign bit specified by PMBus. Energy values are always positive. See the Chip Tick Timer and ADC Timing section for further details on rollover time on the energy and tick fields.

By default, access to the external EEPROM by the MFR_EE_xxx commands is disabled. Before reading or writing data to the EEPROM, the MFR_EE_UNLOCK command must be issued to unlock access. Specific sequences of byte write data are required to unlock.

Table 33. MFR_EE_UNLOCK Sequences

Operation	Data Sequence	PEC Required	EEPROM Area
Unlock for read	0x2B, 0x91, 0xE4	No	All 32 Kbytes
Unlock for read	0x2B, 0x91, 0xE5	Yes	All 32 Kbytes
Unlock for read, write, or erase	0x2B, 0xD4	No	256-byte configuration block
Unlock for read, write, or erase	0x2B, 0xD5	Yes	256-byte configuration block

Access to MFR_EE_UNLOCK always require a PEC byte. Depending on the sequence chosen, PEC can optionally be required for subsequent MFR_EE_ERASE and MFR_EE_DATA access following Table 1. Any sequence but those listed in Table 1 result in the EEPROM staying locked. Reading back from MFR_EE_UNLOCK returns the most recent byte written if EEPROM is successfully unlocked. If the EEPROM is still locked, a read returns 0x00. The EEPROM cannot be unlocked if it is already busy or if data logging is enabled (NV_LOG_EN ≠ 0).

The MFR_EE_ERASE (0xBE) command can be used to erase the 256-byte configuration data area in the external EEPROM. To use this command, MFR_EE_UNLOCK must first be used to unlock the EEPROM. In addition, the EEPROM must not be busy from another command, and data logging must be disabled.

To erase the configuration data, write 0x2B to the command register. During erase, EE_BUSY in MFR_LIVE_STATUS2 are set. After erase completion, the EE_DONE bit in MFR_SYSTEM_STATUS1 is set, which can be used to generate an alert. Erase can take as long as 640 ms (128 times the EEPROM write cycle time).

Note that MFR_EE_ERASE is not strictly required because available 32 Kbyte SPI EEPROM chips all auto-erased before a write.

The MFR_EE_DATA (0xBF) word-wide command is used to read and write data to the 256-byte configuration area of the external EEPROM. To use this command, MFR_EE_UNLOCK must first be used to unlock the EEPROM. In addition, the EEPROM must not be busy from another command, and data logging must be disabled.

The command code can be used for both reads and writes; however the direction cannot be changed suddenly. The first read or write after MFR_EE_UNLOCK sets the access direction. Data is transferred in the same order as it appears in the EEPROM. In general, this results in little-Endian order; however, some internal register words end up split into two separate EEPROM words.

When reading, the first and second words contain fixed information that is not from the EEPROM (see Table 1).

Table 34. MFR_EE_DATA First Two Words for Read

Word	Contents	Description
First	EEPROM format ID	It is always 0x0000 for the LTC4287.
Second	0x0080 or 0x4000	For a 2-byte unlock sequence, 128 words available. For a 3-byte sequence, 16,384 is available.

After the second word, read the number of words indicated. If further words are read, bytes of 0x00 are returned, and the EEPROM is locked.

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When writing, each word of data is written directly to the EEPROM up to the 128 limit. Any further writes are ignored, and the EEPROM is locked.

With EEPROM reads, no handshake is needed because data is already read from the EEPROM in advance of receiving the MFR_EE_DATA command. For writes, the handshake of EE_BUSY and EE_DONE is used as described in the MFR_EE_ERASE (0xBE) section.

Table 35. MFR_FLT_CONFIG (0xD2) Read and Write

Bit(s)	Name	Default	Operation
[7:2]	Reserved	000000	Always returns 000000.
1	OP_TO_FAULT	0	Sets gate overpower fault to the GPIOx fault output.
0	OT_TO_FAULT	0	Sets gate overtemperature fault to the GPIOx fault output.

Table 36. MFR_PGI_FAULT_RESPONSE (0xD5) Read/Write

Bit(s)	Name	Default	Operation	
[7:6]	PGI_RESPONSE	10	Configures response options for the PGI fault.	
			Value	**Meaning**
			00	Ignore fault.
			10	Device shuts down and responds according to the retry settings.
[5:3]	PGI_RETRY	000	Configures retry options for the PGI fault.	
			Value	**Meaning**
			000	Latchoff.
			001	1 retry.
			010	2 retries.
			011	3 retries.
			100	4 retries.
			101	5 retries.
			110	6 retries.
			111	∞ retries.
[2:0]	Reserved	000	Always returns 0.	

Table 37. MFR_FET_FAULT_RESPONSE (0xD6) Read and Write

Bit(s)	Name	Default	Operation	
[7:6]	FET_BAD_RESPONSE	01	Configures response options for the FET_BAD fault.	
			Value	**Meaning**
			00	Ignore fault.
			01	Device continues for FED_BD_FLT_DL. If fault is still present, responds according to the retry settings.
[5:3]	FET_BAD_RETRY	000	Configures retry options for the FET_BAD fault.	
			Value	**Meaning**
			000	Latchoff.
			001	1 retry.
			010	2 retries.
			011	3 retries.
			100	4 retries.
			101	5 retries.
			110	6 retries.
			111	∞ retries.
[2:0]	FETBD_FLT_DL	01	Selects the delay time for the FET_BAD fault.	
			FETBD_FLT_DL	**Delay**
			000	0.073 sec.
			001	0.145 sec.
			010	0.290 sec.

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Table 37. MFR_FET_FAULT_RESPONSE (0xD6) Read and Write (Continued)

Bit(s)	Name	Default	Operation	
			011	0.580 sec.
			100	1.16 sec.
			101	2.32 sec.
			110	4.64 sec.
			111	9.28 sec.

Table 38. MFR_OP_FAULT_RESPONSE (0xD7) Read and Write

Bit(s)	Name	Default	Operation	
[15:5]	OP_TIMER	11111111111	Timer for the OP1 Fault. The timer function combines increment and decrement. Each time that the MFR_PIN is greater than MFR_PIN_OP1_FAULT_LIMIT, an internal counter increments by 2. Each time PIN is less than MFR_PIN_OP1_FAULT_LIMIT, the internal counter decrements by 1. PIN_OP1_FAULT is set if the overpower condition persists for OP_TIMER × 1.13 ms.	
[4:3]	OP_FAULT_RESPONSE	00	Configures response options for the PIN_OP1_FAULT or PIN_OP2_FAULT.	
			Value	**Meaning**
			00	Ignore fault.
			10	Device shuts down and responds according to the retry settings.
[2:0]	OP_FAULT_RETRY	000	Configures retry options for the OP1 or OP2 fault.	
			Value	**Meaning**
			000	Latchoff.
			001	1 retry.
			010	2 retries.
			011	3 retries.
			100	4 retries.
			101	5 retries.
			110	6 retries.
			111	∞ retries.

Table 39. MFR_ADC_CONFIG (0xD8) Read and Write

Bit	Name	Default	Operation
7	15_BIT_MODE	0	Selects 15-bit ADC mode (one reading per 2.2 ms). The default is 12-bit mode, one reading per 0.283 ms. See the Data Converters section for format details.
6	Reserved	0	Always returns 0.
5	ADIN2_SELECT	0	Selects ADIN2 as an auxiliary input for ADC measurement.
4	ADIN1_SELECT	0	Selects ADIN1 as an auxiliary input for ADC measurement.
3	CH2_IOUT_SELECT	0	Selects Channel 2 I_{OUT} ($V_{SENSE2+}$ − $V_{SENSE2-}$) as an auxiliary input for ADC measurement.
2	CH1_IOUT_SELECT	0	Selects Channel 1 I_{OUT} ($V_{SENSE1+}$ − $V_{SENSE1-}$) as an auxiliary input for ADC measurement.
1	VDS_SELECT	0	Enables VDS as an auxiliary input for ADC measurement.
0	VIN_VOUT_SELECT	1	Enables V_{IN} or V_{OUT} as an auxiliary input for ADC measurement. The choice between the two depends on VPWR_SELECT in MFR_CONFIG1. If V_{IN} is selected in VPWR_SELECT, V_{OUT} is available as an auxiliary input. If V_{OUT} is selected in VPWR_SELECT, V_{IN} is available as an auxiliary input.

Table 40. MFR_AVG_SEL (0xD9) Read and Write

Bit(s)	Name	Default	Operation
7	DISP_AVG	1	1 selects averaged values for READ_VIN, READ_VOUT, READ_IOUT and READ_PIN. 0 selects unaveraged values.
[6:4]	Reserved	000	Always returns 000.
[3:0]	ADC_AVERAGE_SELECT	0101	Selects the number of ADC samples per average. See the Chip Tick Timer and ADC Timing section for further details.

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Table 41. ADC_AVERAGE_SELECT Options

Value	Samples	12-Bit Time	15-Bit Time
0000	2	0.566 ms	4.53 ms
0001	4	1.13 ms	9.06 ms
0010	8	2.27 ms	18.1 ms
0011	16	4.53 ms	36.3 ms
0100	32	9.06 ms	72.5 ms
0101	64	18.1 ms	145 ms
0110	128	36.3 ms	290 ms
0111	256	72.5 ms	580 ms
1000	512	145 ms	1.16 sec
1001	1024	290 ms	2.32 sec
1010	2048	580 ms	4.62 sec
1011	4096	1.16 sec	9.28 sec
1100	8192	2.32 sec	18.6 sec
1101	16384	4.64 sec	37.1 sec
1110	32768	9.28 sec	74.2 sec
1111	65536	18.6 sec	148 sec

The MFR_SS_CONTROL (0xDA) register controls snapshot mode, which is a method of requesting a particular channel to be sampled out of normal sequence.

In normal operation, the ADC always cycles through the list of channels specified in MFR_ADC_CONFIG, Bits[5:0]. The ADC also samples the SENSE+/SENSE− channel plus either V_{IN} or V_{OUT} to make power calculations. These readings and derived calculations are stored in their assigned registers as soon as possible after each sample.

A snapshot request is used for two reasons:

- To sample a channel at a specific time
- To retain the sample long enough to read it out without overwriting

The snapshot feature of the LTC4287 does these requests without stopping the normal scanning of the ADC channels. The only compromise is a possible latency up to 566.4 µs to get the data of the selected channel (in 12-bit mode). A snapshot can be requested through a register write or through an external signal connected to a GPIOx pin (REQ_ADC_SS).

To request a snapshot by register write, ensure that the following is done:

- Set the desired channel in SNAPSHOT_SELECT.
- Set REQ_ADC_SS to start it (this can be done at the same time SNAPSHOT_SELECT is updated).
- Wait for SS_DONE to be set to indicate that results are ready to view.
- The snapshot results are visible in the usual ADC locations. (ADC scanning continues in the background values with all updates processed as normal for logging and statistics.)
- Clear REQ_ADC_SS to allow access to the most recent ADC values.

To request a snapshot request via a GPIOx (ADC_SS_SEL) pin, ensure that the following is done:

- Set the desired channel in SNAPSHOT_SELECT.
- Set GPI_SS_EN to enable a snapshot request on the next ADC_SS_SEL, GPIOx pin, rising edge. As previously mentioned, these requests can be done in the same register write.
- Pulse ADC_SS_SEL of the GPIOx pin high when ready for the ADC snapshot.
- The detected edge sets REQ_ADC_SS to 1. From this point forward, the operation is as previously described.

For both cases, another GPIOx pin (ADC_SS_DONE) outputs an active low copy of the SS_DONE bit if that GPIOx pin is configured as ADC_SS_DONE#. The snapshot feature is not available when the ADC is in 15-bit mode. In that case, attempted accesses to MFR_SS_CONTROL are rejected with a no acknowledge (NACK).

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Table 42. MFR_SS_CONTROL (0xDA) Read and Write

Bit(s)	Name	Default	Operation	
7	REQ_ADC_SS	0	Request and ADC Snapshot Reading. Reads the channel indicated in SNAPSHOT_SELECT.	
6	SS_DONE	0	After REQ_ADC_SS is set, SS_DONE goes to 1 to indicate that the snapshot request is complete.	
5	GPI_SS_EN	0	When set, a rising edge on a GPIOx pin causes REQ_ADC_SS to set and to request snapshot access.	
[4:3]	Reserved	00	Always returns 00.	
[2:0]	SNAPSHOT_SELECT	000	Selects one of the six ADC auxiliary inputs for snapshot measurement.	
			SNAPSHOT_SELECT	**Auxiliary ADC Input**
			000	V_{OUT} or V_{IN}
			001	ADIN1
			010	ADIN2
			011	V_{DS}
			100	CH1_IOUT
			101	CH2_IOUT

Table 43. MFR_LOFF (0xDC) Read/W1C

Bits(s)	Name	Default	Operation
6	UV_LOFF	0	Bit is set to 1 when the undervoltage fault is latched off.
5	OV_LOFF	0	Bit is set to 1 when the overvoltage fault is latched off.
4	OT_LOFF	0	Bit is set to 1 when the overtemperature fault is latched off.
3	OC_LOFF	0	Bit is set to 1 when the overcurrent fault is latched off.
2	OP_LOFF	0	Bit is set to 1 when either the overpower faults (OP1 or OP2) are latched off.
1	FB_LOFF	0	Bit is set to 1 when the FET_BAD fault is latched off.
0	PGI_LOFF	0	Bit is set to 1 when the PGI fault is latched off.

Table 44. MFR_SYSTEM_STATUS1 (0xE0) Read/W1C, MFR_SYS_STAT1_SET (0xFECA) Read/W1S and MFR_STAT1_ALERT_MASK (0xFEDA) Read/Write

Bit(s)	Name	Default	Operation
15	ALERT	0	Bit is set to 1 when an alert is generated, which can be cleared via an SMBus write or alert response protocol. The bit can be configured to appear as active low or high on any GPIOx pin.
14	L_ALERT	0	Alternate version of ALERT or latched ALERT. This bit is set by the same conditions that set ALERT. However, this bit can only be cleared by an SMBus write. This bit can be configured to appear on any GPIOx pin as $\overline{\text{L\_ALERT}}$ or L_ALERT.
13	TICK_OVERFLOW	0	Indicates Whether Tick Counter Has Overflowed. 1 = overflowed. 0 = not overflowed.
12	METER_OVERFLOW	0	Indicates Whether Energy Meter Accumulator Has Overflowed. 1 = overflowed. 0 = not overflowed.
11	POWER_LOSS	0	Bit is 1 following a power-on reset or 0 after a reboot-generated reset.
10	RESET_DONE	1	Latched status bit is set after each chip reset (either power-on or reboot).
[9:8]	Reserved	00	Always returns 00.
7	AVERAGE_DONE	0	Set at the completion of an average.
6	ADC_CONV	0	Latched to 1 when a full ADC conversion (current and voltage) completes.
5	EE_DONE	0	Set at the completion of the EEPROM activity requested by a STORE_USER_ALL, RESTORE_USER_ALL, MFR_EE_ERASE, or MFR_EE_DATA command.
4	LOG_FULL	0	Set if all available log entries in the EEPROM are filled. Each time a log entry is read through the MFR_DATA_LOG command, that entry is marked as available for subsequent logs.
3	USER_ERROR	0	Set when configuration data in the EEPROM cannot be read due to a CRC error. Configuration data is read after reset, when a RESTORE_USER_ALL command is issued, or when the REBOOT bit is set in the MFR_REBOOT_CONTROL command.

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Table 44. MFR_SYSTEM_STATUS1 (0xE0) Read/W1C, MFR_SYS_STAT1_SET (0xFECA) Read/W1S and MFR_STAT1_ALERT_MASK (0xFEDA) Read/Write (Continued)

Bit(s)	Name	Default	Operation
2	OP_DATA_ERROR	0	Set when the operating data in the EEPROM of the device cannot be read due to an uncorrectable ECC error. The operating data is read from the EEPROM at the same time configuration data is read. The values of MFR_LOG_RIDX, MFR_LOG_WIDX, USER_SCRATCH_n, USER_TIME, and HS_SHUTDOWN_CAUSE are normally preserved in the EEPROM. In addition, a device lifetime clock is preserved in the EEPROM. If the operating data cannot be read, these registers and fields revert to 0s. If OP_DATA_ERROR is set, data logging is disabled (NV_LOG_EN = 0).
1	EE_CONFLICT	0	Set if a read from MFR_DATA_LOG is terminated due to a log entry write to the EEPROM.
0	MFR_NONE_OF_ABOVE	0	Bit is set if bits in MFR_SYSTEM_STATUS2 are set.

Table 45. MFR_SYSTEM_STATUS2 (0xE1) Read/W1C, MFR_SYS_STAT2_SET (0xFECC) Read/W1S, and MFR_SYS_ALERT_MASK1 (0xFEDC) Read and Write

Bit(s)	Name	Default	Operation
15	POWER_FAILED_WARNING	0	This latched bit is for if POWER_FAILED_STATUS goes active, which happens if the FB input pin goes to less than 2.56 V while the PG_LATCH status bit is set, which indicates that a loss of output voltage after it was initially good.
14	FET_SHORT_WARNING	0	Latched to a 1 if measured (V_{SENSE+} – V_{SENSE-}) exceeds 2 mV while FET is off (FET short was detected). 1 = FET short fault occurred. 0 = no FET short fault.
[13:12]	Reserved	00	Always returns 00.
11	ADIN2_UV_WARNING	0	Latched to 1 when the ADIN2 ADC measurement is less than the threshold set by MFR_ADIN2_UV_LIMIT. 1 = ADIN2 is low. 0 = ADIN2 is not low.
10	ADIN2_OV_WARNING	0	Latched to 1 when the ADIN2 ADC measurement is more than the threshold set by MFR_ADIN2_OV_LIMIT. 1 = ADIN2 is high. 0 = ADIN2 is not low.
9	ADIN1_UV_WARNING	0	Latched to 1 when the ADIN1 ADC measurement was below the threshold set by MFR_ADIN1_UV_LIMIT. 1 = ADIN1 is low. 0 = ADIN1 is not low.
8	ADIN1_OV_WARNING	0	Latched to 1 when the ADIN1 ADC measurement was above the threshold set by MFR_ADIN1_OV_LIMIT. 1 = ADIN1 is high. 0 = ADIN1 is not high.
7	CH2_IOUT_UC_WARNING	0	Latched to 1 when the Channel 2 I_{OUT} ($V_{SENSE2+}$ – $V_{SENSE2–}$) ADC measurement is less than the threshold set by MFR_CH2_UC_LIMIT. 1 = Channel 2 I_{OUT} is low. 0 = Channel 2 I_{OUT} is not low.
6	CH2_IOUT_OC_WARNING	0	Latched to 1 when the Channel 2 I_{OUT} ($V_{SENSE2+}$ – $V_{SENSE2–}$) ADC measurement is more than the threshold set by MFR_CH2_OC_LIMIT. 1 = Channel 2 I_{OUT} is high. 0 = Channel 2 I_{OUT} is not high.
5	CH1_IOUT_UC_WARNING	0	Latched to 1 when the Channel 1 I_{OUT} ($V_{SENSE1+}$ – $V_{SENSE1–}$) ADC measurement is less than the threshold set by MFR_CH1_UC_LIMIT. 1 = Channel 1 I_{OUT} is low. 0 = Channel 1 I_{OUT} is not low.
4	CH1_IOUT_OC_WARNING	0	Latched to 1 when the Channel 1 I_{OUT} ($V_{SENSE1+}$ – $V_{SENSE1–}$) ADC measurement was above the threshold set by MFR_CH1_OC_LIMIT. 1 = Channel 1 I_{OUT} is high.

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Table 45. MFR_SYSTEM_STATUS2 (0xE1) Read/W1C, MFR_SYS_STAT2_SET (0xFECC) Read/W1S, and MFR_SYS_ALERT_MASK1 (0xFEDC) Read and Write (Continued)

Bit(s)	Name	Default	Operation
			0 = Channel 1 I_{OUT} is not high.
3	VDS_UV_WARNING	0	Latched to 1 when the V_{DS} input is less than MFR_VDS_UV_LIMIT.
2	VDS_OV_WARNING	0	Latched to 1 when the V_{DS} input is more than MFR_VDS_OV_LIMIT.
1	IOUT_UC_WARNING	0	Indicates that I_{OUT} is less than the warning limit in MFR_IOUT_UC_LIMIT.
0	PIN_UP_WARNING	0	Indicates that the MFR_PIN is less than the warning limit in MFR_PIN_UP_LIMIT.

Table 46. MFR_PMB_STAT (0xE2) Read and Write

Bit(s)	Name	Operation
[7:5]	Reserved	Always returns 000.
[4:0]	PMB_STATUS	Provides detail for the most recent PMBus transfer that had a problem. A value of 0 indicates no recorded problem. Once set to a non-zero value, PMB_STATUS holds that value until another PMBus transfer has a problem. Table 5 details the code values. The register can also be written. Writing a non-zero value results in the status bit setting shown in Table 5.

Table 47. PMB_STATUS Code Values

Value	Description	Target Bit
0x01	Chip busy due to previous command	STATUS:BUSY
0x02	Chip busy for this command due to the EEPROM	STATUS:BUSY
0x03	Incoming PEC_BAD	STATUS_CML:PEC_FAILED
0x04	Repeated start or stop bit received not on byte boundary	STATUS_CML:MISC_FAULT
0x05	Stop bit received before end, no PMBus error	Not applicable
0x06	Read was NACK'ed before final byte, no PMBus error	Not applicable
0x07	Host read too many bytes	STATUS_CML:MISC_FAULT
0x08	Host wrote too many bytes	STATUS_CML:BAD_DATA
0x09	Target address with R/$\overline{W}$ high rejected	STATUS_CML:MISC_FAULT
0x0A	Bad command code received	STATUS_CML:BAD_CMD
0x0B	Attempt to write invalid data value	STATUS_CML:BAD_DATA
0x0C	Attempt to write a read-only command	STATUS_CML:BAD_DATA
0x0D	Attempt to access the EEPROM related command, no EEPROM present	STATUS_CML:BAD_CMD
0x0E	Attempted write with STORE_USER_ALL to write-protected EEPROM block	STATUS_CML:MISC_MEM_FAULT
0x0F	Write rejected due to WRITE_PROTECT register setting	STATUS_CML:BAD_DATA
0x10	MFR_DATA_LOG interrupted by log write	MFR_SYSTEM_STATUS1:EE_CONFLICT
0x11	Command not accessible while logging enabled	STATUS_CML:BAD_CMD
0x12	PEC byte missing during MFR_EE_UNLOCK, MFR_EE_ERASE, or MFR_EE_DATA access that requires it	STATUS_CML:PEC_FAILED
0x13	Byte count for block write incorrect	STATUS_CML:BAD_DATA
0x14	Reserved	Not applicable
0x15	Read data not available in time	STATUS:BUSY
0x16	SDAO data conflict (another chip pulled down SDA when data was coming from this chip)	STATUS_CML:MISC_FAULT
0x17	SDAO conflict specifically on alert response address (ARA) no PMBus error	Not applicable
0x18	Reserved	Not applicable
0x19	Attempted read of write only (transceiver byte) command	STATUS_CML:MISC_FAULT
0x1A	If CRC errors during an MFR_DATA_LOG read, no PMBus error	Not applicable
0x1B	Log request but no data available	STATUS:BUSY
0x1C	Normal EEPROM function attempted while MFR_EE_UNLOCK is not in locked state	STATUS_CML:MISC_MEM_FAULT
0x1D	MFR_EE_ERASE or MFR_EE_DATA access attempted while MFR_EE_UNLOCK is not in unlocked state	STATUS_CML:MISC_MEM_FAULT
0x1E	Attempt to change MFR_EE_ERASE or MFR_EE_DATA operation while the EEPROM is unlocked	STATUS_CML:MISC_MEM_FAULT
0x1F	Reserved	Not applicable

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Table 48. MFR_CFG_VERS (0xE4) Read and Write

Bit(s)	Name	Default	Operation
7	SKIP	0	Skip Block. When this bit is set in the EEPROM configuration block, it is skipped during RESTORE_USER_ALL (read) commands. 1 = skip block. 0 = read block. Note that the bit can be written to the EEPROM (from this register) with STORE_USER_ALL.
6	WP	0	Write Protect. When this bit is set in the EEPROM configuration block, it is write protected during STORE_USER_ALL (write) commands. 1 = write protected. 0 = not protected. Note: Bit cannot be written to EEPROM with STORE_USER_ALL, use MFR_EE_DATA to write WP bit to EEPROM
5	DUP_EN	0	Duplicate Enable. When this bit is set in this register, a STORE_USER_ALL writes two copies of the configuration: one copy to Block 0 (CFG_ID = 0) and one to Block 1 (CFG_ID = 1). 1 = enables write to both blocks simultaneously. 0 = enables write to block specified with CFG_ID.
4	CFG_ID	0	Configuration Block ID Number. 0 = Block 0. 1 = Block 1.
[3:0]	Reserved	0000	Always returns 0000.

Table 49. MFR_PADS_LIVE_STATUS (0xE5) Read Only

Bit(s)	Name	Description
15	POWER_FAILED_STATUS	POWER_FAILED_STATUS is active when FB input pin goes to less than 2.56 V while the PG_LATCH status bit is set, which indicates that a loss of output voltage after it was initially good.
14	FET_SHORT_STATUS	Indicates potential FET short if (V_{SENSE+} – V_{SENSE-}) exceeds 2 mV while FET is off. 1 = FET shorted. 0 = FET not shorted.
[13:12]	Reserved	Always returns 00.
11	GATE2	Indicates state of the GATE2 pin. 1 = GATE2 pin is high. 0 = GATE2 pin is low.
10	GATE1	Indicates state of the GATE1 pin. 1 = GATE1 pin is high. 0 = GATE1 pin is low.
9	TMR_LOW	Indicates whether the TMR pin is low. 1 = TMR is lower than 0.2 V. 0 = TMR is higher than 0.2 V.
8	PG_LATCH	Latched signal is active when system power seems good. The conditions to set are FB > 2.56 V, V_{GS} > 8 V, and V_{DS} < 2 V for single FET operation. For dual FET operation, either both V_{GS} voltages must be >8 V or one V_{GS} > 8 V while the opposite FET is in active current limit. When either FB is low or both FETs are turned off clears PG_LATCH depending on the PWRGD_RESET_CONTROL bit.
7	EN_INPUT	Bit is 1 to indicate that the EN pin is in the active state.
6	IOUT_OC_STATUS	Overcurrent Condition from the Comparator. 1 = overcurrent. 0 = no overcurrent.
5	VIN_UV_STATUS	Indicates input undervoltage when UV pin is low. 1 = UV low. 0 = UV high.
4	VIN_OV_STATUS	Indicates input overvoltage when OV pin is high. 1 = OV high.

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Table 49. MFR_PADS_LIVE_STATUS (0xE5) Read Only (Continued)

Bit(s)	Name	Description
		0 = OV low.
3	OP1_STATUS	Bit is 1 to indicate that the MFR_PIN exceeds the MFR_PIN_OP1_FAULT_LIMIT value. The bit automatically clears when the MFR_PIN falls to less than that value.
2	FET_BAD_STATUS	Indicates FET_BAD condition is present. 1 = FET_BAD condition present. 0 = FET_BAD condition not present.
1	PGI_STATUS	If a GPIOx pin is in PGI mode, PGI_STATUS = 1 to indicate PGI GPIOx is low. For PGI# mode, PGI_STATUS = 1 to indicate PGI GPIOx is high. In both cases, 1 indicates a potential problem.
0	COMM_STATUS	COMM signal pulled down by other device in system.

Table 50. MFR_METER_CONTROL (0xE9) Read and Write

Bit(s)	Name	Default	Operation
7	METER_RESET	0	Resets energy meter and tick counter until cleared. 1 = reset. 0 = reset cleared.
6	METER_PAUSE	0	Pauses energy meter and tick counter from accumulating until cleared. 1 = energy meter and tick counter paused. 0 = pause cleared.
5	SEL_METER_I	0	Enables current to replace power in the energy meter accumulator. 1 = integrate current. 0 = integrate power.
[4:0]	Reserved	00000	Always returns 00000.

Table 51. MFR_LOG_CONTROL (0xEA) Read/Write

Bit(s)	Name	Default	Operation	
7	FORCE_LOG	0	Forces the device to write a log entry, bit auto-clears after the log is complete.	
6	CLEAR_LOG	0	Clears the non-volatile fault log in the EEPROM, bit auto-clears after the log is cleared.	
5	PL_LOG_EN	0	Set this bit to enable writing a separate log entry in response to a power loss event (VDD_UVLO or INTVCC_UVLO). If the bit is set, DV_{CC} must remove more than 2.1 V for at least 50 ms to write the log entry and finish up any previous log entry in progress. If the bit is 0, the required DV_{CC} holdup time is reduced to 25 ms.	
4	LOG_FULL_WRT	0	Bit enables continuous log entry writes after a trigger until the EEPROM is filled.	
3	SNGL_F_LOG	0	This bit controls the use of fault information when NV_LOG_EN is 01. If SNGL_F_LOG is clear, a 0 to 1 edge for any fault status bit (orange shaded in Figure 62) requests a fault log. When SNGL_F_LOG is set, only fault conditions that turn off GATE1 and GATE2 request a fault log write.	
2	NV_HIZ	0	Set this bit to request direct control of the external EEPROM. Before doing this, NV_LOG_EN must be set to 0 and EE_BUSY must be 0.	
[1:0]	NV_LOG_EN	0	Configures logging trigger for the data logger.	
			NV_LOG_EN[1:0]	**Log Trigger**
			00	If FORCE_LOG set.
			01	If FORCE_LOG set or fault detected.
			10	If FORCE_LOG set, fault or warning detected.
			11	If FORCE_LOG set or if ALERT# asserted.

Table 52. MFR_LOG_CONFIG (0xEB) Read and Write

Bit(s)	Name	Default	Operation
15	Reserved	0	Always returns 0.
[14:12]	LOG_INTERVAL	000	Selects the rate at which data is collected in the RAM history buffer. The rate is once per 2LOG_INTERVAL × 0.2832 ms. The minimum is 0.2832 ms and the maximum is 36.25 ms.
[11:9]	Reserved	000	Always returns 000.
8	LOG_ADIN2	0	Selects ADIN2 as an input for data logging.

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Table 52. MFR_LOG_CONFIG (0xEB) Read and Write (Continued)

Bit(s)	Name	Default	Operation
7	LOG_ADIN1	0	Selects ADIN1 as an input for data logging.
6	LOG_CH2_IOUT	0	Selects Channel 2 I_{OUT} ($V_{SENSE2+}$ – $V_{SENSE2-}$) as an input for data logging.
5	LOG_CH1_IOUT	0	Selects Channel 1 I_{OUT} ($V_{SENSE1+}$ – $V_{SENSE1-}$) as an input for data logging.
4	LOG_VDS	0	Selects V_{DS} as an input for data logging.
3	LOG_VOUT	0	Selects V_{OUT} (SOURCE) as an input for data logging.
2	LOG_VIN	0	Selects V_{IN} (V_{DD}) as an input for data logging.
1	LOG_PIN	0	Selects the MFR_PIN as an input for data logging.
0	LOG_IOUT	0	Selects I_{OUT} (V_{SENSE+} – V_{SENSE-}) as an input for data logging.

Table 53. MFR_COMMON (0xEF) Read Only

Bit(s)	Name	Default	Operation
7	CHIP_NOT_DRIVING_ALERT	1	Bit is 0 when the LTC4287 is pulling down ALERT#.
6	CHIP_NOT_BUSY	1	Bit is 0 when some registers are unavailable for PMBus access.
[5:4]	Reserved	11	Always returns 11.
3	EE_PRES	1	1 = the EEPROM is detected present. 0 = no EEPROM is detected.
[2:0]	Reserved	110	Always returns 110.

Table 54. MFR_LIVE_STATUS2 (0xF0) Read Only

Bit(s)	Name	Default	Operation
7	PMB_BUSY	0	Bit is 1 when some registers are unavailable for PMBus access.
6	EE_BUSY	0	Bit is 1 when external EEPROM is busy.
5	CFG_BUSY	0	Indicates if the EEPROM is busy reading configuration information from the EEPROM. 1 = busy.This bit is set after an initial power-up or a reboot operation.
[4:2]	Reserved	000	Always returns 000.
[1:0]	MODE_INPUT	Not applicable	00 indicates HSSS mode. 01 indicates LSSS mode. 11 indicates parallel mode. If no EEPROM is present, these bits are fixed at initialization time based on Table 8. If EEPROM is attached, the bits reflect the present condition of the MODE pin. 00 is for ground 01 is for Hi-Z or midlevel. 11 is for 5 V.

Table 55. MFR_SD_CAUSE (0xF1) Read Only

Bit(s)	Name	Default	Operation	
[7:4]	Reserved	0000	Always returns 0000.	
[3:0]	HS_SHUTDOWN_CAUSE	0000	Cause of the last hot-swop shutdown, backed up in the EEPROM.	
			HS_SHUTDOWN_CAUSE [3:0]	**Cause**
			0001	OPERATION command
			0010	EN pin
			0011	REBOOT or restart
			0100	INTVCC_UVLO
			0101	Thermal shutdown (TSD)
			0110	VDD_UVLO
			0111	OT_FAULT
			1000	IOUT_OC_FAULT
			1001	PIN_OP2_FAULT
			1010	PIN_OP1_FAULT

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Table 55. MFR_SD_CAUSE (0xF1) Read Only (Continued)

Bit(s)	Name	Default	Operation	
			1011	FET_BAD_FAULT
			1100	VIN_UV_FAULT
			1101	VIN_OV_FAULT
			1110	PGI_FAULT
			1111	COMM_FAULT

Table 56. MFR_CONFIG1 (0xF2) Read and Write

Bit(s)	Name	Default	Operation		
15	Reserved	0	Always returns 0.		
14	THERM_TMR	1	Configures the TMR pin. 1 = thermal timer. 0 = traditional timer.		
[13:10]	ILIM	0101	Configures the sense reference voltage for the current limit, see the Current-Limit Foldback section.		
[9:8]	FB	01	Configures the current-limit threshold vs. the V_{DS} profile in running and start-up modes.		
			FB	**Running Mode**	**Start-Up Mode**
			00	Constant power	Constant power
			01	High power	High power
			10	Constant power	10% fixed low current
			11	High power	10% fixed low current
7	Reserved	0	Always returns 0.		
[6:5]	VDTH	11	Configures drain voltage threshold for starting the FET_BAD fault filtering timer.		
			VDTH	**Threshold**	
			00	50 mV	
			01	100 mV	
			10	150 mV	
			11	200 mV	
[4:2]	COOLING_DL	100	Configures the cooling delay preceding each auto-retry following OC_FAULT, OP_FAULT, or FET_BAD_FAULT.		
			COOLING_DL	**Delay**	
			000	0.580 sec	
			001	1.16 sec	
			010	2.32 sec	
			011	4.64 sec	
			100	9.28 sec	
			101	18.6 sec	
			110	37.1 sec	
			111	74.2 sec	
1	VRANGE_SELECT	1	Sets a voltage range for V_{IN} and V_{OUT} measurements.		
			VRANGE_SELECT	**Voltage Range for V_{IN} and V_{OUT}**	
			0	25.6 V	
			1	102.4 V	
0	VPWR_SELECT	0	Selects the voltage for the power multiplication (optional). See the VIN_VOUT_SELECT bit for interaction with the ADC auxiliary input list.		
			VPWR_SELECT	**Voltage for Power Multiplication**	
			0	V_{IN} (attenuated V_{DD} voltage for input power)	
			1	V_{OUT} (attenuated SOURCE voltage for FET power)	

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Table 57. MFR_CONFIG2 (0xF3) Read and Write

Bit(s)	Name	Default	Operation		
[15:14]	Reserved	00	Always returns 00.		
13	INVERT_EN	0	Set bit to select active low for the EN input.		
12	SEL_1M	0	Set bit to enable 1 Mbit-compatible timing for PMBus.		
[11:10]	GPIO_ADIN2	00	Selects a GPIOx input for ADIN2 ADC measurement.		
			GPIO_ADIN2	**Input**	
			00	GPIO5	
			01	GPIO6	
			10	GPIO7	
			11	GPIO8	
[9:8]	GPIO_ADIN1	00	Selects a GPIOx input for ADIN1 ADC measurement.		
			GPIO_ADIN1	**Input**	
			00	GPIO5	
			01	GPIO6	
			10	GPIO7	
			11	GPIO8	
7	RESET_FAULT_ENABLE	1	Enables fault reset on an edge of the EN pin going active. 1 = EN active edge reset fault register bits. 0 = EN active edge has no impact on fault register bits.		
6	PWRGD_RESET_CONTROL	1	Configures PG_LATCH reset. 1 = FB low resets PG_LATCH. 0 = FET off resets PG_LATCH.		
5	MASS_WRITE_ENABLE	1	Enables mass write or global address to this device and others on the SMBus. 1 = mass write enabled. 0 = mass write disabled.		
4	Reserved	0	Always returns 0.		
3	COMM_ENABLE	1	Set to enable the COMM function of the GPIO5 pin.		
2	EXT_TEMP_ENABLE	1	Enables the use of an external temperature sensor on GPIO3 (default), falls back to on-chip temperature sensor disabled.		
1	DB_EN_ON_EN	1	Enables use of the debounce timer for EN transitions.		
0	DB_DLY	1	Selects debounce delay time for EN and UV transitions and delay time for $\overline{\text{POWER\_GOOD}}$.		
			DB_DLY	**Debounce Delay**	**$\overline{\text{POWER\_GOOD}}$ Delay**
			0	11.3 ms	22.6 ms
			1	90.6 ms	181 ms

Table 58. MFR_GPIO_INV (0xF4) Read and Write

Bit(s)	Name	Default	Operation
[15:12]	Reserved	0000	Always returns 0000
11	ADC_SS_INV	0	Assigns polarity for GPIOx input associated with ADC single-shot trigger input. 0 = rising edge of the GPIOx pin triggers ADC snapshot (ADC_SS_SEL input). 1 = falling edge of the GPIOx pin triggers ADC snapshot (ADC_SS_SEL# input).
10	PGI_INV	0	Assigns polarity for GPIOx input associated with PGI power-good watchdog input. 0 = rising edge of GPIOx prevents PGI fault (PGI input). 1 = falling edge of GPIOx pin prevents PGI fault (PGI# input).
9	RBT_INV	0	Assigns polarity for GPIOx input associated with reboot input. 0 = rising edge of GPIOx pin triggers reboot. 1 = falling edge of GPIOx pin triggers reboot.
8	Reserved	0	Always returns 0.

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Table 58. MFR_GPIO_INV (0xF4) Read and Write (Continued)

Bit(s)	Name	Default	Operation
7	INV8	1	Assigns polarity for GPIO8 output. 0 = GPIO8 pin pulls low when specified output bit is low. 1 = GPIO8 pin pulls low when specified output bit is high.
6	INV7	0	Assigns polarity for GPIO7 output; 0 = GPIO7 pin pulls low when specified output bit is low. 1 = GPIO7 pin pulls low when specified output bit is high.
5	INV6	0	Assigns polarity for GPIO6 output. 0 = GPIO6 pin pulls low when specified output bit is low. 1 = GPIO6 pin pulls low when specified output bit is high.
4	INV5	1	Assigns polarity for GPIO5 output 0 = GPIO5 pin pulls low when specified output bit is low. 1 = GPIO5 pin pulls low when specified output bit is high.
3	INV4	1	Assigns polarity for GPIO4 output. 0 = GPIO4 pin pulls low when specified output bit is low. 1 = GPIO4 pin pulls low when specified output bit is high.
2	INV3	0	Assigns polarity for GPIO3 output. 0 = GPIO3 pin pulls low when specified output bit is low. 1 = GPIO3 pin pulls low when specified output bit is high.
1	INV2	1	Assigns polarity for GPIO2 output. 0 = GPIO2 pin pulls low when specified output bit is low. 1 = GPIO2 pin pulls low when specified output bit is high.
0	INV1	1	Assigns polarity for GPIO1 output. 0 = GPIO1 pin pulls low when specified output bit is low. 1 = GPIO1 pin pulls low when specified output bit is high.

Table 59. MFR_GPO_SEL41 (0xF5) Read and Write

Bit(s)	Name	Default	Operation	
[15:12]	SEL4[3:0]	0101	Selects a GPIO4 output.	
			SEL4[3:0]	**Output**
			0000	Three-state
			0001	GPO4
			0010	CMPOUT
			0011	POWER_GOOD
			0100	FAULT
			0101	IOUT_OC_STATUS
			0110	ADC_SS_DONE
			0111	SHED_LOADS
			1000	OP1_STATUS
			1001	ALERT
			1010	L_ALERT
[11:8]	SEL3[3:0]	1111	Selects a GPIO3 output.	
			SEL3[3:0]	**Output**
			0000	Three-state
			0001	GPO4
			0010	CMPOUT
			0011	POWER_GOOD
			0100	FAULT
			0101	IOUT_OC_STATUS

COMMAND DETAILS

Table 59. MFR_GPO_SEL41 (0xF5) Read and Write (Continued)

Bit(s)	Name	Default	Operation	
			0110	ADC_SS_DONE
			0111	SHED_LOADS
			1000	OP1_STATUS
			1001	ALERT
			1010	L_ALERT
			1111	TEMP
[7:4]	SEL2[3:0]	0100	Selects a GPIO2 output. See the previous SEL4[3:0] rows within this table.	
[3:0]	SEL1[3:0]	0011	Selects a GPIO1 output. See the previous SEL4[3:0] rows within this table.	

Table 60. MFR_GPO_SEL85 (0xF6) Read and Write

Bit(s)	Name	Default	Operation	
[15:12]	SEL8[3:0]	1000	Selects a GPIO8 output. See the previous SEL4[3:0] rows within this table.	
[11:8]	SEL7[3:0]	0010	Selects a GPIO7 output. See the previous SEL4[3:0] rows within this table.	
[7:4]	SEL6[3:0]	0000	Selects a GPIO6 output. See the previous SEL4[3:0] rows within this table.	
[3:0]	SEL5[3:0]	0111	Selects a GPIO5 output.	
			SEL5[3:0]	**Output**
			0000	Three-state
			0001	GPO4
			0010	CMPOUT
			0011	POWER_GOOD
			0100	FAULT
			0101	IOUT_OC_STATUS
			0110	ADC_SS_DONE
			0111	SHED_LOADS
			1000	OP1_STATUS
			1001	ALERT
			1010	L_ALERT
			1111	COMM

Table 61. MFR_GPI_SEL (0xF7) Read and Write

Bit(s)	Name	Default	Operation	
15	Reserved	0	Always returns 0.	
[14:12]	ADC_SS_SEL[2:0]	000	Selects a GPIOx pin as an external trigger for ADC_SS_REQ.	
			ADC_SS_SEL[2:0]	**Input**
			000	GPIO1
			001	GPIO2
			010	GPIO3
			011	GPIO4
			100	GPIO5
			101	GPIO6
			110	GPIO7
			111	GPIO8
11	PGI_EN	0	This bit enables a GPIOx pin to generate a PGI_FAULT (or latched to a 1) if the GPIOx pin input does not match the expected value when the PGI watchdog timer expires.	
[10:8]	PGI_SEL[2:0]	000	Selects a GPIOx pin as a power-good watchdog input. See the previous ADC_SS_SEL[2:0] selection table shown in this table.	
7	RBT_EN	0	This bit enables a GPIOx pin to generate a reboot: turns off the power MOSFETs, waits a programmed delay of 0.5 sec to 68 sec, and then restarts the MOSFETs to power cycle the load. Optionally, chip reset and configuration load may occur during the turn-off period.	

COMMAND DETAILS

Table 61. MFR_GPI_SEL (0xF7) Read and Write (Continued)

Bit(s)	Name	Default	Operation
[6:4]	RBT_SEL[2:0]	000	Selects a GPIOx pin as a reboot trigger input. See the previous ADC_SS_SEL[2:0] selection table shown in this table.
3	Reserved	0	Always returns 0.
[2:0]	CMP_SEL[2:0]	101	Selects a GPIOx pin as an auxiliary comparator input (COMPIN) input. See the previous ADC_SS_SEL[2:0] selection table shown in this table.

This extended version of READ_EIN (0xFA) returns the full contents of the internal energy meter and tick counter of the LTC4287 in a time-coherent sample. The tick counter increments once per 283 µs. If the chip is run continuously, the tick counter rolls over in approximately 14 days.

At the completion of each ADC SENSE+ and SENSE− reading, power is calculated by multiplying the SENSE+ and SENSE− current by the selected voltage (V_{IN} or V_{OUT}). The two 15-bit values (see) are multiplied, and the result shifted left by one bit.

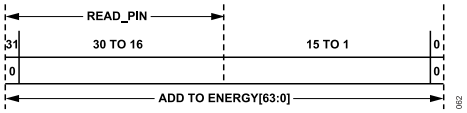


Figure 63. Calculated Power Read Details (READ_PIN) Accumulated by the Energy Meter

Bit 0 and Bit 31 in the 32-bit product are 0s. Bits[31:16] are used for the READ_PIN value. All 32 bits are added to the energy accumulator. See the Chip Tick Timer and ADC Timing section for further details on the input clock speed and energy rollover times.

Table 62. MFR_READ_EIN Format, 12-Byte Block Read

Byte	Contents
0	Energy, Bits[7:0]
1	Energy, Bits[15:8]
2	Energy, Bits[23:16]
3	Energy, Bits[31:24]
4	Energy, Bits[39:32]
5	Energy, Bits[47:40]
6	Energy, Bits[55:48]
7	Energy, Bits[63:56]
8	Tick, Bits[7:0]
9	Tick, Bits[15:8]
10	Tick, Bits[23:16]
11	Tick, Bits[31:24]

Table 63. MFR_READ_BLK (0xFB) Read Only, 16-Byte Block Read

Bytes	Contents
[0:5]	READ_EIN
[6:7]	READ_VIN
[8:9]	READ_VOUT
[10:11]	READ_IOUT
[12:13]	READ_TEMPERATURE1
[14:15]	READ_PIN

Table 64. MFR_ON_OFF_CONFIG (0xFC) Read/Write

Bit(s)	Name	Default	Operation
[15:8]	POWER_OFF_DELAY	00000000	Specifies delay from SHED_LOADS output to FAULT configured GPIOx pin and GATE1 and GATE2 disabled. The delay is 142 µs × POWER_OFF_DELAY.
[7:1]	Reserved	0001110	Fixed value corresponds to PMBus on and off configuration options.
0	NO_DELAY	1	To select no delay from SHED_LOADS to FAULT configured GPIOx pin and GATE1 and GATE2 disabled.

COMMAND DETAILS

Table 65. MFR_REBOOT_CONTROL (0xFD) Read and Write

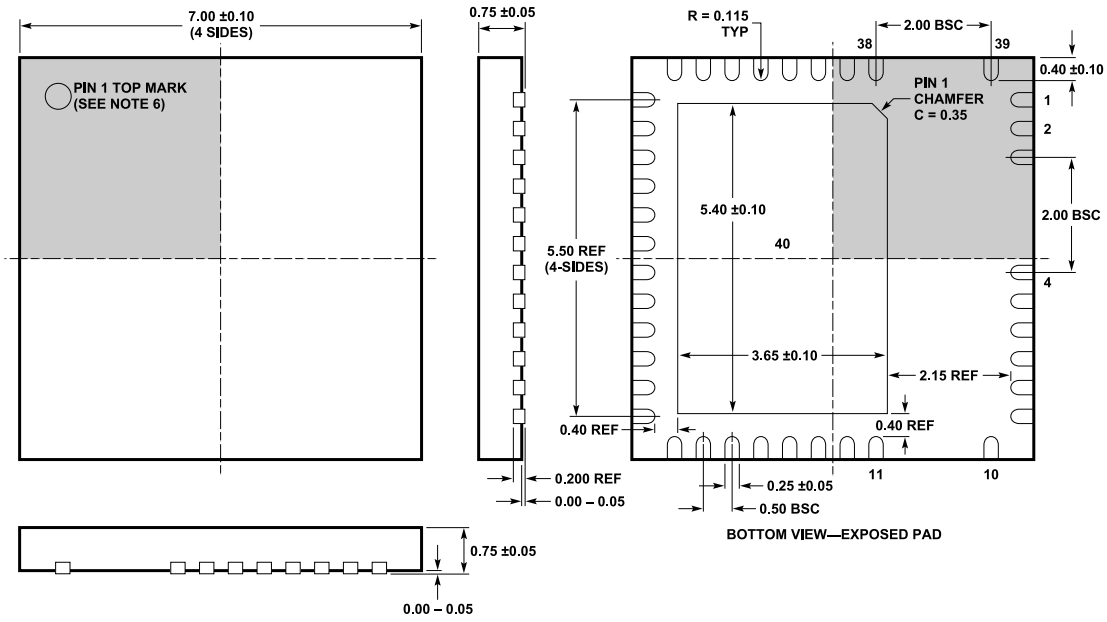
Bit(s)	Name	Default	Operation	
[7:6]	Reserved	00	Always returns 00.	
[5:4]	RBT_INT	00	Selects chip initialization options following the reboot. 00 = chip is reset, configuration data is read from the EEPROM. 01 = chip is reset, but configuration data not read, hardware defaults used instead. 10 = no reset, no configuration read from the EEPROM. FETs are turned off then back on after the auto-reboot turn-on delay, which is detailed in the REBOOT row that follows.	
3	REBOOT	0	Write a 1 to reboot. This bit is not cleared by the reboot operation so software can check that a reboot just took place.	
[2:0]	RBT_EL	000	Configures auto-reboot turn-on delay ($t_{DL(RBT)}$) after the REBOOT bit is set to 1.	
			RBT_DL[2:0]	**Delay**
			000	0.580 sec
			001	1.16 sec
			010	2.32 sec
			011	4.64 sec
			100	9.28 sec
			101	18.6 sec
			110	37.1 sec
			111	74.2 sec

RELATED PARTS

Table 66. Related Parts

Part Number	Description	Comments
LTC4260	Positive, high voltage, hot-swap controller with I^2C-compatible monitoring	8-bit ADC monitoring current and voltages, supplies from 8.5 V to 80 V single MOSFET driver
LTC4238	High voltage, high current, hot-swap controller	Operates from 6.5 V to 80 V, compatible with LTC4287 with COMM/GPIO5 pins dual MOSFET drivers
ADM1272	High voltage, positive, hot-swap controller and digital power monitor with PMBus	Operates from 16 V to 80 V, single MOSFET driver
LTC4282	High current, hot-swap controller with I^2C-compatible monitoring	Operates from 2.9 V to 33 V, 12-bit ADC monitoring current, voltage and power dual MOSFET drivers
LTC4286	High power, positive, hot-swap controller with power monitor via PMBus	Operates from 8.5 V to 80 V, 12-bit ADC monitoring current, voltage, power, energy, temperature

OUTLINE DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

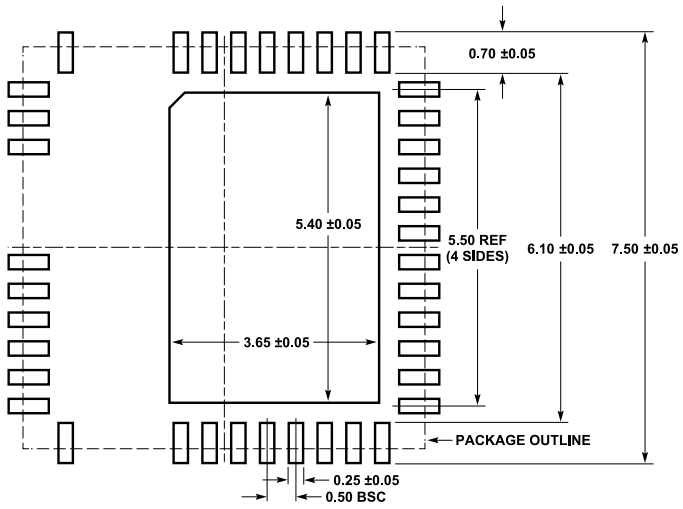


Figure 64. 48(39)-Lead Plastic QFN (7 mm × 7 mm)
(05-08-1792)
Dimensions shown in millimeters

OUTLINE DIMENSIONS

Updated: June 02, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
LTC4287AUK#PBF	−40°C to +125°C	48(39)-Lead Plastic QFN (7mm × 7mm)		05-08-1792
LTC4287AUK#TRPBF	−40°C to +125°C	48(39)-Lead Plastic QFN (7mm × 7mm)	Reel, 2000	05-08-1792

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 67. Evaluation Boards

Model[1]	Description
EVAL-LTC4287-A1Z	Evaluation Board

[1] Z = RoHS-Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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