User's Guide

DAC39RF10EVM Evaluation Module

ABSTRACT

The DAC39RF10EVM is an evaluation board used to evaluate the DAC39RF10, digital-to-analog converters (DAC) from Texas Instruments.The DAC39RF10 is a family of single and dual channel digital-to-analog converter (DAC) with 16-bit resolution. The devices can be used as single channel or dual channel non-interpolation DACs. The device can also be used as interpolating DACs in either direct RF sampling mode or baseband mode. The maximum input data rate is 20.48 GSPS in single channel mode or 10.24 Gsps in dual channel mode or baseband mode. The device can generate signals of up to 10, 7.5, and 5 GHz signal bandwidth (8, 12, and 16-bit input resolution) at carrier frequencies exceeding 8 GHz enabling direct sampling through C-band and into X-band This evaluation board also includes the following important features:

- Transformer-coupled signal output network allowing a single-ended signal output

  with an option to bypass the transformer and use the outputs differentially.
- The LMX1204 clock chip distributes the DAC sampling clock
- The LMK04828, clock generator generates SYSREF and FPGA reference clocks for the high-speed serial interface
- Transformer-coupled clock input network to test the DAC performance with an external low-noise clock source
- High-speed serial data output over a High Pin Count FMC+ interface connector

Note

To improve signal routing quality, serial lane polarity is inverted with respect to the standard FMC VITA-57 signal mapping. Signal mapping and polarity is shown in Table 7-1).

- Device register programming through USB connector and FTDI USB-to-SPI bus translator with option to program from FGPA using SPI through FMC+ connector

DAC39RF10EVM KEY COMPONENTS

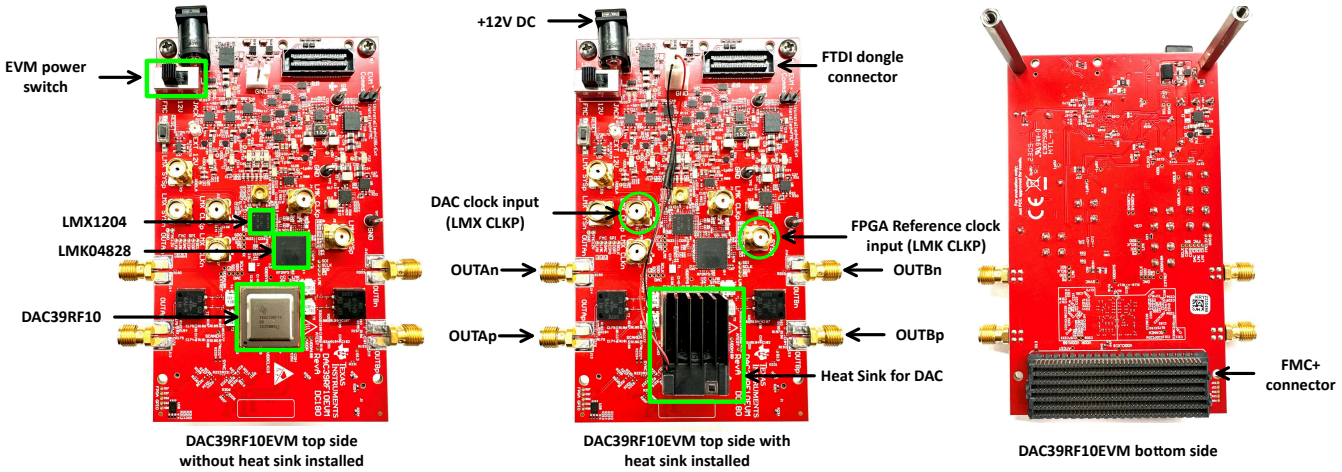


Figure 1-1. EVM Orientation

DAC39RF10EVM can use used with the TSW14J59EVM board(pattern generator board). TSW14J59EVM can quickly and easily interface with the DAC39RF10EVM.

Note

For now only 64b/66b encoding modes from serdes data rate from 6Gbps to 12.8Gbps are supported by the TSW14J59EVM. The support for 8b/10b modes and lower serdes rate will be added to future release of HSDCpro software.

The High-Speed Data Converter Pro (HSDC Pro) software is used to communicate with the TSW14J59EVM and is used to generates the data pattern for DAC39RF10.

The TSW14J59EVM takes the generated data pattern, encodes the data, stores the data in memory, and then sends to DAC39RF10EVM through the the high-speed serial data link(JESD interface).

With proper hardware selection in the HSDC Pro software, the TSW14J59 board is automatically configured to support a wide range of operating speeds of the DAC39RF10EVM, but the TSW14J59EVM board may not cover the full operating range of the DAC device.

Table of Contents

List of Figures

List of Tables

1 Trademarks

Microsoft® and Windows® are registered trademarks of Microsoft Corporation.
Rohde & Schwarz® is a registered trademark of Rohde & Schwarz GmbH & Co.
All trademarks are the property of their respective owners.

2 Required Equipment

The following equipment and documents are included in the DAC39RF10EVM kit:

- Evaluation board (EVM)
- Mini-USB cable
- Power cable
- Type C USB cable
- FTDI dongle to program the DAC EVM with FTDI.

The following equipments are **not** included in the DAC39RF10EVM kit, but are required for evaluation of this product:

- TSW14J59EVM data capture board and related items
- High-Speed Data Converter Pro software.
- PC computer running Microsoft® Windows® 10
- Low-noise signal generator for DEVCLK (Sampling clock) . TI recommends the following generators:
  - Rohde & Schwarz® SMA100B
- Signal-path cables, SMA or BNC (or both SMA and BNC)

By default, the DAC39RF10EVM uses LMX1204 clocking chip to distribute the external clock signal to DAC39RF10 and also to LMK04828 to generate necessary clocks needed for the TSW14J59EVM. A few board modifications enables user to test the DAC39RF10 with other clocking options. The other clocking option are discussed in the Appendix section of the uses guide.

3 Setup Procedure

This section describes how to setup the DAC and TSW14J59 EVMs on the bench with the proper equipment to evaluate the performance of the DAC device.

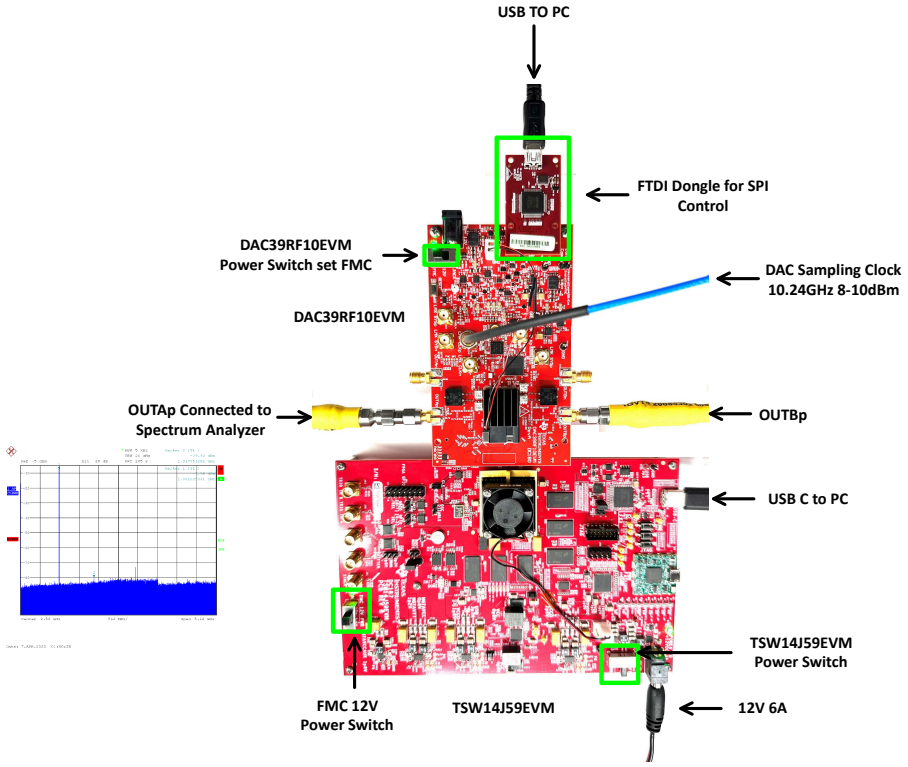


Figure 3-1. DAC39RF10EVM Test Setup

Note

The HSDC Pro software must be installed before connecting the TSW14J59EVM to the PC for the first time.

3.1 Installing the High Speed Data Converter (HSDC) Pro Software

1. Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.

3.2 Installing the DAC39RF10EVM Configuration GUI Software

1. If installing the DAC gui for the first time, please download and install the FTDI drivers from FTDI website.

   Restarting the PC may be required after installing the driver.
2. Download the Configuration GUI software from the EVM tool folder at DAC39RF10EVM GUI.
3. Extract files from the .zip file.
4. Run the executable file (`DAC39RF10.exe`).

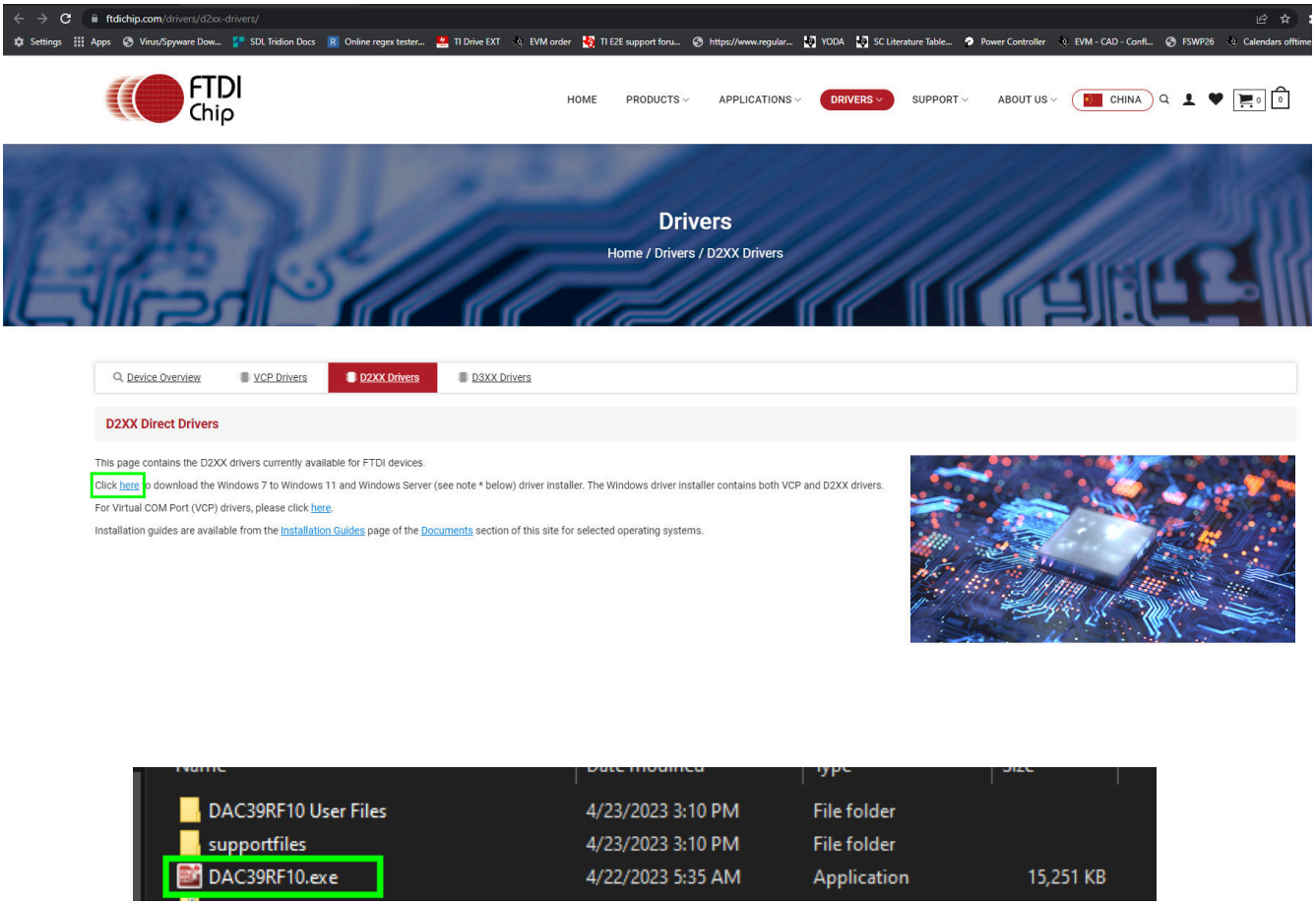


Figure 3-2. FTDI website to download and install the driver.

3.3 Connect the DAC39RF10EVM and TSW14J59EVM

1. With the power off, connect the DAC39RF10EVM to the TSW14J59EVM through the FMC+ connector as shown in DAC39RF10EVM Test Setup. Make sure that the standoffs provide the proper height for robust connector connections.

3.4 Connect the Power Supplies to the Boards (Power Off)

1. Confirm the power switch on the TSW14J59EVM is in off position. Connect the power cable to a 12-V DC (minimum 6A) power supply. Make sure the proper supply polarity by confirming the outer surface of the barrel connector is GND and the inner portion of the connector is 12 V. Connect the power cable to the TSW14J59EVM power connector.
2. DAC39RF10EVM can be powered with 12-V DC(minimum 2 A) though the connector jack(J1) on the DAC39RF10EVM or it can be powered from the TSW14J59EVM via FMC+ connector. There is a switch(SW1) which can be used to select power from the barrel jack on the DAC EVM or from TSW14J59EVM through FMC+ connector. Confirm that the power switch for the DAC39RF10EVM's power supply is set to the opposite position(jack) from which it should be drawing power. If using barrel jack option connect the power cable to a 12-V DC (minimum 2 A) power supply. Make sure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12 V. Connect the power cable to the EVM power connector. The Table can used as a reference to power the DAC EVM.

Table 3-1. Powering the DAC39RF10EVM

DAC39RF10 Powered from	DAC39RF10 Power Switch position	TSW14J59EVM FMC switch position	Power supply needed
TSW14J59EVM via FMC+ connector	**FMC(Default option)**	**ON**	**12V 6A for TSW14J59EVM**
External Supply with jack on DAC39RF10EVM	JACK	OFF	12V 5A for TSW14J59 and 12V 2A for DAC39RF10EVM

CAUTION

Make sure the power connections to the EVMs are the correct polarity. Failure to do so may result in immediate damage. Leave the power switches in the off position until directed later.

3.5 Connect the Spectrum Analyzer to the EVM

Connect a spectrum analyzer to the Aoutp (J13) SMA connector of the DAC39RF10EVM .

When LMX->DACCLK | LMX/LMK->FPGA Clocking option is Used (Default)

1. Connect a signal generator to the LMX CLKp input of the EVM. This signal generator must be a low-noise signal generator. Configure the signal generator for the desired clock frequency in the range of 0.8 to 10.24 GHz (for this example 10.24 GHz is used). For best performance when using an RF signal generator, the power input to the LMX CLKp SMA connector must be 8-10 dBm (2 Vpp into 50 Ω).
2. This step is only need if third clocking option(EXT-> DACLK | LMK->FPGA) is used otherwise skip to next step. Connect a signal generator to the LMK CLKp input of the EVM at SMA (J5). This signal is used to generate the necessary FPGA clock signal. Configure the signal generator for the desired (160 MHz) clock frequency. Set the output power to approximately 5–7 dBm.

Note

a. The FPGA REF clock frequency can be obtained from the DAC39RF10EVM GUI. Once the DAC39RF10EVM GUI is configured to the desired JMODE mode and clock rate. The Reference Clock frequency required by the EVM is displayed on first page of the GUI shown in Configuration of DAC39RF10EVM GUI
b. Make sure that the DEVCLK and Reference clock sources are frequency-locked using a common 10-MHz reference to for functionality.
c. Do not turn on the RF output of any signal generator at this time.

3.6 Turn On the TSW14J59EVM Power and Connect to the PC

1. Turn on the power switch to the TSW14J59EVM.
2. Connect a USB-C cable from the PC to the TSW14J59EVM.
3. If this is the first time connecting the TSW14J59EVM to the PC, follow the on-screen instructions to automatically install the device drivers. See the TSW14J59EVM user's guide for specific instructions.

3.7 Turn On the DAC39RF10EVM Power Supplies and Connect to the PC

1. The default option uses the power from FMC+ connector on TSW14J59EVM. For this option, the FMC power switch on TSW14J59EVM should be set to on postion and power switch on the DAC39RF10EVM shoud be set to FMC(defalut). If external power supply is used to power the DAC EVM. Then turn on the 12-V power supply connected to the barrel jack on the DAC EVM and set the power switch postion on DAC39RF10EVM to JACK postion.

   The green LED(D3) on DAC EVM should turn on, indicating DAC EVM is getting power.
2. Connect the DAC EVM to the PC with the mini-USB cable via the FTDI DONGLE provide with the EVM.

3.8 Turn On the Signal Generator RF Outputs

Turn on the RF signal output of the signal generator connected to LMX CLKp. If external clocking option is used, turn on the RF signal outputs connected to LMK CLKp(FPGA reference clock).

3.9 Launch the DAC39RF10EVM GUI and Program the DAC EVM

The DAC39RF10EVM configuration GUI is installed separately from the HSDC Pro installation and is a stand-alone GUI.

Note

The max clock rate supported by DAC39RF10EVM is 10240 MHz

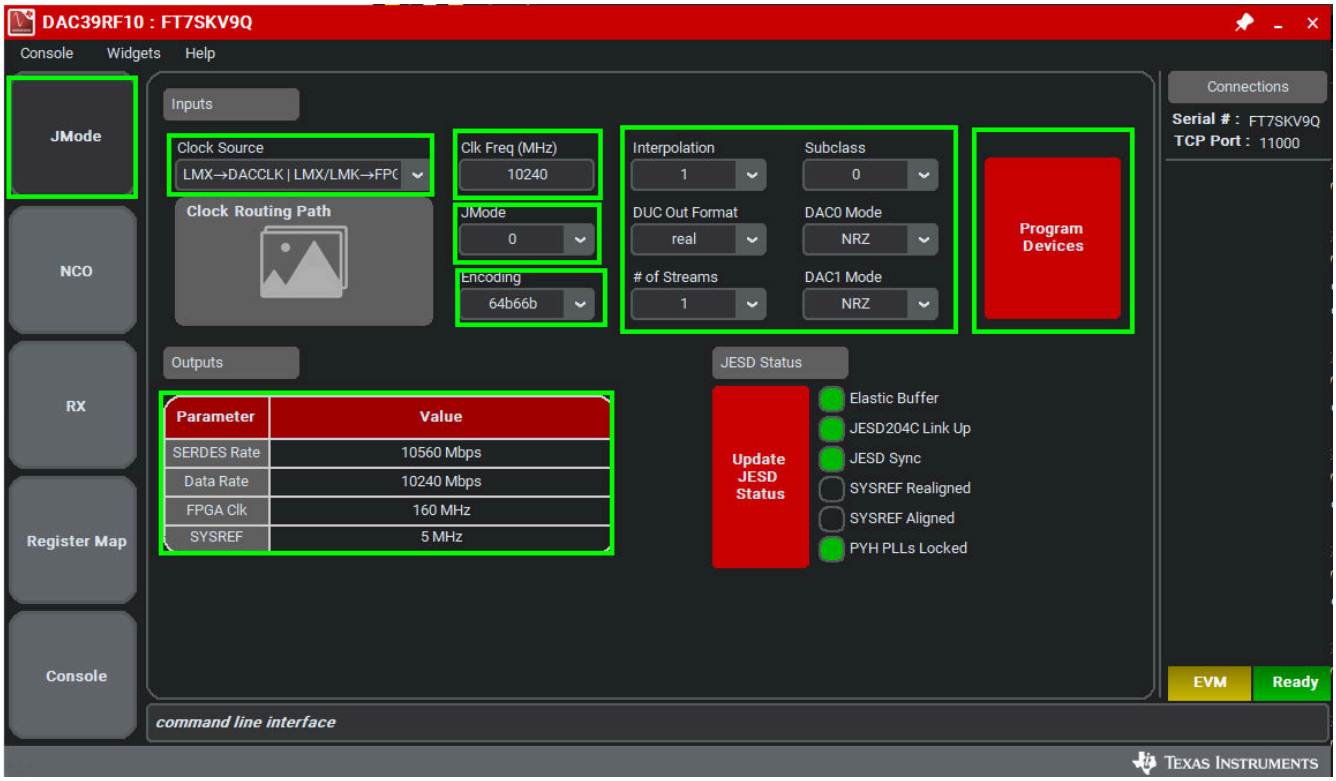


Figure 3-3. Configuration of DAC39RF10EVM GUI

Figure 3-3 and Figure 3-4 show the GUI opened to the *JMODE* tab and *NCO* tab respectively. Tabs at the left of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has three configurable devices, namely the DAC39RF10, LMX1204 and LMK04828. The register map for each device is provided in the device data sheet (DAC39RF10, LMK04828B, and LMX1204, respectively).

1. Lauch the DAC39RF10EVM GUI.
2. Select the LMX->DACCLK | LMX/LMK->FPGA as the clock source.
3. Enter Clk Freq 10240 MHz.
4. Select JMODE0 for JMODE option.
5. Select 64b66b for Encoding option.
6. The other option can be left to default settings.
7. Click *Program Devices* (Note: This action overwrites any previous device register settings.)

3.10 Programming the NCO

The following steps are only needed when DAC is programmed to JMODE 1 to 7. For JMODE0 the NCO configuration can be skipped to the section HSDCpro section. For JMODEs 1 to 7 when number of streams M is greater than or equal to 2 and interpolation factor is also set to greater than or equal to 2, the NCO(numerically controlled oscillator) can be used to mix I/Q baseband signal to generate a higher output frequency signal from the output of the DAC.

Table 3-2 describes the relationship of interpolation factor and number of streams to number of DUCs (Digital up converter) that can be used.

Table 3-2. Supported Interpolation Factors vs Number of DUCs Enabled

Number of Streams	Interpolation Factors	DUCs Enabled
2	2-256x	DUC0
4	4-256x	DUC0, DUC1
6	8-256x	DUC0, DUC1, DUC2
8	8-256x	DUC0, DUC1, DUC2, DUC3

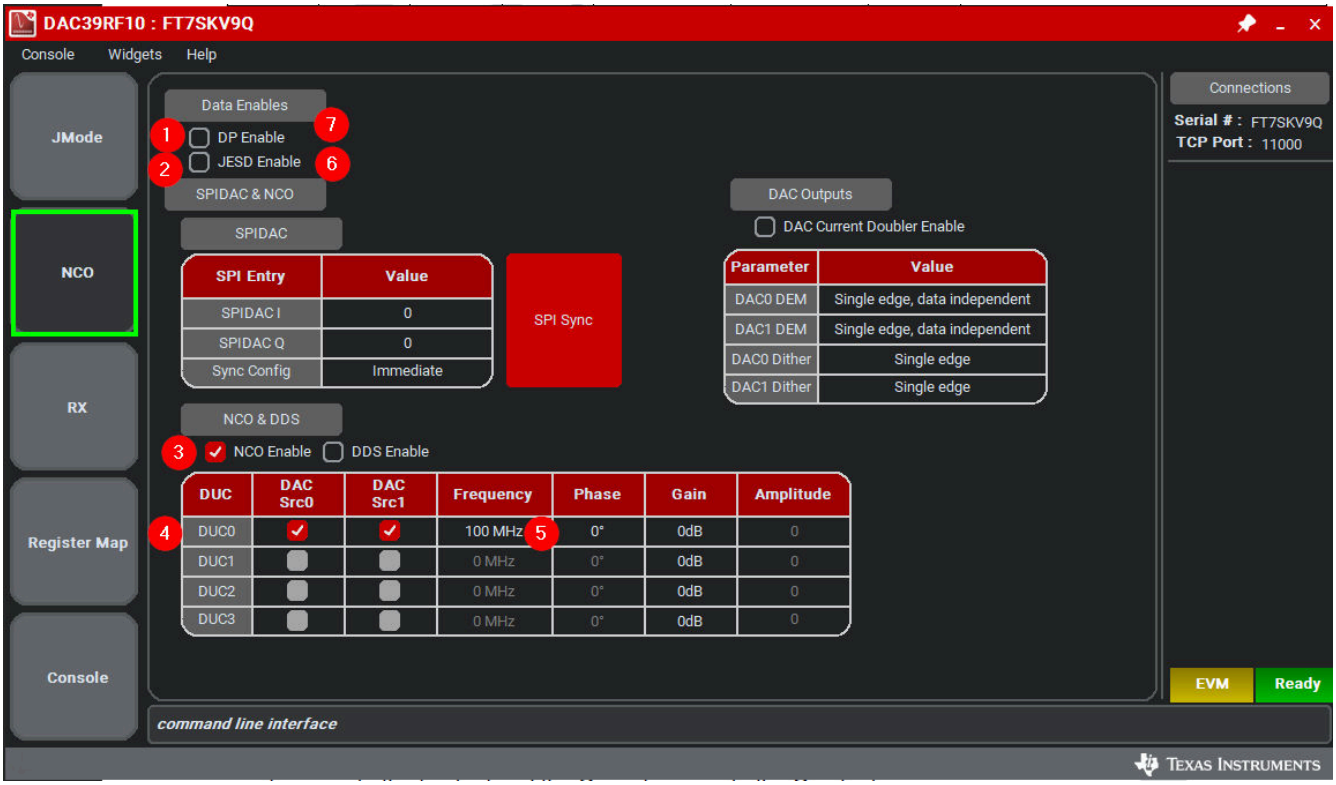


Figure 3-4. NCO TAB CONTROLS

With the EVM gui open on the PC, navigate to NCO tab on upper left side of the GUI.

1. To set the NCO uncheck the DP Enable
2. Unchek the JESD Enable
3. Check the NCO Enable
4. In this example, JMODE was set to 1 and number of stream is set to 2. The interpolation factor is set to 2. In Supported Interpolation Factors vs Number of DUCs Enabled only DUC0 can be used, and other DUCs have been grayed out. The data from DUC0 is routed to DAC0 and DAC1
5. Enter the Frequency in MHz
6. Check the JESD Enable
7. Check the DP Enable.

3.10.1 SPIDAC(NCO only) Operation

The DAC can also be configured in SPIDAC Operation (NCO only mode). In NCO only mode, data streamed from JESD is ignored and DUCs inputs are driven by SPIDAC I and SPIDAC Q. This mode can be enabled when JESD Enable is set to 0, interpolaton factor is greater than or equal to 2 and DP Enable is set to 1, the DAC is configured in NCO only mode. Following Table 3-2 , the correct combination of number of streams and interpolation factor should be selected to enable the desired number of DUCs and setting the desired outputs from respective DACs.

In the Example, all the four DUCs are enabled. DUC0 and DUC1 are routed to DAC0 and DUC2 and DUC3 are routed to DAC1. If more than one DUC is routed per DAC, the DUC data into the DAC must be attenuated to prevent the DAC from saturating.

The NCO only mode can be configured through the GUI by following steps.

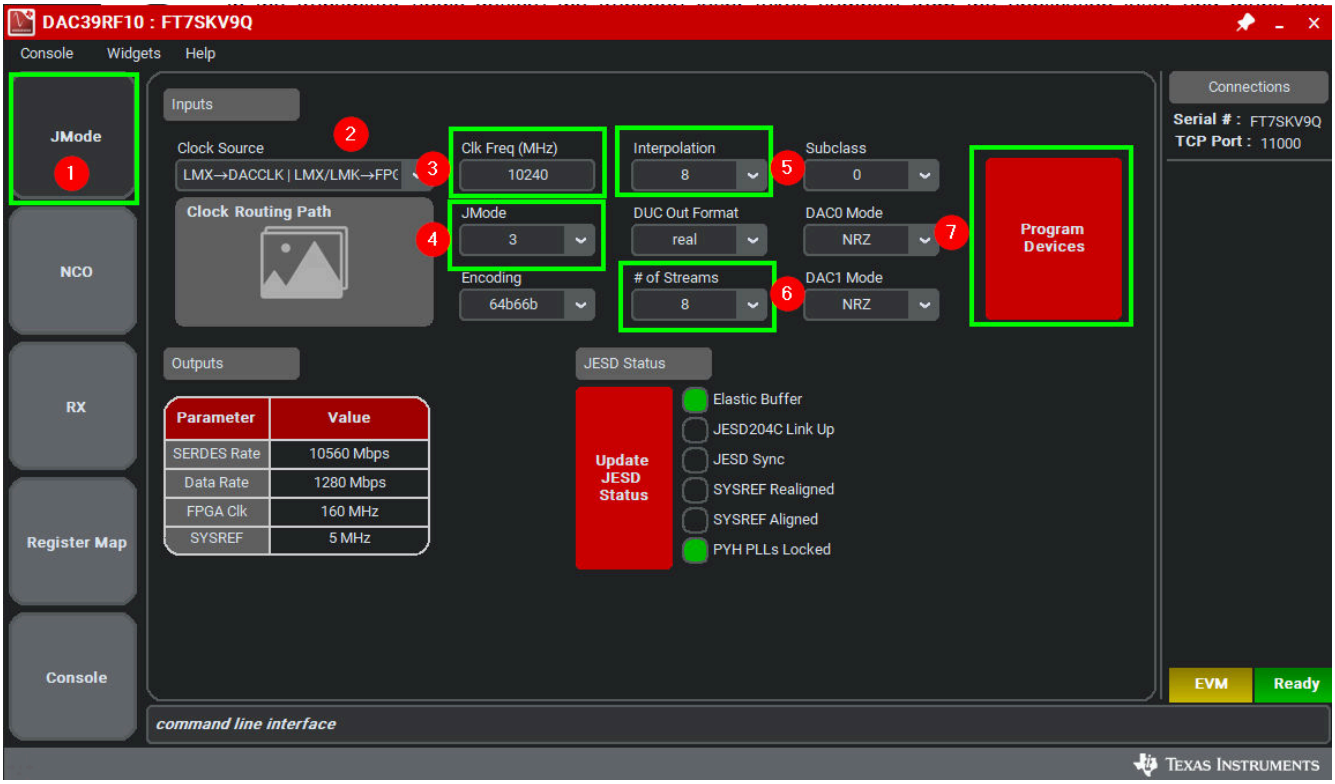


Figure 3-5. NCO only JMODE settings for GUI.

1. Launch the DAC39RF10EVM GUI.
2. Select the LMX->DACCLK | LMX/LMK->FPGA as the clock source.
3. Enter Clk Freq 10240 MHz.
4. Select JMODE3 for JMODE option.
5. Select 8 for Interpolation
6. Select 8 for number of streams
7. Click the button Program Devices.
8. On the NCO tab uncheck the DP Enable
9. Uncheck the JESD Enable
10. For SPIDAC I enter the value of 32767 for full scale output power.
11. Check the NCO Enable
12. Select the correct DUC routing(DUC0 and DUC1 routed to DAC0 and DUC2 and DUC3 routed to DAC1). Since two DUC are routed to single DAC The gain value should be adjusted to -6dB to prevent the DAC from saturating.
13. Enter the desired frequency
14. Check the DP Enable.
15. The DAC should have ouputs on both channels.

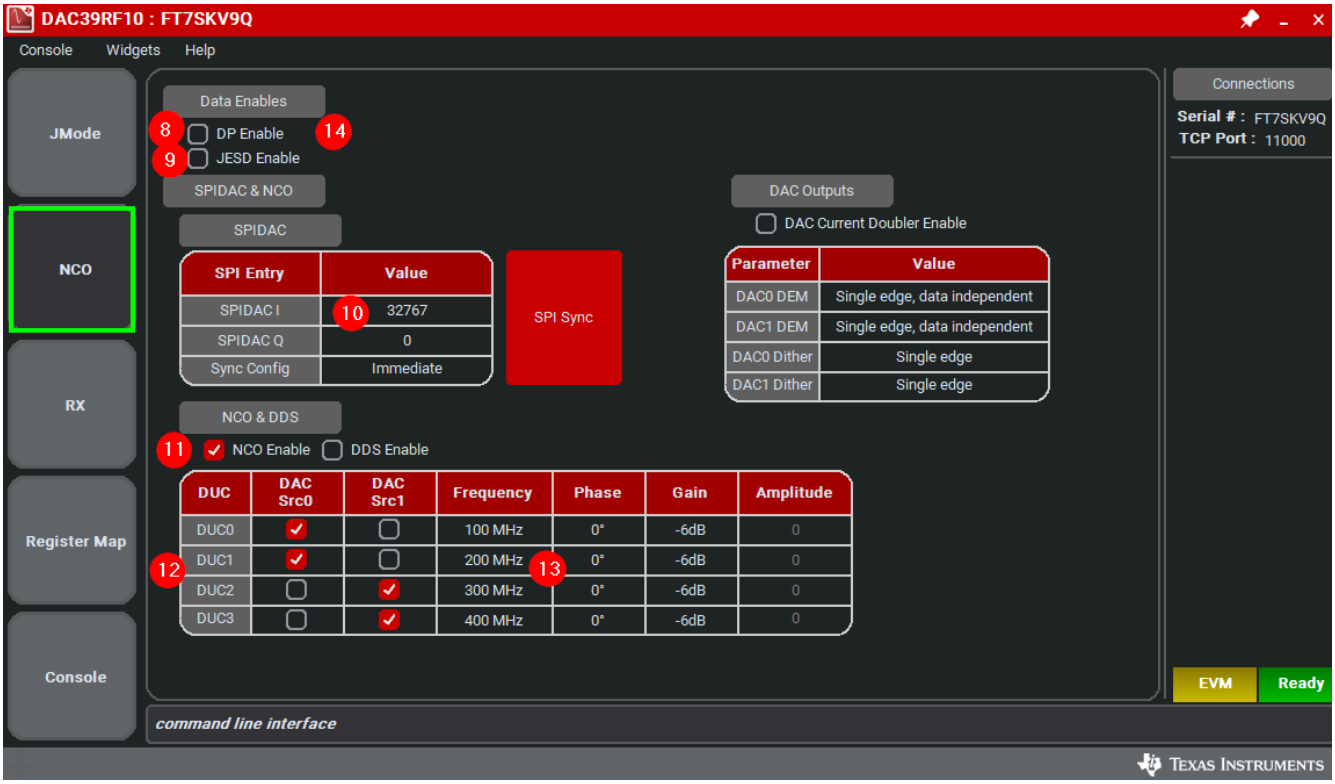


Figure 3-6. NCO only mode GUI settings

Similar to SPI DAC mode, the DDS mode can be used as a lower power option. To enable DDS mode, the following steps are used.

1. Follow steps 1-9.
2. Skip step 10.
3. For 11 step select DDS Enable.
4. Follow step 12 according to requirements.
5. Follow step 13.
6. For Amplitude(Two DUCs routed to single DAC, amplitude reduced by 6 dB from max value of 32767 to 16384) program 16384.
7. Follow step 14.
8. The DAC should have outputs on both channels.

3.11 Launch the HSDCpro Software and Load the FPGA Image to the TSW14J59EVM

1. Launch the HSDCpro 5.303 or later software.
2. Click *OK* to confirm the serial number of the TSW14J59EVM device. If multiple TSWxxxxx boards are connected, select the model and serial number for the one connected to the DAC39RF10EVM.
3. For Device select DAC from drop down menu.

> If the pop up says No Firmware. Please select a device to load firmware into the board click **OK** proceed to next step.

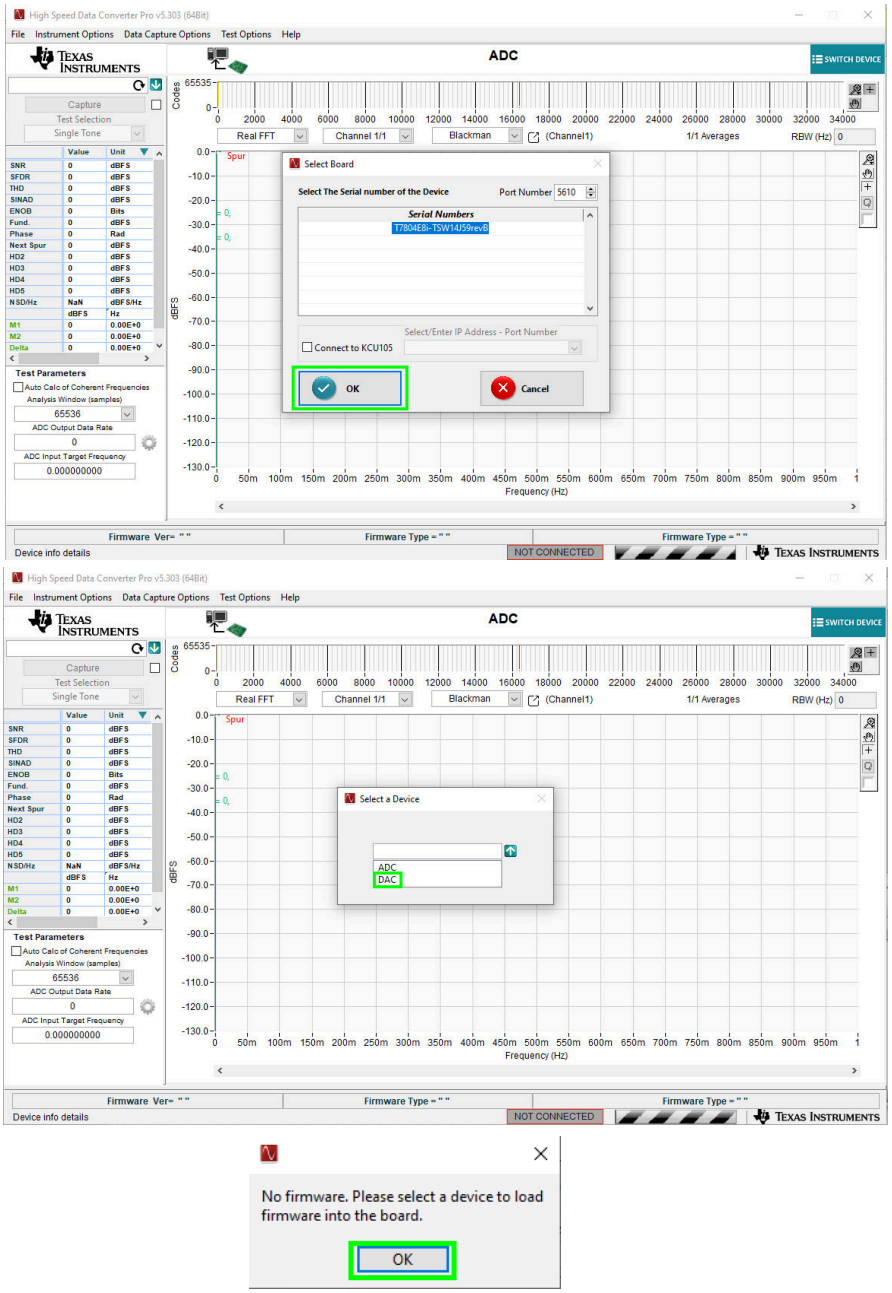


Figure 3-7. Launching HSDCpro and Setup

4. Select the DAC39RF1x_JMODE0 device from the DAC select drop-down in the top left corner.
5. When prompted, click *Yes* to update the firmware(wait for Firmware to download).

Note

If the user configures the EVM with options other than the default register values, different instructions may be required for selecting the device in HSDC Pro. See Section 7 for more details.

Figure 3-8. HSDCpro Setup

6. Enter the Data Rate as "10.24G" or the desired input data rate. The Data rate value can be referenced from the DAC39RF10EVM GUI. It is displayed on output parameter as shown in Configuration of DAC39RF10EVM GUI.
7. For DAC Option dropdown select the "Offset Bin" option.(The DAC39RF10EVM gui always defaults to offset binary).
8. Navigate to lower left side of the HSDCpro GUI to I/Q Multitone Generator section. For # of tones enter 1, for Tone Center enter 1G(1 GHz or desired frequency), # Samples can be left 65536.
9. Tone selection should be "Real", since this is JMODE0 , the DUC/ NCO is bypassed. If other JMODE was configured, such that DUC/NCO was used the Tone selection should be "Complex".
10. Click Create Tones button and then click Send in upper left side of HSDCpro GUI. If a pop appear mentioning the SERDES RATE click OK. The DAC should be sending the programmed frequency to the outputs.

Figure 3-9. HSDCpro Generating the Tone and Sending it to the DAC.

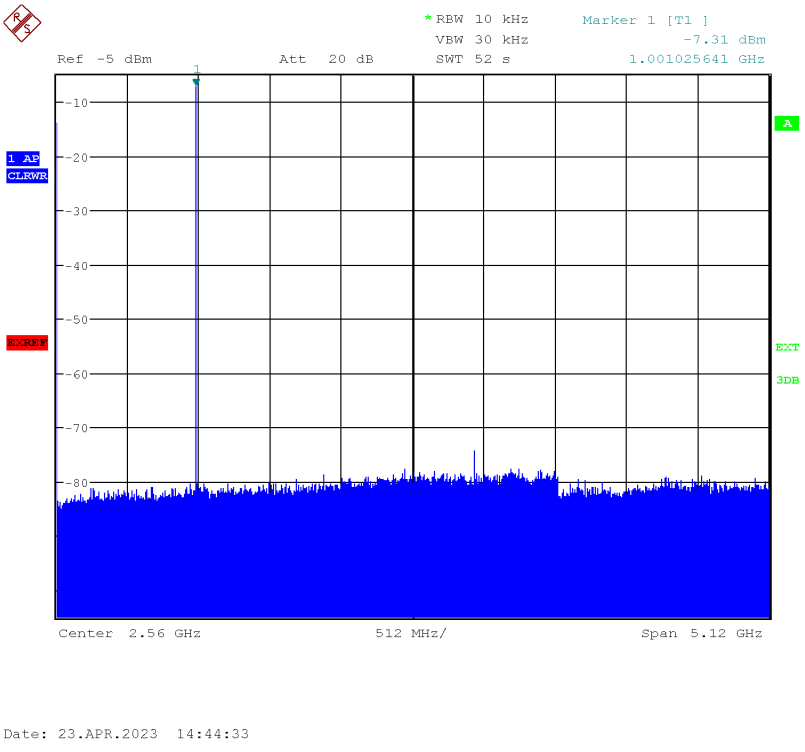


Figure 3-10. DAC Output Displayed on Spectrum Analyzer

4 Device Configuration

The DAC device is programmable through the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the FTDI dongle. A GUI is provided to write instructions on the bus and program the registers of the DAC device.

For more information about the registers in the ADC device, see the DAC39RF10 device data sheet.

4.1 Supported JESD204C Device Features

The DAC device supports some configuration of the JESD204C interface. Due to limitations in the TSW14J59EVM firmware, all JESD204C link features of the DAC device are not supported. Table 4-1 lists the supported and non-supported features.

Table 4-1. Supported and Non-Supported Features of the JESD204C Device

JESD204C Feature	Supported by DAC Device	Supported by TSW14J59EVM
Number of lanes per link (L)	L = 1, 2, 3, 4, 6, 8,12,16(1)	L = 1, 2, 3, 4, 6, 8,12,16 supported
Scrambling	Supported	Supported
Test patterns	PRBS7, PRBS9, PRBS15, PRBS31	Not Supported
Speed	Lane rates from 0.75 to 12.8 Gbps	Lane rates from 2 to 17.16 Gbps $f_{(SAMPLE)}$ parameter must be properly set in HSDC Pro GUI.

(1) Dependent on bypass or decimation mode and output rate selection. Always disable the JESD204 block before changing any of the JESD204C settings. Once the settings are changed, re-enable the JESD204 block.

4.2 Tab Organization

Control of the DAC device features are available in the JMode, NCO and RX tabs.

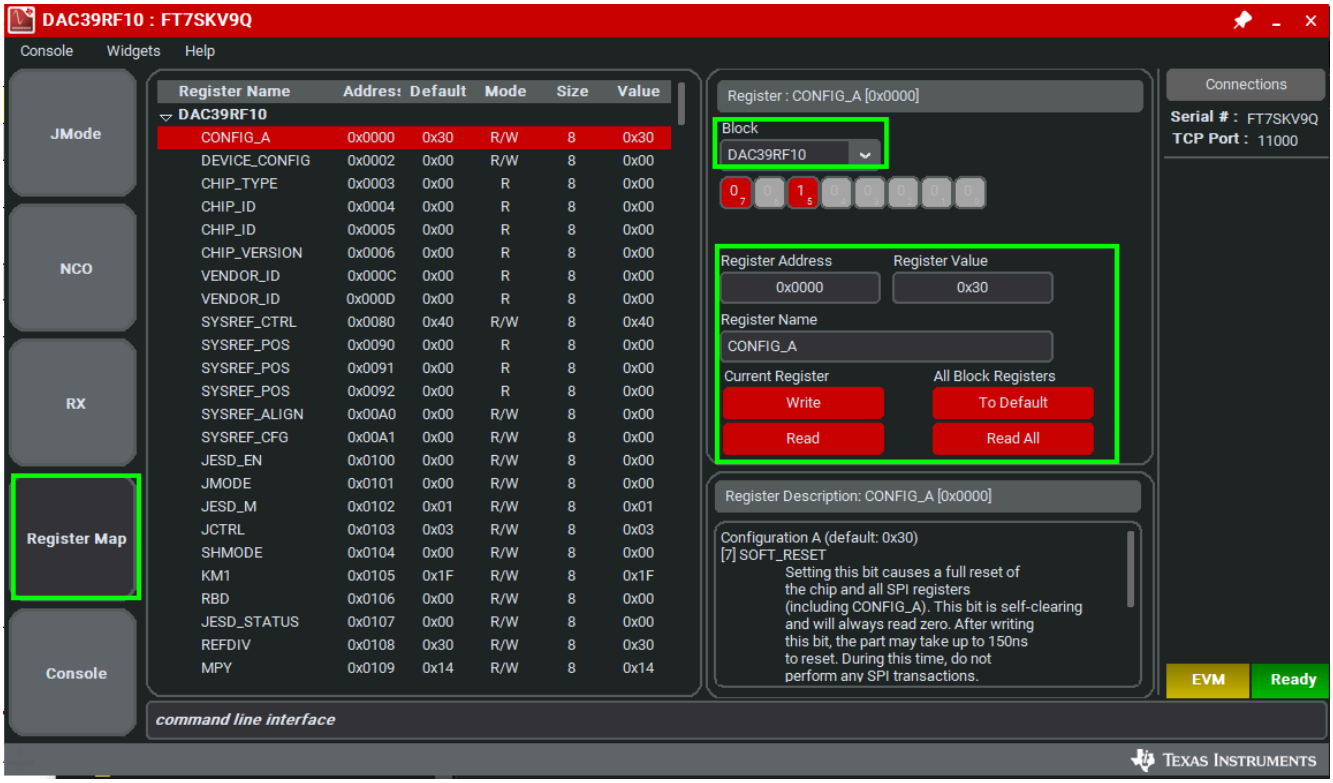
4.3 Register Map and Console Control

The *Register Map* tab, illustrated in Figure 4-1, allows configuration of the devices at the bit-field level. At any time, the controls in Table 4-2 can be used to configure or read from the device.

The Console tab logs all the SPI reads and writes which are performed when various devices are programmed on the DAC EVM . The config files can saved and loaded from the console tab.

Table 4-2. Register Map and Console Controls

Control	Description
Register map summary	Displays the devices on the EVM, registers for those devices, and the states of the registers • Clicking on a register field allows individual bit manipulation in the register data cluster • The value column shows the value of the register at the time the GUI was last updated • The LR column shows the value of the register at the time the register was last read
Write register button	Write to the register highlighted in the register map summary with the value in the *Write Data* field
Write all button	Update all registers shown in the register map summary with the values shown in the *Register Map* summary
Read register button	Read from the register highlighted in the *Register Map* summary and display the results in the *Read Data* field Can be used to re-synchronize the GUI with the state of the hardware
Read-all button	Read from all registers in the *Register Map* summary and display the current state of the hardware
Load Configuration button	Load a configuration file from disk and register address/data values in the file
Save Configuration button	Save a configuration file to disk that contains the current state of the configuration registers
Register Data cluster	Manipulate individual accessible bits of the register highlighted in the register map summary
Individual register cluster with read or write register buttons	Perform a generic read or write command to the device shown in the *Block* drop-down box using the address and write data information



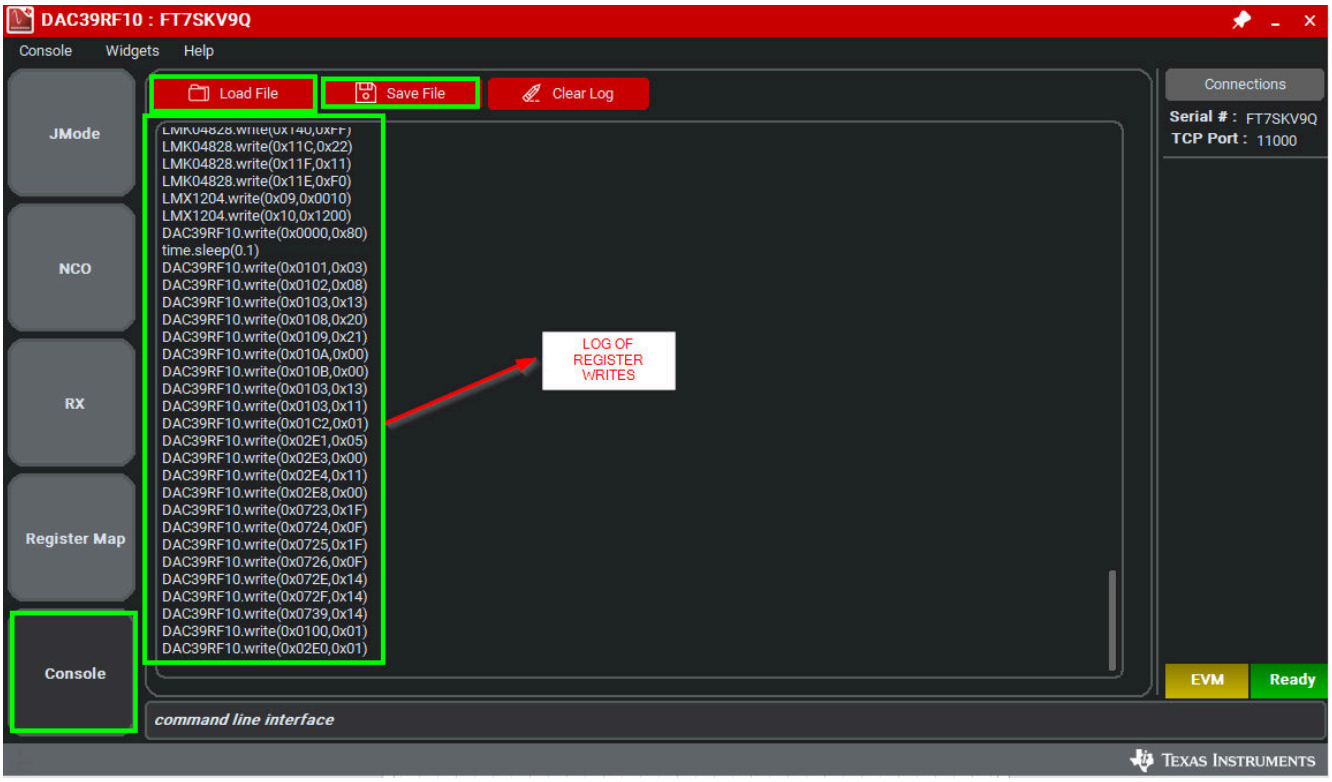


Figure 4-1. Register Map Tab

5 Troubleshooting the DAC39RF10EVM

Table 5-1 lists some troubleshooting procedures.

Table 5-1. Troubleshooting

Issue	Troubleshoot
General problems	• Verify the test setup shown in Figure 3-1, and repeat the setup procedure as described in this document. • Check power supply to EVM and TSW14J59EVM. Verify that the power switch is in the on position. • Check signal and clock connections to EVM. • Visually check the top and bottom sides of the board to verify that nothing looks discolored or damaged. • Make sure the board-to-board FMC+ connection is secure. • Try pressing the CPU_RESET button on the TSW14J59EVM. Also try clicking *Instrument Options* → *Reset Board* after changing the DAC configuration. • Try power-cycling the external power supply to the EVM, and reprogram the DAC, LMX and LMK devices.
TSW14J59 LEDs are not correct	• Verify the settings of the configuration switches on the TSW14J59EVM. • Verify that the clock going to the CLK input is connected and the appropriate LEDs are blinking. • Verify that the DAC device internal registers are configured properly. • If LEDs are not blinking, reprogram the DAC EVM devices. • Try pressing the CPU_RESET button on the TSW14J59EVM. • Try clicking SEND button in HSDC Pro again.
Configuration GUI is not working properly	• Verify that the USB cable is plugged into the EVM and the PC. • Check the computer device manager and verify that a *USB serial device* is recognized when the EVM is connected to the PC. • Verify that the yellow EVM *Status* LED light in the lower right corner of the GUI is lit. If it is not lit, try restarting the GUI and reconfiguring the devices.
Configuration GUI is not able to connect to the EVM	• Use the free FT_PROG software from FTDI chip and verify that the onboard FTDI chip is programmed with the product description *ADC12DJxx00RF* .
DAC output looks incorrect,distorted or there is no output. .	• Verify that the TSW14J59EVM is properly connected to the PC with a USB-C cable and that the board serial number is properly identified by the HSDC software. • Check that the proper DAC device mode is selected. The mode should match in HSDC Pro and the DAC GUI. • Check that the configuration parameters are properly configured. • Select *Instrument Options* → *Download Firmware* and download 'TSW14J59REVB_DAC_64B66B_FIRMWARE.bit'. Try to send again.
Output power looks low	• Check that the spectrum analyzer is set to proper settings. • SMA connector is properly connect to the DAC output and Spectrum analyzer.

6 References

This section provides references to technical documents and user's guides.

6.1 Technical Reference Documents

- DAC39RF10 device data sheet
- TSW14J59EVM user’s guide
- High-Speed Data Converter Pro GUI User's Guide, also available in the help menu of the software
- LMK04828 data sheet
- LMX1204 data sheet
- FTDI USB to Serial Driver Installation Manual (www.ftdichip.com/Support/Documents/InstallGuides.htm)

6.2 TSW14J59EVM Operation

Refer to the TSW14J59EVM user guide for configuration and status information.

7 Appendix

This appendix provides settings for optional ADC device configuration in HSDC Pro.

7.1 Customizing the EVM for Optional Clocking Support

The DAC39RF10EVM can be clocked using 3 different methods: LMX->DACCLK | LMX/LMK-> FPGA option, EXT->DACCLK | LMX/LMK-> FPGA option and EXT->DACCLK | LMK-> FPGA option.

7.1.1 LMX->DACCLK | LMX/LMK-> FPGA option (Default)

By default, the EVM is configured to use LMX->DACCLK | LMX/LMK->FPGA clock option. The user provide a single high freqeuncy(8-10dBm) signal to an SMA labled LMX CLKp. This signal is routed to LMX1204 which generates the buffered DACCLK signal, low freqeuncy DAC SYSERF signal, FPGA reference clocks and FPGA SYSREF signal. The FPGA reference clocks and FPGA SYSREF signal are feed into the CLKIN1 and CLKIN0 of LMK04828. The LMK04828 and is used in clock distribution mode and provides several copies/divided down version of FPGA reference clock and FPGA SYSREF signal.

The EVM can be configured to use LMX->DACCLK | LMX/LMK->FPGA clock option with the following steps:

1. Modify the hardware:
   a. Remove C136 and C139, populate C141 and C142.
   b. Remove C134 and C135, populate C138 and C140
   c. Remove C75 and C76, populate C73 and C74

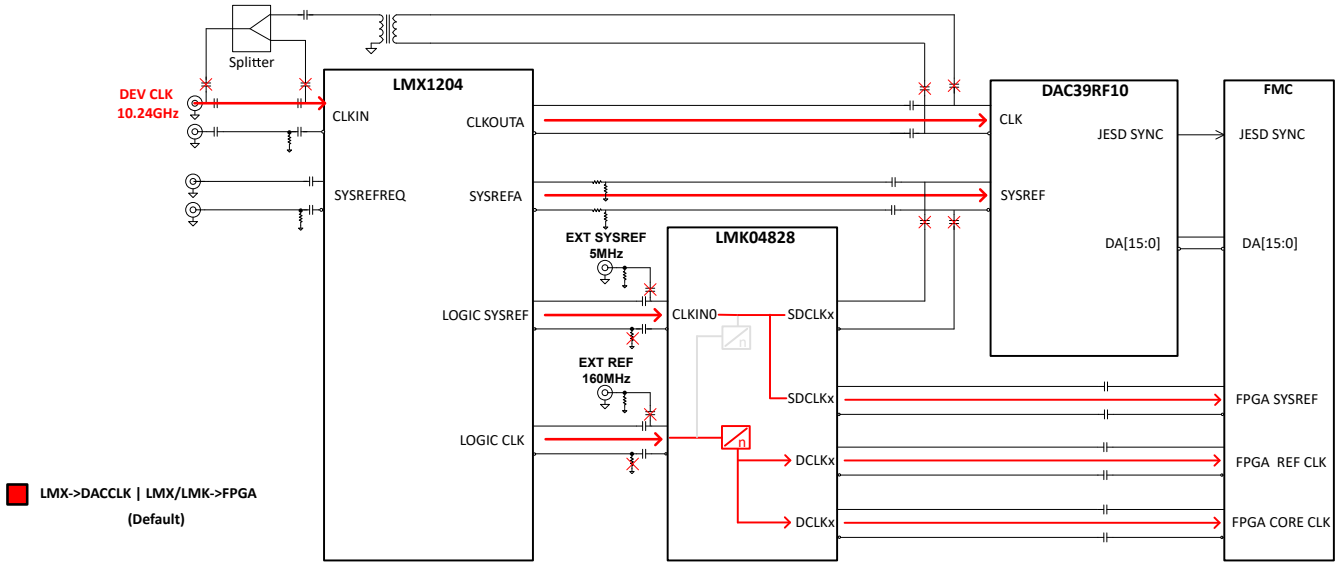


Figure 7-1. LMX->DACCLK | LMX/LMK->FPGA Clocking System Block Diagram

7.1.2 EXT->DACCLK | LMX/LMK-> FPGA Clocking Option

The DAC39RF10EVM can be configured to use EXT->DACCLK | LMX/LMK-> FPGA Clocking option. Similar to above use case The user provide a single high frequency (10-15 dBm) signal to an SMA labeled LMX CLKp. This signal is routed though the splitter to Balun and LMX1204. The Balun converts the single ended signal into differential and is used to clock the DAC. The second output from the splitter is used by LMX1204 which generates the low frequency DAC SYSERF signal, FPGA reference clocks and FPGA SYSREF signal. The FPGA reference clocks and FPGA SYSREF signal are feed into the CLKIN1 and CLKIN0 of LMK04828. The LMK04828 and is used in clock distribution mode and provides several copies/divided down version of FPGA reference clock and FPGA SYSREF signal. Figure 7-2 shows the block diagram of clocking option:

The EVM can be configured to use onboard clocking option with the following steps:

- Remove C141 and C142, populate C136 and C139
- Remove C138 and C140, populate C134 and C135
- Remove C75 and C76, populate C73 and C74

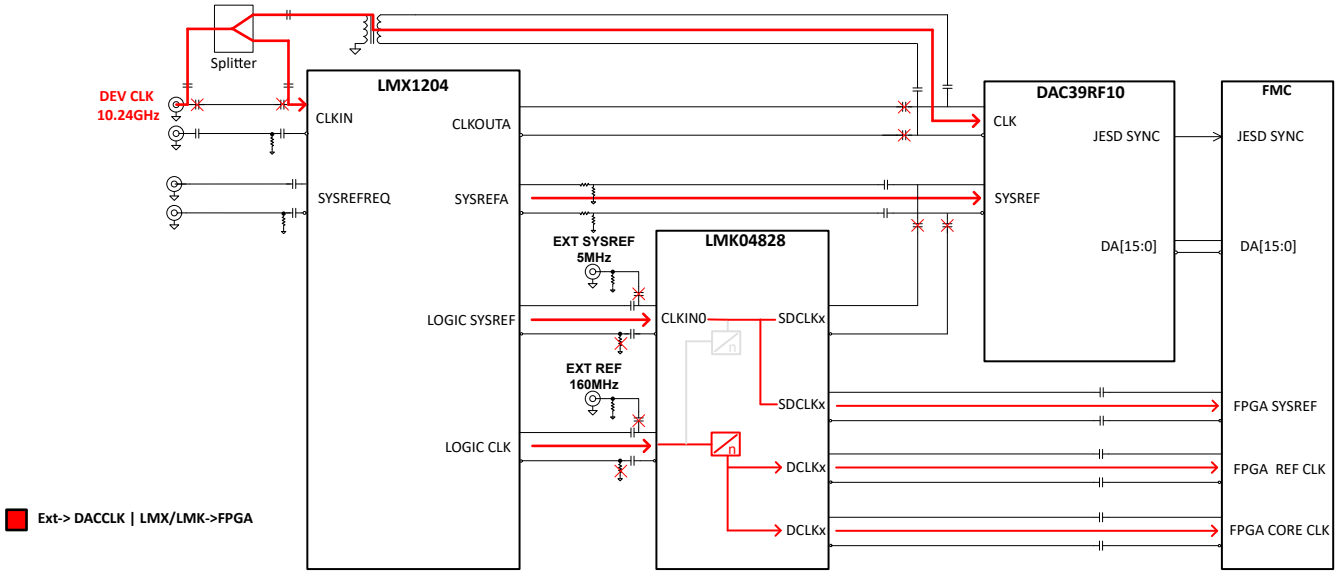


Figure 7-2. EXT->DACCLK | LMX/LMK-> FPGA Clocking System Block Diagram

7.1.3 EXT->DACCLK | LMK-> FPGA Clocking Option

The DAC39RF10EVM can be configured to use EXT->DACCLK | LMK-> FPGA Clocking option. In this use case, the user provide a two clock signal. A high frequency(10-15dBm) signal to an SMA labeled LMX CLKp. This signal is routed though the splitter to Balun and LMX1204. The Balun converts the single ended signal into differential and is used to clock the DAC. The second low frequency signal is CLKIN1 input of LMK04828. The LMK04828 is used to generates the low frequency DAC SYSERF signal, FPGA reference clocks and FPGA SYSREF signal. The LMK04828 is used in clock distribution mode and provides several copies/divided down version of FPGA reference clock and FPGA SYSREF signalFigure 7-3 shows the block diagram of external reference clocking option:

The EVM can be configured to use external reference clocking option with the following steps:

- Remove C141 and C142, populate C136 and C139
- Remove C138 and C140, populate C134 and C135
- Remove C65 and R64, populate C64 and R66
- Remove C73 and C74, populate C75 and C76

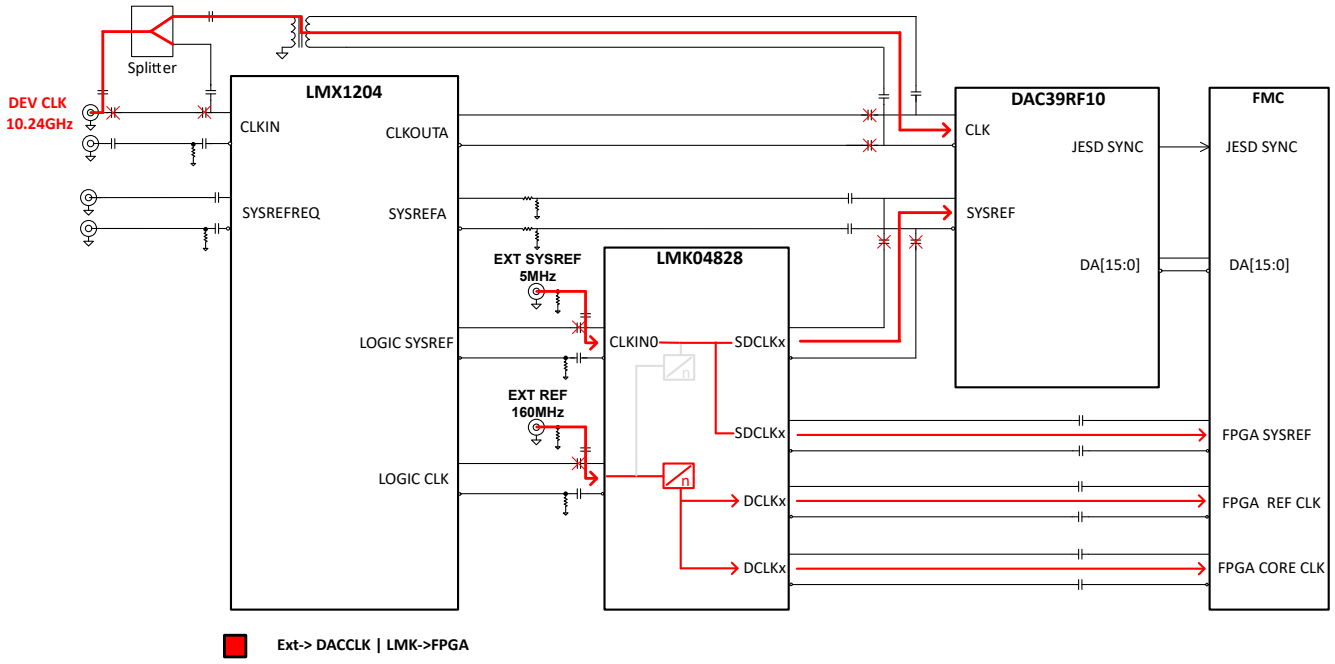


Figure 7-3. External Reference Clocking System Block Diagram

7.2 Signal Routing

Table 7-1 provides the signal routing details for the DAC39RF10EVM.

Table 7-1. DAC39RF10EVM Signal Routing

JESD204C Inputs	FMC(+) Pi	FMC(+) Signal Names(1)
Lane0	A38,A39	DP5_C2M_INV
Lane1	B36,B37	DP6_C2M_INV
Lane2	B32,B33	DP7_C2M_INV
Lane3	A34,A35	DP4_C2M_INV
Lane4	Y30,Y31	DP13_C2M_INV
Lane5	A30,A31	DP3_C2M_INV
Lane6	Z28,Z29	DP12_C2M_INV
Lane7	B28,B29	DP8_C2M_INV
Lane8	Y6,Y7	DP21_C2M_INV
Lane9	C2,C3	DP0_C2M_INV
Lane10	Z8,Z9	DP20_C2M_INV
Lane11	A22,A23	DP1_C2M_INV
Lane12	Z24,Z25	DP10_C2M_INV
Lane13	B25,B26	DP9_C2M_INV
Lane14	Y26,Y27	DP11_C2M_INV
Lane15	A26,A27	DP2_C2M_INV

(1) Red items with _INV in the signal name are inverted with respect to standard FMC polarity.

7.3 Analog Outputs

Table 7-2 provides the different settings for setting the analog inputs path.

Table 7-2. Analog Output Path

Coupling	Output	SMA to Use	Installed componets	DNI components
AC (default)	S/E Balun (500kHz to 9GHz)	OUTAp and OUTBp	R180, R185, R193, R198 = 8.33 Ω and C176, C184 = 0.1 µF	R178, R179, R189,R190, R191,R192, R202,R203
AC	Differential	OUTAp, OUTAn, OUTBp and OUTBn	R178, R179, R189,R190, R191,R192, R202,R203 = 0.1 µF	R180, R185, R193, R198 C176, C184

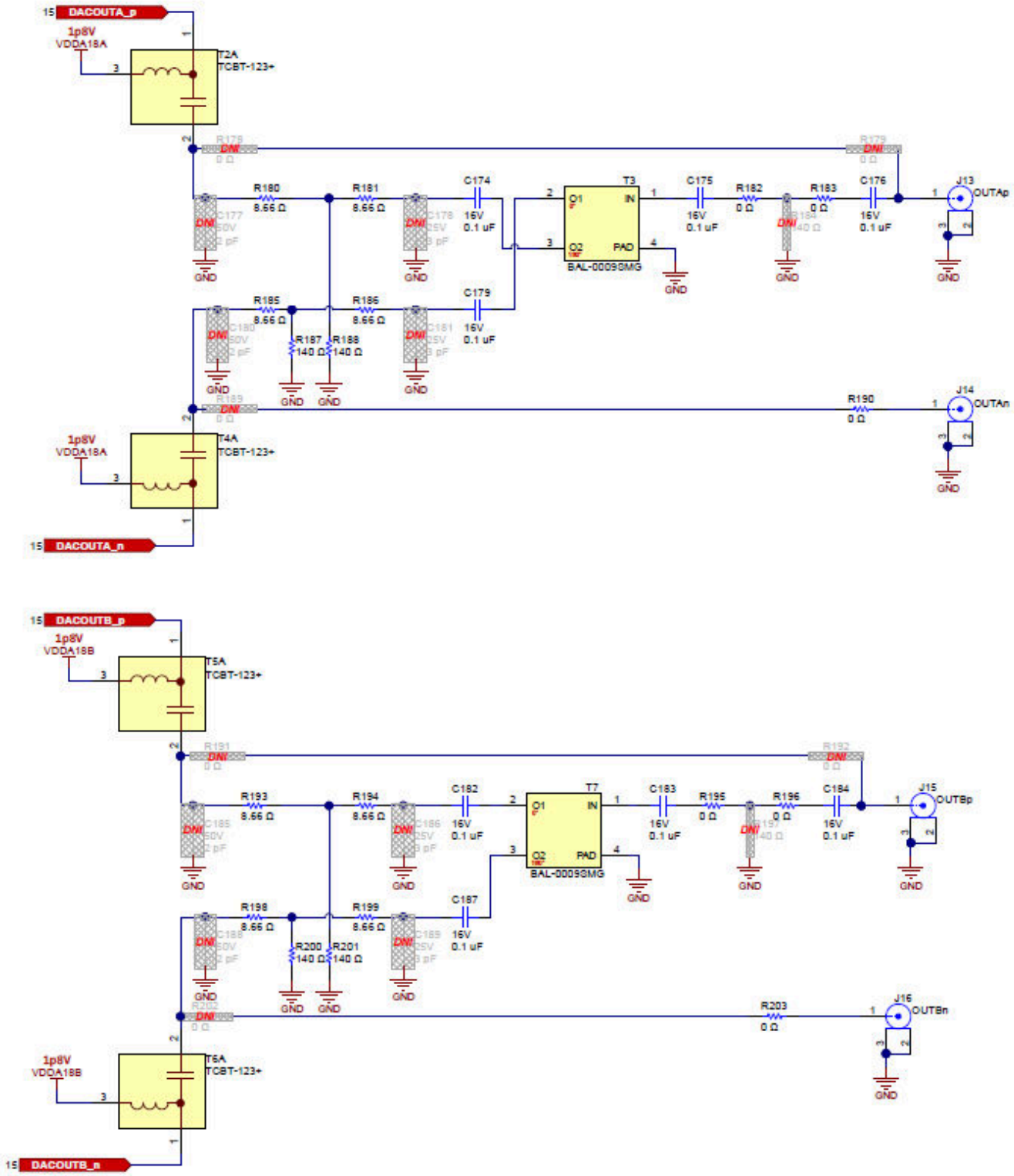


Figure 7-4. Analog Outut Path

A 3 dB attenuation pad is added between the inputs and the ADC. The 3 dB pad helps with the flatness of the frequency response.

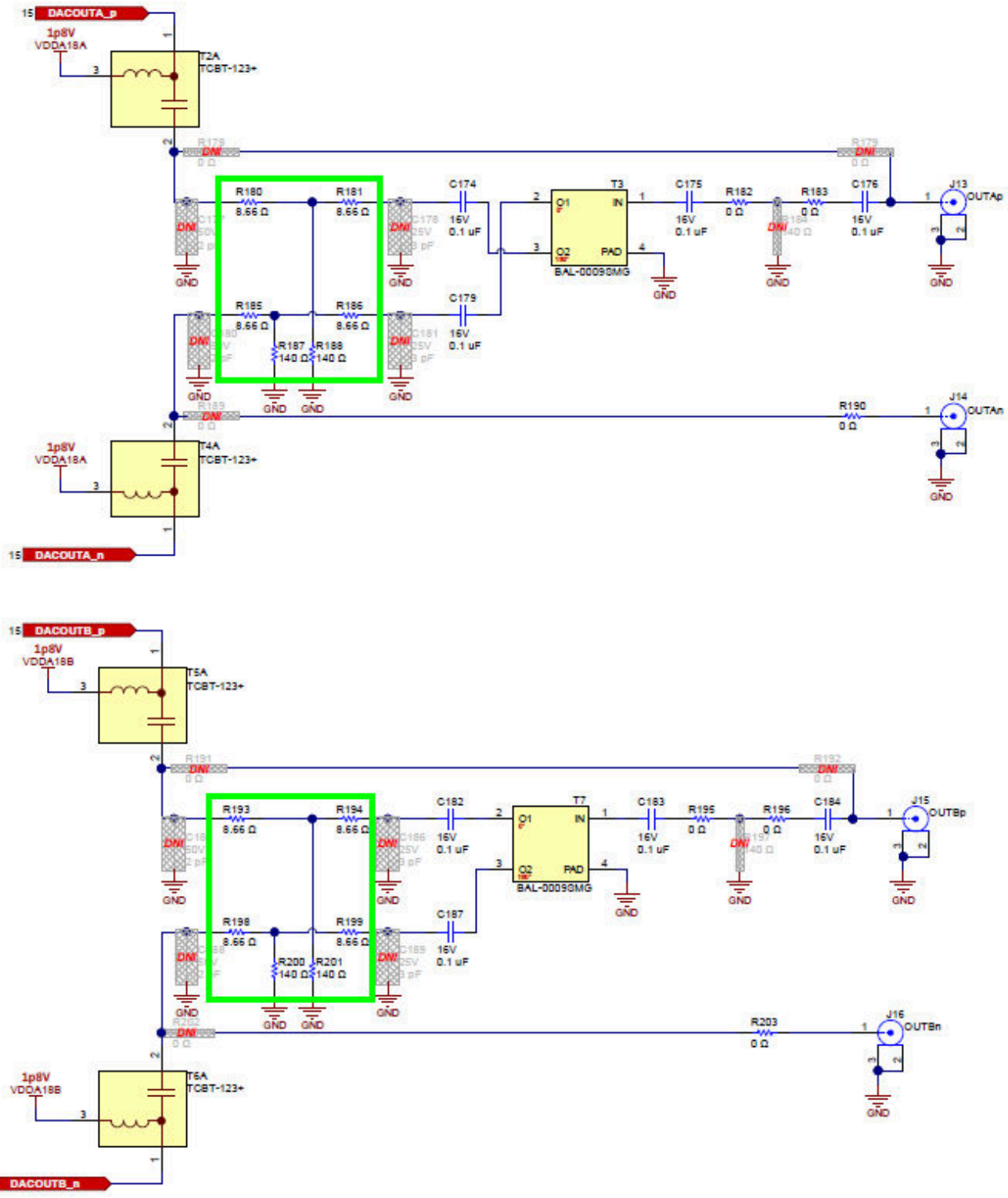


Figure 7-5. 3 dB attenuation pad

7.4 Jumpers and LEDs

Table 7-3 shows the jumper settings and Table 7-4 shows the LED functionality.

Table 7-3. Jumper Settings

Label	Description	Function
J12	Selects the source for SPI signals	Uninstalled(default): SPI signals to various device on the EVM are controlled by the FTDI dongle board. Installed: SPI signals from FMC+ connector are controlling the devices on the EVM(This feature will be supported on next rev of the board).

Table 7-4. LEDs

Label	Function
D3	12 V power indicator

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265