# **TSW12QJ1600 Evaluation Module**

# **User's Guide**



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This user's guide describes the characteristics, operation, and use of the TSW12QJ1600 evaluation module (EVM). This user's guide discusses how to set up and configure the software and hardware, and reviews various aspects of the program operation. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the TSW12QJ1600EVM. In the following sections of this document, the TSW12QJ1600 evaluation board is referred to as the *EVM* and the TSW12QJ1600 device is referred to as the *ADC* device. This document also includes an electrical schematic, printed circuit board (PCB) layout drawings, and a parts list for the EVM.

### Trademarks

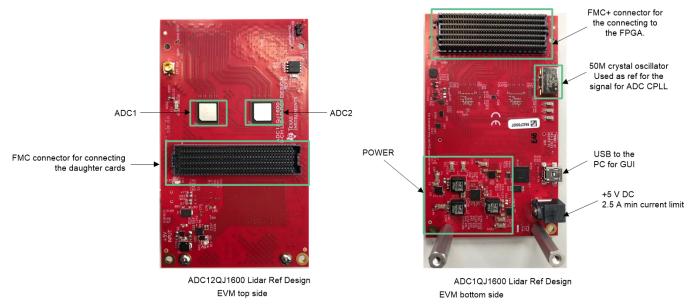
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# Introduction

The TSW12QJ1600EVM is an evaluation board used to evaluate ADC12QJ1600 analog-to-digital converters (ADC) from Texas Instruments with different front end options. The ADC12QJ1600 is a quad channel, 12-bit ADC, capable of operating at sampling rates up to 1.6 Giga- samples per second (GSPS) with four analog input channels. This design has two ADC12QJ1600 devices on the same PCB, this design can be used to demonstrate multiple ADC synchronization, deterministic latency and test the performance of the ADC with various front end options (AC coupled transformer, DC coupled option with LMH32401) The design also demonstrate how clocking scheme can be simplified by daisy-chaining PLL refout from one ADC to other ADC. Eliminating the need to clock distribution chip usually needed by JESD devices. The TSW12QJ1600EVM output data is transmitted over a standard JESD204C high-speed serial interface. This evaluation board also includes the following important features

- Transformer-coupled signal input network allowing a single-ended signal source from 10 MHz to 4 GHz. Option to bypass the transformer and use DC coupled differential inputs
- LM95233 temperature sensor
- High-speed serial data output over a High Pin Count FMC interface connector
  - **NOTE:** To improve signal routing quality, serial lanes are mapped differently with respect to the standard FMC VITA-57 signal mapping.
- Device register programming through USB connector and FTDI USB-to-SPI bus translator with an option to program through the FMC+ connector



### Figure 1-1. EVM Orientation

The digital data from the TSW12QJ1600EVM board is quickly and easily captured with the TSW14J58EVM data capture boards.

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**NOTE:** The TSW14J58EVM can only be used be used for JMODES 8 at a maximum sampling rate of 1GSPS.

The TSW14J58EVM captures the high-speed serial data, decodes the data, stores the data in memory, and then uploads it to a connected PC through a USB interface for analysis. The High-Speed Data Converter Pro (HSDC Pro) software on the PC communicates with the hardware and processes the data.



# Equipment

This section describes how to setup the EVM on the bench with the proper equipment to evaluate the full performance of the ADC device.

# 

## 2.1 Evaluation Board Feature Identification Summary



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## 2.2 Required Equipment

The following equipment and documents are included in the EVM evaluation kit:

- Evaluation board (EVM)
- Mini-USB cable
- Power cable

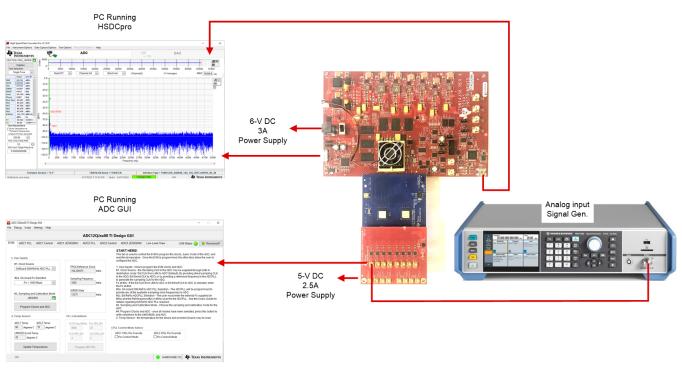
The following equipment is **not** included in the EVM evaluation kit, but is required for evaluation of this product:

- TSW14J58EVM data capture board and related items
- PC computer running Microsoft® Windows® 7, or 10
- One low-noise signal generator for providing a reference signal for the ADC PLL. ONLY need with external reference clocking option is desired. TI recommends the following generators:
  - Rohde & Schwarz® SMA100B
  - Rohde & Schwarz® SMA100A
- One low-noise signal generator for analog input. TI recommends the following generators:
  - Rohde & Schwarz<sup>®</sup> SMA100B
  - Rohde & Schwarz® SMA100A
- Bandpass filter for analog input signal (97 MHz or desired frequency). The following filters are recommended:
  - Bandpass filter, greater than or equal to 60-dB harmonic attenuation, less than or equal to 5% bandwidth, greater than 18-dBm power, less than 5-dB insertion loss
  - Trilithic<sup>™</sup> 5VH-series tunable BPF
  - K&L Microwave<sup>™</sup> BT-series tunable BPF
  - TTE KC6 or KC7-series fixed BPF
- Signal-path cables, SMA to SMP or BNC (or both SMA and BNC)

By default, the TSW12QJ1600EVM is configured to use a 50-MHz onboard crystal oscillator to provide reference input to the ADC PLL which is used to generate the sampling clock to the ADC (In the GUI this option is labeled as " OnBoard 50M Ref to ADC PLL"). A few small board modifications allow the direct external sampling clock option (In the GUI this option is labeled as "Ext Ref to ADC PLL").



# Setup Procedure





**NOTE:** The HSDC Pro software must be installed before connecting the TSW14J58EVM to the PC for the first time.

## 3.1 Install the High Speed Data Converter (HSDC) Pro Software

- 1. Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterprosw. Follow the installation instructions to install the software.
- Download and copy all the INI files required to the HSDCpro directory from the TSW12QJ1600EVM web page on ti.com. The INI files should be copied to following location C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J58 Details\ADC files

## 3.2 Install the Configuration GUI Software

- 1. Download the Configuration GUI software from the TI.com software page .
- 2. Extract files from the .zip file.
- 3. Run the executable file (setup.exe), and follow the instructions.

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## 3.3 Connect the EVM and TSW14J58EVM

With the power off, connect the TSW12QJ1600EVM (with the daughter card already mounted on base board) to the TSW14J58EVM through the FMC+ connector as shown in Figure 3-1. Ensure that the standoffs provide the proper height for robust connector connections.

## 3.4 Connect the Power Supplies to the Boards (Power Off)

- Confirm that the power switch on the TSW14J58EVM is in the off position. Connect the power cable to a 6-V DC (minimum 4 A) power supply. Ensure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 6 V. Connect the power cable to the EVM power connector.
- 2. Confirm that the power switch for the power supply of the TSW12QJ1600EVM is in the off position. Connect the power cable to a 5-V DC (minimum 2.5 A) power supply. Ensure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 5 V. Connect the power cable to the EVM power connector.

### CAUTION

Ensure the power connections to the EVMs are the correct polarity. Failure to do so may result in immediate damage.

Leave the power switches in the off position until directed later.

## 3.5 Connect the Signal Generators to the EVM (RF Outputs Disabled Until Directed)

Connect a signal generator to any of the input labeled J2–J9 on the daughter card connected to the TSW12QJ1600EVM through a bandpass filter and at the SMP connector. This must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal from the generator. Configure the signal generator for 97 MHz, 0 dBm.

### When onboard 50-MHz crystal oscillator is used as a reference for the ADC PLL (Default):

- a. By default, the EVM is set to use the onboard 50-MHz crystal oscillator to supply the 50-MHz reference to the ADC PLL.
- b. Skip this step for default ("OnBoard 50M Ref to ADC PLL ") EVM setup. This step should only be followed when "Ext Ref to ADC PLL mode is desired. The reference clock signal for the ADC PLL of desired frequency (50 MHz to 500 MHz) is applied at the SMP connector EXT CLK (J2). Set the output power to approximately 6–9 dBm.

**NOTE:** Do not turn on the RF output of any signal generator at this time.

## 3.6 Turn On the TSW14J58EVM Power and Connect to the PC

- 1. Turn on the power switch of the TSW14J58EVM.
- 2. Connect a mini-USB cable and USB 3 cable from the PC to the TSW14J58EVM.
- 3. If this is the first time connecting the TSW14J58EVM to the PC, follow the on-screen instructions to automatically install the device drivers. TSW14J58EVM user's guide for specific instructions.

## 3.7 Turn On the TSW12QJ1600EVM Power Supplies and Connect to the PC

- 1. Turn on the 5-V power supply to power up the EVM.
- 2. Connect the EVM to the PC with the mini-USB cable.

## 3.8 Turn On the Signal Generator RF Outputs

Turn on the RF signal output of the signal generator connected to INAP. If Ext Ref to ADC PLL clocking option is used, turn on the RF signal outputs connected to EXT CLK



## 3.9 Open the TSW12QJ1600EVM GUI and Program the ADC and Clocks

The Device Configuration GUI is installed separately from the HSDC Pro installation and is a stand-alone GUI.

ADC12QJxx00 TI Design GUI File Debug Script Settings Help						- 🗆 X						
	ADC12QJ	xx00 TI De	sign GUI									
EVM ADC1.PLL ADC1.Control ADC	1.JESD204C ADC2.PLL A	ADC2.Control	ADC2.JESD204C	Low Level View	USB Status	🔵 🇇 Reconnect?						
1. User Inputs  #1. Clock Source OnBoard 50M Ref to ADC PLL  #2a. On-board Fs Selection Fs = 1000 Msps  #3. Sampling and Calibration Mode JMODE8  Program Clocks and ADC  2. Temp Sensor: ADC1 Temp ADC2 Temp	FPGA Reference Clock 193.359375 MH: Sampling Frequency 1000 MH: SERDES Rate 12375 MH: PLL Calculations VCO Freq (MHz) PLL F83_D	z #1 z #1 z #1 z FS prv z #2 ALL #4 wr vv z	TART HERE! Is tab is used to control ad the temperature. Or infigure the ADC. User Inputs - How to p . Clock Source - the S; stribution mode "Ext CL generate the sampling at#2b. If the Ext CLK F is at#2b. a. On-board 50M Reft iovide any of the availat table regarding Ext Ref . Sampling and Calibr CC. It selections to the LM Temp Sensor - the tem	nce the EVM is program the EVM cloc ampling CLK to the A K from LLK to ADC K to ADC) or by provi J CLK for the ADC. from LLK to ADC or the ADC PLL Selection to ADC PLL Selection be sampling clock from Selection - The user roy(#2c1 mHz) used selection - The user roy(#2c1 mHz) used ADC - once all mode ADC - once all mode	ammed, the other tabs ks and ADC: DC may be supplied th (Default). By providing ding a reference frequ Ext Direct CLK to ADC - The ADCPLL will be squencies to ADC. In the ADCPLL see to the sampling and call hs have been selected	allow the user to rrough LMK in diret a simpling CLK ency to the ADCPLL is selected, enter programmed to IFs supplied (in the Users Guide for bration mode for the press this button to						
68 degrees C 63 degrees C	8000 20	PLL Control Mode Select:										
LM95233 Local Temp 42 degrees C	VCO FB1_DIV VCO FB2_ 4 2	DIV	C1 CPLL Pin Override SPI Control Mode	ADC2 CPLL P								
Update Temperatures	Program ADC PLL											
Idle				😑 HARE	DWARE CO 🐺 TE	exas Instruments						

Figure 3-2. Configuration GUI EVM Tab



Figure 3-2 and Figure 3-3 show the GUI open to the *EVM* tab and *Control* tab respectively. Tabs at the top of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has two configurable devices, namely the TSW12QJ1600. The register map for each device is provided in the device data sheet.

- 1. Open the TSW12QJ1600EVM GUI.
- 2. Select the "OnBoard 50M Ref to ADC PLL" as the clock source.
- 3. Select Fs = 1000 MHz MSPS as the onboard Fs selection option from the drop-down menu.
- 4. Select JMODE8 for the sampling and Calibration mode.
- 5. Click Program Clocks and ADC (Note: This action overwrites any previous device register settings.)

## 3.10 Calibrate the ADC Device on the EVM

		ADC12Q	Jxx00 TI De	sign GUI						
M ADC1.PLL ADC1.Control	ADC1.JESD204C	ADC2.PLL	ADC2.Control	ADC2.JESD204C	Low Level View	USB Status 🧿	参 Recon			
Power and Reset:	Calibration			Gain and Offset:						
Soft Reset Reset Device Registers POWER DOWN LOW POWER MODE Dither: Dither Enable Dither Amplitude Small Dither Amplitude	Disable Penab	le Foreground le Foreground le Background le Background le Low Power B utomatic LP Ca	hange Settings Cal Offset CAL Cal Offset CAL Background CAL I Delay	Input A: Gain Full Scale 40960	0.006 mVpp					
	Status:	eck CAL Status		Digital Mux:	Over-	range:				
	CAL CAL FG_ CAL Sta CAL ST CAL ST	GOOD STOPPED .DONE tus Select AT matches FO gger Source		ADC Channel Ena ADC CH A, B, C &	oV 7 ble	OVR Monitoring Period 7 (5) 512 ADC Samples Over-range Threshold 242 (5) -0.488 dBFS				

Figure 3-3. Configuration GUI ADC Control

- 1. With the EVM GUI open on the PC, navigate to the Control tab.
- 2. To calibrate the ADC, click *Cal Triggered/Running* once, then click it again. This stops and re-starts the Calibration engine.

- 3. To enable background calibration, use the following steps:
  - Navigate to the JESD204C tab and click on JESD Block Enable to stop the JESD204C block.
  - Navigate back to the *Control* tab and click on *Enable Calibration Block* to disable calibration and allow setting changes.
  - Click on Enable Background Cal.
  - If background offset calibration is desired also, click on Enable Background Offset Cal.
  - Click on *Enable Calibration Block* to re-enable the calibration subsystem
  - Navigate to the JESD204C tab and click on JESD Block Enable to re-start the JESD204C block.
  - Navigate back to the *Control* tab and click the *Cal Triggered/Running* button once, then click it again. This restarts the Calibration engine.
- 4. To disable background calibration, use the following steps:
  - Navigate to the JESD204C tab and click on JESD Block Enable to stop the JESD204C block.
  - Navigate back to the *Control* tab and click on *Enable Calibration Block* to disable calibration and allow setting changes.
  - If background offset calibration was enabled, click on *Enable Background Offset Cal* to disable the feature.
  - Click on *Enable Background Cal* to disable the feature.
  - Click on *Enable Calibration Block* to re-enable the calibration subsystem.
  - Navigate to the JESD204C tab and click on JESD Block Enable to re-start the JESD204C block.
  - Navigate back to the *Control* tab and click the *Cal Triggered/Running* button once, then click it again. This restarts the Calibration engine.

## 3.11 Open the HSDCpro Software and Load the FPGA Image to the TSW14J58EVM

- 1. Open the HSDC Pro software.
- 2. Click *OK* to confirm the serial number of the TSW14J58EVM device. If multiple TSWxxxxx boards are connected, select the model and serial number for the one connected to the TSW12QJ1600EVM.
- 3. Select the ADC12QJ1600RD\_JMODE8\_12G\_16G\_divby64 device from the ADC select drop-down menu in the top left corner.
- 4. When prompted, click Yes to update the firmware.
  - **NOTE:** If the user configures the EVM with options other than the default register values, different instructions may be required for selecting the device in HSDC Pro. See Appendix B for more details.
- 5. Enter the ADC Output Data Rate ( $f_{(SAMPLE)}$ ) as "1000M" or the desired output sample rate. This number must be equal to the actual sampling rate of the device and must be updated if the sampling rate changes.

## 3.12 Capture Data Using the HSDC Pro Software

The following steps show how to capture data using the HSDC Pro software (see Figure 3-4):

1. Select the test to perform.

**NOTE:** This calibrate button executes a calibration sequence that is required for full performance. This calibration is performed automatically during the Section 3.9 step but must be performed again, any time the sampling rate changes, after significant temperature change of the ADC, or after exiting the power-down mode. See the TSW12QJ1600 device data sheet, (SBAS960) for details regarding the necessary calibration sequence.



- 2. Select the data view.
- 3. Select the channel to view.
- 4. Click the capture button to capture new data.

Additional tips:

- Use the *Notch Frequency Bins* from the *Test Options* file menu to remove bins around DC (eliminate DC noise and offset) or the fundamental (eliminate phase noise from signal generators).
- Open the *Capture Option* dialog from the *Data Capture Options* file menu to change the capture depth or to enable Continuous Capture or FFT averaging.
- For analyzing only a portion of the spectrum, use the *Single Tone* test with the *Bandwidth Integration Markers* from the *Test Options* file menu. The *Channel Power* test is also useful.
- For analyzing only a subset of the captured data, set the *Analysis Window (samples)* setting to a value less than the number of total samples captured and move the green or red markers in the small transient data window at the top of the screen to select the data subset of interest.

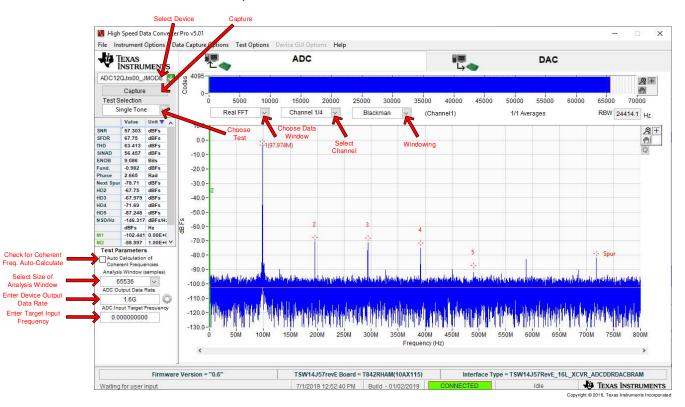


Figure 3-4. High Speed Data Converter Pro (HSDC) GUI



# **Device Configuration**

The ADC device is programmable through the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the EVM. A GUI is provided to write instructions on the bus and program the registers of the ADC device.

## 4.1 Supported JESD204C Device Features

The ADC device supports some configuration of the JESD204C interface. Due to limitations in the TSW14J58EVM firmware, all JESD204C link features of the ADC device are not supported. Table 4-1 lists the supported and non-supported features.

JESD204C Feature	Supported by ADC Device	Supported by TSW14J58EVM						
Number of lanes per link (L)	$L = 2, 3, 4, 6, 8^{(1)}$	L = 1, 2, 3, 4, 6, 8 supported						
Total number of lanes active	2,,3 4, 6, 8	2, 4, 6, 8, 12, 16						
Number of frames per multiframe (K)	$K_{min} = 4-256$ , <sup>(1)</sup> $K_{max} = 256$ , $K_{step} = 4$ , 16 or 32	Most values of K supported, constrained by requirement that $K \times F = 4^n$						
Scrambling	Supported	Supported						
Encoding	8B/10B and 64B/66B	8B/10B						
Test patterns	PRBS7, PRBS9, PRBS15, PBRS23, PRBS31, Ramp, Transport Layer test, D21.5, K28.5, Repeat ILA, Modified RPAT, Serial Out 0, Serial Out 1, Clock test, ADC Test Pattern <sup>(1)</sup>	ILA, Ramp, Long/Short Transport						
Speed	Lane rates from 0.8 to 17.16 Gbps <sup>(1)</sup>	Lane rates from 12 to 16 Gbps $f_{(SAMPLE)}$ parameter must be properly set in HSDC Pro GUI.						

Table 4-1. Supported and Non-Supported Features of the JESD204C Device

<sup>(1)</sup> Dependent on bypass or decimation mode and output rate selection. Always disable the JESD204 block before changing any of the JESD204C settings. Once the settings are changed, re-enable the JESD204 block.

## 4.2 Tab Organization

Control of the ADC1 and ADC2 device features are available in the EVM, ADC PLL, Control and JESD204C tabs for respective ADCs.



### 4.3 Low-Level Control

The *Low Level View* tab, illustrated in Figure 4-1, allows configuration of the devices at the bit-field level. At any time, the controls in Table 4-2 can be used to configure or read from the device.

Control	Description
Register map summary	<ul> <li>Displays the devices on the EVM, registers for those devices, and the states of the registers</li> <li>Clicking on a register field allows individual bit manipulation in the register data cluster</li> <li>The value column shows the value of the register at the time the GUI was last updated</li> <li>The 0-7 column shows the value of the register at the time the register was last read</li> </ul>
Write register button	Write to the register highlighted in the register map summary with the value in the Write Data field
Write all button	Update all registers shown in the register map summary with the values shown in the <i>Register Map</i> summary
Read register button	Read from the register highlighted in the <i>Register Map</i> summary and display the results in the <i>Read Data</i> field Can be used to re-synchronize the GUI with the state of the hardware
Read-all button	Read from all registers in the Register Map summary and display the current state of the hardware
Load Configuration button	Load a configuration file from disk and register address/data values in the file
Save Configuration button	Save a configuration file to disk that contains the current state of the configuration registers
Register Data cluster	Manipulate individual accessible bits of the register highlighted in the register map summary
Individual register cluster with read or write register buttons	Perform a generic read or write command to the device shown in the <i>Block</i> drop-down box using the address and write data information

### Table 4-2. Low-Level Controls

					ΔΓ	00120		0 TI D	)es	iar	G	ш												
_					~				_	-				_	_			_						
/М	ADC1.PLL	ADC1.Control	ADC1	JESD204	C ADO	C2.PLL	ADC	2.Contro	bl	AD	C2.J	ESC	204	с	Lov	v Le	vel Vi	ew		USB	Status 🤇		参 Reco	onneo
Re	gister Map	🗒 🖻 🦁 Y						Lin	ked	Up	date	Mod	de Ir	mme	diat	e	~				Sear	rch	Next	
	• •	gister Name		Address	Default	Mode	Size	Value	17	6	5	4	3	2	1	0	•	Field \	/iew					
Ē		lxx00_ADC1							<u> </u>	-	-	-	-	-	-	Πì								
1		CONFIG_A		0x00	0x30	R/W	8	0xB0	1	0	1	1	0	0	0	0								
		DEVICE_CONFIG		0x02	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0								
	ADC1.	VENDOR_ID_0		0x0C	0x51	R	8	0x51	0	1	0	1	0	0	0	1								
	ADC1.	VENDOR_ID_1		0x0D	0x04	R	8	0x04	0	0	0	0	0	1	0	0								
	ADC1.	USR0		0x10	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0								
	ADC1.	CLK_CTRL0		0x29	0x80	R/W	8	0x80	1	0	0	0	0	0	0	0								
	ADC1.	CLK_CTRL1		0x2A	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0								
		SYSREF_POS_0		0x2C	0x00	R	8	0x00	0	0	0	0	0	0	0	0								
		SYSREF_POS_1		0x2D	0x00	R	8	0x00	0	0	0	0	0	0	0	0								
		SYSREF_POS_2		0x2E	0x00	R	8	0x00	0	0	0	0	0	0	0	0								
		FS_RANGE_0		0x30	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0								
		FS_RANGE_1		0x31	0xA0	R/W	8	0xA0	1	0	1	0	0	0	0	0								
		LOW_POWER1		0x37	0x4B	R/W	8	0x4B	0	1	0	0	1	0	1	1								
		TMSTP_CTRL		0x3B	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0								
		PLLREFO_CTRL		0x3C	0x01	R/W	8	0x01	0	0	0	0	0	0	0	1								
		CPLL_FBDIV1		0x3D	0x00	R/W	8	0x06	0	0	0	0	0	1	1	0								
		CPLL_FBDIV2		0x3E	0x00	R/W	8	0x1A	0	0	0	1	1	0	1	0								
		CPLL_VCOCTRL1 SER PE		0x3F 0x48	0x4F 0x00	R/W R/W	8	0x4A 0x00	0	1	0	0	1	0	1	0								
		SER_PE LVDS_SWING		0x48 0x50	0x00	R/W	8	0x00	0	0	0	0	0	0	0	121								
Ļ		-		0,50	0,00	PO/W	0	0,00	0	0	0	0	0	0	10	0	~							
R	egister Descri	puon							_															
									^	в	ock				_	A	ddres	s	W	/rite Da		Rea	d Data_0	Gene
															$\mathbf{\vee}$	2		0	x		0	×	0	
																			N	Nrite R	egister	Rea	ad Regist	ter

Figure 4-1. Low-Level Register Control Tab



# Troubleshooting the TSW12QJ1600EVM

## Table 5-1 lists some troubleshooting procedures.

### Table 5-1. Troubleshooting

Issue	Troubleshoot							
	<ul> <li>Verify the test setup shown in Figure 3-1, and repeat the setup procedure as described in this document.</li> </ul>							
	<ul> <li>Check power supply to EVM and TSW14J58EVM. Verify that the power switch is in the on position.</li> </ul>							
	Check signal and clock connections to EVM.							
General problems	<ul> <li>Visually check the top and bottom sides of the board to verify that nothing looks discolored or damaged.</li> </ul>							
	Ensure the board-to-board FMC connection is secure.							
	<ul> <li>Try pressing the CPU_RESET button on the TSW14J58EVM. Also try clicking <i>Instrument</i> Options → Reset Board after changing the ADC configuration.</li> </ul>							
	<ul> <li>Try power-cycling the external power supply to the EVM, and reprogram the LMK and ADC devices.</li> </ul>							
	<ul> <li>Verify that the USB cable is plugged into the EVM and the PC.</li> </ul>							
Configuration GUI is not	• Check the computer device manager and verify that a USB serial device is recognized when the EVM is connected to the PC.							
working properly	<ul> <li>Verify that the green USB Status LED light in the top right corner of the GUI is lit. If it is not lit, click the Reconnect FTDI button.</li> </ul>							
	Try restarting the configuration GUI.							
Configuration GUI is not able to connect to the EVM	<ul> <li>Use the free FT_PROG software from FTDI chip and verify that the onboard FTDI chip is programmed with the product description ADC12QJxx00 RD.</li> </ul>							
HSDC Pro software is not	<ul> <li>Verify that the TSW14J58EVM is properly connected to the PC with a mini-USB cable and that the board serial number is properly identified by the HSDC software.</li> </ul>							
capturing good data or analysis results are incorrect.	<ul> <li>Check that the proper ADC device mode is selected. The mode should match in HSDC Pro and the ADC GUI.</li> </ul>							
	Check that the analysis parameters are properly configured.							
	<ul> <li>Try to reprogram the LMK device and reset the JESD204 link.</li> </ul>							
HSDC Pro software gives a	<ul> <li>Verify that the ADC sampling rate is correctly set in the HSDC software.</li> </ul>							
time-out error when	• Try pressing the <i>CPU_RESET</i> button on the TSW14J58EVM. Also try clicking <i>Instrument</i>							
capturing data	<ul> <li>Options → Reset Board after changing the ADC configuration. Try to recapture again.</li> <li>Select Instrument Options → Download Firmware and download</li> </ul>							
	'TSW14J58_64B66B_12G_16G_REFCLKBY64_IID_28.rbf'. Try to capture again.							
Sub optimal massured	• Try clicking <i>Cal Triggered/Running</i> button 2x to re-calibrate the ADC in the current operating conditions. It is located on the <i>Control</i> tab of the configuration GUI.							
Sub-optimal measured performance	Check that the spectral analysis parameters are properly configured.							
	<ul> <li>Verify that bandpass filters are used in the clock and input signal paths and that low-noise signal sources are used.</li> </ul>							



Appendix A SLAU796–July 2020

# References

This section provides references to technical documents and user's guides.

## A.1 Technical Reference Documents

- TSW14J58EVM user's guide
- High-Speed Data Converter Pro GUI User's Guide, also available in the help menu of the software
- FTDI USB to Serial Driver Installation Manual (www.ftdichip.com/Support/Documents/InstallGuides.htm)

## A.2 TSW14J58EVM Operation

See the TSW14J58EVM user guide for configuration and status information.



# HSDC Pro Settings for Optional ADC Device Configuration

This appendix provides settings for optional ADC device configuration in HSDC Pro.

## **B.1** Changing the Number of Frames per Multi-Frame (K)

Changing the number of frames per multi-frame output by the JESD204 transmitter (ADC device) is configured using the K parameter( when using modes with 8B/10B encoding) on the *JESD204C* tab in the *Configuration* GUI. This parameter must be matched by the receiving device, and the SYSREF frequency must also be programmed to a compatible frequency. Ensure that the K value complies with the *K Min* and *Step* values for the selected JMODE. Refer to the TSW12QJ1600 operating modes table in the device datasheet.

## B.2 Customizing the EVM for Optional Clocking Support

The TSW12QJ1600EVM can be clocked using two different methods:

- 1. Onboard 50M ref to ADC PLL clocking option
- 2. Ext Ref to ADC PLL clocking

## B.2.1 Onboard 50M Ref to ADC PLL (Default)

The 50-MHz onboard crystal oscillator is use provide reference signal to ADC's single-ended clock input. The ADC PLL generate a sampling clock for the ADC from this 50 MHz. In this clocking mode, the ADC also generates the reference clock signal for FPGA. FPGA takes this reference clock and generates the SYSREF signal for the ADC and feeds it back to the ADC. Figure B-1 shows the block diagram of the *Onboard 50M Ref to ADC PLL* clocking option:

No hardware change is need to use this mode.



Customizing the EVM for Optional Clocking Support

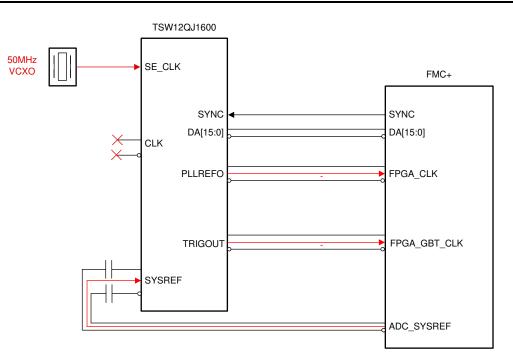
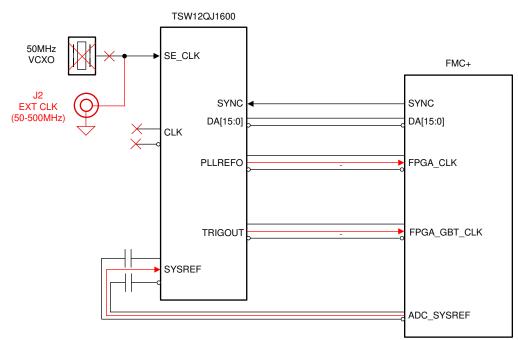


Figure B-1. Onboard 50M Ref to ADC PLL System Block Diagram

## B.2.2 "Ext Ref to ADC PLL"

The reference signal for the ADC PLL is provided externally from External signal generator on SMP labeled EXT CLK(J2). The sampling clock is generate by ADC PLL, from this external provided PLL reference signal. In this clocking mode ADC also generate the reference clock signal for FPGA. FPGA takes this reference clock and generates the SYSREF signal for the ADC and feed it back to the ADC. Figure B-2 shows the block diagram of Ext Ref to ADC PLL clocking option:

• Remove R231, and populate C27.





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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
- 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

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- 3.3 Japan
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